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A Coupled-Inductor DC-DC Converter with Input Current Ripple Minimization for Fuel Cell Vehicles

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Abstract: A coupled-inductor DC-DC converter with a high voltage gain is proposed in this paper to match the voltage of a fuel cell stack to a DC link bus. The proposed converter can minimize current ripples and can also achieve a high voltage gain by adjusting the duty cycle *d* and the turns ratio *n* of a coupled inductor. A passive lossless clamping circuit that is composed of one capacitor and one diode is employed, and this suppresses voltage spikes across the power device resulting from system leakage inductance. The operating principles and the characteristics of the proposed converter are analyzed and discussed. A 400-W experimental prototype was developed, and it had a wide voltage gain range (4–13.33) and a maximum efficiency of 95.12%.

Keywords: coupled inductor; DC-DC converter; high voltage gain; ripple minimization current; fuel cell vehicles

1. Introduction

With extensive use of fossil fuels in transport, power, and heating, addressing the imminent global energy crisis has become an increasing concern [1–3]. In addition, considerations such as the greenhouse effect and increasing air pollution (especially in cities) caused particularly by emissions from fossil fuel vehicles have become significant influences on quality of life and health [4]. Renewable energy vehicles, including fuel cell vehicles, pure electric vehicles, and hybrid energy source vehicles [5,6], can greatly reduce the impact of transport on the environment due to their pollution-free characteristics [7,8]. Fuel cell vehicles have attracted wide attention because of their higher energy conversion rate compared to locomotives [9] and their longer cycle range compared to battery electric vehicles [10]. However, a fuel cell source cannot be connected to the propulsion system's DC bus directly, as it can have a low and variable output voltage and a large output current [11]. As a result, a DC-DC boost converter is needed to lift the voltage of the fuel cell source and to match the DC bus voltage [12]. Above all, a DC-DC converter with a minimal input current ripple and a high voltage gain is extremely important for the future development of fuel cell vehicles.

The traditional DC-DC boost converter features a simple structure and low component counts. However, low voltage gain and high voltage stresses across all semiconductor devices limit its application. Although a three-level DC-DC boost converter lowers the voltage stress to half of the output voltage, the duty cycle is extreme, while the voltage gain is high. A three-level DC-DC converter with a high voltage gain and without extreme duty cycles was proposed in Reference [13], but it



had a greater cost due to the number of semiconductors (eight MOSFETs and four diodes), and the control strategy was also more complicated. In References [14,15], the proposed converters employed switched-capacitor cells to achieve a high voltage gain, while the number of switched-capacitor cells, the volume of the converter, and the cost increased. Coupled inductors have been employed to improve the voltage gain of converters (proposed in [16,17]). However, the higher the voltage gain was, the greater the turns ratio required from the coupled inductors was, which increased the leakage inductance of the coupled inductors and made manufacturing more difficult. A novel high step-up DC-DC converter with coupled inductors and a switched capacitor was proposed in Reference [18]. However, the leakage inductance of the coupled inductors resulted in a high voltage spike across the power switches. An active clamp [19] or a passive snubber circuit [20] are often adopted to solve the aforementioned voltage spike issues. However, the complexity of the control strategy and the circuit also increase. At the same time, these converters have different levels of input current ripples, and a large current ripple has a serious impact on the lifetime of fuel cells [21]. In References [22–24], interleaved converters were proposed to cut down the input current ripple. The improved modulation strategy proposed in Reference [13] could also obtain a lower input current ripple. However, as the voltage gain increased, the input current became large, and therefore the increased current ripple was still a disadvantage for fuel cell sources. An active compensation method was proposed in Reference [25] based on the designed push-pull DC-DC converter by adding an active-clamp circuit to further reduce current ripples in the uninterruptible power supply (UPS) system. However, the method focused on the low-frequency current ripple and employed an extra circuit. A maximum power point tracking (MPPT) control with a perturbed duty ratio D_p was employed in Reference [26] to simply reduce the input ripple current of a proton exchange membrane (PEM) fuel cell. However, it was only suitable for AC output applications. A pre-regulator was introduced in Reference [27] to interface with the main regulator for reducing the current ripple. However, the pre-regulator employed an interleaved structure that was not indispensable. The introduced pre-regulator reduced the power density and increased the cost of the proposed converter. To reduce the low-frequency input current ripple without the auxiliary circuit, a control method based on a front-end DC-DC converter was proposed in Reference [28]. This method intended to modify the DC bus voltage reference and control the DC bus voltage to fluctuate properly at $2f_0$, making the DC bus capacitor support nearly all of the fluctuating power. However, it was not suitable for high-frequency current ripples caused by a charging/discharging current flowing through the input inductor.

Based on the step-up DC-DC converter with an input current ripple minimization proposed in Reference [29], a novel coupled-inductor converter with a high voltage gain is proposed in this paper. The converter benefits from input current ripple minimization, further improves voltage gain, and reduces voltage stresses. A passive lossless clamping circuit is introduced, consisting of one capacitor and one diode. As a result, voltage spikes across the power switch caused by leakage inductance can be suppressed. In addition, the output and the input share a common ground, which can eliminate additional electromagnetic interference (EMI) issues. Section 2 presents the topology of the proposed converter. The operating principles and characteristics of the converter are analyzed in Section 3 in detail. In Section 4, the voltage and current stresses of the semiconductors are analyzed, and a comparison to the counterpart in Reference [29] is made. In Section 5, an experimental prototype is built, and experimental results validate the theoretical analysis.

2. Topology

The topology of the proposed converter and its equivalent circuit are shown in Figure 1a,b, respectively. As the equivalent circuit shows, the coupled inductor is composed of a magnetizing inductance L_M , a leakage inductance L_r , and an ideal transformer whose turns ratio is $n_p:n_s = 1:n$. The inductor L_a and the capacitor C_1 form an input current ripple minimization unit, and the diode D_1 and the capacitor C_4 form a passive lossless clamping circuit. Consequently, the voltage stress across the power switch Q can be clamped to the voltage across C_4 when Q is turned off. The voltage

doubling unit is composed of the capacitor C_2 and the coupled inductor L_s , while the capacitor C_3 and the capacitor C_4 are the energy storage capacitors in the high voltage side.



(b)

Figure 1. The proposed coupled-inductor DC-DC converter. (a) The topology; (b) the equivalent circuit.

3. Analysis of Operating Principles and Characteristics

3.1. Operating Principles

The proposed converter has 10 operating modes (in which Mode G and Mode H cannot coexist simultaneously in a single switching period), and the corresponding current flow paths are depicted in Figure 2.

Mode A: The power switch Q is turned on. The currents that flow through both sides of the ideal transformer decrease rapidly. Meanwhile, diode D_3 is still conducting, and the current flowing through capacitor C_1 starts to decrease. This mode ends when the current flowing in C_3 becomes zero.

Mode B: The current flowing into diode D_3 is no longer able to provide energy for the load and continues to decrease. Accordingly, capacitor C_3 begins to discharge, and the current flowing through it increases. The trends of the currents flowing in other branches of the circuit remain the same. This mode ends when the current flowing through diode D_3 decreases to zero.

Mode C: The currents flowing into both sides of the ideal transformer are reversed and gradually increase. Diode D_2 is turned on, and capacitor C_3 is still discharging. The coupled inductor transfers energy to capacitor C_2 , and it starts to charge. The capacitor C_1 continues to discharge, but its current decreases gradually. Meanwhile, capacitor C_4 continues to charge, and its current gradually decreases to zero, at which time this mode ends.

Mode D: The current flowing through capacitor C_4 begins to reverse and gradually increase, and C_4 begins to discharge. The current flowing through capacitor C_1 continuously decreases, while the current flowing in diode D_2 rises gradually. This mode ends when the current flowing through capacitor C_1 is equal to the current flowing in diode D_2 .

Mode E: The current flowing in diode D_2 continues to increase, and it is larger than the current flowing through capacitor C_1 . As a result, the current flowing through capacitor C_4 continues to rise. When the current flowing into capacitor C_1 decreases to zero, this mode ends.

Mode F: Capacitor C_1 starts to charge, and the current flowing in it increases gradually. Then the current decreases as the capacitor voltage rises.

Mode G: The charging process of capacitor C_2 is completed, and the current flowing in the secondary side of the ideal transformer n_s reduces to zero. The current flowing in the primary side n_p of the ideal transformer increases faster because there is no energy being transferred to the secondary side. This mode does not exist when the duty cycle is small (based on the magnetizing inductor).

Mode H: This mode and Mode G are mutually exclusive, and the converter goes directly into Mode I when Mode G exists. Q is turned off at the beginning, and the magnetizing inductor L_M discharges. As a result, the current flowing into the leakage inductance L_r starts to decrease. Because of the conduction of diode D_1 , the voltage stress across Q is clamped at the voltage across the capacitor C_4 . The capacitor C_4 continues charging. Meanwhile, capacitor C_2 is still in the charging state because the currents flowing into both sides of the ideal transformer have not reversed yet. The diode D_2 remains turned on, and the current flowing through capacitor C_1 begins to decrease. This mode finishes when the current flowing in capacitor C_2 reduces to zero.

Mode I: In this mode, the currents flowing into both sides of the ideal transformer reverse and start to increase, and the current flowing into C_3 begins to decrease because of the conduction of D_3 . When the current flowing into C_3 decreases to zero, this mode ends.



Figure 2. Cont.



Figure 2. Cont.



Figure 2. Current flow paths of the proposed converter in one switching period. (**a**) Mode A; (**b**) Mode B; (**c**) Mode C; (**d**) Mode D; (**e**) Mode E; (**f**) Mode F; (**g**) Mode G; (**h**) Mode H; (**i**) Mode I; (**j**) Mode J; (**k**) Mode K.

Mode J: The current flowing into D_3 continues to increase, and C_3 changes into a charging state. The current trends of other branches remain unchanged. This mode terminates when the current flowing into C_1 decreases to zero.

Mode K: C_1 begins to discharge, and energy is transferred to C_4 from C_1 . As the current flowing through L_a does not change, the current flowing into the primary side n_p falls. As a result, the current

flowing into the secondary side n_s begins to decrease. This mode terminates when the power switch Q turns on.

Mode F, Mode G, and Mode K have the longest durations of these 10 modes (Mode G and Mode H cannot coexist simultaneously), while the other 7 modes are transient states that last for a very short time. As a result, the simplified current waveforms of the circuit elements in a switching period are given in Figure 3.



Figure 3. The simplified current waveforms of the converter. Mode A: End with i_{C3} dropping to 0; Mode B: End with i_{D3} dropping to 0; Mode C: End with i_{C4} dropping to 0; Mode D: End with i_{C1} equaling i_{D2} ; Mode E: End with i_{C1} dropping to 0; Mode I: End with i_{C3} dropping to 0; Mode J: End with i_{C1} dropping to 0.

According to the states of Mode A–Mode G shown in Figure 2, the relationship between inductors and a current ripple can be obtained as

$$L_{\rm M} + L_{\rm a} + L_{\rm r} = \frac{U_{\rm in}d}{2f\alpha I_{\rm L}} \tag{1}$$

where α is the current ripple coefficient. The output filtering capacitors are chosen to be large enough that the voltage ripples can be limited well. Therefore, the relationship between C_4 and its voltage ripple can be obtained as

$$C_4 \ge \frac{\Delta i_{\rm L} T_{\rm s}}{8\Delta u} = \frac{\alpha I_{\rm L} T_{\rm s}}{8\Delta u} \tag{2}$$

3.2. Analysis of Ripple Minimization Characteristics

Assume that the capacitors and the inductors employed are large enough, and the forward voltage and the on-state resistances of all semiconductors are negligible. The average voltages across C_1 , C_2 , C_3 , and C_4 are U_{C1} , U_{C2} , U_{C3} , and U_{C4} respectively; U_{in} is the steady input voltage; u_{La} is the instantaneous inductor voltage; the instantaneous current flowing into L_a is i_{La} and the average inductor current is I_{La} ; and the duty cycle is d.

Over the whole switching period, the input inductor L_a , the capacitor C_1 , and the capacitor C_4 form a closed circuit loop, and the following equation can be derived by applying Kirchhoff's Voltage Laws (KVLs):

$$\begin{cases} u_{La} = u_{in} - u_{C4} + u_{C1} \\ u_{La} = L_a \frac{di_{La}(t)}{dt} \end{cases} ,$$
(3)

where u_{in} is the instantaneous input voltage, and u_{c1} and u_{c4} are the instantaneous voltages across C_1 and C_4 .

Considering the steady state, the inductor L_a satisfies the voltage second balance principle, and thus the average voltage across the inductor L_a is zero in each switching period. Therefore, Equation (4) can be obtained. The voltage ripples across C_1 and C_4 are very close to zero, and the input voltage is regarded as constant in a switching period, so the instantaneous inductor voltage u_{La} is very small, according to Equation (3). Therefore, the current ripple of the inductor current i_{La} can be regarded as zero, which means that input current ripple minimization can be realized:

$$\begin{cases} U_{C1} = U_{C4} - U_{in} \\ U_{La} = 0 \end{cases} .$$
 (4)

It can be seen that the characteristics of current ripple minimization are affected by L_a , u_{C1} , and u_{C4} . The capacitor voltage fluctuation is smaller if the capacitances of C_1 and C_4 are larger, which is beneficial to the realization of current ripple minimization.

3.3. Voltage Gain Analysis

In a steady state, neglecting the other transient state modes, the main modes (Mode F, Mode G, and Mode K) are analyzed. In view of the influence of leakage inductance on the voltage gain, the coupling coefficient $k = L_M/(L_M + L_r)$ is introduced.

When the power switch Q is turned on, the voltage across the primary side n_p of the ideal transformer is equal to kU_{in} , while the voltage across the secondary side n_s is $U_{C2} - U_{C4}$. Equation (5) can be obtained:

$$nkU_{\rm in} = U_{\rm C4} - U_{\rm C2}.$$
 (5)

When the power switch Q is turned off, the voltage across the primary side n_p is changed to kU_{C1} , and the voltage across the secondary side n_s becomes $U_{C3} - U_{C2}$. Therefore, Equation (6) can be obtained:

$$nkU_{\rm C1} = U_{\rm C3} - U_{\rm C2}.$$
 (6)

Applying the voltage second balance principle to the magnetizing inductor $L_{\rm M}$ yields Equation (7):

$$kU_{\rm in}d = k(U_{\rm C4} - U_{\rm in})(1 - d). \tag{7}$$

From Equations (4)–(7), the voltages across C_1 , C_2 , C_3 , and C_4 can be derived as

$$\begin{cases} U_{C1} = \frac{d}{1-d} U_{in} \\ U_{C2} = \frac{nk-nkd+1}{1-d} U_{in} \\ U_{C3} = \frac{nk+1}{1-d} U_{in} \\ U_{C4} = \frac{1}{1-d} U_{in} \end{cases}$$
(8)

Above all, the voltage gain *M* of the proposed converter can be expressed as

$$M = \frac{U_{\text{out}}}{U_{\text{in}}} = \frac{U_{\text{C3}} + U_{\text{C4}}}{U_{\text{in}}} = \frac{nk + 2}{1 - d}.$$
(9)

3.4. Analysis of Passive Lossless Clamping Circuit

As can be seen in Figure 2h, the diode D_1 and the capacitor C_4 form a passive lossless clamping circuit. C_4 can absorb the energy stored in the leakage inductance through D_1 and limit the voltage stress across the power switch Q to U_{C4} . This passive lossless clamping circuit provides a path for transmitting leakage inductance energy to the load. Moreover, it can raise the efficiency of the converter and suppress the voltage spike across the power switch Q caused by leakage inductance L_r .

4. Voltage and Current Stresses and Performance Comparisons

4.1. Voltage Stresses

In view of the analysis of the operating modes, the power switch Q and the capacitor C_4 are connected in parallel when Q is turned off, and D_2 is connected to the capacitor C_3 in parallel when D_2 is turned off. In other words, the voltages across Q and C_4 are equal, and the voltage stress across D_2 is U_{C3} . The voltage stresses across Q and D_2 can be derived as

$$U_{\rm Q} = U_{\rm C4} = \frac{1}{1-d} U_{\rm in},\tag{10}$$

$$U_{\rm D2} = U_{\rm C3} = \frac{nk+1}{1-d} U_{\rm in}.$$
 (11)

Similarly, the voltage stress across D_1 is U_{C4} and the voltage stress across D_3 is U_{C3} when Q is turned on. Thus, the voltage stresses across D_1 and D_3 can be derived as

$$U_{\rm D1} = U_{\rm C4} = \frac{1}{1-d} U_{\rm in},\tag{12}$$

$$U_{\rm D3} = U_{\rm C3} = \frac{nk+1}{1-d} U_{\rm in}.$$
 (13)

It can be concluded that the voltage stresses across the power switch Q and the diode D_1 are independent of the coupled inductors and are only related to the duty cycle d and the input voltage U_{in} . The voltage stresses across diode D_2 and diode D_3 are not only related to d, but are also related to

the turns ratio *n*. Hence, it is beneficial to choose a desired turns ratio *n* for the coupled inductors to obtain a trade-off between the voltage gain and the voltage stresses across D_2 and D_3 .

4.2. Current Stresses

To simplify the calculation of current stresses, the influence of leakage inductance is neglected, which means k = 1 (see Figure 4). When the power switch Q is turned on, the currents flowing into C_1 , C_2 , C_3 , and C_4 are I_{C1on} , I_{C2on} , I_{C3on} , and I_{C4on} ; and the current flowing into L_a is I_{Laon} . I_{npon} is the current flowing into the primary side of the ideal transformer, while I_{nson} is the current flowing into L_r is I_{Lron} . I_{D2} is the current of D_2 . I_{inon} and I_{outon} are the input current and the output current, respectively.



Figure 4. The current distribution in different states: (a) *Q* is turned on; (b) *Q* is turned off.

When the power switch Q is turned off, the currents flowing into C_1 , C_2 , C_3 , and C_4 are I_{C1off} , I_{C2off} , I_{C3off} , and I_{C4off} ; the current flowing into L_a is I_{Laoff} ; and the currents flowing into both sides of the ideal transformer are I_{npoff} and I_{nsoff} . I_{LMoff} is the current flowing into L_M , and the current flowing into L_r is I_{Lroff} . I_{D1} is the current of D_1 , while I_{D3} is the current of D_3 . The input current and the output current are I_{inoff} and I_{outoff} , respectively.

By applying the ampere second balance principle to C_1 – C_4 , the equations can be derived as

$$I_{C1on}d = I_{C1off}(1-d)$$

$$I_{C2on}d = I_{C2off}(1-d)$$

$$I_{C3on}d = I_{C3off}(1-d)$$

$$I_{C4on}d = I_{C4off}(1-d)$$

$$(14)$$

According to Figure 4a, it can be deduced that

$$\begin{pmatrix}
I_{C3on} = I_{outon} \\
I_{C1on} + I_{C2on} + I_{C3on} = I_{C4on} \\
I_{Laon} + I_{C1on} = I_{LMon} + I_{npon} \\
I_{npon} = nI_{nson} = nI_{C2on}
\end{cases}$$
(15)

Similarly, Equation (16) can be derived from Figure 4b:

$$I_{\text{Laoff}} = I_{\text{C1off}} + I_{\text{LMoff}} - I_{\text{npoff}}$$

$$I_{\text{C2off}} = I_{\text{C3off}} + I_{\text{outoff}}$$

$$I_{\text{Laoff}} - I_{\text{outoff}} = I_{\text{C4off}}$$

$$I_{\text{npoff}} = nI_{\text{nsoff}} = nI_{\text{C2off}}$$
(16)

Considering that the load is resistive, and the currents flowing into L_a and L_M are assumed to be constant, Equation (17) can be derived:

$$I_{\text{outon}} = I_{\text{outoff}} = I_{\text{out}}$$

$$I_{\text{Laon}} = I_{\text{Laoff}} = I_{\text{La}} \quad . \tag{17}$$

$$I_{\text{LMon}} = I_{\text{LMoff}} = I_{\text{LM}}$$

In terms of Equations (14)–(17), the capacitor currents can be deduced as Equations (18) and (19):

$$\begin{cases}
I_{C1on} = \frac{n}{d}I_{out} \\
I_{C1off} = \frac{n}{1-d}I_{out} \\
I_{C2on} = \frac{1}{d}I_{out} \\
I_{C2off} = \frac{1}{1-d}I_{out} \\
I_{C3onf} = I_{out} \\
I_{C3off} = \frac{d}{1-d}I_{out} \\
I_{C4on} = \frac{1+n+d}{d}I_{out} \\
I_{C4off} = \frac{1+n+d}{1-d}I_{out} \\
I_{L4off} = \frac{n+2}{1-d}I_{out} \\
\end{cases}$$
(18)
(19)

The current stresses of the power switch Q and the diode D_2 can be obtained according to Figure 4a, Equations (18) and (19):

$$I_{\rm Q} = I_{\rm La} + I_{\rm C4on} - I_{\rm C3on} = \frac{n+2d}{(1-d)d} I_{\rm out},$$
(20)

$$I_{\rm D2} = I_{\rm C2on} = \frac{1}{d} I_{\rm out}.$$
 (21)

Similarly, the current stresses of D_1 and D_3 can be obtained by means of Figure 4b, Equations (18) and (19):

$$I_{\rm D1} = I_{\rm La} - I_{\rm C1off} - I_{\rm C2off} = \frac{1}{1 - d} I_{\rm out},$$
(22)

$$I_{\rm D3} = I_{\rm C2off} = \frac{1}{1-d} I_{\rm out}.$$
 (23)

4.3. Performance Comparisons

The proposed converter was compared to the converter in Reference [29] without considering the influence of leakage inductance. The specific comparisons are shown in Table 1. The voltage stress across the diode D_1 was larger than the output voltage in the converter of Reference [29], while the voltage stresses across all semiconductors in the proposed converter were less than the output voltage. Moreover, the proposed converter could achieve a much higher voltage gain at the cost of one more diode and one more capacitor. The voltage gain M versus the duty cycle d is shown in Figure 5 when the turns ratio n is equal to 1 and 2.

Converter in [29]	Proposed Converter
(nd+1)/(1-d)	(n+2)/(1-d)
$\frac{1}{1-d}U_{in}$	$\frac{1}{1-d}U_{in}$
$D_{\mathbf{C}}: \frac{1}{1-d}U_{\mathbf{in}}$	$D_1: \frac{1}{1-d}U_{\text{in}}$
$D_1: \frac{n+1}{1-d}U_{in}$	$D_2, D_3: \frac{n+1}{1-d}U_{in}$
$\frac{nd+1}{(1-d)d}I_{\text{out}}$	$\frac{n+2d}{(1-d)d}I_{\text{out}}$
$D_{\rm C}: \frac{nd+1}{2(1-d)d}I_{\rm out}$	$D_1, D_3 : \frac{1}{1-d}I_{\text{out}}$
$D_1: \frac{nd+1}{(1-d)d}I_{\text{out}}$	$D_2: \frac{1}{d}I_{\text{out}}$
1	1
2	3
Yes	Yes
	Converter in [29] (nd + 1)/(1 - d) $\frac{1}{1-d}U_{in}$ $D_C: \frac{1}{1-d}U_{in}$ $D_1: \frac{n+1}{1-d}U_{in}$ $\frac{nd+1}{(1-d)d}I_{out}$ $D_C: \frac{nd+1}{2(1-d)d}I_{out}$ $D_1: \frac{nd+1}{(1-d)d}I_{out}$ 1 2 Yes

Table 1. Comparisons of two types of converters with input current ripple minimization.



Figure 5. Curves of voltage gain versus duty cycle for two types of converters with input current ripple minimization.

5. Experimental Results and Analysis

In order to validate the feasibility of the proposed converter, a 400-W prototype was developed, as shown in Figure 6. An adjustable DC source with a voltage range of $U_{in} = 30-100$ V was used as the input of the converter to simulate a fuel cell source. The output voltage was controlled to 400 V by a voltage loop implemented on a digital signal processor (DSP) TMS320F28335. The experiment parameters are listed in Table 2. According to Equation (1), the current ripple coefficient α is defined as 0.2, and a large L_a can reduce the input current ripple: Therefore, L_a and L_M were taken as 241 μ H and 368 μ H, respectively. From Equation (2), the voltage ripple Δu is defined as 0.5 V. Considering practical experience and the laboratory conditions, C_2 – C_4 were taken as 540 μ F, and C_1 was taken as 270 μ F.

The voltage stresses across all of the semiconductors for d = 0.625 and $U_{out} = 400V$ are shown in Figure 7. Figure 7a shows the voltage stresses across Q and D_1 , which were equal to 133 V, while Figure 7b shows the voltage stresses across D_2 and D_3 , which were 267 V, which was consistent with the theoretical analysis. In addition, the energy stored in the leakage inductance was released through the diode D_1 when Q was turned off. As a result, the voltage spike across the power switch Q was reduced significantly. The current flowing into the inductor L_a and the voltage across the capacitor C_1 are shown in Figure 8. The input current I_{in} , which flowed into L_a , had no fluctuation in each switching period, and neither did the voltage across C_1 . Thus, it could be concluded that input current ripple minimization was achieved, as analyzed in Section 3.2. Figure 9 shows the currents flowing into both sides of the coupled inductors. The capacitor C_2 received energy from the coupled inductors when Qwas turned on. On the contrary, the current I_{Lp} flowing into the primary side started to decrease when Q was turned off, C_2 started to discharge, and the current I_{Ls} flowing into the secondary side transferred energy to the load through D_3 . The experimental results were consistent with the theoretical analysis.



Figure 6. The experimental prototype of the proposed converter.

	Parameters	Values	-
	Rated power P _n	400 W	-
	Switching frequency f_s	20 kHz	
	Capacitor C_1	270 µF	
	Capacitors C_2 , C_3 , and C_4	μ 540 μF	
	Inductor L _a	241 μH	
	Magnetizing inductor L_M	1 368 μH	
	Leakage inductance L_r	3.25 μH	
	Turns ratio $n_{\rm p}:n_{\rm s}$	1:1	
	Output voltage U _{out}	400 V	
	Input voltage U _{in}	30–100 V	
	Power switch Q	IXTH88N30P	
	Diodes D_1 – D_3	DPG60C300HB	
	-		-
		· · · · · · · · · · · · · · · · · · ·	
			U _{D2} (100V/div)
d d	= 0.625	d = 0.625	
A		A:	*
······································	$J_{\rm D1}(100\rm V/div)$		$U_{\rm D2}(100\rm V/div)$
janan ja	Bernet Berne		
B	t(10 us/div)	B	$t(10\mu s/div)$
A=100 U B=100 U	10μs Tria: ΑΓ	A=100 V B=100 V	10µs Trig: AJ

Table 2. Experiment parameters.



(a)

(b)



Figure 8. The current flowing into the inductor L_a and the voltage across the capacitor C_1 .



Figure 9. The currents flowing into both sides of the coupled inductor.

Figure 10 shows that with the voltage control loop, the output voltage U_{out} could be kept constant at 400 V, even when the input voltage U_{in} varied from 30 V to 100 V continuously. This demonstrated that the proposed converter could operate well in a wide voltage gain range from 13.33 to 4.



Figure 10. The output voltage and the wide-range input voltage from 30 V to 100 V.

The efficiencies of the proposed converter with different input voltages and different powers were measured by a power analyzer (YOKOGAWA/WT3000), as shown in Figure 11. When the input voltage $U_{in} = 100$ V and the load power P = 400 W, the proposed converter reached a maximum conversion efficiency of 95.12%. The minimum efficiency was 89.24% when the input voltage $U_{in} = 40$ V and the load power P = 400 W. To sum up, with the same power, as the voltage gain increased (i.e., the input voltage decreased), the efficiency of the proposed converter decreased. Since the input current rose as the low-side voltage decreased, the copper loss and the switching losses of the converter rose. Therefore, the efficiency of the converter appeared to degrade at a high voltage gain.



Figure 11. Efficiencies of the proposed converter with different output powers at different input voltages (i.e., different voltage gains) when $U_{out} = 400$ V.

6. Conclusions

A coupled-inductor DC-DC converter with a high voltage gain and input current ripple minimization was proposed in this paper. The converter can obtain a wide voltage gain range, and the voltage stresses across all semiconductors are lower than the output voltage. In addition, the proposed converter can benefit from the minimization of input current ripples. Furthermore, the passive lossless clamping circuit effectively suppresses voltage spikes caused by leakage inductance. Therefore, it is a good candidate for the power interface of fuel cell vehicles.

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