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Review

Low-Voltage GaN FETs in Motor Control Application; Issues and Advantages: A Review

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Abstract: The efficiency and power density improvement of power switching converters play a crucial role in energy conversion. In the field of motor control, this requires an increase in the converter switching frequency together with a reduction in the switching legs' dead time. This target turns out to be complex when using pure silicon switch technologies. Gallium Nitride (GaN) devices have appeared in the switching device arena in recent years and feature much more favorable static and dynamic characteristics compared to pure silicon devices. In the field of motion control, there is a growing use of GaN devices, especially in low voltage applications. This paper provides guidelines for designers on the optimal use of GaN FETs in motor control applications, identifying the advantages and discussing the main issues. In this work, primarily an experimental evaluation of GaN FETs in a low voltage electrical drive is carried out. The experimental investigation is obtained through two different experimental boards to highlight the switching legs' behavior in several operative conditions and different implementations. In this evaluative approach, the main GaN FETs' technological aspects and issues are recalled and consequently linked to motion control requirements. The device's fast switching transients combined with reduced direct resistance contribute to decreased power losses. Thus, in GaN FETs, a high switching frequency with a strong decrease in dead time is achievable. The reduced dead time impact on power loss management and improvement of output waveforms quality is analyzed and discussed in this paper. Furthermore, input filter capacitor design matters correlated with increasing switching frequency are pointed out. Finally, the voltage transients slope effect (dv/dt) is considered and correlated with low voltage motor drives requirements.

Keywords: GaN FET; low voltage inverter; dead time; power stage integration; light e-mobility; gan fet driver circuit; dv/dt in switching leg; input current and voltage ripple

Citation: Musumeci, S.; Mandrile, F.; Barba, V.; Palma, M. Low-Voltage GaN FETs in Motor Control Application; Issues and Advantages: A Review. *Energies* **2021**, *14*, 6378. https://doi.org/10.3390/en14196378

Academic Editor: Mario Marchesoni

Received: 6 September 2021
Accepted: 4 October 2021
Published: 6 October 2021

1. Introduction

In the application scenario of motion control, low voltage high dynamic drives are widely used. Low voltage drives (<100 V) are applied in several advanced technological fields such as robotics, home appliances, warehousing automation, CNC machines, e-mobility and unmanned aerial vehicles (UAVs) [1–3]. The electrical drive's dynamic performance is strongly influenced by the technology of the power switches on which the inverter's topology is based. In the field of low voltage switching devices (with breakdown voltage up to 100 V), silicon (Si) MOSFETs with in trench-gate technology are low-cost standard switches available in a wide range of current rating and can reach quite satisfactory high switching frequencies [4,5]. Nowadays, high electron mobility transistors (HEMT) Gallium Nitride (GaN) devices are becoming increasingly used, especially in low voltage applications, due to their superior features, such as high dynamic characteristics, high power density and very high-temperature ratings, compared to pure silicon MOSFET devices with similar current rating [6]. In high voltage applications, GaN devices are in continuous development and compete with silicon carbide (SiC) MOSFETs, silicon (Si)

super junction MOSFETs and IGBTs, which have higher technological maturity [7]. The penetration of GaN devices in these sectors is still partially due to the lower breakdown voltage (up to 650 V, currently available on the market) and only for specific applications with high switching frequency (up to a few MHz range) [7].

In low voltage applications for power ratings up to 400 W, there are also integrated switching leg solutions which include a driver circuit in the same package. This monolithic approach acts by reducing parasitic inductances and optimizing switching performance to reduce losses and ringing voltage, thus allowing the designer to downsize cooling requirements and improving converter reliability [8]. For a higher power rate, discrete GaN FETs (Field Effect Transistors) are used to reach high current density switching legs. However, wide bandgap (WBG) GaN devices allow higher switching frequency in inverter topologies for drive applications compared with silicon MOSFETs. The switching frequency increase also leads to some advantages. It minimizes the current ripple in the motor and enables the reduction of overall capacitance value in the DC link, allowing the replacement of electrolytic with smaller non-polarized capacitors [9]. Furthermore, the GaN FETs high switching transients, both in the rise time and the fall time, leads to a strong reduction of the dead time in the switching leg circuits. In the inverter leg, the dead time duration influences the quality of the output waveforms of the voltage, increasing the number of harmonics, thus worsening the total harmonic distortion (THD) [10]. The waveforms distortion caused by dead time is affected by its length, given the switching frequency and the input DC voltage. The reduction of dead time enabled by advanced GaN FETs as a switching solution improves the shape of the waveforms without the use of dedicated software resources to compensate for the waveform distortion drawbacks [11].

In this paper, the main advantages and disadvantages of GaN FETs in inverter topologies for low voltage high dynamic performance electrical drives are analyzed and discussed. The impact of HEMT devices in high power density electrical drive evolution is pointed out considering the state of art and perspectives. The use of GaN FETs allows integration of inverter topologies with AC motors to realize a compact and reliable motor control system [12,13]. The integration of the electric machine and its driving topology is beneficial to electric motor drive modularity, avoiding electrical cables, reducing voltage ringing and EMI content [14]. Furthermore, in an integrated modular motor drive (IMMD) the cooling system can be achieved by the motor case. These benefits are more noticeable in multiphase motor drives [15].

The article provides a wide investigation on the extensive use of low voltage GaN FET devices in motion control applications. Clear information to the design of the technological and application benefits of these HEMT devices for ever smaller and more reliable applications of electric drives is presented. The troublesome features of these devices are also considered, and possible solutions or reductions in drawbacks presented. The GaN FETs advantages and issues are carried out primarily by an experimental investigation approach. The main results were obtained using two experimental inverter boards. In one of these experimental boards, the switching legs were implemented with an integrated solution, while the other inverter board was equipped with higher power density GaN FETs to evaluate several operative conditions.

Furthermore, the paper deals with the impact of switching frequency increasing in GaN FETs in the design of inverter DC link capacitors. In addition, the problems of high dv/dt and the benefits of dead time reduction are explored. Moreover, the problems of layout and reductions of parasitic inductances are pointed out. Current measurement conditions in the noise environment due to the highest achievable switching frequencies are also considered.

The paper is structured as followings. In Section 2 the power stages are described considering the technology issue, the layout matter and the main gate driver requirements. In Section 3, the input current and voltage ripple issues are analyzed at increasing switching frequencies to evaluate the impact on the passive device design. In Section 4 the dead time reduction benefits are considered and discussed. In Section 5, the voltage transients (dv/dt)

effect in the switching leg and motor drive application is further investigated. Finally, in Section 6, switching evaluation of an enhanced inverter board with discrete GaN FETs solution is carried out.

2. GaN FETs-Based Inverter Legs Power Stage

GaN FETs in efficient power conversion applications help designers in increasing power density compared to equivalent pure silicon current rate MOSFETs. To understand the benefits and drawback of the HEMT applications, an overview of the GaN FETs technology is required.

2.1. Low-Voltage GaN FETs Operation and Technology Survey

Low-voltage HEMT switches applied in the inverter topologies switching legs are an enhancement-mode gallium nitride transistor. GaN FETs are normally-off devices that operate in a very similar way to silicon power MOSFETs. The physical structure is shown in Figure 1, highlighting both the inner resistances and parasitic capacitance distributions. The key role of the HEMT operation is the two-dimensional electron gas (2DEG) phenomenon acting at the interface between a heterostructure of AlGaN and GaN [16]. 2DEG causes high mobility of electrons by lowering the conduction resistance compared with a MOSFET of similar current density. The 2DEG zone is indicated in Figure 2a.

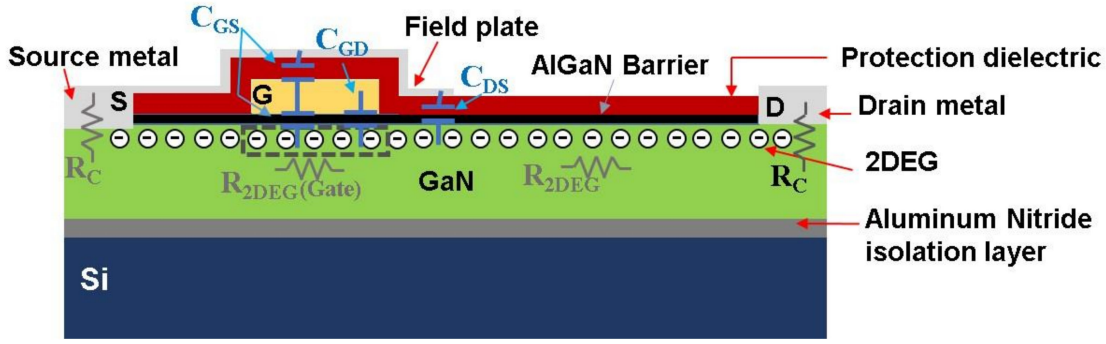

Figure 1. Simplified enhancement-mode GaN FET structure. The physical structure is shown in the on-state operation with the activated channel under the gate (dotted line). The 2DEG area is indicated. The on-resistances and the parasitic capacitors distribution are also highlighted.

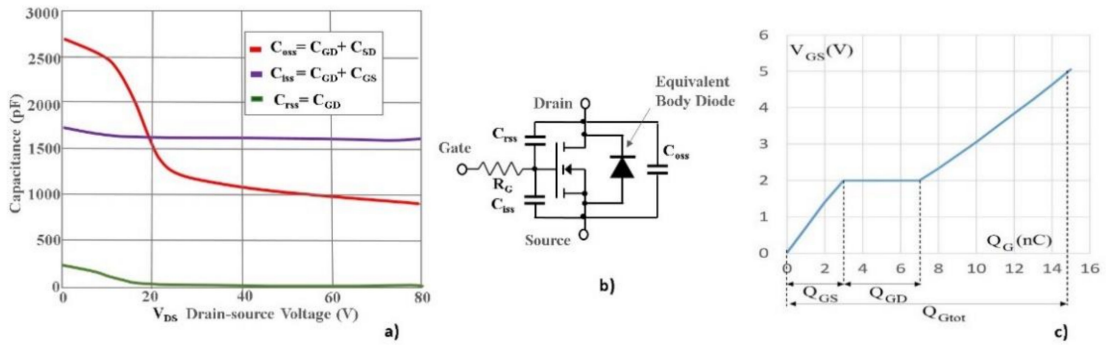

Figure 2. (**a**) Parasitic capacitors behaviour versus drain source voltage (VDS) variation. (**b**) GaN FET model with parasitic capacitors, inner gate resistor and equivalent body diode symbol. (**c**) Gate charge of 80 V 1.8 mΩ HEMT GaN FET (EPC2206).

To turn on the GaN FET, a positively charged (p-type) p-Gate is grown on top of the AlGaN barrier. When the p-Gate is positively polarized (with respect to the source) it acts as an enhancement-mode structure leading to a field-effect creating a conduction channel. The positive gate voltage attracts electrons under the gate zone, restoring the bidirectional channel between the drain and the source sections. The depletion layer area under the p-Gate area is restored when the positive voltage between gate and source is removed

(turn-off process). At the turn-off condition, block voltage capability is achieved. The main device technology characteristics for evaluation in device operation investigation are the following

- gate threshold,
- conduct resistance and temperature behaviour,
- structure parasitic capacitors,
- reverse conduction mode.

The threshold voltage V_{GSth} is the gate-source voltage that allows the starting channel current conduction in the planar structure of Figure 1. It depends on the p doping of the gate area and of AlGaN/GaN HEMT on the doped AlGaN layer thickness [17]. Furthermore, in low voltage GaN FETs, the V_{GSth} features a low dependence on the temperature compared to MOSFET devices.

The GaN FET planar structure (Figure 1) features a low direct resistance when the channel between the source and drain is created. The inner resistance of the GaN FETs structure is composed of the sum of the contact resistances of the drain and source metal with the 2DEG (the R_C resistances in Figure 1) and the resistances related to the 2DEG region. In the 2DEG region under the gate, the electron concentration depends on both the technological characteristics of the gate structure (p-Gate in this case of study) and the gate-source voltage level [17]. Under the gate, the 2DEG region features a further specific resistance value called $R_{2DEG(gate)}$. In Figure 1 the inner resistances distribution is depicted considering the 2DEG region (R_{2DEG}), the specific gate contribution $R_{2DEG(gate)}$ and the two contact resistances R_C before described. The whole inner resistance is given by

$$R_{on,GaN} = 2 \cdot R_c + R_{2DEG} + R_{2DEG(Gate)} \quad (1)$$

R_{2DEG} is related to several technological parameters such as electronic mobility (μ_{2DEG}), the quantity of electrons in the 2DEG area (N_{2DEG}), the length of the 2DEG channel (L_{2DEG}) between the source and drain, and the 2DEG width (W_{2DEG}) [17]. Furthermore, it is also reliant on the charge constant q ($1.6 \cdot 10^{-19}$ C) as described in the following

$$R_{2DEG} = \frac{L_{2DEG}}{q \cdot \mu_{2DEG} \cdot N_{2DEG} \cdot W_{2DEG}} \quad (2)$$

Considering thermal behavior, the GaN FET shows a positive temperature coefficient as with the MOSFET device [18].

In Figure 1, the parasitic capacitor distribution is depicted. The C_{GS} is composed of the contribution of two capacitors. The first is the capacitor between the gate and the field plate. The second is the junction capacitance obtained between the gate to the planar channel. The C_{GD} value is lower compared to C_{GS} (Figure 2c). The structure design results in excellent dv/dt immunity. Furthermore, the C_{GS} obtained is small, and equivalent to a low-voltage and current density silicon MOSFET device. The reduced C_{GS} allows very short delay times, reducing the overall switching time. C_{DS} is the main contributor of the C_{oss} output capacitance ($C_{oss} = C_{DS} + C_{GD}$). C_{oss} is also remarkably lower than in a MOSFET of equivalent characteristics. Consequently, the power losses P_{Coss} described in (3) are reduced.

$$P_{C_{oss}} = \frac{1}{2} \cdot f_{sw} \cdot C_{oss} \cdot V_{DS} \quad (3)$$

where f_{sw} is the switching frequency and V_{DS} is the drain to source voltage [19].

The capacitors' behavior versus Drain to Source voltage variation for an 80 V device with a typical $R_{DS,on}$ = 1.8 mΩ are depicted in Figure 2c.

The input capacitors, C_{iss} and C_{rss}, are described in the simplified GaN FET model (composed with the MOSFET symbol for GaN device) in Figure 2b. These input capacitors are involved in the gate charge (Q_G). The gate charge curve is similar to that of a MOSFET device (as shown in Figure 2c). The GaN FET structure strongly reduces Q_G. The total gate charge (Q_{Gtot}) necessary for switching on the GaN FET is related to a V_{GS} of 5 V. In

Figure 2c the Q_{GS} and Q_{GD} quantity relative to the contribution of G_{GS} and C_{GD} are also indicated. The gate charges Q_G and $R_{DS,on}$ are the two parameters needed to optimize the GaN Figure of Merit (FOM) [19].

$$FOM = R_{DS,on} \cdot Q_{Gtot} \tag{4}$$

The FOM is more much more advantageous than in a MOSFET device with equivalent current density and breakdown voltage. Furthermore, the gate Q_{Gtot} (Figure 2c) sets the minimum rise time $t_{rise,min}$ for the gate voltage transient as

$$t_{rise,min} = \frac{Q_{Gtot} \cdot R_G}{V_{GS}} \tag{5}$$

where R_G is the gate resistance and V_{GS} is the fixed gate voltage (V_{GS} = 5 V in the used GaN FETs) [20].

The GaN FET structure is a lateral device (Figure 1) without a bipolar parasitic device such as the body diode of MOSFETs. It is a natural bidirectional device acting with a V_{GS} suitably over the threshold voltage (V_{GS} = 5 V in the case of study) to obtain the 2DEG condition. When HEMT GaN operates in the reverse conduction, it features almost the same resistance characteristics as in direct operation. Below the threshold voltage, the GaN FET does not have a p-n diode like the MOSFET device, but it shows such behavior. In reverse conduction, the reverse voltage source to drain (V_{SD}) characteristic curve is quite similar to a diode with a less steep slope. Furthermore, the V_{SD} characteristic has a positive temperature coefficient with respect to the case of the MOSFET in which the direct voltage V_F of the body diode decreases with increasing temperature. The reverse conduction with V_{GS} = 0 shows a higher V_{SD} typical of 1.7 V up to 2 V higher than a MOSFET. On the contrary of MOSFET, in the enhancement-mode GaN structure, the minority carriers typical of a p-n diode thus are not involved in the reverse conduction operation consequently, the reverse recovery charge (Q_{rr}) does not appear [21].

2.2. Packaging Issue and Integrating Solutions

The package solution plays a crucial role in stray inductance reduction to allow the increase of switching frequencies without high ringing in the switching waveforms and to avoid voltage overshoot. A low-inductance package design acts in decreasing power dissipation and limits electromagnetic interference (EMI). In a GaN FET, the die size is smaller than in a MOSFET of equivalent current density and breakdown voltage with a noticeable package volume reduction. The GaN FET packages must feature efficient cooling paths at the top and at the bottom areas. Furthermore, in the case of a half-bridge solution for a high side device, electrical insulation is necessary to a ground-referenced heat sink. In a monolithic half-bridge solution, the substrate is maintained at the low side source potential [17]. A package solution for low voltage discrete GaN FETs considered in this paper is the EPC® (Efficient Power Conversion) chip-scale package (CSP) arrangement. In this package arrangement, "solderable bars" are grown on the surface of the device. After this process the chip is flipped and soldered directly onto a printed circuit board (PCB). The CSP solution leads to a noticeable parasitic inductance reduction. Furthermore, efficient cooling paths can be achieved. The CSP solution is depicted in Figure 3. The solderable bars are shown in Figure 3a with the pin connections. The package assembly on the PCB is drawn in Figure 3b. Finally, a photo of a PCB top layer of a half-bridge circuit with discrete device in CSP arrangement is shown in Figure 3c.

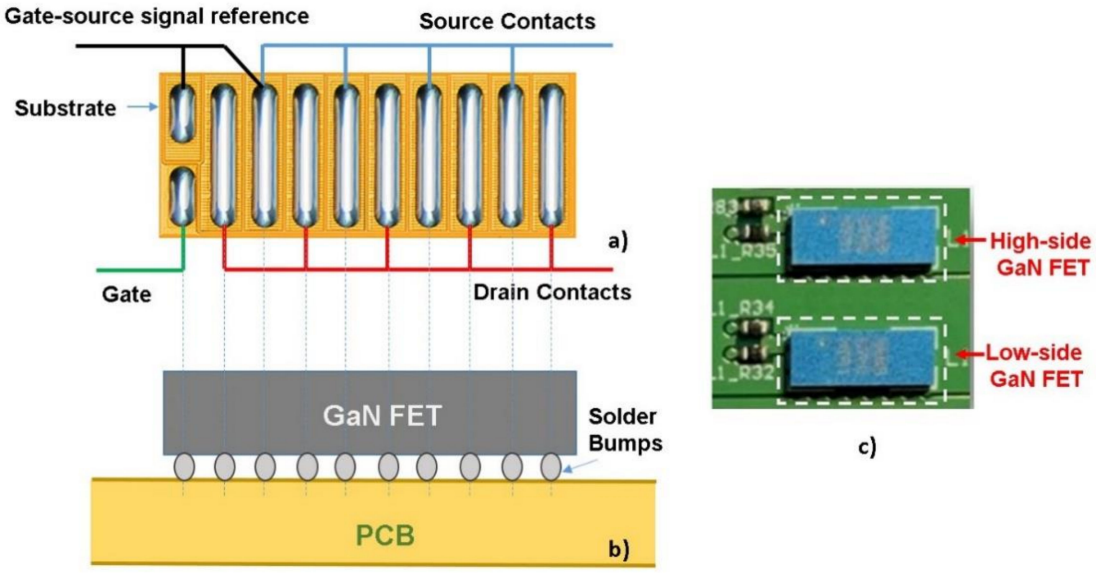

Figure 3. (**a**) Solderable bars package solution with connection of the source, drain, gate and substrate contacts. (**b**) Package and PCB assembly. (**c**) Photo of a top-layer of the PCB with a discrete device in the CSP solution for a half-bridge circuit.

Power Stage Integration

Recent developments of GaN technology allow the integration of a power stage half-bridge in a symmetric or asymmetric configuration [22,23] together with signal control circuits for low power converter applications (up to 400 W). The integration step allows driving the gate of the GaN FET and monitoring some device parameters. The power stage monolithic integration reduces the common source inductance (CSI), optimizing the power and gate loop inductances and, consequently, leads to an increase in switching performance. Furthermore, in the converter arrangement, the PCB layout is simplified. Moreover, the integration approach improves the system's reliability.

The monolithic power stage circuit integrated with the driver circuit realized in the HEMT GaN technological arrangement is reported in Figure 4. The power stage GaN FETs are composed of a maximum 80 V V_{DS} voltage with an $R_{DS,on}$ typically equal to 8.5 mΩ with a rated output current (@ f_{sw} =1 MHz), $I_{out,max}$ =15 A (GaN monolithic device—EPC 2152). The bias supply voltage is equal to 12 V.

A bootstrap circuit is provided to supply the voltage for the high side gate driver. In the monolithic arrangement, there are also two buffers to supply the requested gate current, a level shift circuit to control signal for the high side device, and a logic interface to the control signal to obtain a suitable dead time. Furthermore, an under voltage-lockout (UVLO) circuit is implemented. The integrated half-bridge circuit can be driven by CMOS or TTL logic levels signals coming, for example, from a microcontroller unit that runs a control algorithm.

The integrated modules based on GaN technology allow easy arrangement of a Brushless DC (BLDC) motor drive inverter. The power rate target of this inverter topology may be oriented to a light e-mobility such as in electrically-assisted bikes (typical e-bike power rate 250 W) as shown in Figure 5.

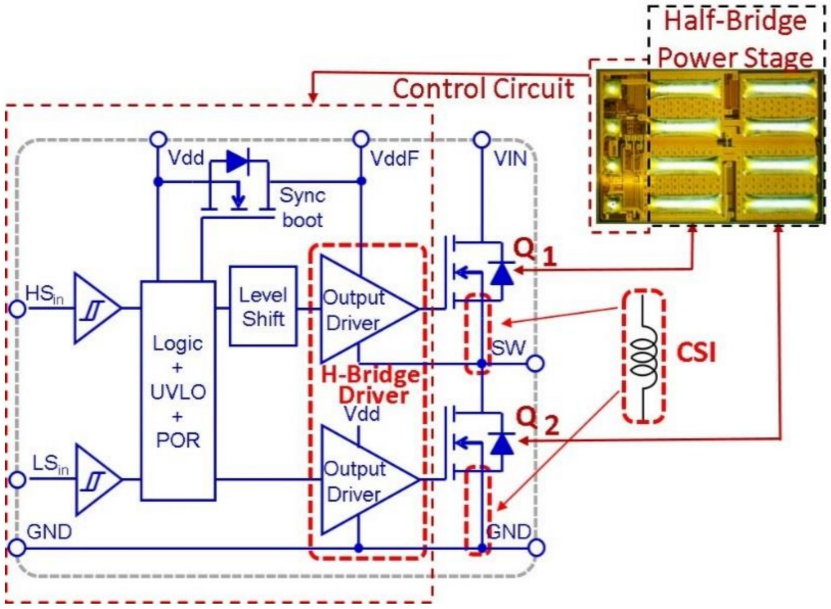

Figure 4. Principle scheme of a monolithic half-bridge GaN FETs with a driver circuit. The chip view is highlighted with the solderable bars package solution. The common source inductance position is depicted.

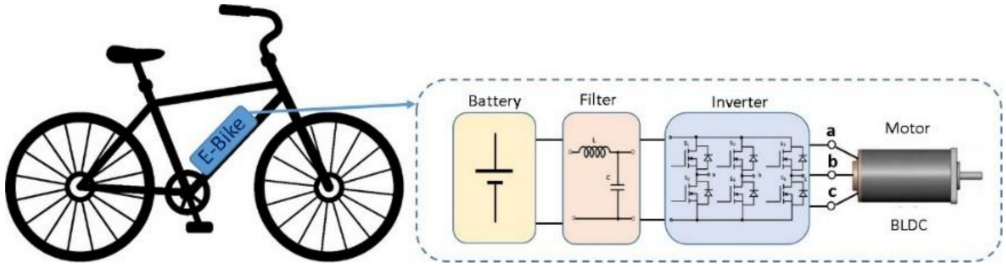

Figure 5. e-bike motor drive system schematic principle.

2.3. Inverter Circuit Arrangement

The two inverter circuits boards used in the experimental tests were based on 80 V of breakdown voltage GaN FETs. The first inverter circuit was based on the monolithic half-bridge circuit with driver circuit integrated on the same chip (EPC 2152). The schematic of a BLDC motor drive inverter board is shown in Figure 6a. It enables PWM switching frequencies up to 3 MHz with a maximum output current (I_a, I_b, I_c) of 10 A and a DC link voltage typically of 48 V (up to 60 V). At a 48 VDC supply voltage with switching frequency f_{sw} equal to 100 kHz, at a 21 ns dead-time setting the output maximum power rate is P_{out} = 400 W. The schematic presented is adapted from [24], where the characteristics of the board are dealt with in more detail. In Figure 6a, the current and voltage sense circuits are shown. Due to the voltage transient (dv/dt) caused by the GaN FETs switching, an LC- filter can be inserted in the output path of every single leg. It can be configured as either a low pass harmonic filter or an EMI filter. Furthermore, the connector pins are also described. In Figure 6b a picture of the inverter board top side is shown. In Figure 6b, the GaN FET power stage positions in the layout arrangement are highlighted with the shunt resistor, the control pin connector and Hall sensors or encoder interface.

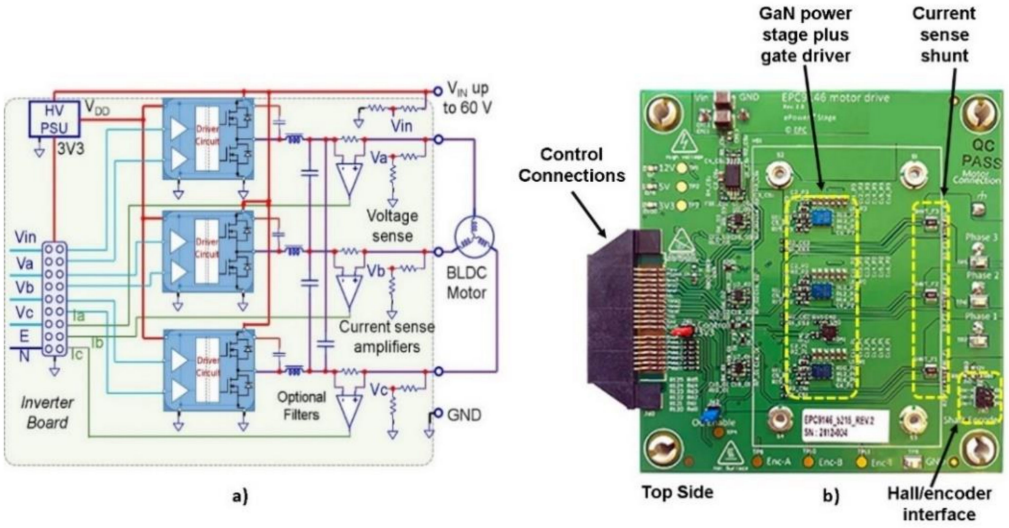

Figure 6. (**a**) Inverter board schematic. (**b**) Photo of the top side of the inverter board.

The second inverter experimental board is based on GaN FETs 80 V of breakdown voltage and a $R_{DS,on}$ equal to 1.8 mΩ (EPC2206). The switches in every bridge leg are based on two discrete GaN FET featuring a 6.1 × 2.3 mm package. The supply voltage is 48 V (the board was designed for a DC link voltage up to 60 V). The output phase current nominal was $15A_{rms}$. In the experimental board, there are two kinds of current sensing networks, source, and phase, and the user can decide which to use. Every bridge leg in the source path of a lower GaN FET has a sensing resistor R_S to measure the switching leg current, and to monitor the overcurrent to activate the protection circuit. The same signal can also be measured in phase through a phase current resistor R_{SL}. The maximum power is rated up to 1.5 kW. The general schematic of a battery powered inverter for PM sinusoidal drive with two the sensing current network is shown in Figure 7a. A picture of the inverter board top side is shown in Figure 7b with a zoomed view of a bridge leg arrangement and phase resistor.

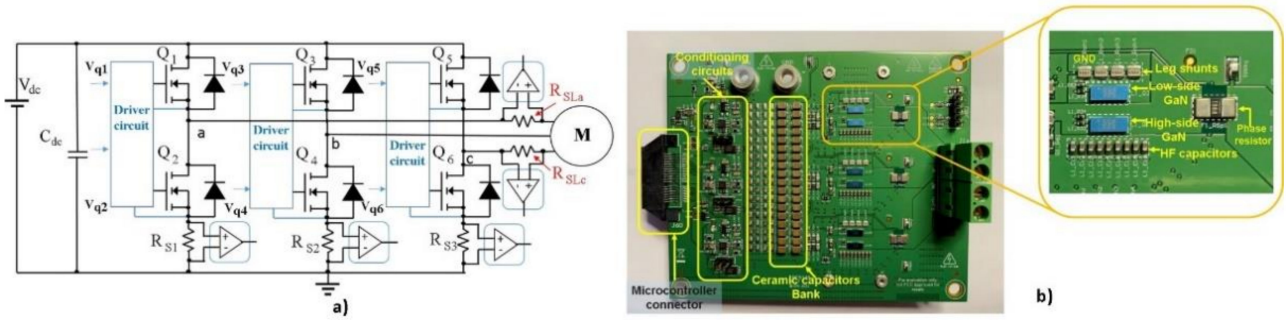

Figure 7. (**a**) Inverter board schematic with current sensing arrangement on the phase and in the switching leg (**b**) Photo of the top side of the inverter board with a zoomed view of a half-bridge relative to the phase a.

2.3.1. Notes on the Inverter Legs Layout

The switching leg layout is slightly more complex because there are leg shunts resistors. The main criterion to observe for optimal layout rules that guarantees the lowest inductance in the power loop is the symmetric arrangement in the component placement and the constraint of the entire high-frequency path in the top and first inner layers. Furthermore, by reducing stray inductance in the high-frequency power loop it is possible to decrease the drain overvoltage and reduce EMI contents [25]. Moreover, the power loop has a negative effect on the gating signal. Therefore, the length paths of the power loop and driver loop may be arranged as short as possible (power loop and gate loop are depicted in Figure 8). In this way, the coupling between these two loops is greatly significant.

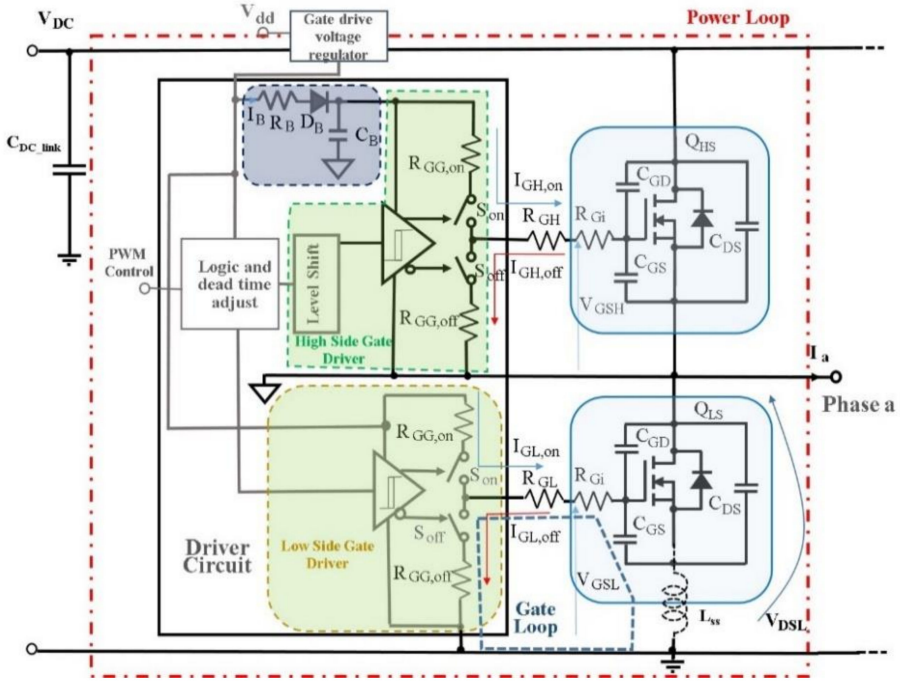

Figure 8. Schematic of the driver circuit and power stage of a switching leg (phase a).

Stray inductance reduction in the gate driver loop is achievable by placing the driver circuit on the back of the PCB board to reduce the distances between the driver output pins and both the gate and source kelvin pins of the GaN FET device. In this way it is feasible to obtain faster transients (8–10 V/ns with a gate resistance, R_G = 10 Ω) in switching and, consequently, a lower switching loss. Moreover, the leg shunt sensor resistor is made with four SMD resistors in a parallel connection (1 mΩ) to obtain a further reduction of parasitic inductance. A good practice for layout allows the routing of low voltage analog signals from the shunt resistors across the PCB, without picking noise, to the amplifiers and then to the microcontroller analog/digital converter pins. The main objective is to perform a kelvin measurement of the shunt resistor voltage and keep the signal traces as close as possible inside a Faraday cage made of analog ground layers above and below the routing layer.

2.3.2. Driver Circuit Requirements

The driver circuit is of crucial importance in obtaining the best performance for the GaN FETs. It supplies the gate charge requirement to speed-up the transients at turn-on and turn-off [26]. The device is driven in the on state by a 5 V pulse. In gallium nitride HEMT devices, the gate voltage cannot be raised above 6 V. To be turned off, V_{GS} must be in the range from 0 to −4 V. Generally, the solution of integrated driver circuits optimizes the parasitic inductances, by being placed in the layout as close as possible to the GaN FET [25]. In Figure 8, the driver circuit for an inverter leg is depicted. The GaN FET model with the parasitic capacitors and the stray inductor L_{SS} in the source path of LS are highlighted.

Through the driving resistance, it is possible, as in the case of a MOSFET, to control di/dt and the dv/dt. In many solutions, the on and off paths are made with different gate resistances. In the integrated solutions, the power supply of the high-side gate driver is provided by a bootstrap circuit in which the C_B capacitance (from Figure 8) must provide the gate charge required according to the following inequality:

$$C_B \geq \frac{Q_G}{V_{dd} - V_{FB} - R_B \cdot I_B - V_{GG,off}} \quad (6)$$

where $V_{GG,off}$ is the minimum voltage allowed across the capacitor C_B during the off-state of the high-side MOSFET, while V_{FB} is the forward diode voltage [27]. The signal to command the high side switch sent from the logic circuit is sent through a level shift circuit.

Considering the high-side device, the power losses of the driver circuit P_{Dr} become significant as the switching frequency increases and are linked to the resistor network $R_{GG,on}$ at turn-on, the $R_{GG,off}$ at turn off and, the to the gate charge by the relation

$$P_{Dr} = \Delta V_{GS} \cdot Q_G \cdot f_{sw} \cdot \left(\frac{R_{GG,on}}{R_{GG,on} + R_G + R_{Gi}} + \frac{R_{GG,off}}{R_{GG,off} + R_G + R_{Gi}} \right) \quad (7)$$

In Equation (7), the internal gate resistance R_{Gi} of the MOSFET device is also considered [5]. The gate current peak $I_{G,peak}$ at the turn-on pulse (t_{on}) is related to the input capacitances:

$$I_{G,\,peak} = \frac{(C_{GS} + C_{GD}) \cdot V_{GS}}{t_{on}} \quad (8)$$

Furthermore, the driving circuit may have additional monitoring and protection features against power supply under-voltage and overcurrent, or short-circuit, in a hard switching fault (HSF) or a fault under load (FUL) [28].

2.3.3. Current Sensing Arrangement

When using discrete GaN FETs or integrated bridge legs in an inverter topology to drive a motor, it is quite common to use current sensing placed in a phase path connected with a galvanically isolated integrated circuit (IC). The IC extracts the low voltage differential signal through the resistor to transmit the sensed current signal to the low-frequency current conditioning circuits. This approach has the advantage of providing the user with continuous access to the phase current signal for the entire PWM period. In these cases, a sampled signal is extracted around the middle of the symmetrical PWM cycle to reduce the effect of current ripple in the inductance, and also to avoid switching events in which the signal can be influenced by dv/dt. Compared to current sensing with the resistor on the source of the lower device in the bridge leg, the conditioning cost is higher, and the signal is more susceptible to disturbances. In fact, the leg sensing signal is extracted referring the IC to the inverter ground, avoiding galvanic isolation. On the other hand, the bandwidth of the sensing ICs in the phase path is less than the leg sensing solution.

When the phase voltage is high, the signal across the leg shunt resistor is zero. When the phase voltage is low, the current flowing in the phase sensing resistor also flows in the leg sensing resistor so that the two amplified signals overlap. Conventional field-oriented control algorithms (FOC) measure the current in the middle of the phase when the voltage $V_{DS,LS}$ is low to limit measurement noise (the sampling points position of the microcontroller algorithm are indicated in Figure 9). The sensing signals on the phase resistors or switching leg resistors can be used to detect the overcurrent of every single leg for the prompt activation of analog circuit protections. On the other hand, resistances in the sources require accurate design of the layout to minimize parasitic inductances and, therefore, voltage ringing that can be reflected on the current measurement. In Figure 9, voltage measurement of the sensing current in phase *a* and in the relative bridge leg are shown. The output sensing voltage variation of the bridge leg is in the range of 3.3 V, from which the 0 reference is settled to 1.65 V as shown in Figure 9. Furthermore, the voltage signal of both phase and bridge leg sensing are 180 degrees out of phase with respect to the actual phase current I_a, due to the arrangement of voltage acquisition in differential amplifiers (see Figure 7a)

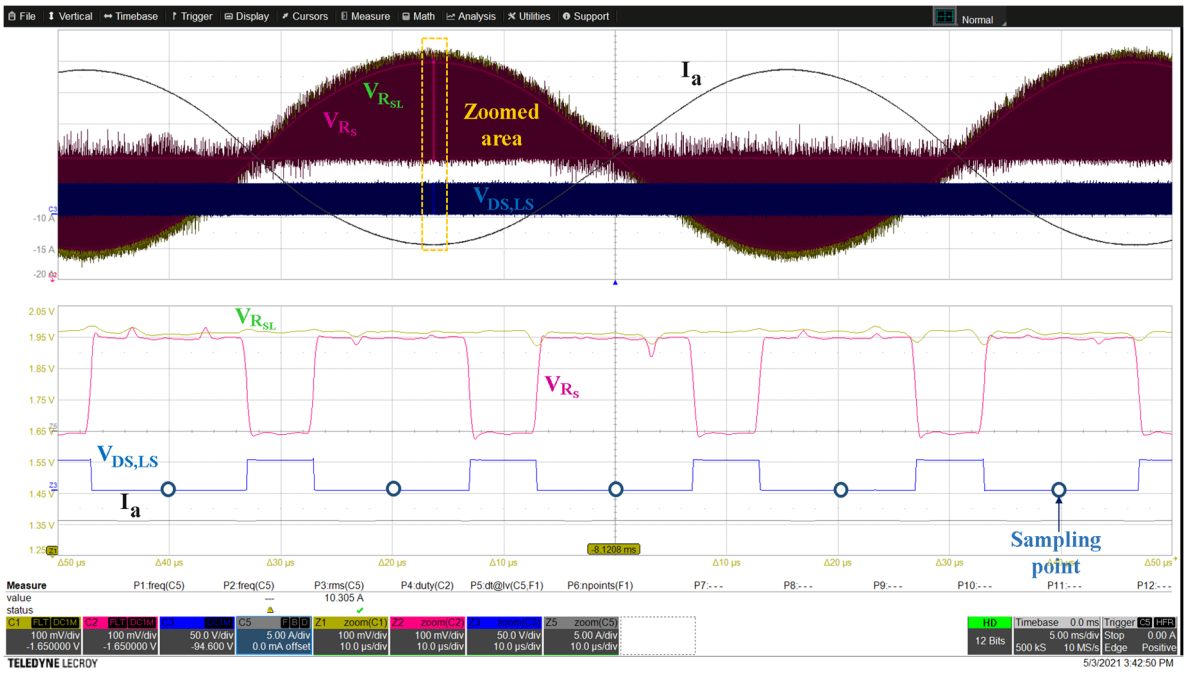

Figure 9. Sensing circuit in the two cases of phase and bridge leg voltage detection solution. Experimental waveforms during switching cycles and a zoomed view. The sampling point positions for the analog to digital signal are highlighted. I_a = 5 A/div, $V_{DS,LS}$ = 50 V/div, V_{RS} = V_{RSL} = 100 mV/div, switching cycle t = 5 ms/div, zoomed view t = 10 µs.

3. Input Current and Voltage Ripple Issues

The DC-link capacitor balances fluctuating instantaneous power exchange between the battery and the inverter. The DC-Link capacitor stabilizes the "ripple" caused by the inverter high-frequency power switching circuits. In the system performance, a reliable and small size DC-link capacitor plays a key role. Typically, four types of capacitors, such as an aluminium electrolytic capacitor, a metalized polypropylene film capacitor, a tantalum polymer and hybrid polymer, and a multilayer ceramic capacitor, are available as a DC-link capacitor. Headline capacitor specifications are related to size, cost, lifetime and reliability. Other parameters for control are capacitance/voltage (CV) ratio, equivalent series resistance (ESR), low stray inductances, ripple current rating and working temperature. The best capacitor selection depends on a trade-off among these parameters, and strongly connected to the capacitance values need of the capacitor link to reduce both the input voltage and current ripple. Increased switching frequencies result in reduced capacitor values.

Typical MOSFET-based inverters for battery-operated motor drive applications run at a PWM frequency in the range 20–40 kHz. In battery-operated inverters running at 20 kHz PWM, there is a critical voltage and current ripple across the inverter's battery cables. Usually, the voltage ripple is a square wave, and the current ripple is a triangular wave. These ripples on the battery cable are a source of EMC (radiated and conducted), and stress the battery, reducing its lifetime. The typical industrial solution is to reduce this stress using a DC-side LC filter. This LC input filter reduces both ripples at the expense of the system's efficiency, volume, weight, reliability, and lifetime.

In a battery-powered inverter, the input current $i_D(t)$ is the sum of three components: the DC average current (I_D), the low-frequency, and the high-frequency (at the switching frequency) component (Δi_D). In the case of a balanced load, such as a BLDC motor, the low-frequency component is zero. Therefore, the input instantaneous current is

$$i_D(t) = I_D + \Delta i_D \quad (9)$$

Neglecting the inverter losses, the input/output power balance leads to

$$I_D = \frac{3}{2} m_a I_0 \cos \varphi \tag{10}$$

where m_a is the modulation index, I_0 is the peak output phase current and φ is the phase angle between output voltage and current. Δi_D is the alternating ripple current and i_C absorbed by the capacitor.

The design of the capacitor (C_f) value is based on the expected voltage ripple. The peak-to-peak DC-Link voltage ripple amplitude Δv_{pp} is related to the high-frequency current component.

$$\Delta v_{pp} = \left| \frac{1}{C_f} \int_0^{t_s} \Delta i_D(t) dt \right| \cong \frac{1}{C_f} |\Delta I_D| t_s \tag{11}$$

where t_s is the specific application time interval fixed by the space vector modulation strategy. From (11) the capacitance value of C_f can be calculated. This design approach takes into account the behaviour of the current and voltage ripple shapes in the case of symmetrical space vector modulation. This capacitor value design procedure is based on [29]. In this analytical methodology, two operating conditions are considered. In the first case, a purely resistive load is supposed ($\varphi = 0$). In the second case, the worst operative condition is presumed with a purely inductive load ($\varphi = 90°$). The two relationships to achieve the correct input capacitor value in the two considered conditions are

$$C_f \geq \frac{1}{8 f_{sw}} \frac{I_0}{\Delta v_{pp,max}} \; ; \; C_f \geq \frac{1}{4 f_{sw}} \frac{I_0}{\Delta v_{pp,max}} \tag{12}$$

As can be seen from the two relationships in (12), as the frequency increases, the capacitance value decreases for a given peak-to-peak ripple voltage [29]. The inductance of the input LC filter (Figure 10a) can be calculated from the LC resonant frequency

$$f_r = \frac{1}{2\pi \sqrt{L_f C_f}} \tag{13}$$

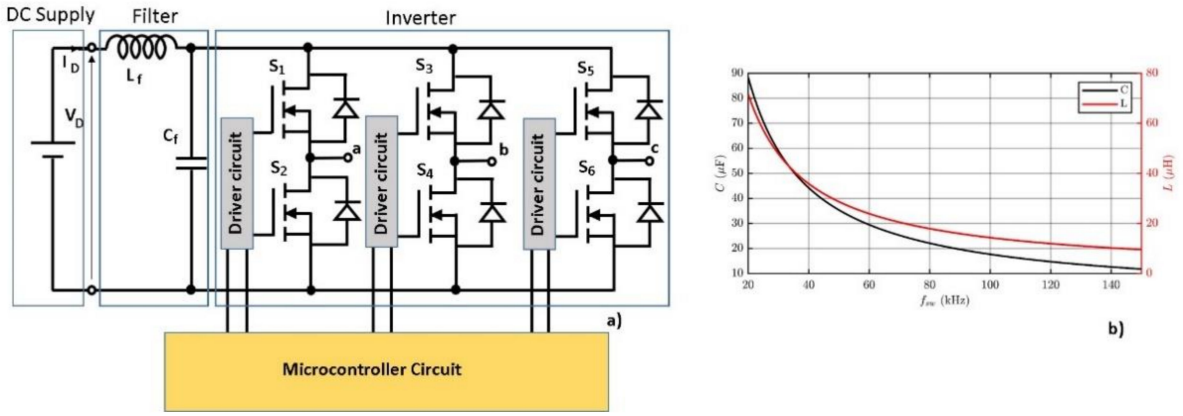

Figure 10. (**a**) Simplified low-pass filter schematic in the input side of the battery-powered inverter; (**b**) graphic of the passive component of the filter versus the switching frequency.

The f_r value is typically chosen at 1/10 of the switching frequency to obtain a proper filtering action of the PWM components. The value of the filter values versus the switching frequency f_{sw} is depicted in Figure 10b, considering capacitor C_f extracted in the worst case of (12) and L_f by means of (13) with $f_r = 1/10\ f_{sw}$, and considering a theoretical $\Delta v_{pp} = 1$ V. From the results shown in Figure 10b, a strong reduction of the passive filter components at increasing switching frequency is evident.

Experimental Evaluation of the Input Electrical Quantities Versus Switching Frequency Variation

The objective of this experimental investigation is to correlate the filter components and the input electrical quantities behaviour versus switching frequency variation. The low pass filter components in the experimental board are from a standard 20 kHz MOSFET inverter for a 250 W BLDC motor drive with a monolithic switching leg (e-bike application). The LC filter values are L_f = 2.7µH, the electrolytic capacitor C_f = 660µF obtaining about 200 mV of Dv_{pp}. The output current I_0 is fixed at 5 A and the input voltage is 36 V. In the preliminary experimental results, the filter capacitor size improves as the switching frequency increases. Two operative conditions are highlighted. The first one at 20 kHz with an electrolytic capacitor in the filter cell. In the second case, a modulation strategy with a switching frequency of 100 kHz is implemented. In this last case, three kinds of capacitors (aluminium electrolytic, tantalum and ceramic capacitors) are involved in the switching evaluation to obtain a voltage ripple peak equivalent to the basic case at 20 kHz. In Figure 11a the experimental setup picture is shown. In Figure 11b a zoomed picture of the electrolytic capacitor filter cell is shown. In Figure 11c the ceramic capacitors filter cell is depicted. Finally, the tantalum solution is shown.

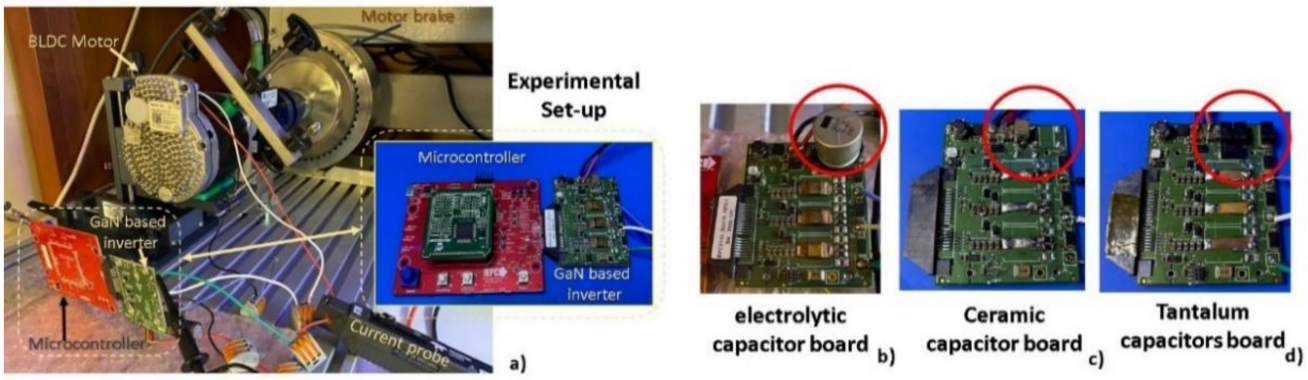

Figure 11. (**a**) Picture of the experimental set-up with a zoomed view of the microcontroller and GaN FET based inverter. (**b**) Inverter board with electrolytic capacitor filter. (**c**) Inverter board with ceramic capacitor filter. (**d**) Inverter board with tantalum capacitor filter.

In Figure 12a,b the switching waveforms at 20 kHz and 100 kHz with the designed filter with electrolytic capacitors (2 electrolytic capacitors with a value of 330 µF) are shown. The aluminium electrolytic capacitor with increasing switching frequency shows its limits. Comparing Figure 12a,b the current ripple at 100 kHz is reduced but the electrolytic capacitor features a ringing noise on a voltage ripple due to parasitic components, making the improvement obtained on the current ripple useless.

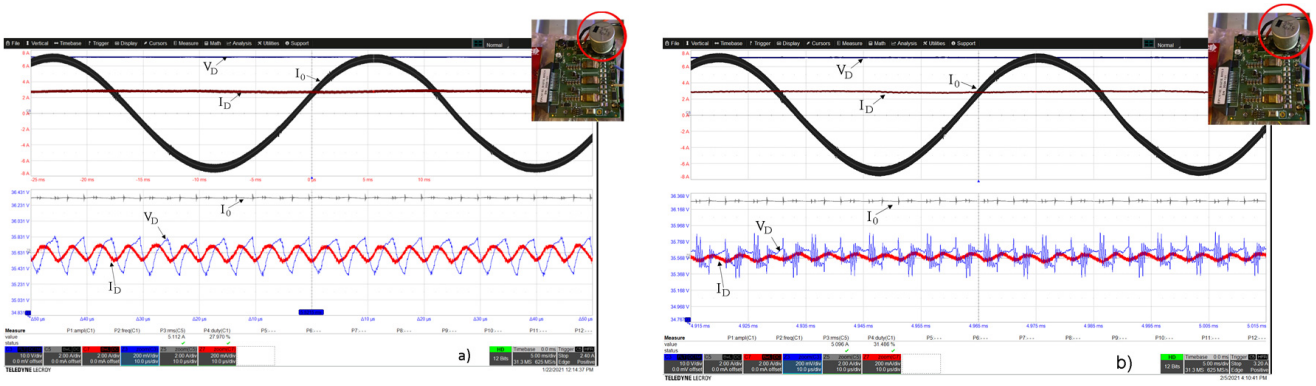

Figure 12. Switching waveform with C_f = 660 µF, dead time 21 ns at $I_0 = I_a$ = 5 A, V_{DC} = 36 V: (**a**) 20 kHz of the switching frequency; (**b**) 100 kHz of the switching frequency. Upper waveforms V_D = 10 V/div, I_D = 2 A/div, I_0 = 2 A/div, t = 5 ms bottom zoomed waveforms V_D = 200 mV/div, I_D = 200 mA, I_0 = 2 A/div, (**a**) t = 50 ms, (**b**) t = 10 µs.

At 100 kHz, maintaining the same peak-to-peak level of the ripple voltage, a lower value capacitor can be used. From design considerations that will be addressed based on the description of the previous section, the same ripple level is obtained by a capacitor between 22 and 30 µF. The lower capacitance values can be obtained with better performing high frequencies capacitor technologies in both polarized and non-polarized solutions. In Figure 13a the C_f is equal to 22 µF in a ceramic technology. In Figure 13b the same voltage ripple level is obtained by means of 30 µF tantalum capacitors. Ceramic capacitors are more attractive because they are used in DC to RF frequency. They are capable of handling high voltages. Furthermore, they feature low ESR and equivalent series inductance (ESL) with volume substantially reduced. Tantalum capacitors have high capacitance density, smaller package size are more easily obtainable than aluminium electrolytic capacitors They have lower leakage currents and stability characteristics at a higher cost.

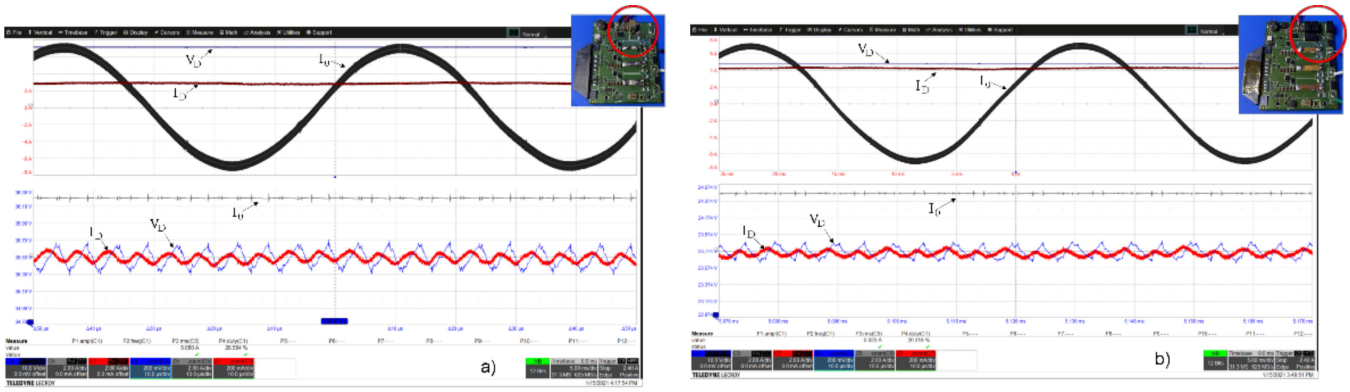

Figure 13. Switching waveform with dead time of 21 ns at $I_0 = I_a = 5$ Arms $V_D = 36$ V, 100 kHz of the switching frequency (**a**) C_f ceramic equal to 22 µF, (**b**) C_f tantalum equal to 30 µF. Upper waveforms $V_D = 10$ V/div, $I_D = 2$ A/div, $I_0 = 2$ A/div, t = 5 ms bottom zoomed waveforms $V_D = 200$ mV/div, $I_D = 200$ mA, $I_0 = 2$ A/div, t = 10 µs.

4. Dead Time Effect on the Motor Drives Inverters

In voltage source inverters, the dead time is necessary to avoid bridge shoot during the switching operation. However, the dead time chosen should be as small as possible to limit the equivalent voltage drop at the inverter output. Moreover, GaN devices operate in reverse conduction mode during the dead time. In fact, in GaN FETs no body diode reverse recovery is present. Instead, the voltage $V_{SD,Q2}$ of the GaN devices is larger than the usual V_F of body diodes in Si MOSFETs. Therefore, dead time must be chosen accurately to the smallest possible value to reduce power losses. In general, the dead time $t_{dt,off}$ must cover the switching time of the GaN device. Considering the lower device Q_2 turn-off, $t_{dt,off}$ must be higher than the off transient delay time $t_{d,off}$ and the transient time $t_{sw,off}$.

$$t_{dt,off} \geq t_{d,off} + t_{sw,off} \tag{14}$$

A similar dead time evaluation for the Q_2 turn-on ($t_{dt,on}$) switching event may be considered. During dead time, equivalent body diode free-wheeling acts to introduce further power losses as described in (15) where the voltage drop V_F depends on the GaN FET technology characteristics.

$$P_{dt} = V_F \cdot I_L \cdot (t_{dt,on} + t_{dt,off}) \cdot f_{sw} \tag{15}$$

The on-dead time $t_{dt,on}$ and the off-dead time $t_{dt,off}$ can be chosen in different ways based on the application request [30]. If $t_{dt,on}$ is equal to $t_{dt,off}$ the dead time is simply defined as t_{dt}. From the modelling of dead time starting from (15), it is possible to evaluate losses related to the variation of dead time at different output currents as shown in Figure 14a. As shown in Figure 14a, dead-time losses due to the body diode voltage drop V_F increase linearly with total dead-time widening. Dead-time losses due to Q_{rr} are

absent, while in MOSFETs the Q_{rr} losses are noticeable [31]. The comparative qualitative waveforms of the power losses for MOSFETs and GaN FETs are shown in Figure 14b [32]. Despite lower losses due to the reduced voltage V_F in the MOSFETs, the contribution of the body diode Q_{rr} produces greater losses as the dead time decreases.

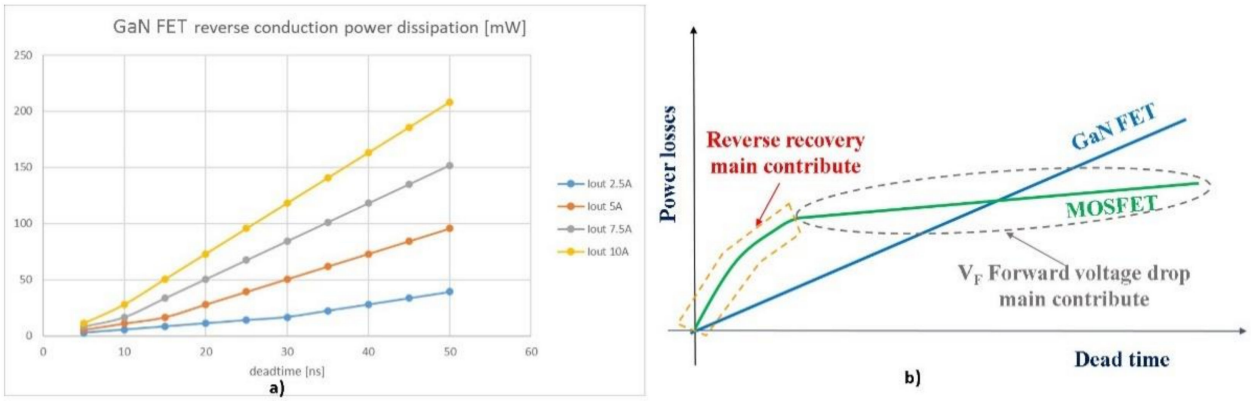

Figure 14. (**a**) Dead time power losses versus dead time variation at different output current (EPC2206 GaN FET). (**b**) Qualitative curves for comparison of dead time losses for MOSFETs and GaN FETs.

In the inverter leg, dead time influences the quality of the output waveforms of the voltage, increasing the number of harmonics and worsening the total harmonic distortion (THD) [10]. The distortion created by dead time is affected by its length, given the switching frequency and the input DC voltage. The reduction of both the rise time and the fall time with GaN FETs used as switches leads to a strong reduction of dead time in the leg switching circuits.

In the inverter leg shown in Figure 15a, the gate commands V_{g1}, V_{g2} are obtained by comparing the triangular carrier signal v_{tr} with the modulation control voltage v_{mod}, as shown in Figure 15b. The dead time is necessary to avoid cross conduction of the switching devices, but introduces a nonlinear effect that influences the output waveform quality [11,33]. This leads to an output phase voltage error v_{dt}, which can be expressed as follows [33]:

$$v_{dt} = \frac{4}{3} \cdot f_{sw} \cdot V_{DC} \cdot t_{dt} \cdot \text{sign}(i) \quad (16)$$

and depends on the sign of the inverter phase current i. The voltage average output waveforms are affected by a ΔV discontinuity when the current changes its sign, as shown in Figure 15c.

For the output average voltage related to phase A, the ΔV_{AN} is related to the dead time width and the i current sign. The voltage average output waveforms are affected by ΔV discontinuity when the current changes its sign, as shown in Figure 15c. For the output average voltage related to phase A, ΔV_{AN} is related to the dead time width and the i current sign.

The effect of this voltage distortion can be visualized more easily if represented in the (α,β) frame and in the (d,q) rotating frame [34], synchronous with the phase current *i*. The result of these transformation is depicted in Figure 16. It is evident that the dead time distortion leads to an almost constant voltage error in the direct axis (i.e., voltage error at the fundamental frequency) and a zero-mean value error at six-times the fundamental frequency on the quadrature axis [10,34]. This means that is a distortion in the fundamental component of the current and one at a higher harmonic order. While the first can be easily compensated by the current regulator integral part, the latter is the source of noncompensated distortions, which influence the phase current as they might be above the bandwidth of the current loop. Another effect of the dead time is well-known in the field of sensorless control. In such applications, the control techniques use an observer and estimators to orient the control frame to the actual frame of the electrical machine. These algorithms

require the reconstruction of the voltage applied to the inverter and must also, therefore, consider its nonideal behavior to avoid introducing orientation errors [33,35].

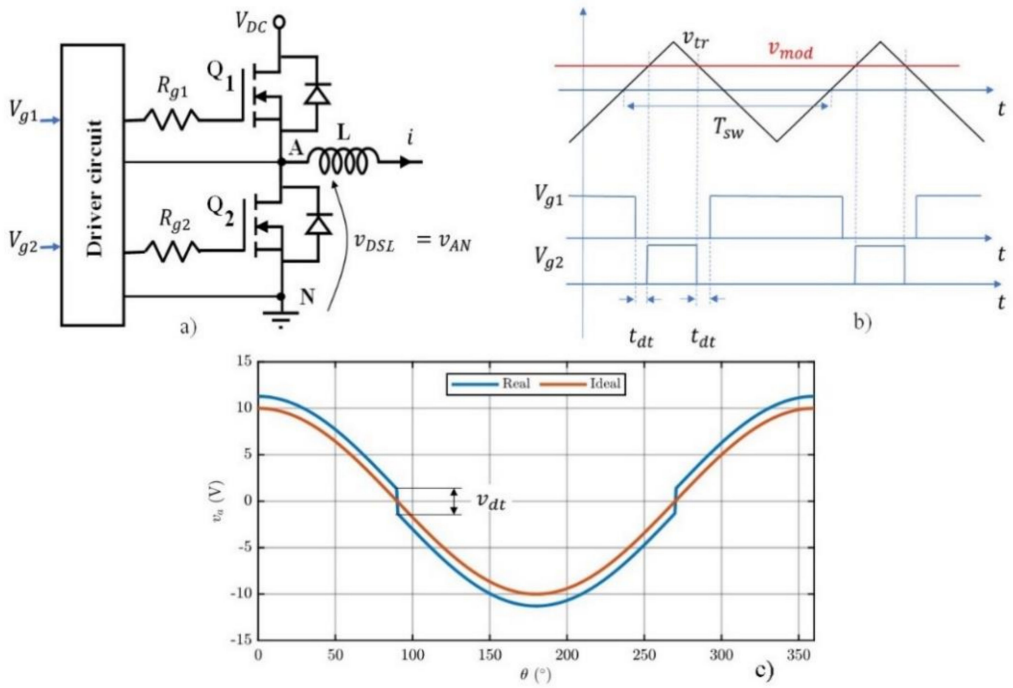

Figure 15. (**a**) Simplified inverter switching leg schematic. (**b**) Phase A, control signal generation by PWM technique with dead time. (**c**) Dead time effect on the moving average value of the inverter output voltage.

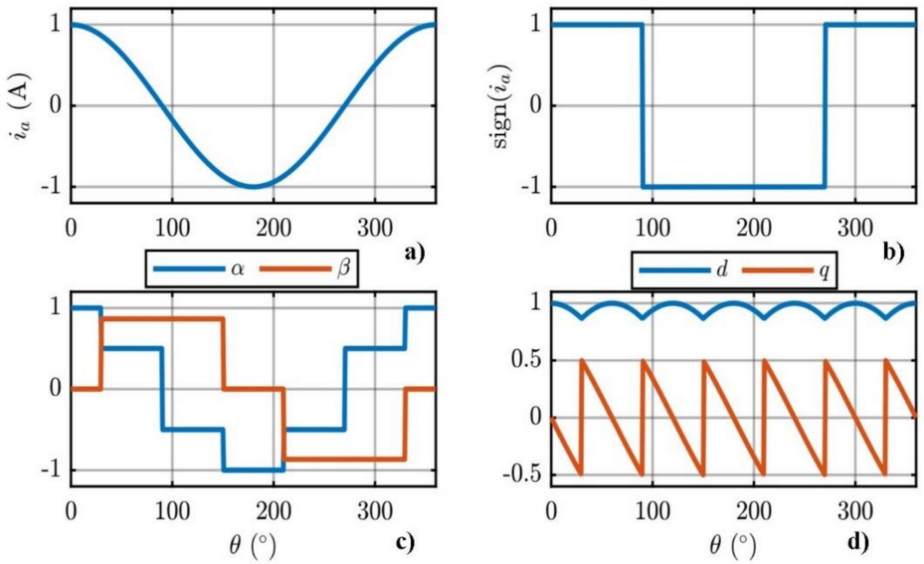

Figure 16. Dead time effect modeling in the stationary reference frame and in the synchronous reference frame. (**a**) Top left: current of phase a. (**b**) Top right: sign(i_a). (**c**) Bottom left: sign(i_a) function in per unit in the stationary (α,β) frame. (**d**) Bottom right: sign(i_a) function per unit in the rotating (d,q) frame, synchronous with the phase a current.

The nonlinearity of the average voltage output waveforms related to the above-mentioned dead time distortions is usually compensated by implementing various open-loop and closed-loop algorithms [11,36–38], which also include self-commissioning techniques to identify the magnitude of these voltage drops [35].

In this paper, a simple and straightforward open loop compensation algorithm is considered. This method simply adds a feed-forward term, opposite to the dead time voltage drop ΔV_{AN} when the phase current i changes its polarity. The quality of this software solution depends on the correct sensing of the current sign. Other more sophisticated techniques may improve compensation performance. However, they often require much more complex algorithms or hardware modifications, which would burden the control system and increase its complexity and tuning.

To avoid any compensation, and largely improve the quality of the current waveform, the best option is to reduce the dead time duration.

In the case of GaN FET applications as switches in an inverter leg, the dead time can be selected in the range of tens of ns, thereby making the hardware solution very attractive compared to the software technique because it implies a saving of software and hardware resources.

Simulation and Experimental Results

The evaluation of the dead time selection was carried out implementing a three-phase inverter driving a BLDC in a software tool (PLECS©). The inverter dc bus was fixed at 48 V, the maximum motor load current was 10 A, the switching frequency was set to 40 kHz and the control frequency to 20 kHz. In the first simulation results, a dead time of 500 ns (typical of the Si MOSFET) was compared with a dead time of 14 ns, easily available with the latest generation of the GaN FETs.

In the first simulation result, a dead time equal to 14 ns led to a negligible speed ripple compared to the case of dead time equal to 500 ns (Figure 17a). In the second simulation result, the speed ripple of the dead time selected at 14 ns was compared with the dead time compensation technique in the case of the dead time equal to 500 ns. As shown in Figure 17b the peak-to-peak amplitude of the speed ripple was more symmetrical in the case of 14 ns dead time. Furthermore, the maximum peak values were similar.

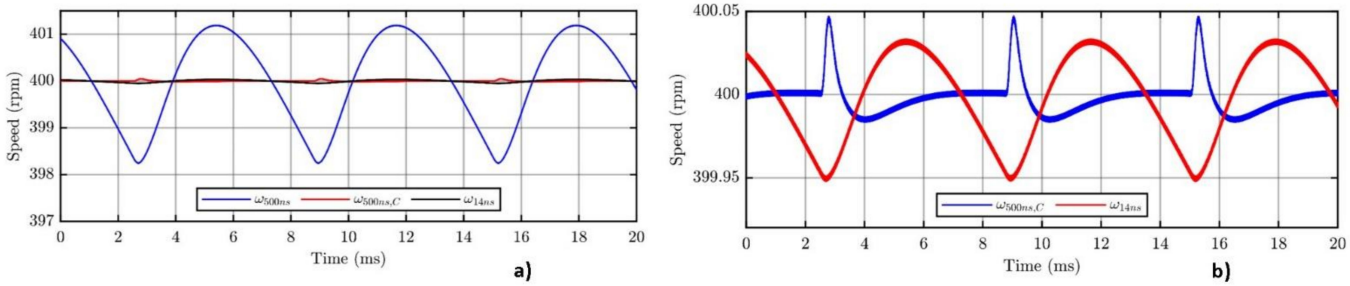

Figure 17. Dead time effect in the speed ripple. (**a**) Dead time equal to 500 ns compared with dead time of 500 ns with compensation and dead time reduced of 14 ns. (**b**) Magnified view of Figure 17a for speed ripple comparison at 14 ns of dead time and 500 ns dead time with software compensation.

The current waveforms in the case of 14 ns dead time showed very low waveform distortion compared to the 500 ns dead time with and without software compensation. In Figure 18a simulation of the phase a current is reported at 500 ns (i_{500ns}) dead time compared to 500 ns with compensation ($i_{500ns,C}$) and a dead time of 14 ns (i_{14ns}). The zoomed view of the current across the passage for 0 in the three cases is shown in Figure 18b. The better waveform shape with 14 ns is shown in the inspection view of Figure 18b.

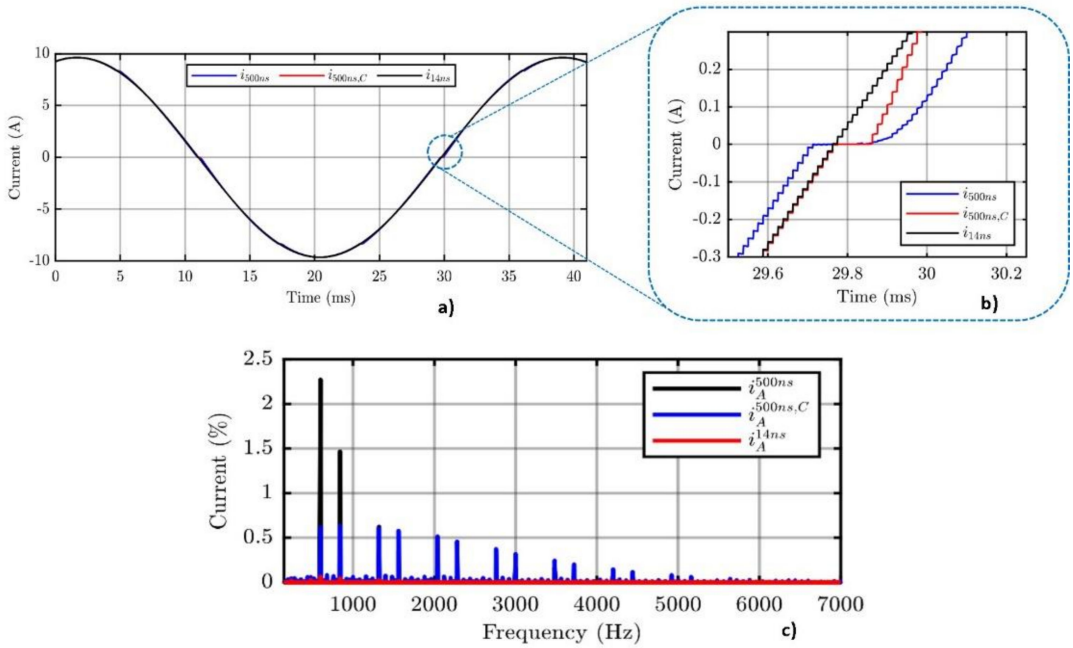

Figure 18. (**a**) Dead time effect on the current waveform of phase a in the three cases. (**b**) Zoomed view of current zero crossing in the three cases. (**c**) Harmonic content comparison for the load current in the case of dead times equal to 14 ns, 500 ns and 500 ns with compensation.

Considering the load current harmonic spectrum, the lowest harmonic content was obtained in the case of a dead time of 14 ns, as shown in Figure 18c.

The experiments were carried out on an EPC9146 [17] board driving a BLDC motor, as can be seen in the block diagram of Figure 19a. The tested motor drive operated from a 48 V DC supply voltage delivering up to 3.7 A into each phase of the motor with a Field Oriented Control (FOC) [39]. We used a 40 kHz PWM frequency (20 kHz control frequency) and 500 ns dead time that are typical of Si MOSFET-based inverters. The experimental set-up is shown in Figure 19b.

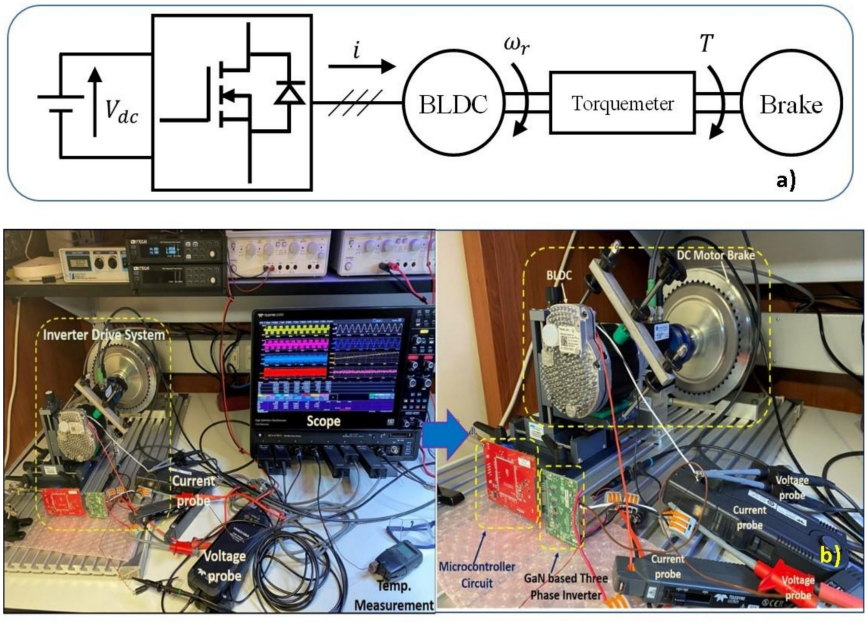

Figure 19. (**a**) Diagram of the experimental setup. The BLDC drive is connected to a brake to regulate torque loading. (**b**) Photo of the experimental setup.

Three tests were carried out at a mechanical speed $\omega_r = 400$ rpm:

1. $t_{dt} = 500$ ns with no dead time compensation algorithm (see Figure 20).
2. $t_{dt} = 500$ ns with the compensation algorithm described previously (see Figure 21).
3. $t_{dt} = 14$ ns with no dead time compensation algorithm (see Figure 22).

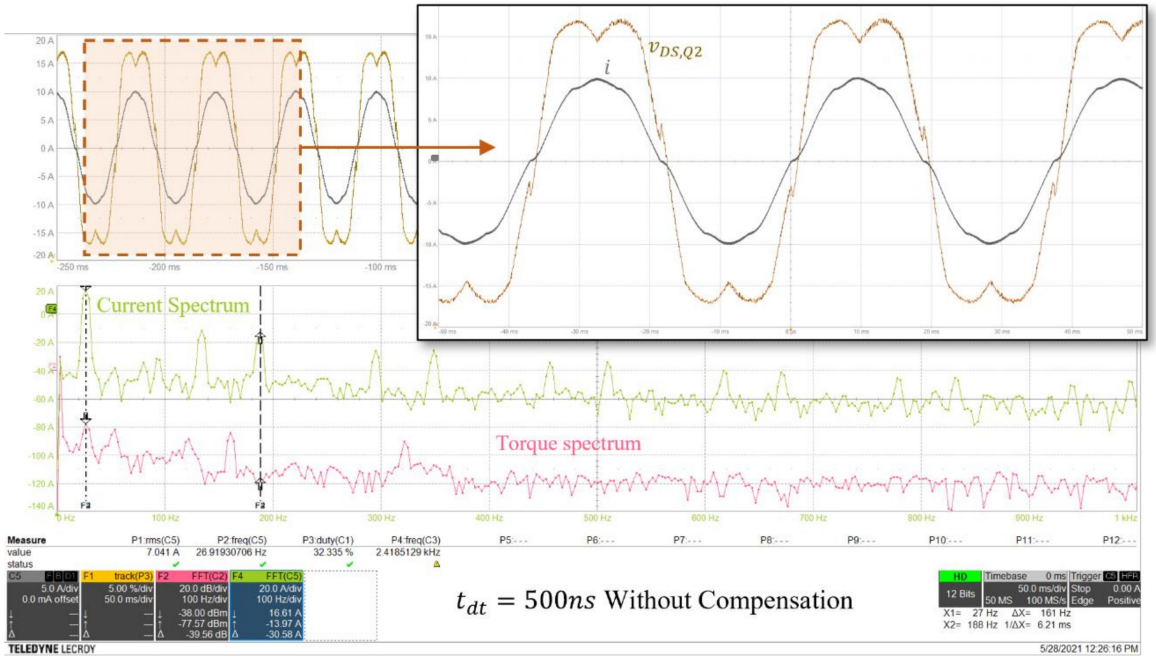

Figure 20. Motor current in the time domain and DFT of the phase current and machine mechanical torque 50 ms/div. $t_{dt} = 500$ ns and no compensation algorithm. C5: motor phase current i_0 = 5 A/div. F1: reconstructed inverter voltage v_{DSL} = 5 V/div. F2: DFT of the mechanical torque 500 mV/Nm. F4: DFT of the inverter phase current.

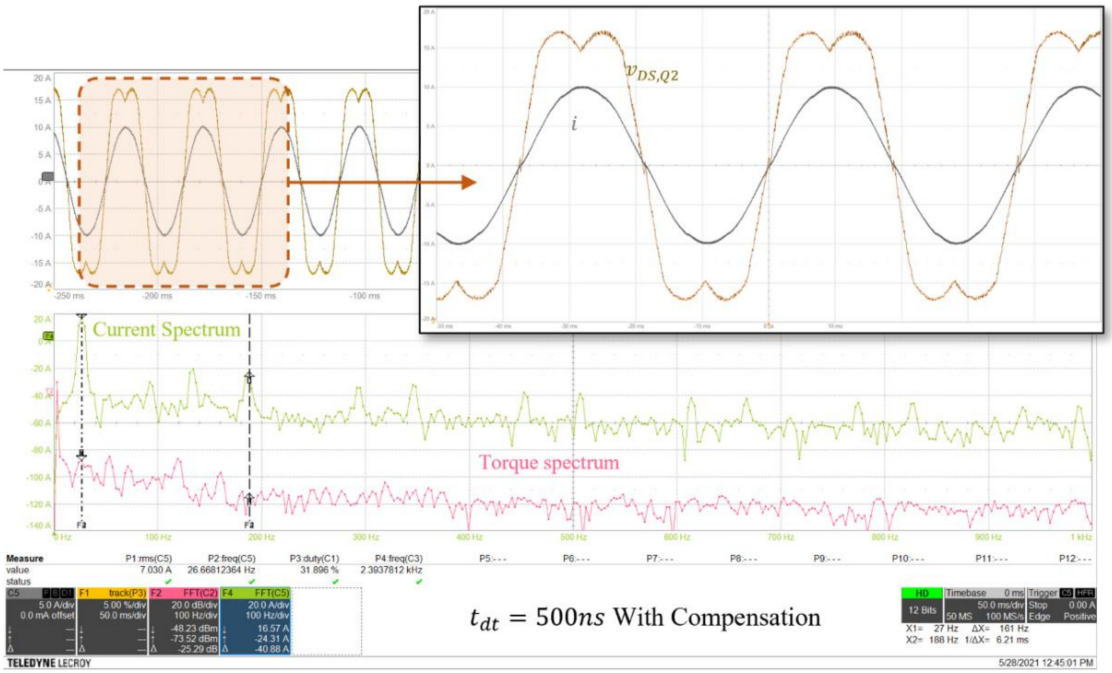

Figure 21. Motor current in the time domain and DFT of phase current and machine mechanical torque 50 ms/div. $t_{dt} = 500$ ns and no compensation algorithm. C5: motor phase current i_0 = 5 A/div. F1: reconstructed inverter voltage v_{DSL} = 5 V/div. F2: DFT of the mechanical torque 500 mV/Nm. F4: DFT of the inverter phase current.

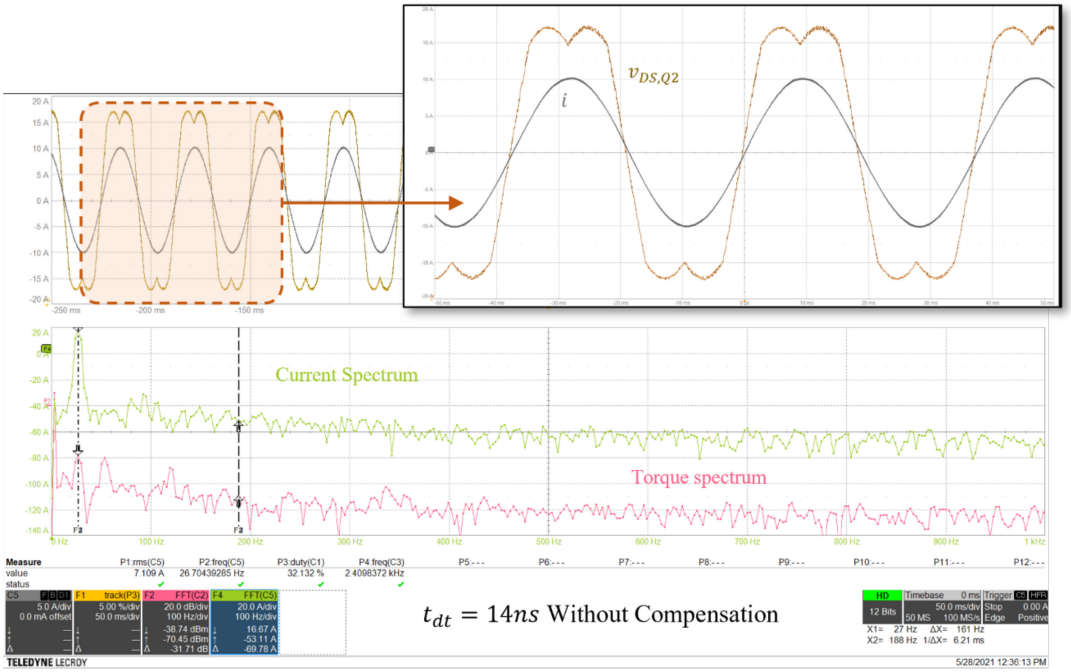

Figure 22. Motor current in the time domain and DFT of phase current and machine mechanical torque 50 ms/div. t_{dt} = 14 ns with no compensation algorithm. C5: motor phase current i = 5 A/div. F1: reconstructed inverter voltage $v_{DS,Q2}$ =5 V/div. F2: DFT of the mechanical torque 500 mV/Nm. F4: DFT of the inverter phase current.

As it can be seen in these waveforms, the 500 ns dead time significantly distorts the phase current. This can be highlighted from a spectral analysis of both the phase current and mechanical torque T. As is displayed in Figure 20, the dead time distortions lead to a large harmonic content at the 5th and 7th harmonic on the phase current, corresponding to the 6th harmonic in the mechanical torque [40].

This effect can be mitigated by implementing a dead time compensation strategy, leading to the results shown in Figure 21. As can be clearly seen in the current and torque spectrum, the compensation strategy greatly improves the quality of the electrical and mechanical quantities, reducing the low order harmonic content. These harmonics are, however, not fully compensated, since the adopted method is based on an open-loop paradigm [40].

Adjusting the dead time to 14 ns, which is something that can only be achieved with GaN devices, the waveforms greatly improve, as shown in Figure 22. The phase current waveform is much smoother with a 14 ns dead time and the effect is clearly highlighted by spectral analysis, where the low order harmonics are almost eliminated.

5. dv/dt Effect in the Switching Leg

In GaN FET devices, the high dv/dt achievable leads to some consideration in inverter applications. The sinusoidal control voltage of the inverter causes a dv/dt variation during a commutation cycle. In Figure 23a,b the phase node voltages of rising and falling edges switching are reported. The switching waveforms are carried out at a peak phase current I_{peak} = 15 A and V_{dc} = 48 V at 50 kHz of switching frequency. The experimental waveforms of Figure 23 are obtained with infinite persistence to show the dv/dt range of variation. The time limits of the dv/dt waveforms set the minimum dead time t_{dt} duration ($t_{dt,on}$ = $t_{dt,off}$ = 50 ns in the discrete GaN FETs based inverter for the experimental validation).

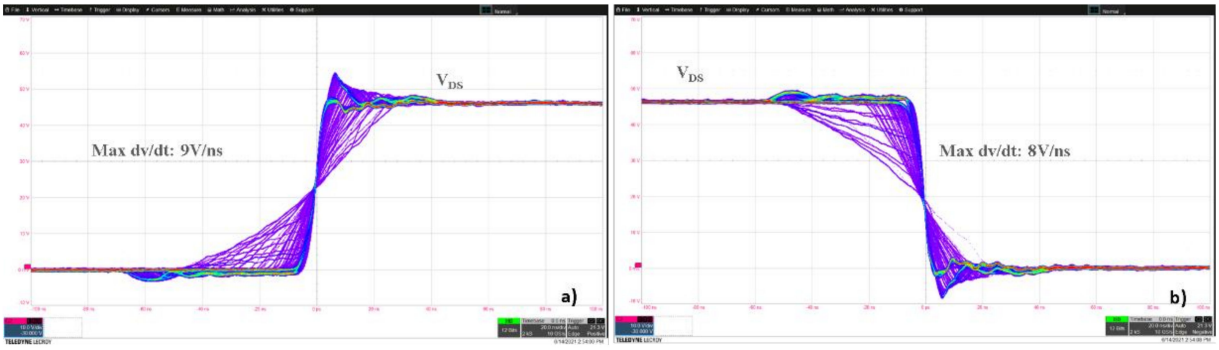

Figure 23. Experimental waveforms obtained with infinite persistence to show the dv/dt range of variation. (**a**) Rising edge switching of the node voltage V_{DS} relative to the phase a. (**b**) Falling edge switching of the node voltage V_{DS} relative to the phase a. $V_{DS,LS}$ = 10 V/div, t = 10 ns/div.

In GaN FETs the threshold voltage, V_{GSTH}, is lower than in equivalent current density MOSFET devices. In the GaN switch used in the inverter experimental board, V_{GSTH} is in the range 1.5 to 2.5 V. This low threshold voltage could cause erroneous turn on when the device in the off-state has a high dv/dt. In high dv/dt applications, the gate driver constraints are crucial to avoid the shoot-through phenomena. A switching leg circuit with gate driver interaction and high dv/dt current paths is shown in Figure 24a, while the qualitative waveforms of the node voltage switching, and the gate voltage of the higher and lower devices, are shown in Figure 24b. The gate voltage requirements can be achieved by reducing critical damping of the gate drive turn-on switching due to interaction with the power loop by means of accurate layout design. In addition, the turn-on and turn-off transient requirements are different, which necessitates the use of independent gate resistors to adapt the turn-on and turn-off gate-loop damping. Considering the low-side device, parasitic source inductance produces an oscillation on the gate voltage at the dv/dt of the node voltage of the switching leg. The ringing voltage is dependent on the switching frequency. At switching frequencies up to 100 kHz, the contribution of inductance is reduced compared to cases of DC-DC converters operating at MHz frequencies. Therefore, in correspondence with dv/dt, the peak due to parasitic input capacities are mainly detected as shown in Figure 25.

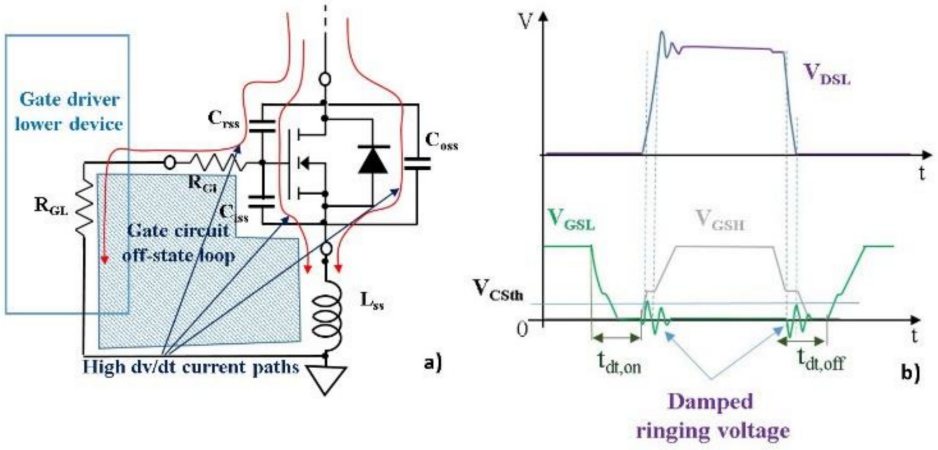

Figure 24. (**a**) Low-side GaN FET device in off-state current paths and parasitic passive components model. (**b**) Qualitative switching waveforms of the node voltage, low-side gate voltage V_{GSL} and high-side gate voltage V_{GSH}.

Figure 25. Experimental waveforms of the gate-source voltage of the lower device of inverter leg (phase a) under the rise of the inverter leg node voltage (lower device-drain-source voltage). The dv/dt effect acts a gate voltage spike under the GaN threshold voltage (V_{GSTH}) V_{DSL} =10 V/div, V_{GSL} =1 V/div, t_{main} =2 µs, t_{zoom} = 50 ns/div.

The experimental waveforms depicted in Figure 25 are carried out at turn-on of the higher switch of an inverter leg with the lower device in the off condition at 10 A of phase current. Figure 25 shows the reduced gate voltage spike in the lower leg device (zoomed view with t_{zoom} = 50 ns) in correspondence with the high dv/dt of the node voltage. This spurious pulse is under the V_{GSTH} due to the mixed effect of the reduced parasitic capacitance of GaN FET and a suitable driver circuit solution.

6. Discrete GaN FET-Based Inverter Switching Evaluation

In this section we consider a permanent magnet AC (PMAC) motor driven by a GaN FET-based inverter with a sensor-less FOC technique implemented in a microcontroller circuit [41]. The load current variation is obtained by a suitable motor brake. The main characteristics of the motor used are reported in Table 1. In Table 2, the test conditions of the inverter board are recalled. The experimental evaluation is carried out without heat-sink in inverter operation. In Figure 26a, the input and output waveforms for two phases at a switching frequency f_{sw} = 50 kHz and $I_{a,b,rms}$ = 15 A are reported.

Table 1. Electric motor main characteristics.

PMAC MOTOR	Motor Voltage Range V_m [V]	Nominal Rms Current I_m [A]	Angular Speed Max ω_{mx} [rpm]
	24–75	10	3010

Table 2. Inverter operative test conditions.

GaN Inverter	Bus Voltage V_{dc} [V]	Switching Frequency f_{sw} [kHz]	Dead Time [ns]
	48	20 50 100	50

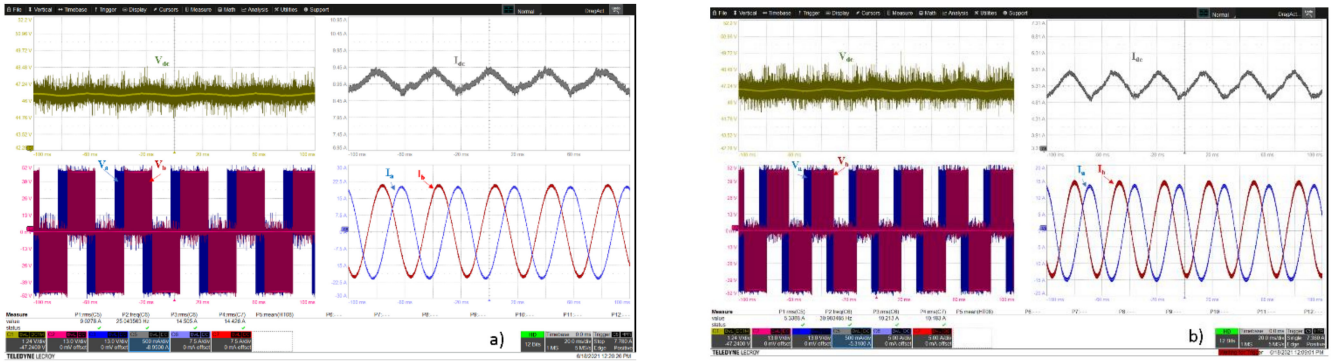

Figure 26. (**a**) Experimental waveforms of the input and output inverter values at f_{sw} = 50 kHz. V_{dc} = 1.24 V/div, I_{dc} = 500 mA/div, V_a = V_b = 13 V/div, I_a = I_b = 7.5 A/div, t = 20 ms/div. (**b**) Experimental waveforms of the input and output inverter values at f_{sw} = 100 kHz. V_{dc} = 1.24 V/div, I_{dc} = 500 mA/div, V_a = V_b = 13 V/div, I_a = I_b = 5 A/div, t = 20 ms/div.

In Figure 26b, the input and output experimental waveforms in the operative conditions of $I_{a,b,rms}$ = 10 A at 100 kHz are shown. The advantage is that the input voltage and current ripple decrease when the PWM frequency is increased, allowing the designer to remove the electrolytic capacitors and use only ceramic capacitors that are smaller, lighter, and more reliable, as described in Section 3. The experimental board is composed on the top surface with ceramic capacitors and on the bottom with electrolytic capacitors that can be removed when the switching frequency increases. The current waveform of phase a, with the first harmonic of the phase voltage is depicted in Figure 27a, while in Figure 27b the zoomed view of the current ripple and the voltage pulses at 100 kHz of switching frequency for the same inverter phase are shown.

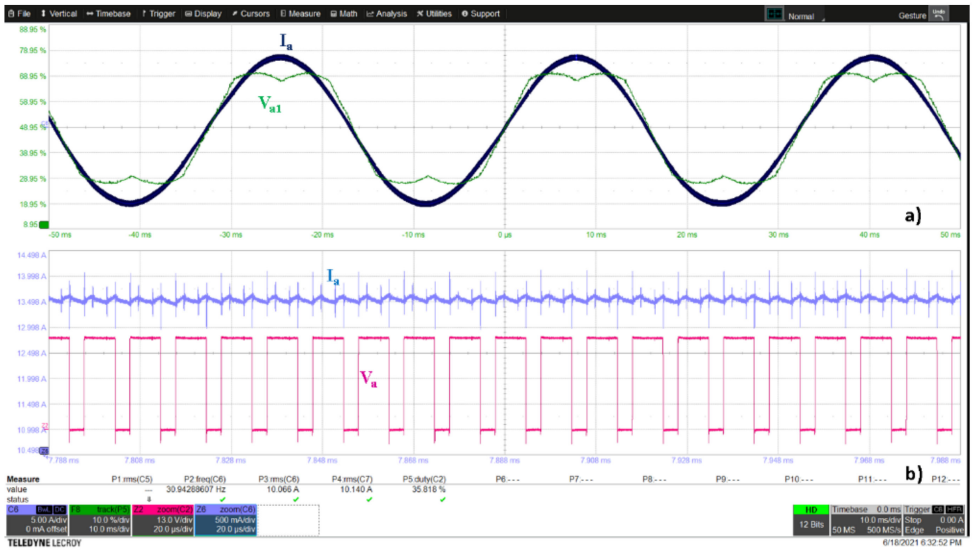

Figure 27. Experimental waveforms of output voltage and current of phase a. (**a**) Phase current and first harmonic of output inverter voltage. I_a = 5 A/div, V_{a1} = 5 V/div, t_{main} = 10 ms. (**b**) Voltage pulses and current ripple. (**a**) 1.24 V/div, I_a = 500 mA/div, V_a = 13 V/div, t_{zoom} = 20 µs/div.

Finally, the inverter efficiencies in the three cases reported in Table 2 are described in Figure 28. Efficiencies are quite similar, in the range of 20 to 50 kHz. At 100 kHz efficiency is quite high but slightly lower than in the previous cases.

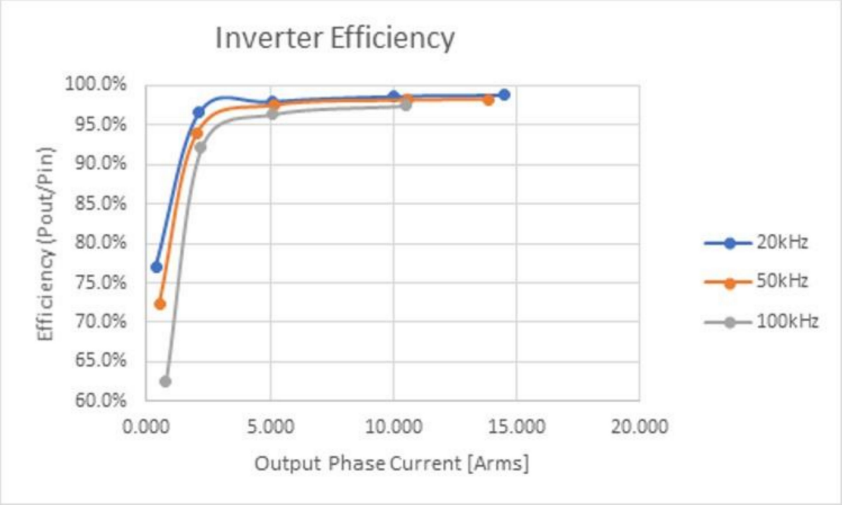

Figure 28. Inverter efficiency at motor current variation (rms) for three switching frequencies: 20 kHz, 50 kHz, 100 kHz.

Thermal Behavior

Gallium nitride-based HEMT devices feature, like silicon power MOSFETs, a positive coefficient temperature suitable for parallel connection [42,43] to increase the current density in the converter arrangement. In the experimental board, the thermal response in steady state conditions occurs without a heatsink exploiting the PCB extension contact with the GaN package solution. Long-term reliability is related to thermal fatigue and package wear-out [44,45]. Thus, thermal management plays a crucial role. In the case without a heatsink the main thermal resistance to consider involved in heat exchange is the thermal resistance relative to the junction to the solder bump (see Figure 3a) $R_{\theta JB}$. This is the thermal resistance from the device junction to the bottom of the solder bumps without consideration of the type or size of the mounting circuit board. If the designer knows the thermal characteristics and environment of the application arrangement, the thermal resistances of all the subparts can be added algebraically. In the case of an additional heat-sink on the top of the GaN FET, it is necessary to consider the thermal resistance junction-to-case $R_{\theta JC}$ to correct the design of the heat-sink thermal resistance. In the experimental measurement considered, temperature behaviour at $I_{a,b,c,rms}$ = 10 A without a heatsink with f_{sw} = 50 kHz and V_{dc} = 48 V is shown in the infrared picture in Figure 29. The infrared camera measurement shows a quite satisfactorily reduced increase of the GaN FETs temperature.

Figure 29. Infrared picture of experimental board without heat sink at V_{dc} = 48 V, $I_{a,b,c,rms}$ = 10 A, f_{sw} = 50 kHz.

7. Discussion

In battery-source motor drive applications, the DC bus voltage ranges from 24 V_{dc} to 96 V_{dc}. In this kind of power conversion system, pure silicon MOSFETs are the switches more used currently. In hard-switching inverter topology with MOSFETs, the PWM frequency is kept below 40 kHz due to the limits of conduction losses and switching losses. Furthermore, the relative switching speed leads to a dead time design in the range of 200 to 500 ns. GaN FET devices feature high commutation speed with lower switching losses compared to equivalent current rate low voltage Si MOSFETs. Planar structure, together with the presence of the 2DEG phenomenon, allows a reduction of conduction resistance, also improving direct losses. Moreover, in reverse conduction, the p-n junction of the body diode is not present in the HEMT physical structure, from which, in hard switching operation, reverse recovery losses do not occur. A GaN is a bidirectional device driven by a suitable gate circuit voltage. During reverse conduction without a positive gate signal (natural reverse conduction), its behavior is similar to a diode on direct conduction with a voltage drop higher than a MOSFET body diode. From the high commutation speed obtainable, the minimum dead time reachable (a few tens of ns) reduces the losses achievable in the reverse conduction. Furthermore, the reduced dead time allows a better quality of the output voltage and current during half bridge operation. The dead time reduction increases the efficiency of the electric motor under the same operating conditions.

Indeed, the decrease of dead time leads to a sinusoidal current closer to the ideal one, leading to lower motor losses and a torque constant closer to the theoretical one [46]. Increasing switching frequency using GaN FETs as switches allows reduced size of the input filter. When the PWM frequency is increased, the input filter, made of one inductor and suitable paralleled electrolytic capacitors, can be replaced with ceramic capacitors. This leads to several advantages in the inverter design approach because ceramic capacitors feature lower series impedance with a minimum in the operative field between 100 kHz and 200 kHz. Furthermore, ceramic capacitors are more stable in temperature and more reliable compared with electrolytic capacitors. The overall achievement is a more compact and reliable inverter system for the same power rating. This overall reduction in the size of the power converter makes it possible to create modules that can be integrated directly with the motors, creating a modular motor-drive system that is very useful in terms of compactness and reliability [15].

The profile of the input and output capacitances are more advantageous than MOSFETs. In particular, the values of C_{rss} versus the voltage applied between drain and source are much lower, so that high switching speeds and dv/dt are reached [47]. High switching transients feature high dv/dt (up to 8 V/ns). In low voltage applications, these high dv/dt

values are not as dangerous in the stresses of motor insulation systems as in high voltage inverters [48]. Output filters in the output switching leg path can be added to perform a low pass harmonic filter or an EMI filter to reduce the impact of transient switching voltages [49]. The GaN FET exhibits a high current density and low channel resistance. The R_{DSon} has a positive temperature coefficient. The high-power density achievable leads to significant self-heating, which decreases device performance because thermal management to optimize heat transfer is essential [50]. The thermal resistance junction to the case is lower than in equivalent silicon devices, providing good thermal conductance. The device package is crucial in heat-flux exchange. The correct package solution allows dissipation of the generated heat through the two main heat conduction paths:

– to the PCB at the board-side
– to the case at the other side.

Both of these, heat conduction paths can benefit from thermal management strategies.

In the PCB layout, in-plane heat conductance is dependent on the number of layers. More layers provide more paths to dissipate heat.

Furthermore, by placing thermal vias near or under the GaN FET pads, self-heating can be reduced [51].

Inverter application fault conditions are another crucial point but are not covered in this article for the sake of brevity. Only a few notes on short circuits are reported. The short-circuit behavior in HSF or FUL conditions is similar in terms of withstanding capability time. The absence of parasitic bipolar structures does not cause latch or loss of gate control, as happens with IGBT devices. This is a favorable property for short protection circuits. The gate circuit design is a key point at which to monitor and control fault conditions [52,53]. The gate driver protections must be set to occur in a few microseconds. A typical withstand time of ten microseconds is easily achievable of low voltage GaN FETs [54,55].

Ultimately, the GaN FET device can be used advantageously in motor control applications. The benefits of the GaN devices come with a higher cost, which is typical with new technology introduction.

Future work will be related to more in-depth study of the dead time as the voltage transients vary, and the development of multilevel inverter applications to evaluate the effectiveness and problems of using GaN in these more complex topological structures.

8. Conclusions

GaN FET is increasingly being used in many high switching frequency converter applications due to its advantageous power loss and size reduction characteristics. In motor control applications, the increased switching frequency allowed by the HEMT devices beyond a certain level is not always a winning design choice. This paper describes the advantages and issues to be solved when using GaN FETs in applications of low voltage electric drives currently widely used in industrial, robotic and automotive fields. The technology of the device is described in relation to the considered application, highlighting the characteristics and parameters of the GaN FET that mainly affect the operation of the inverters when they are used as power switches. Two experimental boards with different power rates and GaN FETs characteristics are described and evaluated in terms of performance and measurement capability of the main electrical parameters used in the field of drives. The impact of using GaN FET in reducing the input filter, reducing dead time for enhancement of reverse conduction losses, and improving the quality of the output waveforms, is pointed out. Furthermore, the effect of dv/dt in low voltage driving motors is highlighted. Finally, an experimental evaluation of the actual board, with a discrete GaN, is carried out at different switching frequencies to evaluate efficiency, as well as dynamic and thermal performance. The survey carried out shows that the GaN device has a great potential for application in the field of motion control and the capability of significantly increasing performance of the motor-drive system in terms of:

- quality of the current output waveforms
- torque obtained by reducing the harmonics and related oscillations

- total system efficiency.

Furthermore, the device's high-power density, and the integration capability connected with the increase in switching frequency, allows production of very compact inverters for optimized arrangement of the converter and the electric motor, thus leading to modular motor-drive applications that are increasingly requested in different fields such as electric mobility and robotics.

Author Contributions: Conceptualization, S.M. and M.P.; methodology, F.M., S.M. and M.P.; software, F.M., M.P. and V.B.; validation, M.P., F.M. and S.M.; formal analysis, S.M., F.M.; investigation, M.P. and V.B.; resources, S.M.; data curation, F.M. and M.P.; writing—original draft preparation, S.M. and F.M.; writing—review and editing, V.B., F.M. and M.P.; visualization, V.B.; supervision, M.P. and S.M. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data sharing not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

GaN	Gallium Nitride
FET	Field Effect Transistor
HEMT	High Electron Mobility Transistors
WBG	Wide Bandgap
SiC	Silicon Carbide
Si	Silicon
UAV	Unmanned Aerial Vehicles
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
EMI	Electromagnetic Interference
THD	Total Harmonic Distortion
IMMD	Integrated Modular Motor Drive
2DEG	Two-Dimensional Electron Gas
AlGaN	Aluminum Gallium Nitride
FOM	Figure of Merit
EPC	Efficient Power Conversion
CSI	Common Source Inductance
PCB	Printed Circuit Board
CSP	Chip-Scale Package
UVLO	Voltage-Lockout
CMOS	Complementary MOS
TTL	Transistor-Transistor Logic
BLDC	Brushless DC
PWM	Pulse Width Modulation
PM	Permanent Magnetic
SMD	Surface Mounting Device
HSF	Hard Switching Fault
FUL	Fault Under Load
FOC	Field-Oriented Control
LS	Low Side
HS	High Side
CV	Capacitance/Voltage
ESR	Equivalent Series Resistance

ESL	Equivalent Series Inductance
PMAC	Permanent Magnetic AC

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