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Design of Nonlinear Backstepping Double-Integral Sliding Mode Controllers to Stabilize the DC-Bus Voltage for DC–DC Converters Feeding CPLs

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Abstract: This paper proposes a composite nonlinear controller combining backstepping and double-integral sliding mode controllers for DC–DC boost converter (DDBC) feeding by constant power loads (CPLs) to improve the DC-bus voltage stability under large disturbances in DC distribution systems. In this regard, an exact feedback linearization approach is first used to transform the nonlinear dynamical model into a simplified linear system with canonical form so that it becomes suitable for designing the proposed controller. Another important feature of applying the exact feedback linearization approach in this work is to utilize its capability to cancel nonlinearities appearing due to the incremental negative-impedance of CPLs and the non-minimum phase problem related to the DDBC. Second, the proposed backstepping double integral-sliding mode controller (BDI-SMC) is employed on the feedback linearized system to determine the control law. Afterwards, the Lyapunov stability theory is used to analyze the closed-loop stability of the overall system. Finally, a simulation study is conducted under various operating conditions of the system to validate the theoretical analysis of the proposed controller. The simulation results are also compared with existing sliding mode controller (ESMC) and proportional-integral (PI) control schemes to demonstrate the superiority of the proposed BDI-SMC.

Keywords: backstepping double-integral sliding mode control scheme; constant power load; exact feedback linearization approach; Lyapunov stability theory; negative-resistance characteristics; non-minimum phase; nonlinear dynamical model

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1. Introduction

Over the past few decades, the power electronic converters (PECs) have been widely used in vehicular power systems (VPSs) (e.g., space vehicles, sea, land, etc.) and in renewable energy source (RES)-based systems (e.g., DC and AC microgrids) due to their voltage step-up, step-down, or conversion capabilities [1–5]. Recently, the power electronic-based DC distribution networks (DCDNs) are becoming more popular owing to their distinct advantages in terms of efficiency, controllability, flexibility, etc. [6,7]. However, two major challenges need to be addressed for a stable and reliable operation of power electronic-based DCDNs in conjunction of RESs, where the first challenge is the low terminal voltage of RESs while important to maintain a relatively high and stable terminal voltage of the DC-bus as all loads and RESs are either directly or indirectly connected to this bus [8–10]. As a results, DC–DC boost converters (DDBCs) are usually used in DCDNs as the interface between the DC-bus and RESs, which need to be appropriately controlled to achieve the desired DC-bus voltage [11,12]. On the other hand, the maintenance of

stable and reliable operations becomes even more challenging when a large number of DC–DC converters are used to interface loads and RESs [13–15]. The second challenge is the instability issue caused by constant power loads (CPLs) in DCDNs with tightly coupled power electronic converters [16–18]. It is well-known that the constant power is drawn by CPLs, and consequently, it exhibits negative-impedance characteristics that destabilize as well as even cause blackouts [18,19]. Thus, it is essential to design an advance controller that not only deals with the destabilization but also provides quick dynamic response while guaranteeing the stability of the system.

Several control strategies have been proposed to resolve the instability issue of DDBCs caused by CPLs. Passive damping methods are proposed in [18,20] to neutralize the destabilization effect by increasing the damping into a system. However, these methods have limited applications due to their high costs and large sizes of passive elements such as capacitors and inductors. To alleviate these drawbacks, active damping methods such as virtual impedance [21], virtual resistance [22], and virtual capacitor [23] are proposed for stabilizing the system by adding extra control loops to reshape impedances. In these methods, the destructive effects of CPLs are mitigated by enforcing the unstable poles into the stable region through the modification in control loops. However, the satisfactory performance of these damping methods is highly dependent on the switching frequency. Thus, a voltage–current (V–I) droop-based dual-loop control scheme is proposed in [24] to stabilize the system by injecting sufficient damping torque into networks that overcomes the aforementioned drawbacks. However, a small variation in the droop gain leads to an inaccurate power sharing in networks [24]. To overcome this issue, an adaptive V–I droop control approach is proposed in [25] in which the virtual resistance is emulated at the output terminal of converters. However, these control approaches so far discussed here can only ensure the stability of the system near nominal operating points as these control schemes are developed by considering small disturbances around actual operating regions. Therefore, the system will be unstable when large disturbances due to variations in RESs and loads appear in the system.

A model predictive controller (MPC) is proposed in [26] to improve the stability of the system and extends the operating point. Though the MPC can handle the operating point issue, it cannot ensure better transient behaviors in the presence of large disturbances as it is designed without considering model uncertainties. This limitation is addressed in [27,28] by designing a hybrid MPC using the Takagi–Sugeno fuzzy-based scheme in conjunction with a traditional MPC. However, an accurate dynamical model is required to achieve the desired performance, which is always practically obstructed due to the presence of external disturbances and model uncertainties. Furthermore, the online computational complexity of MPCs limited their practical application in real-time platforms.

Nonlinear control schemes can be used to stabilize the system by considering the nonlinearity issue of CPLs and non-minimum phase problem of DDBCs. In [29], a passivity-based nonlinear controller is designed to resolve the instability issue due to CPLs while improving the transient and dynamic behaviors of the DC-bus voltage. However, the damping performance is severely affected with variations in the system parameters, which is overcome in [30] by proposing an adaptive passivity-based approach. However, the major drawback of these approaches is that the non-minimum phase problem of DDBCs cannot be avoided and further deteriorates the overall stability margin under large disturbances. Moreover, a time-scale model is required to design these controllers, which are quite hard to deal with in realistic applications.

Nonlinear feedback linearizing controllers (FBLCs) have an uncertainty/noise decoupling capability as discussed in [31–34], and these controllers are used in [35,36] for stabilizing the DC-bus voltage by overwhelming the non-minimum phase problem associated with DDBCs and the instability issue caused by CPLs. Though the approaches in [35,36] tackle the instability issue due to CPLs, the elimination of non-minimum phase problems is not completely achieved. Another FBLC is proposed in [37], where the non-minimum phase problem associated arising from DDBCs is avoided by considering the

inductor current as an output function. However, the zero-dynamic stability is not presented in [37] though it is important and the control law in [37] is derived only for resistive loads though nonlinear dynamics of CPLs lead to unstable operation. Moreover, the performance of FBLC schemes so far discussed here highly rely on the precise parametric information of the system, which is quite impossible as these parameters change due to changes in operating points. On the other hand, the nonlinear sliding mode controller (SMC) is an effective approach for dealing with robustness against parameter uncertainties and external disturbances in both nonlinear and linear systems [38,39]. Hence, the parameter sensitivity problem of a FBLC can be resolved using SMC schemes and a robust pulse width modulation (PWM)-based SMC is used in [40] to achieve the desired transient and steady-state performance of DC microgrids where DDBCs feed CPLs. Similar approaches are presented in [41,42] to achieve the same control objective as that of [40]. Though SMCs effectively handle the effects of parameter variations, the utilization of a discontinuous function and fixed gain for the sliding surface results in unwanted chattering in control laws, which can even damage power electronic converters in practical applications.

The shortcomings of SMCs are overcome in [43–46] by proposing a nonlinear backstepping controller (BSC), and these controllers are explored in [47] for stabilizing DC-bus voltage in the DDBC feeding CPLs. However, the implementation of the BSC still requires knowing the accurate parameters of the system as neither parametric uncertainties nor external disturbances are incorporated during the design. The issues related to parametric uncertainties and external disturbances are alleviated in [48] using an adaptive BSC for ensuring the large signal stability of the DCDN with CPLs. However, an observer is used to estimate external disturbances, which is quite an expensive approach. Moreover, the non-minimum phase problem associated with DDBCs is not dealt with in this work. To avoid this drawback, a composite controller that is a combination of FBLC and adaptive BSC schemes is proposed in [49,50], where the non-minimum phases problem and impacts of the negative-impedance due to CPLs are canceled by transforming the nonlinear model into a linear canonical form. However, these controllers do not ensure better transient response when the system parameters change due to wide variations of operating points. Apart from this, the zero dynamic stability for the remaining state variables that are not transformed through the feedback linearization process is not discussed in these papers. To address the aforementioned problems, an SMC and adaptive BSC are combined in [51]. However, a conventional sliding surface is used in this controller ,which leads to the chattering phenomena in the control effort and makes it impossible to ensure the desired control performance.

Motivated from the limitations of existing literature, a composite scheme based on the backstepping double integral-sliding mode controller (BDI-SMC) is proposed in this work to enhance the stability of DDBC feeding CPLs in DCDNs. In this work, the issues related to the non-minimum phase arising from DDBCs and negative-impedance behaviors of CPLs are tackled by canceling nonlinearities and transforming the nonlinear dynamical model into a feedback linearized model using the exact feedback linearization approach. A double integral-sliding surface is then considered to derive the control law that can enhance the steady-state tracking performance while eliminating unwanted chattering effects. Afterwards, the actual control law is determined following design steps in both BSC and SMC. Finally, the feasibility of the actual control input in terms of maintaining the stability is analyzed using the Lyapunov function. A simulation study is conducted considering different operating scenarios of the system to verify its effectiveness. Additionally, its superiority is demonstrated by comparing the results with those of traditional nonlinear SMC and PI controllers.

2. System Description and Its Dynamical Model

The overall structure of a DCDN is depicted in Figure 1. It is well-known that the DC source generally consists of renewable energy-based distributed generation systems (DGS) such as solar photovoltaic (PV) system, rectifier in conjunction wind power generation

systems, etc., which works as the main power supply. The DDBCs are commonly used for interfacing the DC source with the main DC-bus so that the voltage requirement of various loads can easily be met. Among these loads, some tightly regulated loads draw constant power from the DC-bus, which are also known as CPLs and exhibit negative-impedance characteristics. The electrical characteristic of CPLs can be described using the following voltage–current relation:

$$i_{CPL} = \frac{P_{CPL}}{v_{bus}} \tag{1}$$

where i_{CPL} denotes the current of a CPL, P_{CPL} represents the power of a CPL, and v_{bus} is the DC-bus voltage. The concept of the small disturbance analysis can be applied around an equilibrium point of Equation (1). Based on this analysis, the equivalent impedance of a CPL can be expressed as follows:

$$R_{CPL} = \frac{\partial v_{bus}}{\partial i_{CPL}} = -\frac{P_{CPL}}{I_{CPL}^2} \tag{2}$$

where I_{CPL} is the CPL steady-state value of the current. From Equation (2), it is obvious that the negative-impedance behavior of a CPL creates a negative impact on the performance, i.e., it decreases the damping of the system, which further destabilizes the system, especially when it is connected with a converter. Since the nonlinearity introduced into system is due to CPLs, traditional linear controllers cannot guarantee the stability against large disturbances. Hence, the employment of a nonlinear controller is essential to neutralize the nonlinear effect of CPLs. However, to achieve such an objective from a controller, it is necessary to have an appropriate dynamical model. Hence, a dynamical model for DDBCs feeding a CPL is developed in the following to meet the controller design requirement.

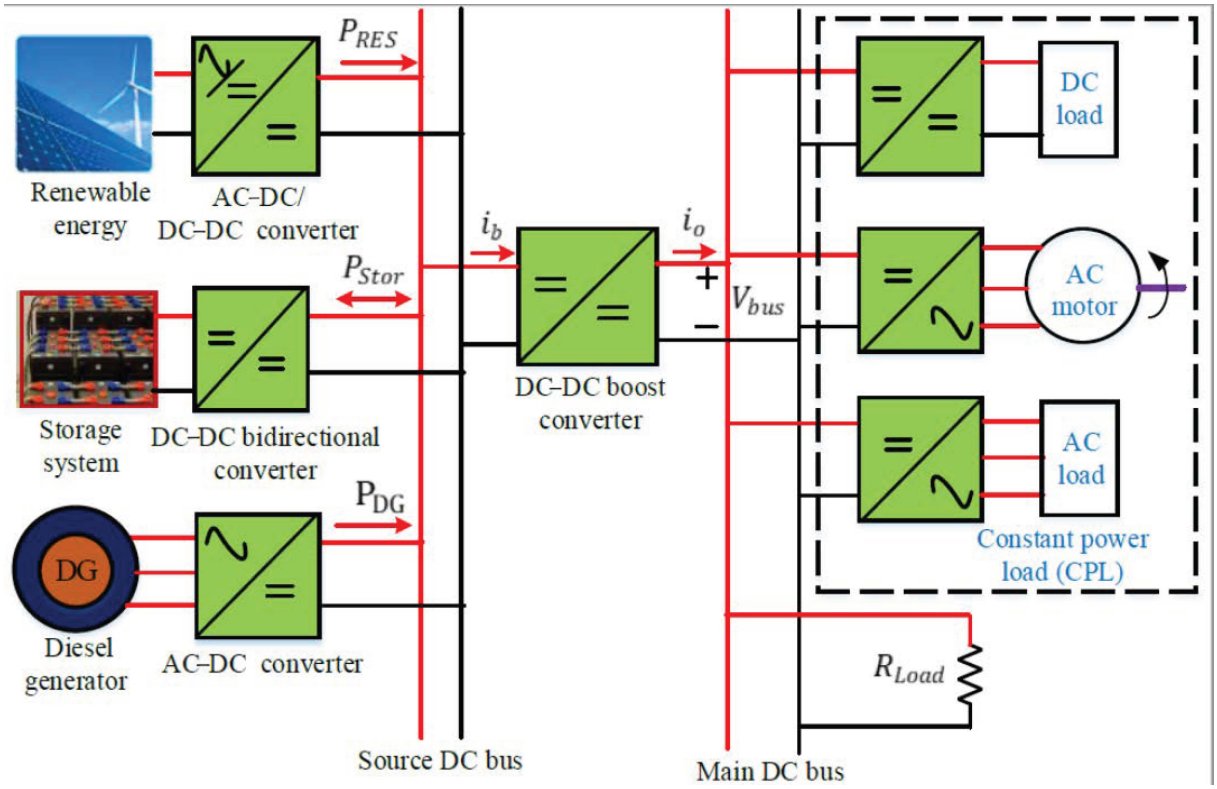


Figure 1. Typical layout of a DCDN.

The simplified structure of a DDBC feeding a CPL in DCDNs is shown in Figure 2. In this configuration, a current controlled source is used to represent a lumped CPL whereas

the lumped resistive load is represented by R_{Load}. It is worth mentioning that the input DC voltage source of the DDBC will be obtained from RESs or another DC–DC converter. Now, according to the simplified structure as shown in Figure 2, the expression of its model while on (T_{on}) and off (T_{off}) can be obtained as follows:

$$\dot{x} = (A_{on}x + b_{on})u + (A_{off}x + b_{off})(1 - u) \tag{3}$$

with

$$A_{on} = \begin{bmatrix} -\frac{r_b}{L_b} & 0 \\ 0 & -\frac{P_{CPL}}{v_{bus}} \end{bmatrix}, \; b_{on} = \begin{bmatrix} \frac{V_{in}}{L_b} \\ 0 \end{bmatrix}, \; A_{off} = \begin{bmatrix} -\frac{r_b}{L_b} & -\frac{1}{L_b} \\ \frac{1}{C_{bus}} & -\frac{P_{CPL}}{v_{bus}} \end{bmatrix}, \; b_{off} = \begin{bmatrix} \frac{V_{in}}{L_b} \\ 0 \end{bmatrix}, \; and \; x = \begin{bmatrix} i_b \\ v_{bus} \end{bmatrix}$$

where i_b represents the inductor current, V_{in} is the input voltage of the converter, v_{bus} is the main DC-bus voltage, L is the inductor, r_b is the parasitic resistance of an inductor, u is the duty cycle, and C_{bus} is the DC-bus capacitance. It worth noting that the inductor current, i_b, and the main DC-bus voltage, v_{bus}, are considered state variables. It is well-known that a discontinuous converter model can be approximated by a continuous model by selecting the converter switching frequency as being higher than the natural frequency. Hence, for continuous conduction mode (CCM) operations, the discontinuous control input u can be replaced by the duty ratio μ, which is a continuous function in the subinterval [0, 1]. Therefore, by considering the CCM operation, the model as represented by Equation (4) can be expressed as follows:

$$\begin{aligned} \frac{di_b}{dt} &= -\frac{r_b}{L_b} i_b + \frac{V_{in} - v_{bus}}{L_b} + \frac{v_{bus}}{L_b}\mu \\ \frac{dv_{bus}}{dt} &= \frac{1}{C_{bus}}\left(i_b - \frac{v_{bus}}{R_{Load}} - \frac{P_{CPL}}{v_{bus}}\right) - \frac{i_b}{C_{bus}}\mu \end{aligned} \tag{4}$$

The proposed BDI-SMC is designed based on the model as described by Equation (4) which is discussed in the next section.

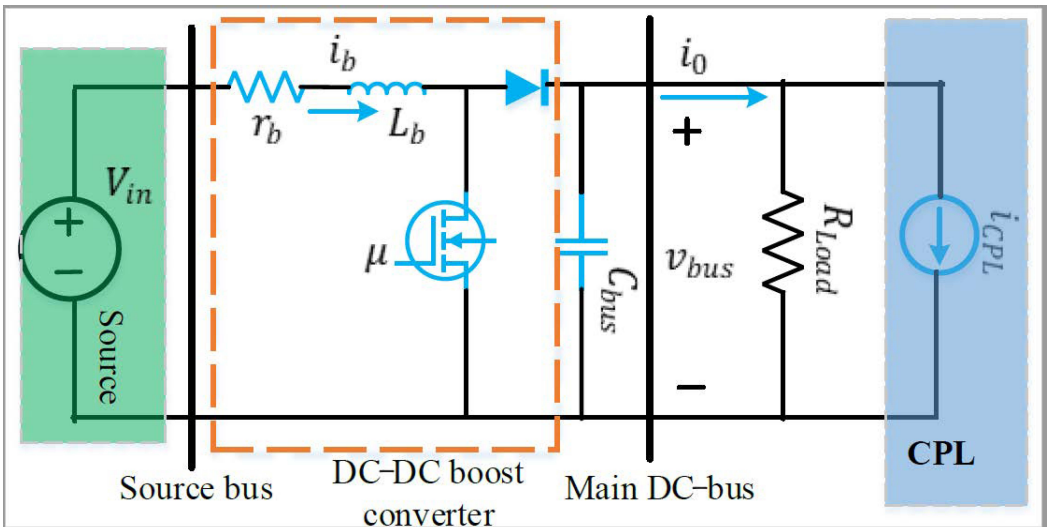


Figure 2. The simplified structure of a DDBC feeding a CPL.

3. Proposed Controller Design Approach

In this section, the proposed BDI-SMC is designed for DDBCs feeding CPLs. The key control objective is to achieve fast transient and desired steady-state tracking errors of the DC-bus voltage. However, the dynamical model represented by Equation (4) is not suitable for designing the BDI-SMC in its current form. Hence, the following steps need to be followed to make the model suitable for the controller design:

- Transformation of the model into an exactly linearized system using an exact feedback linearization approach and making it suitable to apply the backstepping control approach;
- Elimination of the non-minimum phase problem of DDBCs by considering the total stored energy and its rate of change as two new state variables;
- Derivation of the control law using the proposed scheme that satisfies the desired tracking performance to track the DC-bus voltage; and
- Stability analysis of the whole system with the newly derived control input performed using the Lyapunov stability theory.

All these steps are discussed in detail through the following subsections.

3.1. Transformation of the Model into an Exactly Linearized System Using the Exact Feedback Linearization

The transformation of the nonlinear model of the DDBC with a CPL in Equation (4) can be represented as the following generalized form:

$$\begin{aligned} \dot{x} &= f(x) + g(x)u \\ y &= h(x) \end{aligned} \tag{5}$$

where $x = [x_1, x_2, \ldots, x_n]^T$ is the state of the system, u is the input, y is the output of the system, and $f(x)$ and $g(x)$ are nonlinear functions of states and parameters with $g(x) \neq 0$. Fitting Equations (4) into (5), it can be written as follows:

$$f(x) = \begin{bmatrix} -\frac{r_b}{L_b}x_1 + (\frac{V_{in}-x_2}{L_b}) \\ \frac{1}{C_{bus}}(x_1 - \frac{x_2}{R_{Load}} - \frac{P_{CPL}}{x_2}) \end{bmatrix}, \text{ and } g(x) = \begin{bmatrix} \frac{x_2}{L_b} \\ -\frac{x_1}{C_{bus}} \end{bmatrix}^T$$

where $x = [i_b \;\; v_{bus}]^T$ and $u = \mu$. The following steps are necessary to transform the nonlinear system into an exactly linearized system using the exact feedback linearization scheme.

Step 1: Selection of the output function

The feedback linearizability depends on the output of the system, which can be selected in a different way. For the DDBC with a CPL, the output function can be chosen as any of the states (i.e., the capacitor voltage or inductor current) and the combination of these states in the form of the total energy of the system. The system becomes partially linearized when the capacitor voltage is selected as the output. Hence, the system will be a non-minimum phase one as the internal dynamic stability cannot satisfy the stability criterion. This issue can be tackled by selecting the inductor current as the output, which also makes the system partially linearized but with the stable internal dynamic. However, the regulation of the output voltage by indirectly controlling the inductor current results in excessive overshoot and slower response. Under this situation, the output needs to be chosen in such a way that satisfies the requirement of the exact linearization approach, i.e., the system is exactly linearized for which the relative degree of the exactly linearized system is equal to the order of the system. Based on this discussion, the total stored energy is considered an output function that can be expressed as follows:

$$y = h(x) = \frac{1}{2}L_b i_b^2 + \frac{1}{2}C_{bus}v_{bus}^2 \tag{6}$$

Step 2: Relative degree calculation

In this step, the relative degree for the nonlinear system as presented by Equation (5) is calculated using the Lie derivative while considering the output function in Equation (6). To calculate the relative degree, the following condition should be satisfied:

$$L_g L_f^{r-1} h(x) \neq 0 \tag{7}$$

In Equation (7), r is the relative degree while L represents the Lie derivative along the vector field denoted by the subscript. To satisfy the condition for the exact linearization approach, the relative degree of the nth order system will be $r = n$, which satisfies the following expressions:

$$\begin{aligned} &L_g L_f^{1-1} h(x) = L_g L_f^{2-1} h(x) = \ldots = L_g L_f^{n-2} h(x) = 0 \\ &L_g L_f^{n-1} h(x) \neq 0 \end{aligned} \tag{8}$$

Based on the model and output function, the following expressions are obtained:

$$\begin{aligned} r = n = 2 \\ L_g L_f^{1-1} h(x) = 0 \end{aligned}$$

and

$$L_g L_f^{n-1} h(x) \neq 0$$

Hence, the system is exactly linearized.

Step 3: Nonlinear coordinate transformation and exact linearization

In this step, the coordinate transformation technique is adopted to convert the original x state variables into new z state variables, which can be discussed as follows:

$$z_1 = h(x) = L_f^{1-1} h(x) = \frac{1}{2} L_b i_b^2 + \frac{1}{2} C_{bus} v_{bus}^2 \tag{9}$$

in which the dynamic can be written as

$$\dot{z_1} = \frac{\partial h(x)}{\partial x} \dot{x} \tag{10}$$

Using Equation (5), Equation (10) can be written as follows:

$$\dot{z_1} = \frac{\partial h(x)}{\partial x} f(x) + \frac{\partial h(x)}{\partial x} g(x) u = L_f h(x) + L_g L_f^{1-1} h(x) u \tag{11}$$

Since $L_g L_f^{1-1} h(x) = 0$, Equation (11) can be written as follows:

$$\dot{z_1} = z_2 = L_f h(x) = V_{in} x_1 - \frac{x_2^2}{R_{Load}} - P_{CPL} - r_b x_1^2 \tag{12}$$

Equation (12) can be written as follows:

$$\dot{z_2} = L_f^2 h(x) + L_g L_f^{2-1} h(x) u = \nu \tag{13}$$

Since $L_g L_f^{2-1} h(x) \neq 0$, the original nonlinear system can be represented as the following exactly linearized form:

$$\begin{aligned} \dot{z_1} = z_2 \\ \dot{z_2} = \nu \end{aligned} \tag{14}$$

where z_1 and z_2 are the state variables of the exactly linearized system and ν is the control variable of the transformed linear systems. The model in Equation (14) can be rewritten as follows:

$$\begin{aligned} \dot{z_1} = z_2 \\ \dot{z_2} = \nu = a(x) + b(x) \mu \end{aligned} \tag{15}$$

where

$$a(x) = L_f^2 h(x) = \frac{(V_{in} - 2x_1 r_b)(V_{in} - x_2 - r_b x_1)}{L_b} - \frac{2x_2}{R_{Load} C_{bus}}(x_1 - \frac{x_2}{R_{Load}} - \frac{P_{CPL}}{x_2})$$

$$b(x) = L_g L_f h(x) = \frac{(V_{in} - 2x_1 r_b)x_2}{L_b} + \frac{2x_1 x_2}{R_{Load} C_{bus}}$$

The proposed controller is designed based on this model, which is discussed in the following subsection.

3.2. Controller Design

In this subsection, the control law is determined using the combination of backstepping and double integral-sliding mode control schemes. Here, the main objectives are to track z_1 and z_2, which ultimately ensures the desired tracking of the DC-bus voltage under large disturbances. The following steps describe the design process for the proposed BDI-SMC.

Step 1: For fulfilling the design objective, the first tracking error (e_1) can be defined as follows:

$$e_1 = z_1 - z_{1(ref)} \tag{16}$$

where $z_{1(ref)}$ is the reference value of the state z_1, which can be calculated as follows:

$$z_{1(ref)} = \frac{1}{2} L_b i_{b(ref)}^2 + \frac{1}{2} C_{bus} v_{bus(ref)}^2 \tag{17}$$

where $i_{b(ref)}$=$\frac{P_{CPL}}{V_{in}}$ is the reference value of the inductor current and $v_{dc(ref)}$ is the reference value of the DC-bus voltage. Now, the dynamic of e_1 using Equation (16) can be obtained as follows:

$$\dot{e_1} = z_2 - \dot{z_{1(ref)}} \tag{18}$$

As the actual control input does not appear in Equation (18), z_2 is assumed to be the virtual control input and γ is assumed to be the corresponding stabilizing function or virtual control law. Hence, the final error (e_2) can be defined as follows:

$$e_2 = z_2 - \gamma \tag{19}$$

Using Equation (19), Equation (18) can be rewritten as follows:

$$\dot{e_1} = e_2 + \gamma - \dot{z_{1(ref)}} \tag{20}$$

At this stage, it is required to check the stability of the tracking error dynamic $\dot{e}_1$, and to do this, the following Lyapunov function (LF) is considered:

$$W_1 = \frac{1}{2} e_1^2 \tag{21}$$

in which the time derivative using Equation (20) can be written as follows:

$$\dot{W}_1 = e_1[e_2 + \gamma - \dot{z_{1(ref)}}] \tag{22}$$

From Equation (22), γ can be selected as follows:

$$\gamma = -k_1 e_1 + \dot{z_{1(ref)}} \tag{23}$$

where k_1 is a positive constant. Substituting Equations (23) into (22) yields the following:

$$\dot{W}_1 = -k_1 e_1^2 + e_1 e_2 \tag{24}$$

From Equation (24), it can be seen that, if $e_2 = 0$, then $\dot{W}_1 \leq 0$. To achieve this, the next step is essential.

Step 2: The dynamic of e_2 can be written as follows:

$$\dot{e_2} = \dot{z_2} - \dot{\gamma} \tag{25}$$

Using Equation (15), the dynamic of e_2 can be expressed as follows:

$$\dot{e_2} = a(x) + b(x)\mu - \dot{\gamma} \tag{26}$$

At this instant, a double-integral sliding surface in term of e_2 can be selected as follows:

$$S = e_2 + \alpha_1 \int e_2 dt + \alpha_2 \int \int e_2 dt dt \tag{27}$$

where α_1 and α_2 are constant parameters of the sliding surface. The dynamic of Equation (27), using the value of $\dot{e}_2$, can be expressed as follows:

$$\dot{S} = a(x) + b(x)\mu - \dot{\gamma} + \alpha_1 e_2 + \alpha_2 \int e_2 dt \tag{28}$$

It is well-known that appropriately selecting a reaching law is very important to mitigate the chattering while improving the convergence time. Hence, a reaching law is selected as follows to meet the above objective:

$$\dot{S} = -\beta_1 sgn(S) - \beta_2 S \tag{29}$$

where β_1 and β_2 are positive constants and the chattering effect depends on these values. Combining Equations (28) and (29), it can be written as follows:

$$a(x) + b(x)\mu - \dot{\gamma} + \alpha_1 e_2 + \alpha_2 \int e_2 dt = -\beta_1 sgn(S) - \beta_2 S \tag{30}$$

From Equation (30), the actual control law can be determined as follows:

$$\mu = -\frac{1}{b(x)}[a(x) - \dot{\gamma} + \alpha_1 e_2 + \alpha_2 \int e_2 dt + \frac{1}{S} e_1 e_2 + \beta_1 sgn(S) + \beta_2 S] \tag{31}$$

Substituting Equation (31) into Equation (28) yields

$$\dot{S} = -\beta_1 sgn(S) - \beta_2 S - \frac{1}{S} e_1 e_2 \tag{32}$$

The following Lyapunov function is selected to ensure overall stability with the derived control law:

$$\dot{W}_2 = W_1 + \frac{1}{2} S^2 \tag{33}$$

Using Equations (24) and (32), $\dot{W}_2$ can be written as follows:

$$\dot{W}_2 = -k_1 e_1^2 - \beta_1 |S| - \beta_2 S^2 \tag{34}$$

Since $k_1 > 0$, $\beta_1 > 0$, and $\beta_2 > 0$, $\dot{W}_2 \leq 0$. Thus, the overall stability of the system is guaranteed with the designed control law as represented by Equation (31). The effectiveness of the designed BDI-SMC is demonstrated in the next section.

4. Simulation Results

To verify the effectiveness of the designed composite BDI-SMC strategy, a similar simulation model as that shown in Figure 2 is built on the MATLAB/Simulink platform.

The nominal voltage of the main-DC bus of the distribution network is considered as 110 V while the rated power of DC loads is considered as 2 kW. In order to capture the highest destabilization effect of the DC load on the DC distribution network, a pure CPL is considered the DC power demand rather than taking into account the composite load demand. The frequency of the power electronic interface boost converter is set as 5 kHz with a sampling frequency of 100 kHz to evaluate the performance of the designed BDI-SMC. It is well-known that, during the implementation of controllers, it is essential to know the system parameters. Hence, the system parameters used for the simulation study are listed in Table 1. The gain parameters of the designed nonlinear controller are listed as follows: $k_1 = 1000$, $\alpha_1 = 70$, $\alpha_2 = 0.45$, $\beta_1 = 100$, and $\beta_2 = 0.01$. It is worth mentioning that the gain parameters are selected based on the trial and error method to meet the desired control objective.

Table 1. Nominal system parameters of the system.

Parameters	Description	Value
V_{in}	Supply voltage	55 V
V_{bus}	Main DC-bus voltage	110 V
P_{CPL}	Nominal power in constant power load	2 kW
r_b	Parasitic resistance of an inductor	2 mΩ
L_b	Inductance of the converter	5 mH
C_{bus}	Capacitance of the main DC-bus	6 mF
R_{Load}	Resistive Load	∞

The performance of the BDI-SMC is verified by widely varying the operating region by considering the variations in the reference power of CPLs, main DC-bus reference voltage, and input power in terms of the input source voltage. Therefore, the following three case studies are considered to demonstrate the performance of the designed controller:

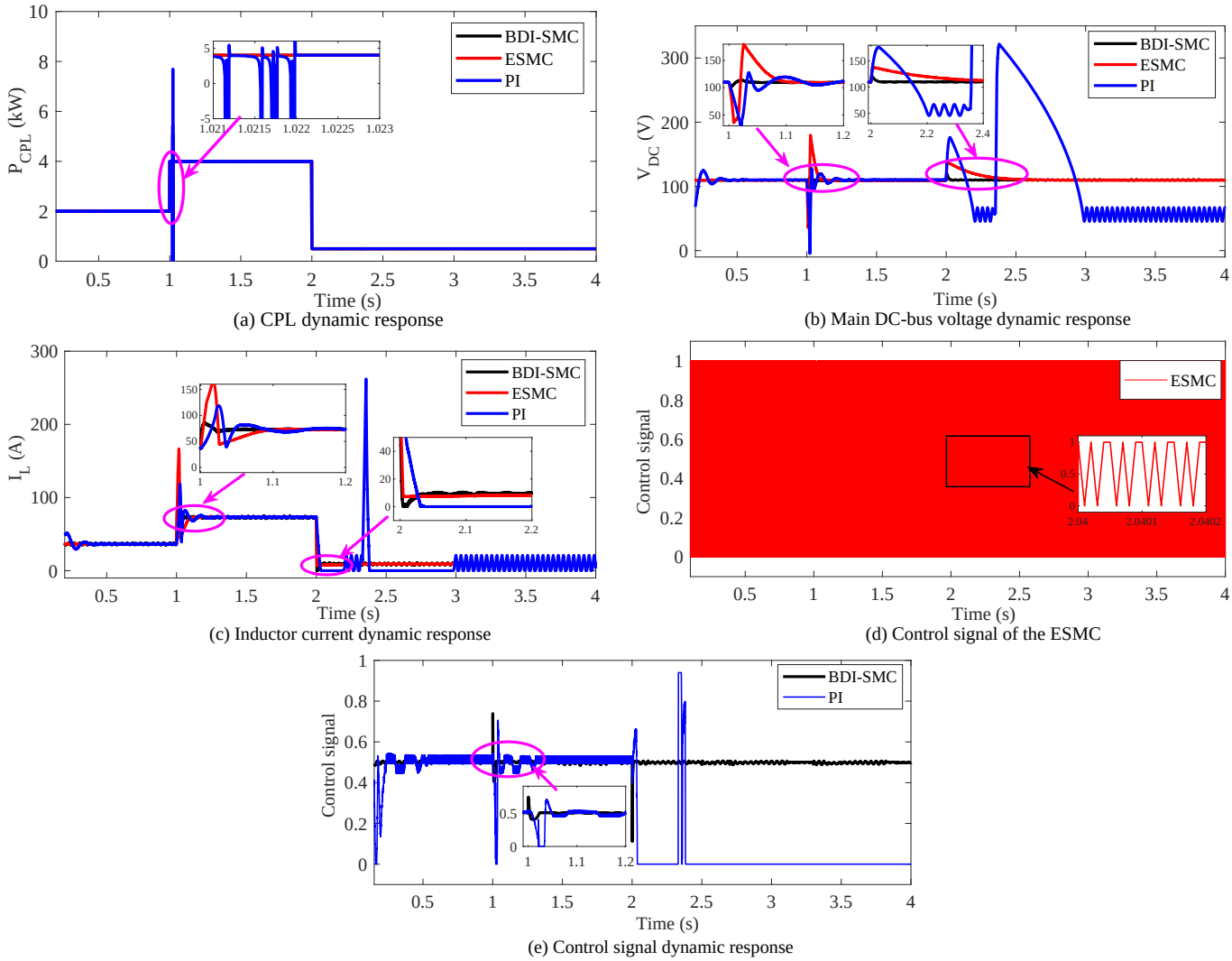
- **Case I:** Controller performance investigation with variations in the reference power of the CPL;
- **Case II:** Controller performance investigation with variations in the reference voltage of the DC-bus; and
- **Case III:** Controller performance investigation with variations in the input voltage.

To show the merits of the designed BDI-SMC, the performance is also compared with the existing SMC (ESMC), as proposed in [40], and with a conventional proportional-integral (PI) controller.

Case I: Controller performance investigation with variations in the reference power of the CPL

In this scenario, the variation in the reference power of CPLs is taken into consideration to evaluate the performance of the designed controller and existing controllers. At the beginning of the simulation, the rated power of the CPL is considered as 2 kW whereas it is increased to 4 kW at t = 1 s. On the other hand, other parameters are kept unchanged. Due to the transient power of CPLs, as shown in Figure 3a, the post-disturbance dynamic response of the main DC-bus and inductor current are affected, which can be seen in Figure 3b,c, respectively. From these responses, it can be observed that all three controllers can ensure stability. However, the designed BDI-SMC can provide faster dynamic responses along with less undershoot compared with the ESMC and PI. Again at t = 2 s, the CPL power is decreased from 4 kW to 500 W, which is considered a large disturbance in the system. Due to this large disturbance, the conventional PI controller is unable to provide sufficient damping torque into the networks, consequently leading to instability in both the main DC-bus voltage and inductor current, which can be clearly seen from Figure 3b,c. Meanwhile, both the designed BDI-SMC and the ESMC can ensure stability, which can be clearly seen from Figure 3b,c, respectively. However, though both controllers can maintain zero output voltage tracking errors, the designed BDI-SMC ensures a faster settling time and less overshoot. The corresponding control signal for all three controllers is depicted in

Figure 3d,e, where it is obvious that the designed control signal is more stable compared with the PI and ESMC controllers. Furthermore, it can be observed that the designed controller can effectively eliminate the chattering effect on the PWM whereas the ESMC cannot attenuate the chattering effect.



(a) CPL dynamic response

(b) Main DC-bus voltage dynamic response

(c) Inductor current dynamic response

(d) Control signal of the ESMC

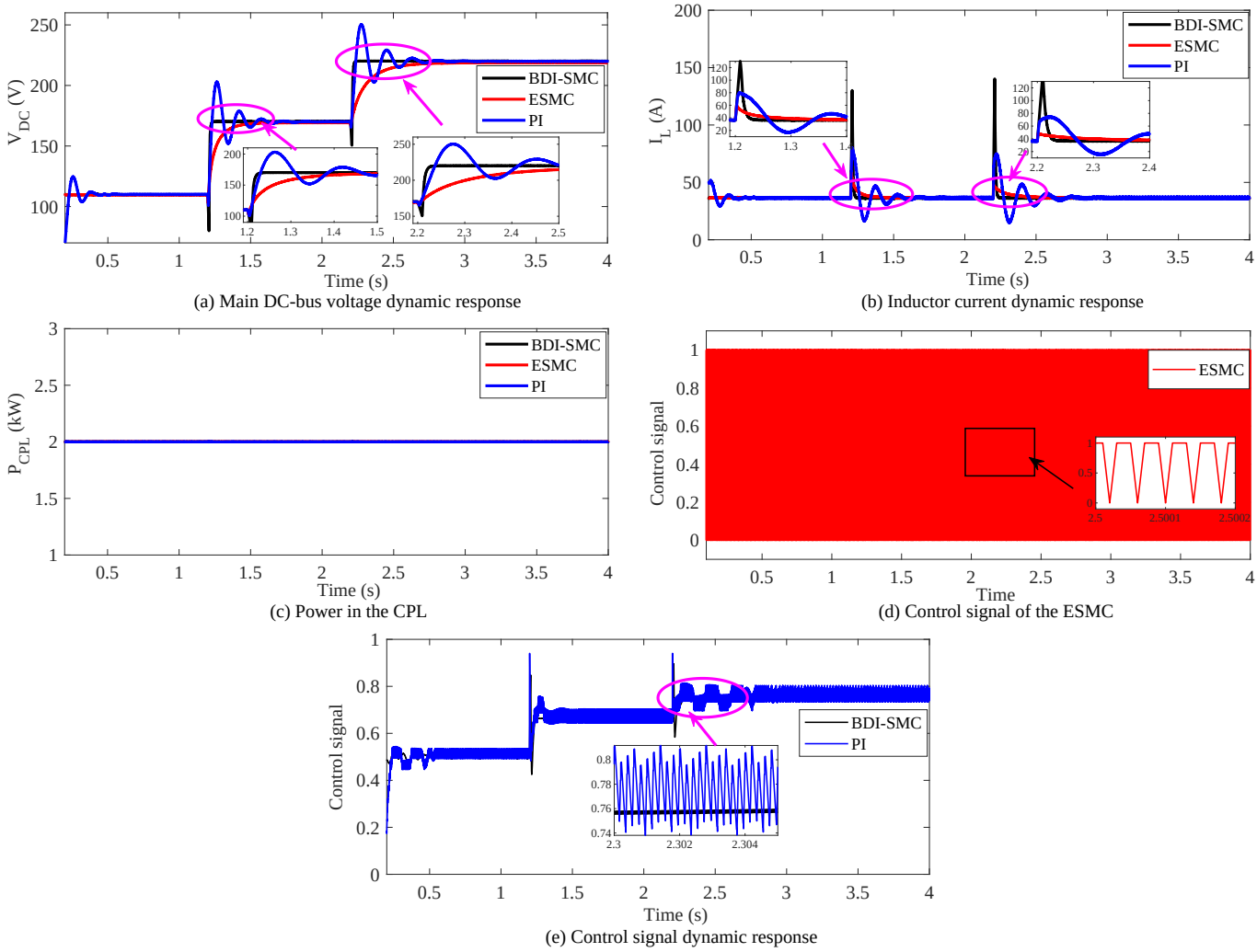
(e) Control signal dynamic response

Figure 3. Dynamic response of the system with the variations in the CPL reference power.

Case II: Controller performance investigation with the variations in the reference voltage of the DC-bus

In this case study, the main DC-bus voltage increases from its equilibrium state 110 V to 160 V at t = 1.2 s and again increases from 160 V to 220 V at t = 2.2 s, whereas the CPL is set as 2 kW. The corresponding system responses are illustrated in Figure 4. From Figure 4a, it can be observed that the PI and ESMC cannot ensure a main DC-bus voltage tracking performance with a faster settling time and less overshoot/undershoot whilst the BDI-SMC can quickly track the new reference main DC-bus voltage as the settling time overshoot/undershoot are close to zero. Similarly, from Figure 4b, it can be observed that the designed BDI-SMC can provide a faster dynamic performance compared with the ESMC and PI. However, although the overshoot/undershoot in the inductor current is less with the ESMC, the control signal contains higher chattering, as illustrated in Figure 4d. As a result, the switching losses are higher, which reduces the overall system performance. On the other hand, the designed BDI-SMC is able to provide an oscillation-free control signal to the PWM compared with the ESMC, which can be clearly seen from

Figure 4d,e. Throughout this simulation study, the load power is constant due to the electrical characteristics of the CPL, which is shown in Figure 4c.



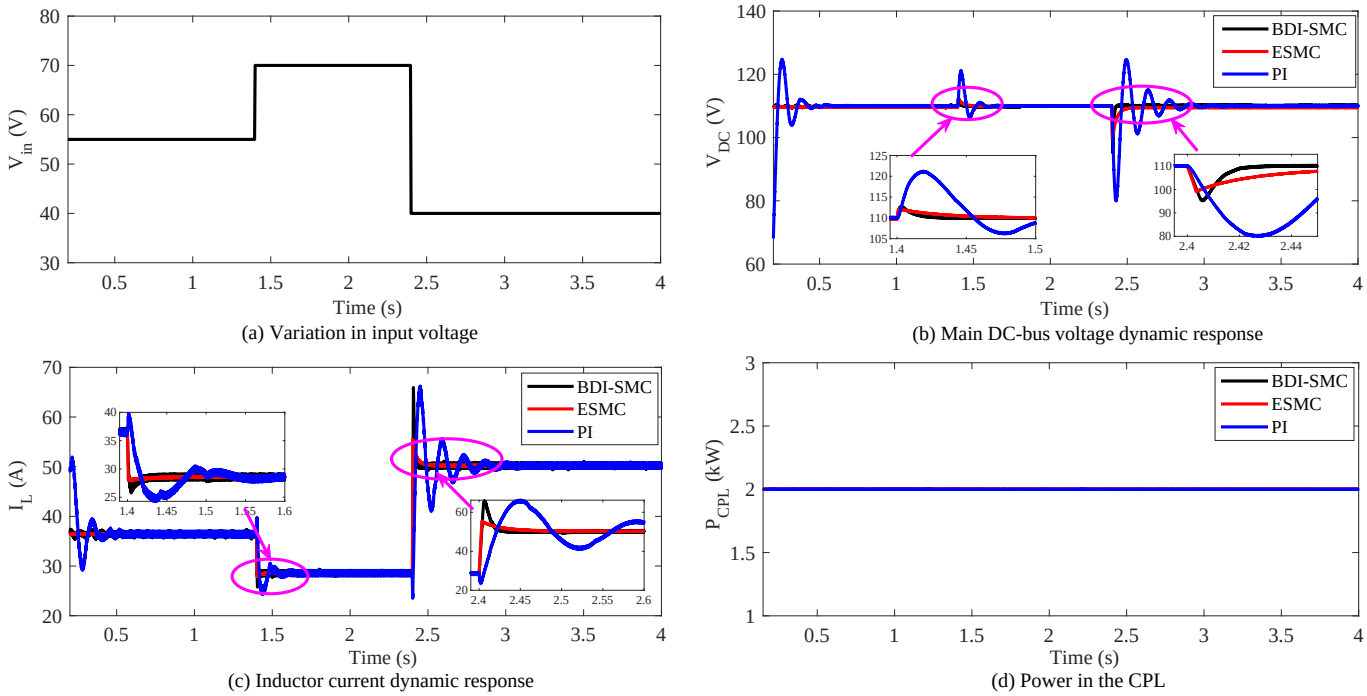
(a) Main DC-bus voltage dynamic response
(b) Inductor current dynamic response
(c) Power in the CPL
(d) Control signal of the ESMC
(e) Control signal dynamic response

Figure 4. Dynamic response of the system with the variations of the main DC-bus reference voltage.

Case III: Controller performance investigation with the variations in the input voltage

Practically, the output power of RESs is continuously changeable due to their intermittent characteristics. To show that impact on the distribution network, in this case study, the variation in the input power is considered. For this purpose, the input voltage of the DC voltage increases from 55 V to 70 V and decreases from 70 V to 40 V at t = 1.4 s and t = 2.4 s, respectively. Figure 5 shows the corresponding dynamic responses of the system. From Figure 5b,c, it can be observed that all three controllers can accurately track the main DC-bus voltage and inductor current when input voltage variation occurs. However, the designed BDI-SMC has a faster dynamic response and a smaller overshoot compared with the ESMC and conventional PI control methods. Moreover, it can be seen that the CPL remained unchanged at the equilibrium state 2 kW, which is illustrated in Figure 5d.

From the above simulation results, it can be concluded that the designed BDI-SMC can provide fast dynamic convergence speed, accurate tracking of the DC-bus voltage, and good large disturbances stability for a DC–DC boost converter feeding a CPL. Moreover, it is obvious that the stability of the DC-bus voltage is not destroyed even after the large variations in the CPL power. Hence, the simulation result is consistent with the theoretical analysis.



(a) Variation in input voltage

(b) Main DC-bus voltage dynamic response

(c) Inductor current dynamic response

(d) Power in the CPL

Figure 5. Dynamic response of the system with the variations in the input voltage.

5. Conclusions

A composite nonlinear controller combining the backstepping control theory and double integral-sliding mode control theory is proposed for a DC–DC boost converter feeding a CPL with distribution networks. In order to design the proposed controller, a canonical form is developed using the exact feedback linearization approach by considering the total stored energy as the output function. Based on the canonical form of the model, a composite nonlinear controller is designed to guarantee DC-bus voltage stability under large disturbances of a DC–DC boost converter feeding CPLs with negligible steady-state tracking error and fast transient responses. The effectiveness and theoretical analysis of the designed controller are verified through simulation results. In the future, a robust adaptive nonlinear composite controller will be designed by considering both parametric uncertainty and external disturbances.

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Abbreviations

The following abbreviations are used in this manuscript:

BDI-SMC	Nonlinear Backstepping Double Integral-Sliding Mode Controller
BSC	Nonlinear Backstepping Controller
CPL	Constant Power Load
CCM	Continuous Conduction Mode
DGSs	Distributed Generation Systems
DDBC	DC–DC Boost Converter
DCDNs	DC Distribution Networks
ESMC	Existing Sliding Mode Controller
FBLCs	Nonlinear Feedback Linearizing Controllers
MPC	Model Predictive Controller
PV	Solar Photovoltaic
PECs	Power Electronic Converters
PI	Proportional-Integral Controller
PWM	Pulse Width Modulation
RESs	Renewable Energy Sources
SMC	Sliding Mode Controller
VPSs	Vehicular Power Systems

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