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Symmetrical Cascaded Switched-Capacitor Multilevel Inverter Based on Hybrid Pulse Width Modulation

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Abstract: Multilevel inverters have been widely used in various industrial applications such as renewable energy generation and electric vehicles. An improved circuit of symmetrical cascaded switched-capacitor multilevel inverter is proposed so that the reactive power is absorbed by its power supply instead of capacitors. Then, a special hybrid pulse width modulation strategy combing level-shifted pulse width modulation (LS-PWM) and phase-shifted pulse width modulation (PS-PWM) was developed for the inverter. With this modulation algorithm, the power between cascaded units is automatically balanced, and the voltage of the capacitor in each unit is also automatically balanced to the dc input voltage. In addition, the optimized capacitor voltage ripple makes it possible to use a smaller capacitor to produce a better output voltage waveform. Theoretical analysis, simulation and experimental results show that the equivalent switching frequency of the cascaded multilevel inverter is twice the original frequency so that the output voltage harmonics are only distributed near even multiples of the carrier frequency.

Keywords: cascaded multilevel inverter; switched-capacitor; PWM modulation; reactive power

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1. Introduction

Recently, multilevel inverters have been widely used in photovoltaic power generation, energy vehicles and high voltage DC (HVDC) transmission since it not only offers the advantage of low voltage stress across switching devices on the occasion of high voltage application but also generates a sinusoidal output waveform with reduced harmonic distortion at low switching frequency [1,2].

Basically, multilevel inverters can be categorized into three types: diode-clamped, capacitor-clamped, and cascaded H-bridge. One dc voltage source is equipped in the diode-clamped and capacitor-clamped multilevel inverter, which utilizes diodes or capacitors to divide the dc source voltage into multiple voltage levels. A large number of power switches, complex switching strategies and capacitor voltage balancing control are required for the clamped-type multilevel inverter [3–5]. On the other side, the cascaded H-bridge multilevel inverter has less switch voltage stress, and it is easy to realize the modular design. However, multiple isolated dc sources are required [6,7].

In order to overcome the limitation of the conventional multilevel inverters, a variety of novel topologies have been proposed, such as modular multilevel converter (MMC) [8,9], Z-source inverter [10,11], switched boost inverter [12,13], switched-capacitor (SC) inverter [14–24], etc. The switched-capacitor multilevel inverter has especially gained more popularity because of its self-voltage balancing and boosting ability. In [17,18], by constructing an H-shaped SC cell with three switches and two voltage sources (dc sources or capacitors), the voltage sources are connected in series or parallel by controlling the three switches appropriately, thus more numbers of voltage levels are generated. In [19],

two switches of an SC cell are replaced by two diodes so that the modulation circuit design is simplified. In [20], a new SC cell consisting of four switches, two diodes and two capacitors is proposed to produce more output voltage levels. A single back-end H-bridge inverter is connected in [17–20], and the voltage stress of the H-bridge power switches is large, which is equal to the maximum voltage level of the dc bus.

In order to reduce the voltage stress of the H-bridge switches and the number of isolated dc voltage sources, the switched-capacitor techniques are integrated into a cascaded H-bridge multilevel inverter in [21] by adding bidirectional switches between H bridges. Most of the dc voltage sources in the cascaded multilevel inverter are replaced by capacitors, which are charged by a single dc source with the help of bidirectional switches. Further, a low-voltage SC cell and a high-voltage SC cell consisting of seven switches, four capacitors and two diodes are inserted into the dc sides of two cascaded H-bridges to generate more output voltage levels [22]; however, the modulation for power switches is rather complex.

A simple SC cell, consisting of two switches, one diode and one capacitor, is embedded between the dc power supply and H-bridge [23,24]. With the SC cell, two voltage levels in the dc bus and five voltage levels in the output of the H-bridge are obtained. Nevertheless, when reactive power flows from the inductive load to the input, the backflow current would keep charging the capacitor in the SC cell due to the existence of the diode. Thus, it is possible that the capacitor voltage reaches far beyond the dc source voltage when dealing with large reactive power. In addition, symmetrical phase-shift modulation in [23] leads to a power imbalance between cascaded units. Different dc voltage source values are assigned in [24] to produce the maximum number of voltage levels at the output, which aggravates the problem of the power imbalance between cascaded units.

In this paper, the diode of the SC cell in [23,24] is replaced by a power switch, realizing a bidirectional current flow and thus improving the reactive power capability of the inverter. As a result, each cascaded unit involves one capacitor and seven transistors as well as one dc source. More output levels can be obtained by cascading multiple units. Besides, a hybrid pulse width modulation combining level-shifted pulse width modulation (LS-PWM) and phase-shifted pulse width modulation (PS-PWM) was developed for the symmetrical cascaded switched-capacitor multilevel inverter. With this modulation algorithm, the power between cascaded units as well as the voltage of the capacitor in the SC cell is automatically balanced, and the capacitor voltage ripple is effectively minimized. In summary, with the hybrid pulse width modulation, the proposed cascaded SC multilevel inverter has the following highlights:

- ➢ Self-balanced capacitor voltages;
- ➢ Self-balanced power among cascaded SC cells;
- ➢ Reduced capacitor voltage ripple;
- ➢ Enhanced reactive power capability.

2. Cascaded Switched-Capacitor Multilevel Inverter

2.1. Circuit Description

Figure 1 shows a switched-capacitor multilevel inverter cascaded by n units, and every unit consists of a dc voltage source E_i ($i = 1, 2, \ldots, n$), an SC cell, and an H-bridge.

The main difference between Figure 1 and the proposed circuit in [23] is that the charging diode of SC is replaced by MOSFET (S_{i5}). As mentioned above, the reactive power capability of the inverter can be improved, and the system power loss can also be significantly reduced since the conduction loss of a MOSFET is much smaller than that of a diode, especially when the charging current is large in low voltage side.

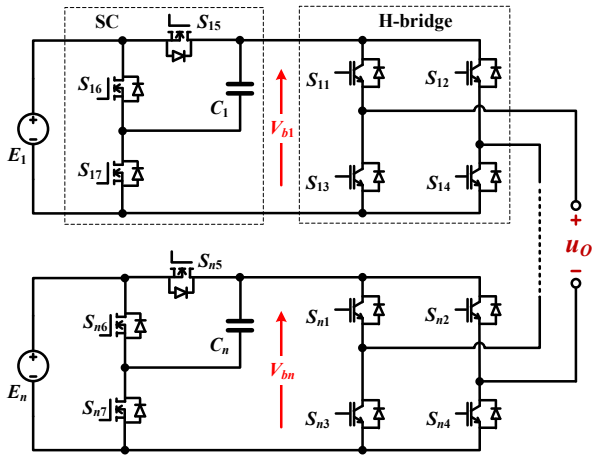


Figure 1. Cascaded switched-capacitor multilevel converter.

2.2. Operation Principle

In each unit, the SC cell includes switches (S_{i5}, S_{i6}, and S_{i7}) and capacitor C_i, and the H-bridge is composed of switches S_{i1}~S_{i4}. In the SC cell, the switches S_{i5} and S_{i7} are turned on/off simultaneously and have a complementary pulse signal with S_{i6}. When S_{i5} and S_{i7} are turned on, and S_{i6} is off, the capacitor C_i is parallelly connected to the dc source, and the dc bus voltage V_{bi} is equal to E_i. When S_{i5} and S_{i7} are turned off, and S_{i6} is turned on, the capacitor C_i is in series with the dc source. Since C_i was charged to the dc source voltage E_i in the previous state, the dc bus voltage V_{bi} is equal to $2E_i$. It can be concluded that the capacitor is charged when connected in parallel and discharged when connected in series. By converting the capacitor and the dc source in series or in parallel connection, the dc bus has two voltage levels: E_i and $2E_i$. With the operation of the H-bridge, a total of five voltage levels is produced for each unit, i.e., 0, $\pm E_i$ and $\pm 2E_i$. The detailed operation state circuits under resistive load are shown in Figure 2. From the analysis, power switches of different voltage ratings should be selected for the SC cell and H-bridge. The voltage stress of all power switches in the SC cell is E_i, and the voltage stress of switches in the H-bridge is $2E_i$.

If the dc sources are independent, and its voltage meets $E_{i+1} = 3E_i$ or $E_{i+1} = 5E_i$, the circuit shown in Figure 1 is configured as an asymmetric cascaded switched-capacitor multilevel inverter, from which more voltage levels are produced. However, since the voltage and power rating of each unit is different, each unit needs to be designed separately, and it is difficult to realize the modular design.

If the dc source values are equal to E, the circuit shown in Figure 1 is configured as a symmetrical cascaded switched-capacitor multilevel inverter. The voltage rating of each cell is the same, and its power rating is also the same under appropriate modulation strategy; therefore, modular design is realized, and only a single unit needs to be designed. In the following, we focus on a symmetrical switched-capacitor multilevel inverter cascaded by two units. Five voltage levels of 0, $\pm E$ and $\pm 2E$ are produced by each unit, so the cascaded inverter has a total of $5 \times 5 = 25$ working status, resulting in nine voltage levels of 0, $\pm E$, $\pm 2E$, $\pm 3E$ and $\pm 4E$ for the inverter's output, as shown in Table 1. However, there is only one combination for the output voltage level $\pm 4E$, and there are several redundant states for other voltage levels. Therefore, it is important to design the modulation algorithm to select an appropriate redundant state in order that the power between cascaded modules can be balanced automatically and the voltage ripple of the switched capacitor could be minimized.

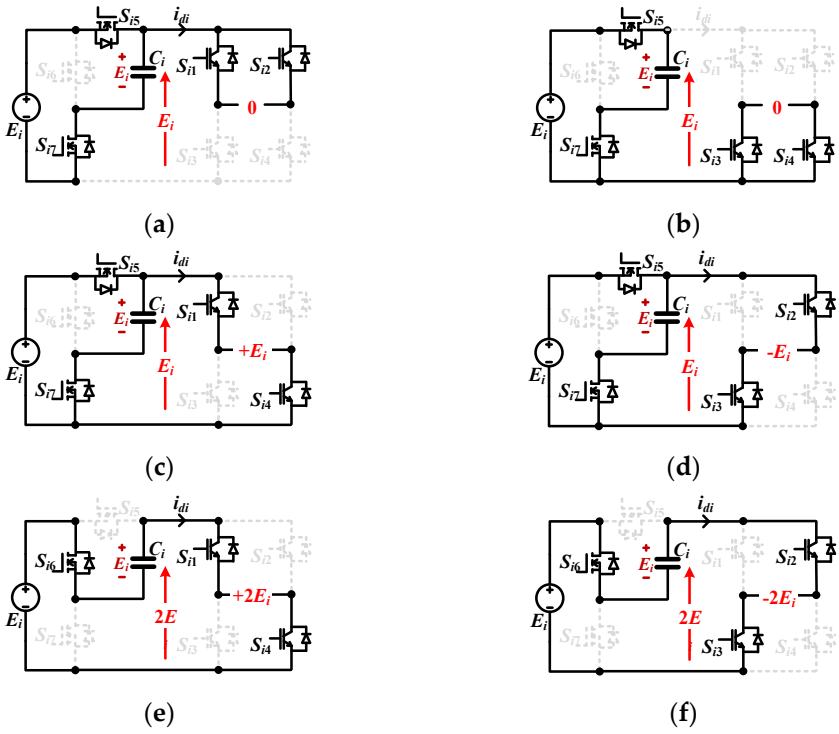


Figure 2. Switching modes of an optimized cascaded unit. (**a**) Mode 1, (**b**) Mode 2, (**c**) Mode 3, (**d**) Mode 4, (**e**) Mode 5, (**f**) Mode 6.

Table 1. Working status of the cascaded inverter.

Number	u_{O1}	u_{O2}	u_O
1	+2E	+2E	+4E
2	+2E	+E	+3E
3	+E	+2E	
4	+E	+E	
5	0	+2E	+2E
6	+2E	0	
7	+E	0	
8	0	+E	+E
9	+2E	−E	
10	−E	+2E	
11	+2E	−2E	
12	+E	−E	
13	0	0	0
14	−E	+E	
15	−2E	+2E	
16	−2E	+E	
17	+E	−2E	−E
18	0	−E	
19	−E	0	
20	0	−2E	
21	−2E	0	−2E
22	−E	−E	
23	−2E	−E	−3E
24	−E	−2E	
25	−2E	−2E	−4E

2.3. Enhanced Reactive Power Capability of the Proposed Circuit

Since the current of the dc bus i_{di} is always positive under resistive load, the switching modes of our proposed circuit and the one in [23] are completely the same. However, there is a significant difference between the two circuits if an inductive load is connected. As shown in Figure 3, when the load is inductive, a phase shift φ between the output voltage and output current of the inverter will lead to a negative i_{di} in the dc bus. Take the first-half period, for example, i_{di} is negative during $0\sim t_2$ and positive during $t_2\sim t_4$.

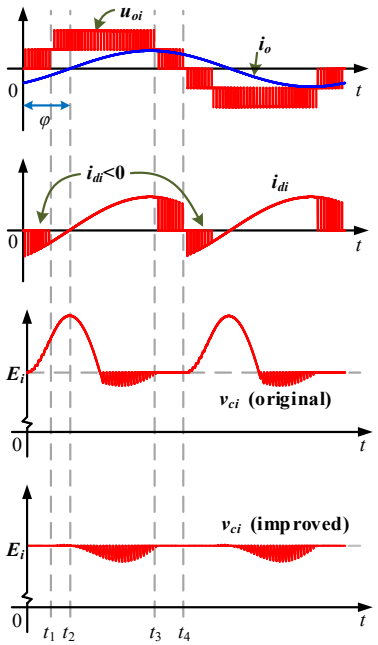


Figure 3. Operation waveforms under inductive load.

During $0\sim t_2$, for our proposed circuit, as shown in Figure 2e, at Mode 5, when the dc bus voltage is $2E_i$, the negative i_{di} will charge the capacitor C_i and cause a voltage rise on the capacitor. To the next state, when the dc bus voltage switches to E_i, as shown in Figure 2c, due to the existence of the switch S_{i5}, the capacitor discharges immediately, and its voltage is clamped to the dc source voltage E_i. In contrast, for the proposed circuit in [23], due to the existence of diode in SC cell, whether in Mode 3 or Mode 5, as shown in Figure 4, the negative current i_{di} keeps charging the capacitor. The process continues until the current i_{di} reverses at t_2 instant, which results in a continuous rise of the capacitor voltage during $0\sim t_2$.

When the output voltage u_{oi} is negative, according to the switching modes of Mode 4 and Mode 6 in Figures 2 and 4, the situation is quite similar. The capacitor voltage of our proposed circuit is maintained around the source voltage E_i, but the capacitor voltage of the inverter in [23] will keep rising until the inverter's output voltage and current are in the same direction. It is obvious that the reactive power capability in [23] is limited due to its high capacitor voltage, while the proposed circuit in this paper can work properly under a large inductive load.

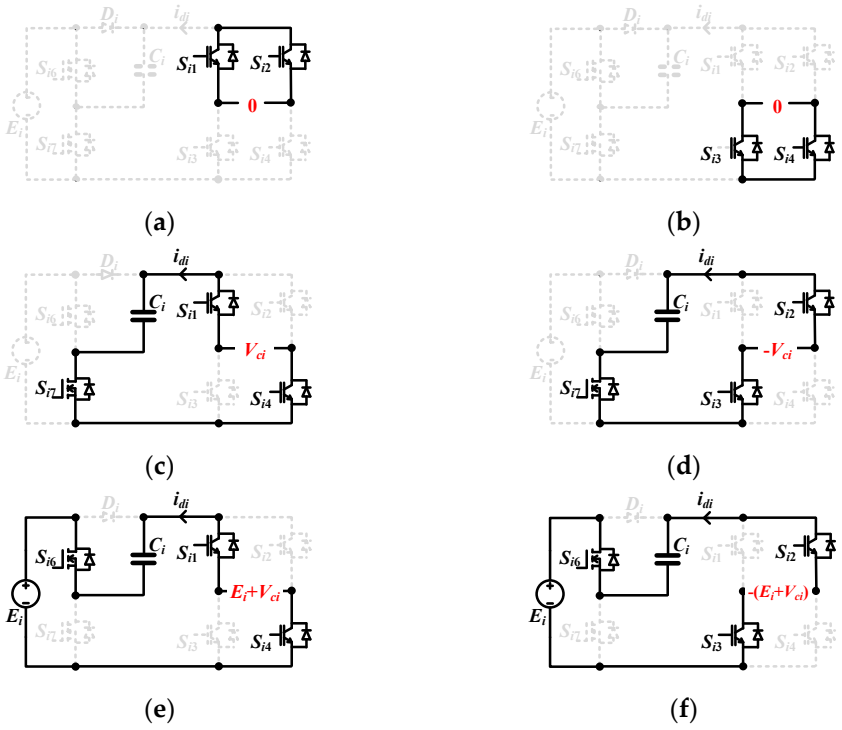


Figure 4. Switching modes of the inverter in [23] under inductive load. (**a**) Mode 1, (**b**) Mode 2, (**c**) Mode 3, (**d**) Mode 4, (**e**) Mode 5, (**f**) Mode 6.

3. Modulation Strategy

3.1. Hybrid Pulse Width Modulation

LS-PWM and PS-PWM are two of the most commonly used modulation strategies for a conventional multilevel inverter. As discussed above, five-level voltage is produced by each unit in the proposed cascaded multilevel inverter, which can be modulated using LS-PWM with four carriers. With LS-PWM, in addition, a high-quality output waveform of an inverter is achieved by charging and discharging the capacitor of SC cell alternatively in high frequency, the voltage of the capacitor is automatically balanced and the voltage ripple of the capacitor could be minimized. As for symmetrical cascaded units, PS-PWM is a good choice when using which power between cascaded units is automatically balanced. Therefore, by combining PS-PWM and LS-PWM, a hybrid pulse width modulation for a nine-level inverter is provided in Figure 5. With this hybrid modulation, power balancing between cascaded units and the capacitor voltage ripple minimization can both be achieved.

In Figure 5, e_s is the modulating signal with amplitude A_{ref}, and e_1~e_8 are carriers. The level-shifted carriers e_1 ~ e_4 have the same phase, which is compared with the modulating signal to generate switching control signals for the first cascaded unit. Similarly, the level-shifted carriers e_5~e_8, whose phase is opposite to e_1~e_4, are compared with the modulating signal for generating switching control signals for the second cascaded unit. It can be seen from Figure 5, five voltage levels of 0, $\pm E$ and $\pm 2E$ are produced for the output (u_{o1} and u_{o2}) in each unit, and a nine-level output voltage (u_o) of 0, $\pm E$, $\pm 2E$, $\pm 3E$ and $\pm 4E$ is obtained by cascading two units. It was noted that for each unit, when the output voltage is switching between $+E$ and $+2E$, the capacitor operates in charging and discharging mode alternately in high frequency. Therefore, the capacitor voltage can be balanced to dc input voltage automatically, and the voltage ripple of the capacitor can be minimized.

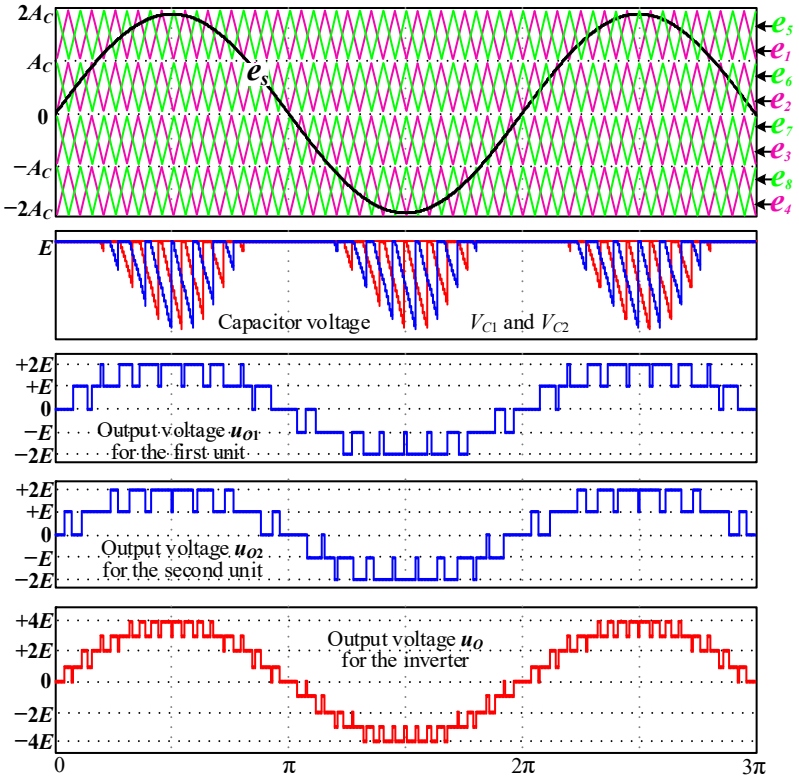


Figure 5. Modulation principle of hybrid PWM.

The modulation index is defined as

$$M = \frac{A_{ref}}{2A_c} \tag{1}$$

where A_c is the peak-to-peak amplitude of the carriers.

The operating status of each switch in the cascaded inverter is given in Table 2, where "↓" and "↑" represent capacitor discharging and charging, respectively.

Table 2. Operating status of each switch.

Status							Capacitor Status	Output Level
S_{i1}	S_{i2}	S_{i3}	S_{i4}	S_{i5}	S_{i6}	S_{i7}		
1	0	0	1	0	1	0	↓	$+2E$
1	0	0	1	1	0	1	↑	$+E$
1	1	0	0	1	0	1	↑	0
0	0	1	1	1	0	1	↑	0
0	1	1	0	1	0	1	↑	$-E$
0	1	1	0	0	1	0	↓	$-2E$

According to Table 2 and Figure 5, the modulation logic of switching control signals in the first cascaded unit can be summarized as follows. When $e_s > 0$, the control signal of S_{11} satisfies $v_{gs11} = 1$, which is complementary to control signal of S_{13}; when $0 < e_s < e_2$ or $e_s < e_3$, the control signal of S_{12} satisfies $v_{gs12} = 1$, which is complementary to control signal of S_{14}; when $e_4 < e_s < e_1$, the control signals of S_{15} and S_{17} satisfy $v_{gs15} = v_{gs17} = 1$, which is complementary to the control signal of S_{16}. Similarly, the modulation logic of switching control signals in the second cascaded unit is shown as follows: when $e_s > 0$, $v_{gs21} = 1$; when $0 < e_s < e_6$ or $e_s < e_7$, $v_{gs22} = 1$; when $e_8 < e_s < e_5$, $v_{gs25} = 1$. Thus, the logic modulating circuit of hybrid pulse width modulation is shown in Figure 6.

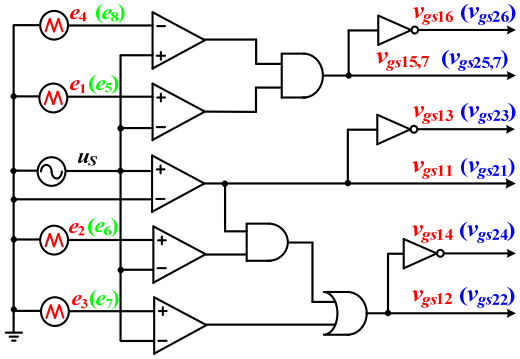


Figure 6. Modulating logic circuit of hybrid PWM.

The hybrid pulse width modulation strategy described above can be easily extended to a symmetrical cascaded multilevel inverter cascaded by n units. Switching control signals in each unit is still generated from the modulating circuit in Figure 6, and the phase shift between different carrier sets for cascaded units should be set to $(360/n)$ °.

3.2. Harmonic Analysis of Output Voltage

Assuming the capacitor voltage is equal to E, the Fourier transform of the inverter output voltage can be expressed as

$$\begin{aligned} u_o &= E[4M\cos(\omega_0 t)+ \\ &\textstyle\sum_{i=1}^{8}\sum_{m=1}^{+\infty}\sum_{n=-\infty}^{+\infty} A_{mni}\cos(n\omega_0 t + m\omega_c t + m\alpha_i)] \end{aligned} \tag{2}$$

where ω_0 and ω_c are the frequency of modulating signal and carriers, respectively. A_{mni} is the amplitude of harmonics caused by the i-th carrier centering at the frequency of $n\omega_0 + m\omega_c$, and α_i is the phase angle of the i-th carrier.

In addition, A_{mni} is equal to 0 when $m + n$ is an even number [25]. In the proposed hybrid pulse width modulation, the phase difference between two sets of carrier signals is 180°; thus, the harmonics generated from two cascaded units cancel each other when m is an odd number, and the harmonics only need to be considered when m is an even number.

3.3. Power Balance

As discussed above, in the hybrid pulse width modulation, a single modulating signal and two sets of carriers of opposite phases are utilized. From (2), the fundamental component of the output voltage is independent of the carrier; thus, the fundamental power in two cascaded units is equal.

Considering the harmonic component of the multilevel output voltage is low, the power dissipated by the harmonic current can be neglected. Therefore, the output power of each unit approaches, and power balancing is realized automatically.

4. Capacitor Voltage Ripples

With the hybrid pulse width modulation, the capacitor in the SC cell operates alternately in series and in parallel with the dc voltage source. The capacitor voltage is clamped to dc voltage E whenever it is connected in parallel with the source, so the voltage ripple of the capacitor is proportional to the integral of discharging current and is inversely proportional to its capacitance.

The integral of discharging current takes the maximum value when the modulating signal e_s reaches its peak A_{ref}. The discharging current and capacitor voltage are given in Figure 7 when a pure resistive load R is connected.

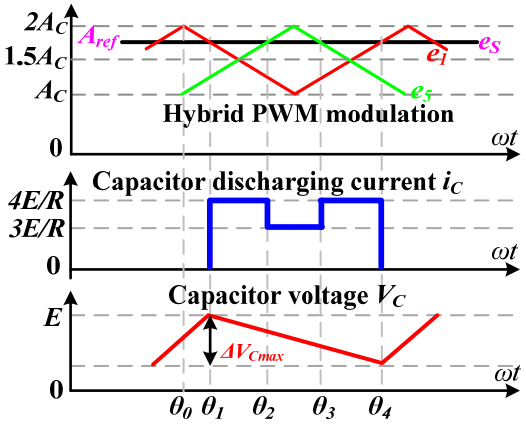


Figure 7. The maximum capacitor voltage ripple.

The maximum capacitor voltage ripple can be expressed as

$$\Delta V_{Cmax} = \frac{E}{RC}\left[\int_{\theta_1}^{\theta_2} 4d(\omega t) + \int_{\theta_2}^{\theta_3} 3d(\omega t) + \int_{\theta_3}^{\theta_4} 4d(\omega t)\right] \tag{3}$$

Based on a similar triangle theory, it can be further expressed as

$$\Delta V_{Cmax} = \frac{(5A_{ref}/A_C - 6)}{RCf_C} = \frac{(10M - 6)E}{RCf_C} \tag{4}$$

where f_C is the frequency of carriers e_1~e_8.

The capacitor satisfies

$$C > \frac{10M - 6}{\alpha R f_C} \tag{5}$$

where $\alpha = \Delta V_{Cmax}/E$ represents the allowable ripple voltage across the capacitors, and it is normally set around 10%.

5. Simulation Verification

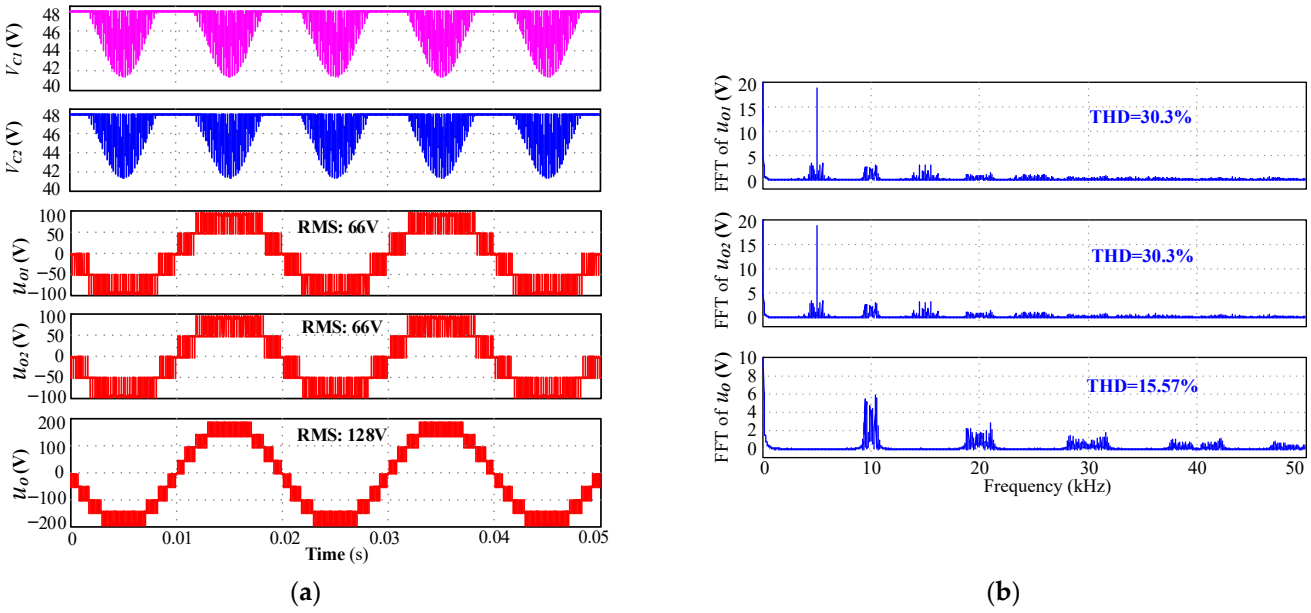
In order to verify the effectiveness of the proposed symmetrical switched-capacitor multilevel inverter and its hybrid pulse width modulation, a simulation model was built in PSIM. The simulation parameters are listed in Table 3.

Table 3. Parameters of the cascaded multilevel inverter.

Parameters	Simulation	Experiment
E	48 V	48 V
M	0.95	0.95
f_0/f_C	50 Hz/5 kHz	50 Hz/5 kHz
C_1, C_2	100 μF	100 μF
S_{15}~$_{17}$, S_{25}~$_{27}$	Ideal switch	IRFI4410Z
S_{11}~$_{14}$, S_{21}~$_{24}$	Ideal switch	IRF640
Load	50 Ω/50 Ω-50 mH/10 Ω-50 mH	50 Ω/50 Ω-53 mH

Figure 8 shows the simulation results under the 50 Ω load condition. As shown in Figure 8a, a five-level output voltage is produced by each unit, and a nine-level output voltage is generated by cascading two units. Since the RMS value of output voltage in each unit is measured the same as 66 V, it can be deduced that the power of each cascaded unit is equal, and the power between two cascaded units is automatically balanced. Moreover, the capacitor voltage is balanced to the dc input voltage by using hybrid PWM. From the FFT analysis result in Figure 8b, the voltage harmonics of each unit are distributed near the

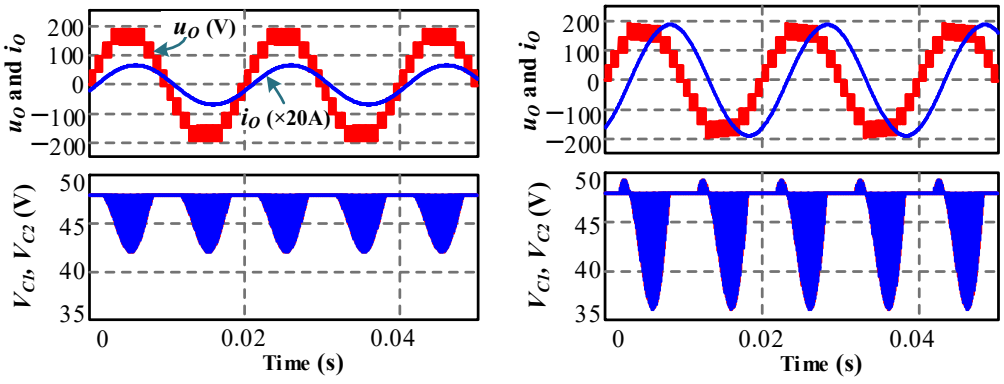
carrier frequency (5 kHz) and its multiples (10 kHz, 15 kHz, . . .), while the harmonics of the total output voltage are located near even multiples of the carrier frequency (10 kHz, 20 kHz, . . .), showing that the equivalent switching frequency after cascading is increased to twice the carrier frequency.



(**a**) (**b**)

Figure 8. Simulation waveforms for a resistive load: (**a**) Output voltage and capacitor voltage ripple; (**b**) FFT analysis result of output voltage.

Figure 9 shows the simulation waveforms under inductive load. It can be seen that the capacitor keeps the voltage around the dc input voltage due to the clamping of S_{i5}, and the inverter works properly even when the reactive power demand is large. For comparison, the cascaded inverter using a diode in the SC cell [23] is also simulated, and the simulation results are shown in Figure 10. It can be seen that the capacitor voltage is far beyond the dc input voltage because the diode prevents the current flow, and the reversing current keeps charging the capacitor in the SC cell. The output voltage waveform is heavily distorted, as shown in Figure 10b, and the overvoltage of capacitors might cause some safety issues. Thus, the optimized topology in this paper, by simplifying replacing the diode with MOSFET, improves not only the performance of the inverter under inductive load but also the system's reliability.



(**a**) (**b**)

Figure 9. Simulation waveforms for the optimized inverter with inductive loads: (**a**) 50 Ω-50 mH; (**b**) 10 Ω-50 mH.

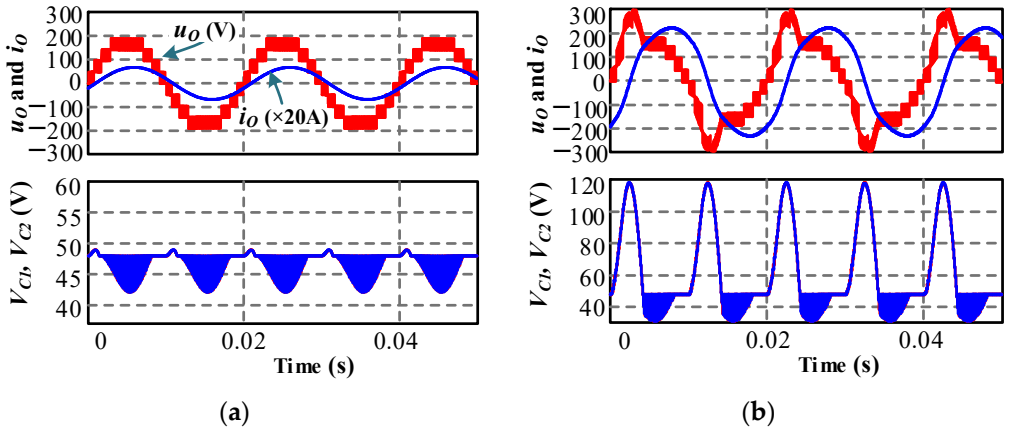


Figure 10. Simulation waveforms for the original inverter with inductive loads: (**a**) 50 Ω-50 mH; (**b**) 10 Ω-50 mH.

In order to compare the reactive power capability of the proposed circuit and the inverter in [23], the capacitor voltage ripple with different inductive loads is depicted in Figure 11. Assuming that the limitation of capacitor voltage ripple is 15% E_i, i.e., ΔV_{Cmax} = 7.2 V, with the inverter in [23], the ripple will reach the limitation when the inductance increases to 120 mH and the power factor of the inverter is about 0.798. With the proposed circuit in this paper, as shown in Figure 11, the voltage ripple will never exceed the limitation even with a large inductance.

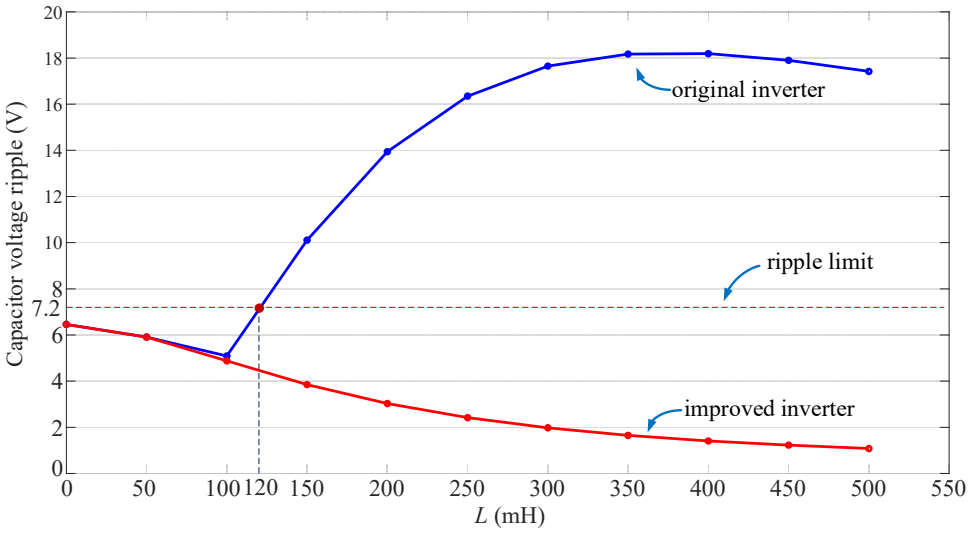


Figure 11. Capacitor voltage ripple versus load inductance (R = 50 Ω).

Compared to the power factor of [0.798,1] in [23], the power factor is extended to [0,1] for our proposed circuit, which has demonstrated an enhanced reactive power capability.

On the other side, the proposed circuit has a smaller voltage ripple on the capacitor under the same inductive load, which means that the capacitance required can be reduced. Therefore, an electrolytic capacitor could be replaced by a film capacitor featuring a long lifetime and high reliability.

6. Experimental Verification

A prototype is also built. The parameters are listed in Table 3, and the experiment bench is shown in Figure 12. In the experiment, the hybrid modulation strategy illustrated in Figure 3; Figure 4 is realized using a DSP microcontroller. The generated control signals are sent to power switches through the optocoupler.

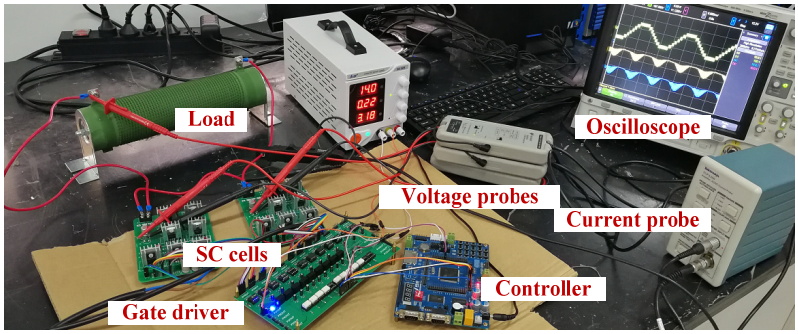


Figure 12. Experiment bench.

Figure 13 shows the experimental waveforms for a resistive load. The proposed switched-capacitor multilevel inverter cascaded by two units can generate a nine-level output voltage with a step voltage of 48 V. The RMS value of output voltage is measured as 125.84 V, which is close to the simulation value (126 V). By using hybrid PWM modulation, the capacitors are charged and discharged alternately, obtaining a high-quality output voltage waveform with a small capacitor (100 μF). In addition, the voltage of each capacitor is automatically balanced, and their voltage ripple is almost the same, which means that the transferred power in cascaded units is balanced automatically.

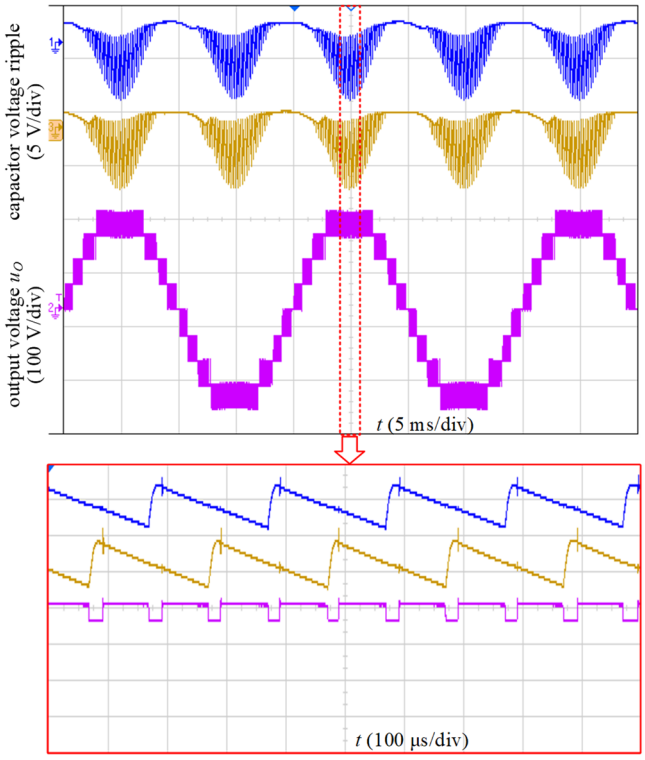


Figure 13. Experimental waveforms for a resistive load.

Figure 14 shows the experimental waveforms for an inductive load. In Figure 14a, the waveforms of capacitor voltage, output voltage and output current are shown. It shows that the capacitor voltage balancing and power balancing between cascaded units are realized. The FFT analysis of output voltage is shown in Figure 14b. It is shown that the harmonics are mainly distributed around even multiples of the carrier frequency, i.e., 10 kHz, 20 kHz and 30 kHz, which coincides with theoretical analysis and simulation results. The FFT analysis of output current is shown in Figure 14c, which indicates that the output current is a pure sine wave without containing any harmonics.

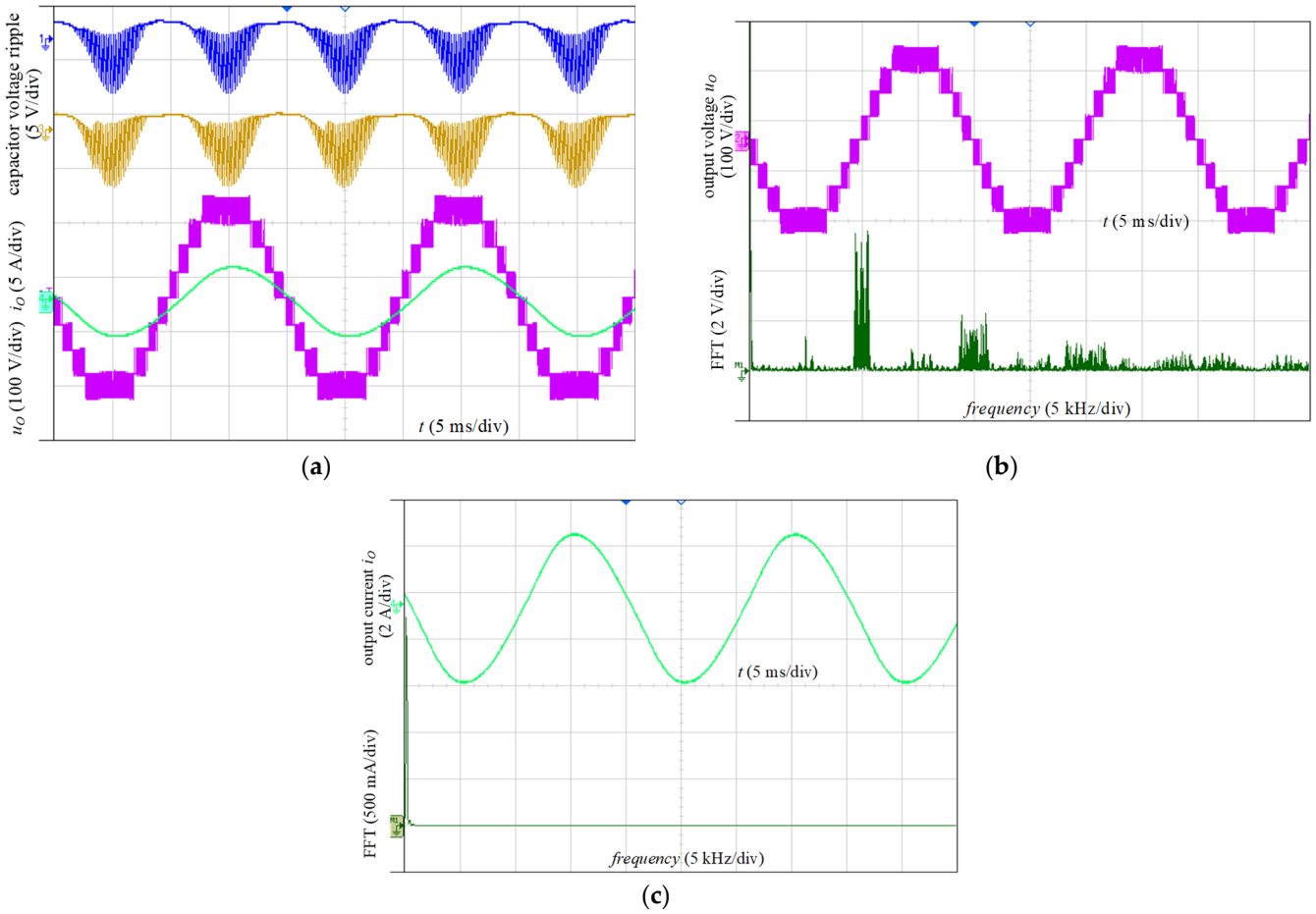


Figure 14. Experimental waveforms for an inductive load: (**a**) Waveforms of output voltage, output current, and capacitor voltage; (**b**) FFT analysis of output voltage; (**c**) FFT analysis of output current.

The relationship between the system efficiency and output power is achieved in Figure 15 by adjusting the value of the resistive load. The results show that the efficiency of the inverter is larger than 92% when the power ranges from 24 W to 222 W. Especially, the efficiency is larger than 97% when the output power is larger than 50 W. It is obvious that the inverter has a high efficiency over a wide load range.

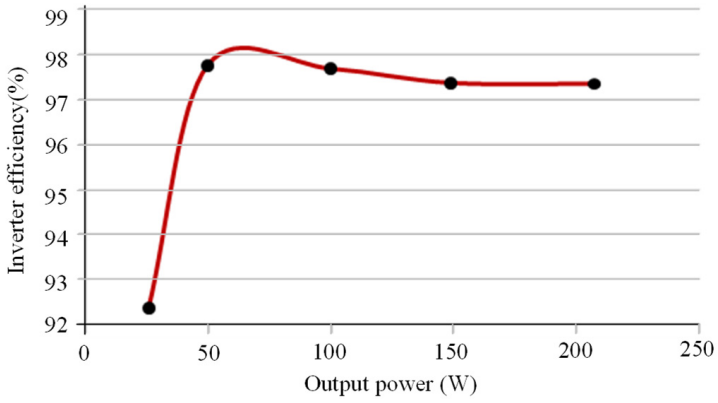


Figure 15. Efficiency versus output power.

7. Conclusions

In this paper, an optimized symmetrical switched-capacitor multilevel inverter was proposed, and a hybrid pulse width modulation strategy combining LS-PWM and PS-PWM was applied. The theoretical analysis, simulation results and experimental results are provided. Compared to the inverter in [23], the proposed multilevel inverter has the following advantages:

(1) With LS-PWM, a five-level output voltage is produced for each cascaded unit, and the capacitor voltage can be balanced to the dc input voltage automatically. The capacitor keeps charging and discharging alternately in high frequency so that only a small capacitor is needed to minimize the capacitor voltage ripple;
(2) With PS-PWM, power balancing between cascaded units is realized automatically. The equivalent switching frequency of the cascaded inverter is increased to twice the carrier frequency; therefore, the harmonics of the output voltage is located near even multiples of the carrier frequency;
(3) It has superior reactive power capability and reliability.

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