*energies*

MDPI

*Article*

# Non-Linear Switching Circuit for Active Voltage Rectification and Ripples Reduction of Piezoelectric Energy Harvesters

**Mahesh Edla [1,*], Yee Yan Lim [1], Deguchi Mikio [2] and Ricardo Vasquez Padilla [1]**

[1] Faculty of Science and Engineering, Southern Cross University, East Lismore, NSW 2480, Australia; limy0018@gmail.com (Y.Y.L.); ricardo.vasquezpadilla@fmgl.com.au (R.V.P.)
[2] Department of Electronics and Control Engineering, National Institute of Technology, Niihama College, Niihama 790-8570, Japan; deguchi@ect.niihama-nct.ac.jp
* Correspondence: mahesh.edla@scu.edu.au or maheshedla26@gmail.com

**Abstract:** This paper describes an improved non-linear switching circuit (INLSC) for active rectification of voltage and reduction of ripples in the voltage waveform for the piezoelectric energy harvesting (PEH) system. The proposed converter controls the alternating current (AC) generated by the piezoelectric device (PD) under mechanical vibration. The proposed circuit combines the boost and buck-boost processes through a switching process, which functions in both positive and negative cycles. In addition, it controls the voltage and frequency of the load capacitor. In this process, the passive components in the circuit are energised by being short with the AC voltage using switching signals, which facilitates the active rectification of ultra-low AC voltage. Design considerations, theoretical analysis, simulations and experimental results are presented. It was shown that the circuit was able to control the switching signal and to convert low AC voltage (0.44 $V_i$) to high direct current (DC) voltage (6.5 $V_{dc}$) while achieving an output power of 469 µW which outperforms the existing similar circuits and synchronous rectifier circuit. The ripples in the rectified voltage were also comparatively less. Application-wise, the proposed circuit could power a manually connected 7-segments display, commonly used for traffic applications.

**Keywords:** AC-DC conversion; boost; buck-boost; switching circuit; 7-segment display; piezoelectric devices; rectifier-less circuit; synchronous rectifier circuit



**Citation:** Edla, M.; Lim, Y.Y.; Mikio, D.; Padilla, R.V. Non-Linear Switching Circuit for Active Voltage Rectification and Ripples Reduction of Piezoelectric Energy Harvesters. *Energies* **2022**, *15*, 709. https://doi.org/10.3390/en15030709

Academic Editor: Joachim Vollbrecht

Received: 2 November 2021
Accepted: 14 January 2022
Published: 19 January 2022



## 1. Introduction

Power electronic circuits play a significant role in the piezoelectric energy harvesting (PEH) system by acting as a mediator to convert the AC voltage, which is generated by PD from mechanical energy (ME) [1–3] into direct current (DC) voltage. In practice, the PD generates limited power due to its high internal impedance and erratic waveform due to random vibrations from nature. Therefore, the efficiency of electronic circuits is essential to minimise losses during the conversion process. The converted DC voltage can be used in various applications, namely charging of storage devices [4], powering of wireless sensor nodes for structural health monitoring and powering small scale devices for military and medical use [5].

Numerous AC-DC rectification circuits for PEH systems have been developed and reported in the literature [6–18]. The simplest one is a conventional full-bridge rectifier (FBR) circuit. Despite their simplicity and popularity, this rectifier circuit suffers from several limitations: (1) It comprises of diodes, which results in unavoidable voltage drop across them; (2) it does not step up the voltage of PD, which limits its application as most of the electronic devices require 2–3 $V_{dc}$; (3) the presence of ripple voltage ($V_r$) in the converted voltage waveform. Therefore, it is arduous to design a power electronic circuit suitable for converting and boosting the low voltage generated by PD, as well as to reduce the ripples in converted voltage waveform. Various enticed circuits/methods have also

been proposed in the literature, namely single-stage, dual-stage, and non-linear circuits. The key difference between the single and the dual-stage circuits is that a single-stage circuit includes AC-DC conversion, while the dual-stage includes AC-DC and DC-DC conversion stages. A flow chart illustrating the process of single and dual-stage circuits for the PEH system is depicted within the context of Figure 1a,b.

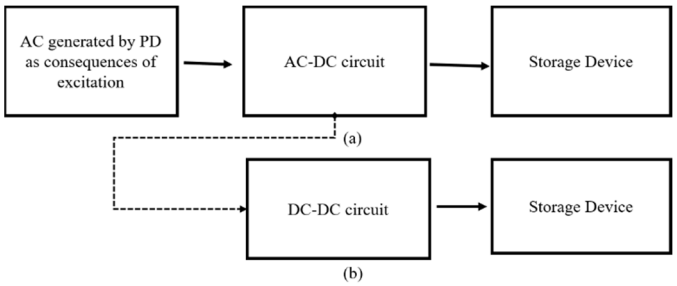


**Figure 1.** A summary of PEH process (**a**) Single-stage, (**b**) Dual-stage.

A recent study on a single-stage rectifier circuit by the authors [4,19] improved MOSFET bridge rectifier circuit into a self-powered H-Bridge circuit. The proposed circuit was proven applicable with ultra-low voltage and high-frequency excitation. The outcome showed that the proposed circuit notably increased the output voltage and power produced from the PD in comparison with FBR circuits. The ripples in rectified voltage waveform were also lower, in comparison with the conventional rectifier circuit. However, the output voltage was low, which was insufficient for powering any electronic devices.

A dual-stage rectifier circuit was proposed by [20], where a controller varied the switching frequency (fs) of the step-down converter circuit to maximise the output power flowing into the battery. However, due to its switching frequency, the switching losses were higher than the output power. Another possible way of converting low voltage into regulated DC is by using a dual-stage converter [21]. This circuit achieved maximum power flowing into the storage by controlling the ripples of the output. However, the proposed dual-stage circuit was very complex and costly.

Another approach, namely an energy-harvester circuit with a clock booster for PEH, was proposed by [22] to minimise the voltage drop in the rectification process. The proposed circuit, also known as the second stage converter, included a clock booster to maximise the pulses' amplitude and turn the buck-boost converter quickly. It was constructed in CMOS and tested through simulation. The output voltage was nearly 0.8 $V_{dc}$ at a frequency of 100 kHz with an input voltage of 1.6 $V_{ac}$. Despite the use of additional components in the circuit, the rectified voltage was limited and unstable. Synchronous rectification is another well-known power extraction method for PEH. One of its main advantages is that the power generated by PD is independent of the connected load. However, recent literature [10,23–25] mainly focused on synchronous power rectification using the non-linear technique. Active rectification is not possible because the PD delivers low output power in most cases.

To address the abovementioned shortcomings (i.e., voltage drop, low voltage and ripple voltage) of the FBR circuit (i.e., linear circuit), a non-linear approach is proposed in this study.

This paper mainly focuses on the improvement of active rectifiers; however, the proposed circuit does not involve auxiliary interfaces. The main novelty of the proposed circuit and similar circuits (i.e., similar to INLSC) [22,26–30], is that the proposed circuit also efficiently works with the duty cycle of 50%, input voltage of 0.44 $V_i$, and achieves maximum output power, which is not possible by the abovementioned literature circuits in comparison with INLSC circuit. In addition, the proposed INLSC circuit requires only one PD, whereas other literature circuits adopted a few PD's, which results in additional costs. Besides, the applicability of similar circuits is not shown in the literature. Therefore, as a primary rule, an active and non-linear rectifier circuit is desired to achieve a high

rectified voltage (HRV) and high output power (HOP) with only 50% of the duty cycle. However, the balance between HRV and HOP has not been adequately addressed in the literature. Therefore, this study proposes a non-linear circuit, aiming to achieve optimal rectified voltage and high output power with active rectification. To verify the applicability, INLSC was also tested briefly with a 7-segment display.

The motivation of this proposed study is to utilise the benefits of the conventional boost converter [31], buck-boost converter [32], and synchronous rectifier circuits [23,33,34]. As a result, the proposed circuit is expected to reduce the voltage drop in the rectification process, boost the input voltage, and minimise the ripples in the output voltage waveform. The proposed circuit, namely an improved rectifier-less switching circuit, INLSC, consists of both boost and buck-boost operations controlled by a switching process using bidirectional switches. This circuit employs a polarity detector and an inductor that enables low voltage operation with less complexity. Besides, it uses only one capacitor to reduce complexity and cost.

To validate the performance of the proposed INLSC, a series of experimental tests and numerical simulations were carried out in this study. A real-life application, which is not attempted in the literature, is also presented in the proposed study.

## 2. Power Extracting Circuits for PEH

This section asserts the basics of the PEH system, including internal circuit modelling of PD and commonly used conventional circuits in the rectification process. Subsequently, the proposed INLSC is outlined.

### *2.1. Optimal Power Flow of PD*

A vibrating PD is modelled as an AC current source, $i_i$ (t) or a voltage source, $V_i$ (t) in parallel or in series with its internal capacitance, $C_P$, respectively, to ascertain its power flow characteristics depicted within the context of Figure 2. The generated voltage or current fluctuates with the mechanical vibrations; however, it is assumed to be constant regardless of external loading [9].

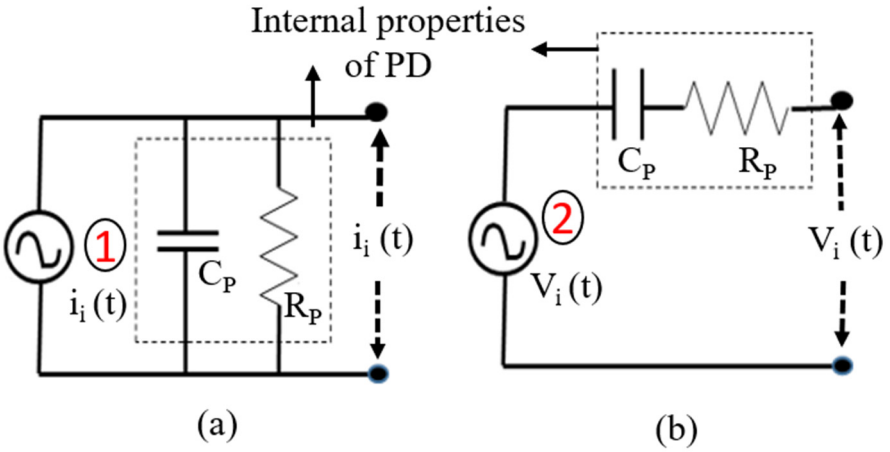


**Figure 2.** A vibrating PD circuit model (**a**) Current source and (**b**) Voltage source.

### *2.2. Conventional FBR Circuit*

The simplest rectifier circuit to convert AC to DC is the FBR circuit. The operation of the FBR circuit and its corresponding output waveforms are outlined in Figure 3.

From Figure 3, it can be observed that the current produced by PD needs to first charge its internal capacitor, $C_P$. During this period, the PD voltage is less than the sum of rectified voltage and forward voltage (i.e., PD voltage $\leq V_{dc} + 2\,V_d$), where $V_d$ is the voltage drop across diodes. Thus, the FBR is blocked, and the load capacitor, $C_L$ does not charge. Such process occurs in both positive and negative half cycles. Intervals 1 and 3 are known as non-harvesting periods (i.e., PD is charging its internal capacitor). When the magnitude

of the PD voltage matches the rectified voltage (i.e., PD voltage $\geq V_{dc} + 2\,V_d$), the FBR is in conduction state. The load capacitor is now charged. Intervals 2 and 4 are known as harvesting periods [4,19,35].

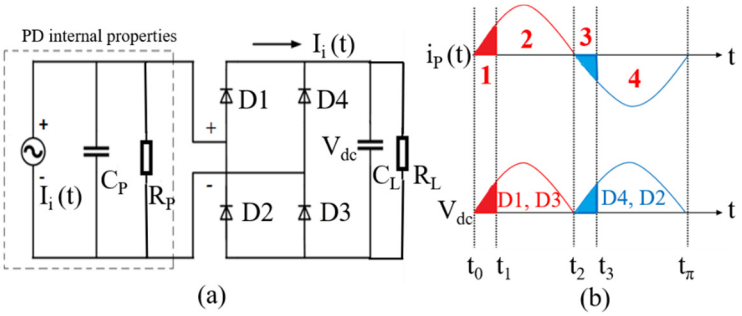


**Figure 3.** AC-DC rectification using FBR circuit (**a**) PD and FBR circuit, (**b**) Output waveforms.

The PD voltage ($V_i$) and the DC voltage ($V_{dc}$) rectified by FBR circuit are illustrated in Figure 4a,b, respectively. From Figure 4b, it can be noticed that, in the positive half cycle, the PD voltage charges the load capacitor from $V_2$ to $V_m$. Then, at $t = \pi/2$, the load capacitor discharges through the load resistor $R_L$, and the ripple voltage is depicted in Figure 4c. Besides, the currents through the load capacitor, $C_L$ and resistor, $R_L$, denoted as $i_{CL}$ and $i_{RL}$, respectively, are shown in Figure 4d,e.

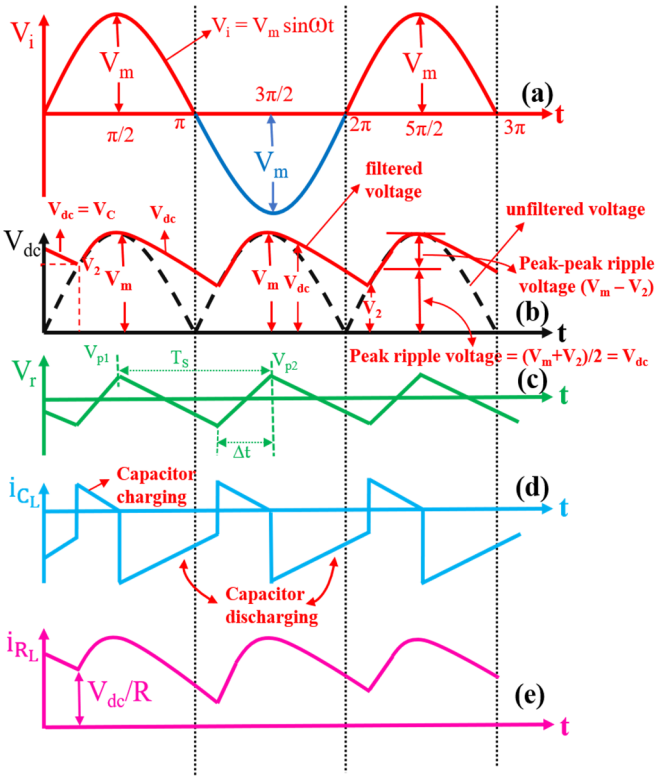


**Figure 4.** Various output waveforms of an FBR circuit (neglected $C_P$): (**a**) PD voltage, $V_i$, (**b**) Rectified voltage, $V_{dc}$, (**c**) Ripple voltage, $V_r$, (**d**) Current through load capacitor, $i_{CL}$ and, (**e**) Current through resistor, $i_{RL}$.

The description of a negative half cycle is herein omitted, as it is similar to the positive half cycle. It can be seen from Figure 4 that the maximum voltage drop occurs between $V_m$

to $V_2$ (i.e., $V_m - V_2$). From Figures 2 and 4, the PD voltage applied to the proposed circuit can be expressed as follows [36]:

$$V_i\,(t) = V_m\,\sin\left(\frac{2\,\pi\,t}{T_{in}}\right) \tag{1}$$

where $T_{in}$ is the period of vibration of PD and $V_m$ is the magnitude of the AC.

Referring to Figure 4c, considering one cycle of charging and discharging time of FBR as $T_s$, and the charging time as $\Delta t$, the discharging time period can be written as:

$$T_s - \Delta t \tag{2}$$

Considering the load capacitor, $C_L$ is charged and discharged through load resistor, $R_L$, the voltage of the capacitor can be expressed as:

$$V_{dc}\,(t) = V_{dc}\,e^{\left(\frac{-t}{R_L C_L}\right)} \tag{3}$$

The maximum value of the ripple voltage, $V_{P1}$ and the minimum value of the peak ripple voltage, $V_{P2}$, can then be derived:

$$V_{P1} = V_m \tag{4}$$

$$V_{P1} = V_{dc} = V_m\,e^{\left[\frac{-(T_S - \Delta t)}{R_L C_L}\right]} \tag{5}$$

Assuming that $\Delta t \ll T_s$:

$$V_{P1} = V_{dc} = V_m\,e^{\left[\frac{-(T_S)}{R_L C_L}\right]} \tag{6}$$

1st assumption:

$$V_m\left[1 + \left(1 + \left(\frac{-T_S}{R_L C_L}\right)^1 . \frac{1}{1!} + \left(\frac{-T_S}{R_L C_L}\right)^2 . \frac{1}{2!} + \left(\frac{-T_S}{R_L C_L}\right)^3 . \frac{1}{3!}\right)\right] \tag{7}$$

Assuming that $T_s \ll R_L\,C_L$:

$$V_{P2} = V_m\left[1 - \left(\frac{T_S}{R_L C_L}\right)\right] \tag{8}$$

In addition, the ripple voltage (Figure 4c) can be written as:

$$V_{ripple} = (\text{max peak} - \text{min peak}) \tag{9}$$

$$= (V_{P1} - V_{P2}) \tag{10}$$

Substituting Equations (6) and (8) into Equation (10), the ripple voltage of the FBR circuit can be written as:

$$V_{ripple} = V_m\left[\frac{T_s}{R_L C_L}\right] \tag{11}$$

$$\text{Considering } T_S = \frac{1}{f_s\,(\text{frequency})'} \tag{12}$$

$$V_{ripple} = V_m\,\frac{1}{2\,f_s R_L C_L} \tag{13}$$

From Figure 4, it can be observed that the rectified voltage differs from the expected DC voltage. This issue (i.e., ripple voltage) is also taken into consideration in this study. A switching control circuit that includes boost and buck-boost modes is proposed to overcome these issues, namely forward voltage, boosting voltage, and ripple reduction.

### *2.3. Proposed Circuit's Benifits*

For ease of switching operation, bidirectional switches are used, which consist of four N-MOSFETs. These switches work in both positive and negative half cycles simultaneously. In addition, one inductor and one capacitor are included in the circuit. The main benefits of the proposed switching circuit are:

- Low input voltage for activation;
- Smaller size and lower cost;
- Able to boost low voltage into high voltage;
- Able to reduce ripples in the output waveform;
- It utilises the internal body diode of the transistors to reduce the forward voltage, which reduces the cost.

Further explanation of the circuit is delineated in the following sections.

## 3. Operation Principle

The proposed INLSC and its operation are depicted in Figure 5. An input AC voltage of 0.44 $V_i$ at a frequency of 100 Hz is utilised to rectify the output of the PD. In order to convert AC into DC, the switches must be able to conduct and to block the currents in both cycles during ON and OFF conditions.

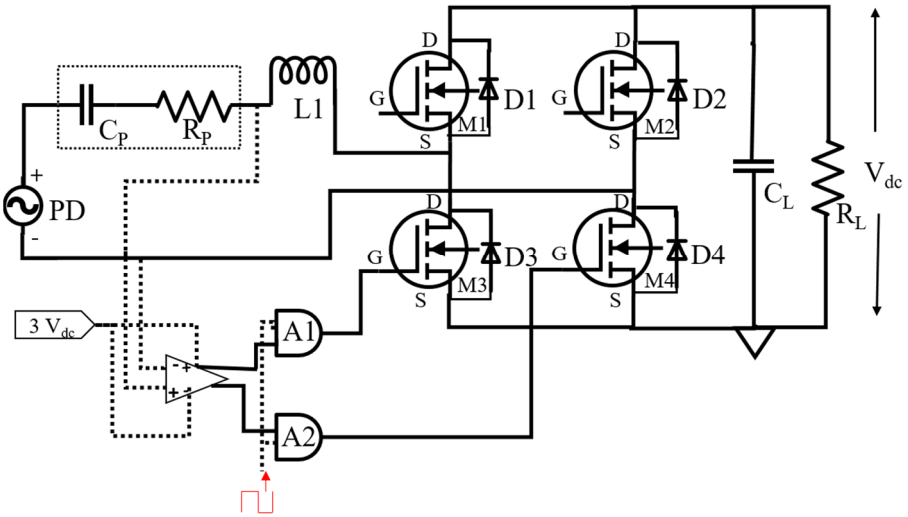


**Figure 5.** Schematic of the proposed INLSC (M1–M4: MOSFET switches, G: Gate, D: Drain, S: Source, A1, A2: Logic gates).

Therefore, four MOSFET (bidirectional) switches were adopted and connected. Note that, in both positive and negative half cycles, switches M3 and M4 were only in ON state, while M1 and M2 are in OFF state, which prevents the circuit from reverse recovery loss. In other words, the voltage stored in the load capacitor could not flow back to the PD, and this process is known as return phenomenon, which is a significant research gap in the SSHI method [33,37]. Therefore, these M1, M2 switches are always in OFF state.

In this study, a polarity detector is employed to detect the polarities of PD. Therefore, the switches M3 and M4 are always synchronised with the PD voltage. When the polarity detector detected the polarity, the resultant signal was sent to the logic AND gates, A1 and A2. Besides, the gates were also powered by PWM (pulse with modulation) of the controller [2].

Thus, the output signal of the polarity detector and the pulse signal was compared. The resultant signals from both AND gates (A1 and A2) are sent to switch M3 and M4, respectively. The switch, M3 conducts in positive half cycle, while the switch, M4 works in negative half cycle. In the positive half-cycle of the PD voltage, it operates as a boost converter while in the negative half cycle, it works as a buck-boost converter. This type

of discontinuous mode (DCM) circuit has the advantage of limiting the switching losses. Besides, it reduces the reverse recovery loss of the diode.

In this operation, the proposed circuit possesses four main operating modes in each half cycle. Modes 1–4 and Modes 5–8, corresponding to the positive half cycle and the negative half cycle, respectively. Each mode is described below:

**Mode 1:** In the beginning, the PD charges its internal capacitor, $C_P$ while the proposed INLSC is in OFF state.

**Mode 2:** During $t_0$, the switch, M3 is in ON state, and the PD voltage feeds the inductor, L1. The current flow path in this mode is PD–L1–M3–D4–PD. Thus, the inductor is energised. However, since the inductor does not allow a sudden change in current, the current linearly increases from zero to its peak value. At this instant, the load capacitor powered the load resistor, $R_L$.

**Mode 3:** During this time, the switch, M3 is in OFF state. The energised inductor in Mode 2, freewheels via D1, which is an internal body of M1. As stated above, the inductor does not discharge instantly as well; it discharges linearly and charges the load capacitor, $C_L$. However, the capacitor also energises linearly since it does not allow a sudden change in voltage. Therefore, it charges from zero to its peak value.

**Mode 4:** When the inductor current reaches zero through the internal body diode, D1 of M1, the internal body diode turned OFF automatically. This mode effectively eliminates the reverse recovery loss of the diode since in practice, a diode is not physically presence. Besides, switch M1 is in OFF state.

**Mode 5:** Modes 4–8 occur in the negative half cycle of PD. This mode is similar to Mode 1, but it works in the negative half cycle of the PD and charges its internal capacitor.

**Mode 6:** During this time, the switch, M4 is in ON state, while the other switches are in OFF state and the PD feeds the inductor, L1. The current flow path in this mode is PD–M4–D3–L1–PD. Thus, the inductor is energised from zero to its peak value. At this instant, the load capacitor powered the load resistor, $R_L$.

**Mode 7:** During this time, the switch, M4 is in OFF state. The energised inductor in Mode 6, freewheels via D2, which is an internal body of M2. As stated above, the inductor discharges and charges the load capacitor linearly. Therefore, the load capacitor charges from zero to its peak value.

**Mode 8:** When the inductor current discharges to zero, the internal body diode, D2 of M1 is turned OFF automatically. This mode eliminates the reverse recovery loss of the diode since there is no presence of a diode in practice. Besides, the switch M2 is in OFF state.

Considering the operating modes, both M1 and M2 are in OFF state in both positive and negative half cycles while the other two switches, M3 and M4, are in ON and OFF states simultaneously.

## 4. Theoretical Analysis and Design

To increase the extracted output power from PD and reduce the ripples in the output waveform, two key aspects were considered in the design of the circuit, namely the impedance matching and the switching process. It is worth noticing that the impedance of the proposed converter circuit can be varied by adjusting the duty cycle. Considering the primary focus of this study is on the basic topology of circuit and its verification, sinusoidal AC voltage was taken as input voltage to simplify the process of analysis. The proposed circuit enjoyed the benefits of lower cost and complexity, as only one inductor and one capacitor were used. Unlike most previously proposed circuits, no diode was used to transfer the energy from inductor to load capacitor. For the purpose of analysis, a few assumptions were made for the switching process:

- The output load capacitor must be large enough to keep the rectified voltage stable.
- The switching frequency, $f_s$ should be higher than the external vibration frequency applied to the PD to minimise the ripples. Besides, due to high $f_s$, the vibration frequency of PD is assumed constant across each switching period [31,36]. Subsequently,

the PD voltage can also be considered as a constant voltage source, as expressed in Equation (1).

- For ease of calculations, internal properties of passive components in the circuit are not taken into consideration.

In addition, the power semiconductor components used in the proposed circuit turns ON with the zero current switching (ZCS) method. Due to this reason, most of the switching losses could be eliminated. The switching signals applied to the switches, namely M3 and M4, are shown in Figure 6. The proposed circuit integrated the boost and buck-boost operations in the positive and negative half cycles, respectively by applying the abovementioned switching signals to M3 and M4. The operation loops of the circuit in the positive half cycle are outlined below and plotted in Figure 7.

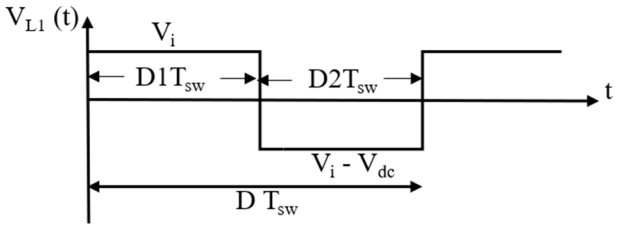


**Figure 6.** Switching signals applied to gate terminals, M3 and M4.

where D1 and D2 are the duty cycle of ON and OFF periods, respectively, and $T_{sw}$ is the switching frequency of the duty cycle. $V_{L1}$ is the voltage across the inductor.

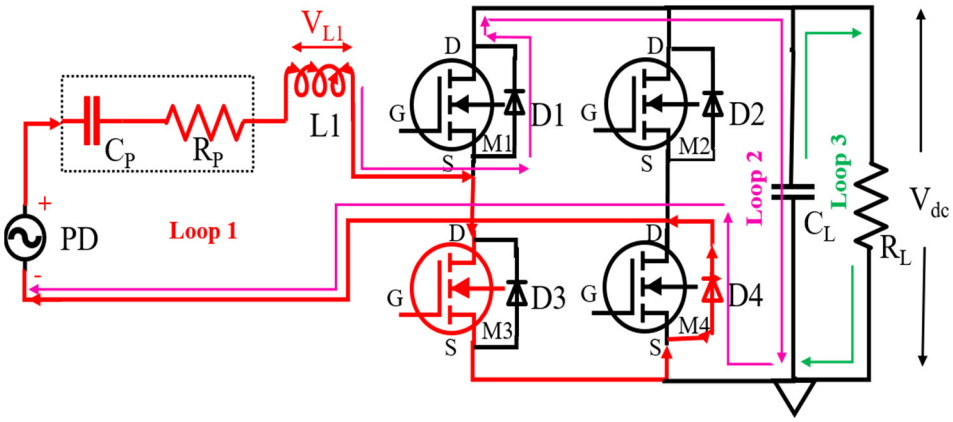


**Figure 7.** The operation loops in the positive half cycle.

**Loop 1:** Loop 1 occurs in Mode 2. During this time, the PD voltage charges the inductor, L1 and the circuit is shorted. Therefore, the voltage across the inductor, $V_{L1}$ is equal to the PD voltage, $V_i$, and it can be expressed as:

$$V_{L1} = V_i \tag{14}$$

At this instant, the load capacitor is powering the load resistor. Thus, the voltages across the load capacitor and resistor are the same, and the current flow through $C_L$ can be expressed as:

$$i_{C_L} = \frac{-V_{dc}}{R_L} \tag{15}$$

**Loop 2:** Loop 2 takes place in Mode 3. At this time, the load capacitor is powered by the peak inductor current, $i_{pk}$, which was initially charged in Mode 2. The voltage across the inductor can be expressed as:

$$V_{L1} = V_i - V_{dc} \tag{16}$$

Furthermore, the current through $C_L$ is expressed as:

$$i_{C_L} = i_{L1} - V_{dc}/R_L \tag{17}$$

**Loop 3:** Loop 3 occurs in Mode 4. When all the switches are in OFF condition, no PD voltage and current are flowing through the circuit. At this time, the PD voltage and current across the inductor can be expressed as:

$$V_{L1} = 0, i_i\,(t) \tag{18}$$

Furthermore, the current through the load capacitor can be written as:

$$i_{C_L} = \frac{-V_{dc}}{R_L} \tag{19}$$

The output waveforms of the proposed INLSC in switching process, when the switches are in ON, OFF state, are shown in Figure 8. The inductor slope during the time interval from $t_0$ to $t_1$ can be expressed as:

$$\frac{di_{L1}\,(t)}{dt} = \frac{V_{L1}\,(t)}{L1} = \frac{V_i}{L1} \tag{20}$$

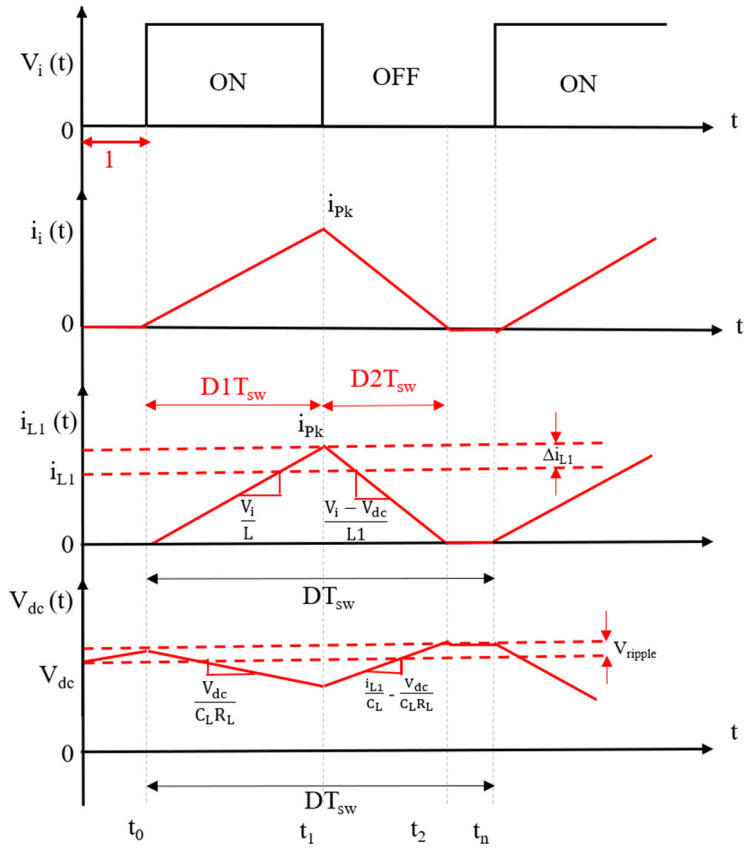


**Figure 8.** Waveforms of the proposed circuit when switching signals are applied in positive half cycles.

Similarly, the current slope of inductor, L1 can be written as:

$$\frac{di_{L1}\,(t)}{dt} = \frac{V_{L1}\,(t)}{L1} = \frac{V_i}{L1} \tag{21}$$

From Equations (20) and (21), the peak ripple current of inductor, $\Delta i_{L1}$ is solved:

$$\Delta i_{L1} = \frac{V_i}{2L1} DT_{sw} \quad (22)$$

Similarly, slope of the load capacitor in time intervals of $t_0$ to $t_1$, and $t_1$ to $t_2$ are shown in Figure 8. Note that the energy stored in an inductor by the PD and voltage stored in the load capacitor by the inductor must be the same. From the capacitor slope equations, the ripple voltage can be written as follows:

$$\Delta V_{dc} = \frac{V_i}{2C_L R_L} DT_{sw} \quad (23)$$

However, to verify the performance of the electronic circuit, it is necessary to calculate the voltage gain and power. Therefore, in this study, the peak value of input current is only calculated in the boost mode. A similar trend was observed in other modes, and it can be represented as follows [36]:

$$i_{Pk}\,(t) = D1\ T_{sw}\ V_i/L1 \quad (24)$$

As per inductor volts-second balance, net volt-seconds added to inductor during one switching period is:

$$V_i\ D1T_{sw} = (V_{dc}/2 - V_i)\ D2T_{sw} \quad (25)$$

$$D2Tsw = \frac{V_i\ D1\ Tsw}{\left(\frac{V_{dc}}{2} - V_i\right)} \quad (26)$$

From the above, in each switching time, the average input power, $P_{in}$ can be derived:

$$P_{in} = V_i\ i_{Pk}\ (D1 + D2)/2 \quad (27)$$

The boost ratio was designed based on a specific application, and the power output from the circuit was based on $R_L$, which was connected in parallel to the proposed circuit. To meet the requirement of the application, the inductor, the duty cycles, and the switching frequency must be designed accordingly. The larger is the switching frequency, the smaller is the inductance.

Therefore, to reduce the cost, complexity and weight of the proposed circuit, a higher frequency was chosen to reduce the ripples. The drawback of higher switching frequency is the inherent higher losses. The voltage ratings of the passive components in the proposed circuit were chosen higher than the rectified/output voltage for safe operation. One significant advantage of the proposed circuit is the sole use of internal body diodes of the MOSFETs, which are always in turn OFF state to transfer the stored energy in the inductor, while the other circuits in the literature [38–41] were using separate diodes. As a result, the forward voltage drop, rectification losses, cost, and complexity of the circuit can be reduced.

## 5. Simulation Results

Waveforms of the proposed circuit with the input voltage of 0.44 $V_i$ at a frequency of 100 Hz (time period: 10 ms or 0.01 s), simulated using LTSPICE and the enveloped inductor current, and rectified voltage, is shown in Figure 9.

In the simulation, the PD source impedance was neglected to produce an ideal waveform for ease of verification of the proposed concept. In the experiment, the ideal source was replaced by the actual PD. To further understand the performance of simulation waveforms, namely the zoom-in view of a positive half cycle with the duty cycle of 0.50 and the resultant rectified voltage (in both half cycles) due to switching, is shown in Figure 10.

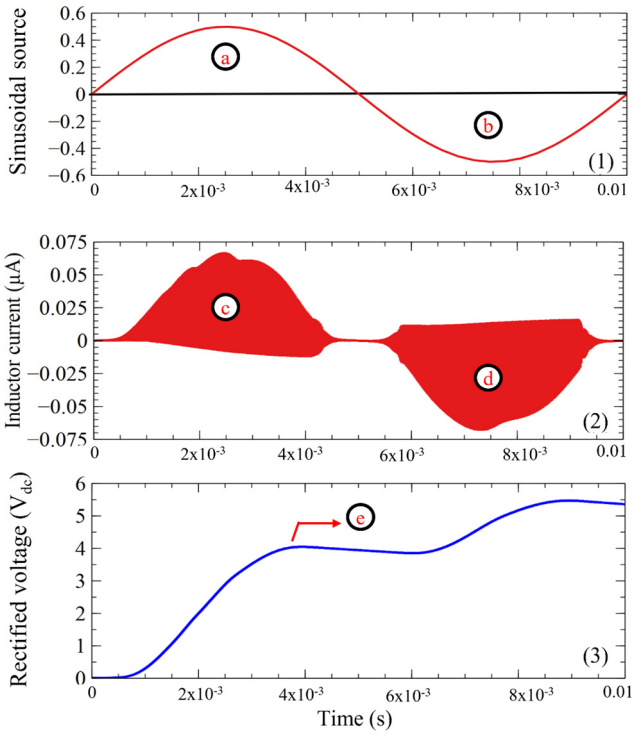


**Figure 9.** Simulation results with an ideal source (**1**) Sinusoidal source, (**2**) Inductor current, (**3**) Rectified voltage, (**a**,**b**) Positive, negative cycles, (**c**,**d**) Inductor current in positive and negative half cycles, (**e**) Rectified voltage.

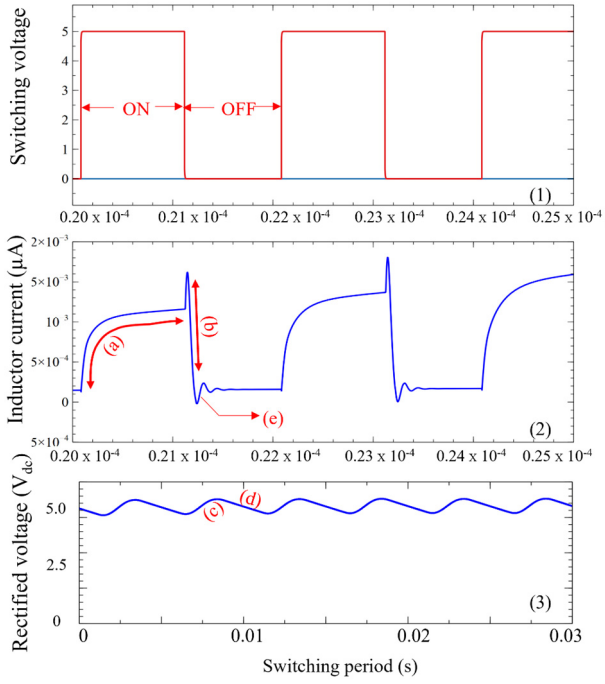


**Figure 10.** Zoom-in view of the switching period (**1**) Switching, (**2, 3**) Inductors and load capacitor energising process, (**a**) Mode 2, (**b**,**c**) Mode 3, (**d**) Mode 4, (**e**) Inductor leakage current.

## 6. Experimental Results and Discussion

The experimental setup and the proposed circuit constructed on a breadboard are shown within the context of Figure 11. The performance of the circuit was tested using one test setup. In this test, the power extracted from the PD through the proposed circuit was

investigated by varying the input voltages at a fixed frequency. Table 1 summarises various components and their parameters for the abovementioned testing scenario.

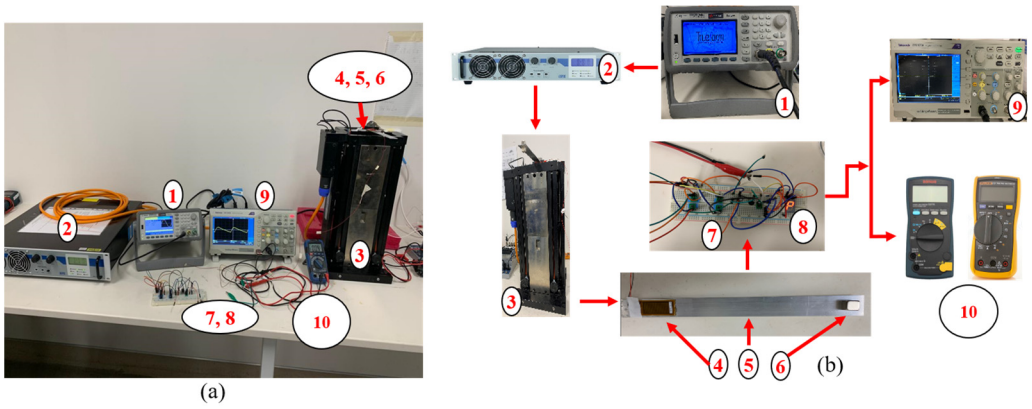


**Figure 11.** An experimental setup and its flowchart (**a**) Experimental setup, (**b**) Proposed circuit with individual experimental devices, (1) Function generator, (2) Amplifier, (3) Mechanical shaker, (4, 5, 6) PD, Aluminium beam, Proof mass, (7, 8) INLSC, 7-segment display, (9) Oscilloscope, (10) Ammeter, Voltmeter.

**Table 1.** Parameters of various components used in the experiment.

| Components | Parameters |
|---|---|
| MOSFETs (M1, M2, M3, M4) | 0.3 $V_{th}$, 20 V |
| Inductors (L1–L4) | 4.7, 10, 22, 47 µH |
| Load capacitors ($C_L$: C1–3) | 1, 10, 100 µF |
| Load resistors ($R_L$) | 100 kΩ, 200 kΩ, 300 kΩ, and 400 kΩ |
| Vibration frequency | 100 Hz |
| Input voltage | 0.44 $V_i$ |
| Switching frequency | 50 kHz |
| Duty cycle | 0.50, 0.87 |

The experimental setup and flow chart of this study is shown in Figure 11. The piezoelectric cantilever beam was made up of an aluminium beam (dimensions: 205 × 20 × 1 mm), with one end fixed on the vibration shaker (APS—113), while the other end of the cantilever beam carried two permanent magnets. These permanent magnets were placed at the tip of the aluminium beam, acting as proof mass. A microfiber composite (MFC) patch (category: M2814-P2, 37 mm × 17 mm × 0.180 mm, $C_P$ = 33.90 nF) was attached near the fixed end of the aluminium beam, where the highest strain occurred.

A function generator (Agilent 33210A) was used to deliver a sinusoidal signal to a power amplifier (2706, B & K Agilent), which then amplified the signal before activating the shaker. The shaker generated mechanical excitations according to the input vibration frequency and amplitude to excite the piezoelectric cantilever beam.

For this test, the vibration frequency was fixed at 100 Hz, and the amplitude of input voltage was adjusted to obtain the desired peak open-circuit (OC) voltages during the experiment. Then, the OC voltage was connected to the proposed circuit for conversion into DC. The converted DC voltage was stored in a capacitor, which behaved like a battery or source for low electric current at a fixed voltage level. The average current of the proposed circuit was calculated using a resistor that was connected in parallel with the proposed circuit. A voltmeter (FLUKE 117) and an oscilloscope (TBS 1052B) was used to measure the voltage across the capacitor.

In addition, the calculated current through the load was also verified using a current meter (CD 771). The experimental waveforms of the proposed circuit with the duty cycle of 0.87 are presented in Figure 12.

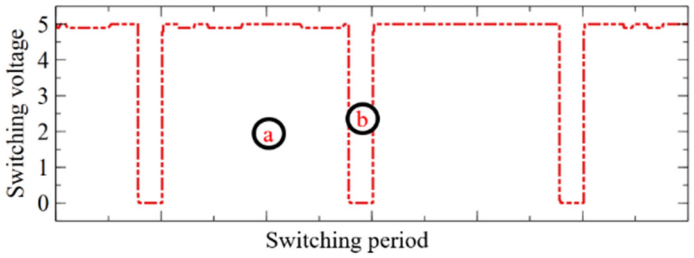


**Figure 12.** Applied Gate voltage to M3 waveform in the positive half cycle.

When the abovementioned switching signals (Figure 12) were applied to the proposed circuit, the applied gate voltage, energising inductor current, and energising inductor current, the rectified voltage over one switching period are shown in Figures 13 and 14. Besides, the extracted rectified voltage and calculated output power over different resistances are shown in Figure 15.

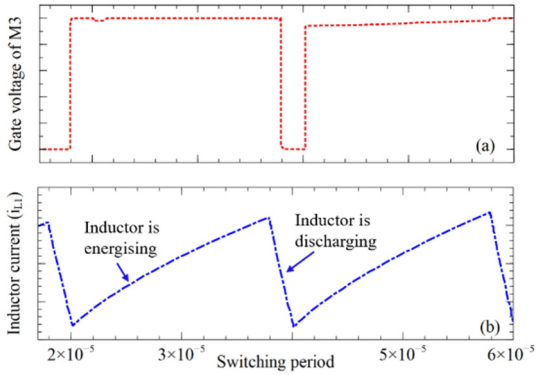


**Figure 13.** Applied Gate voltage and inductor current over one switching period according to Mode 2 and Mode 3.

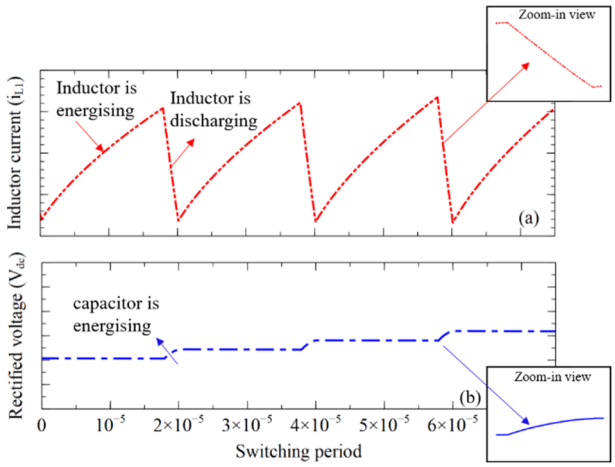


**Figure 14.** Inductor current and rectified voltage of the proposed converter.

As can be seen from Figure 15a, the rectified voltage through the proposed circuit increased with its load resistance at constant input voltage and inductance. It can also be noticed that the proposed circuit was extracting the highest rectified voltage with an inductance of L1 at a resistance of 400 KΩ. Ohm's law can be used to explain the positive correlation between the rectified voltage and resistance. Besides, as stated above, the PD current charged the inductor in the form of a magnetic field. When the PD current began to flow into the inductor, an opposing magnetic force was generated. At this time, in the positive cycle, the switch S1 was turned ON and OFF. Therefore, when the switch

was ON, the PD current in the inductor was shorted in the circuit, which resulted in a higher magnetic field across the inductor as changing the magnetic field caused the higher potential difference.

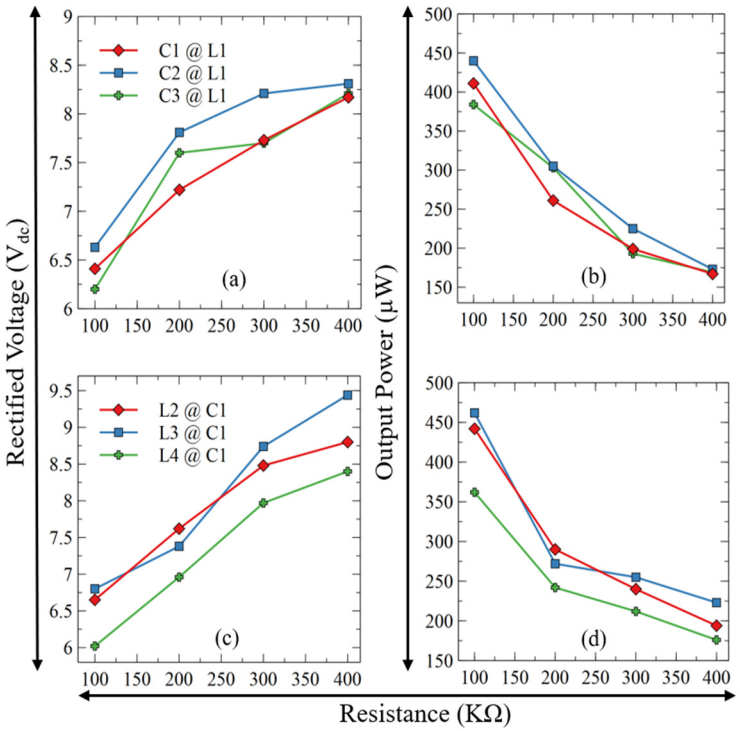


**Figure 15.** Outputs at different resistances of the proposed circuit with input voltage of 0.4 $V_i$ (**a**,**c**) Rectified voltage, and (**b**,**d**) Output power.

When the switch was in the OFF state, the stored magnetic field across the inductor discharged through the switch, M1, to charge the load capacitor. In other words, the enveloped inductor current (L1 = 4.7 μH) was synchronised with the PD at 100 Hz. As a result, it delivered maximum rectified voltage.

During this time, the voltage across and current through the load resistor was measured to calculate the extracted output power through the proposed circuit, as illustrated in Figure 15b. The resistors in Table 1 were connected sequentially as load. Note that only the case of inductance, L1 = 4.7 μH is presented with the three load capacitors. In Figure 15c,d, only the case of load capacitor, C1 = 1 μF with different inductances is presented, as other capacitances followed the same trend.

As identified in Figure 15, the increasing trend of rectified voltage was observed with other inductances as well. Despite using the inductance of L3 = 22 μH, the proposed circuit has delivered maximum rectified voltage and output power. Overall, the proposed circuit delivered a maximum output power of 469 μW with an input voltage of 0.44 $V_i$ at 100 Hz.

Figure 16 illustrates the captured voltage waveform of the proposed circuit using the oscilloscope (input voltage = 0.5 $V_i$, inductance = 22 μH, frequency = 100 Hz). The rectified voltage waveform was compared with a recently published H-Bridge circuit [3]. It can be observed that the ripples in the voltage rectified by the proposed circuit were significantly less pronounced in comparison with the H-Bridge circuit. The main reason for the fewer ripples through the proposed circuit was the inclusion of the non-linear method and the switching process, while the H-Bridge includes only the linear method. The following observations were also made regarding ripples reduction:

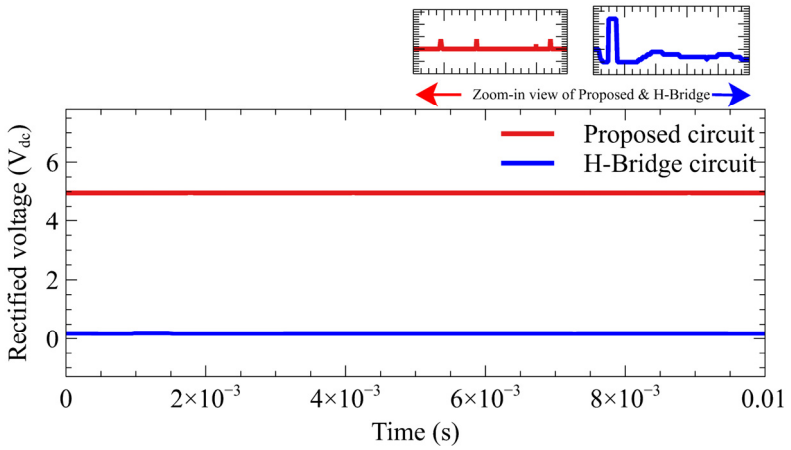


**Figure 16.** Rectified voltage of the proposed and H-Bridge circuit.

- By neglecting the smaller ripples in the output voltage of the proposed circuit, the discharging time was much shorter than the H-Bridge circuit (Zoom-in view).
- The ripples in the H-Bridge circuit could also be controlled by applying the switching method proposed in this study.

Note that the proposed circuit was also tested with other input voltages, namely 0.55 $V_i$ and 0.75 $V_i$, at various frequencies, namely 100, 110, 120, 130 Hz. However, only the case of input voltage of 0.44 $V_i$ at a frequency of 100 Hz is presented, where the proposed circuit delivered prominent output in comparison with other scenarios, and the remaining testing scenario trends were similar.

Finally, the applicability of the proposed circuit was tested through powering a 7-segment display, as shown in Figure 17. For such purpose, the load resistor was replaced with a 7-segment display, which is commonly used in traffic applications. The segment display was manually connected on the breadboard, and it is noted that the proposed circuit could power the 7-segment display, which was not shown in the existing similar designs and literature.

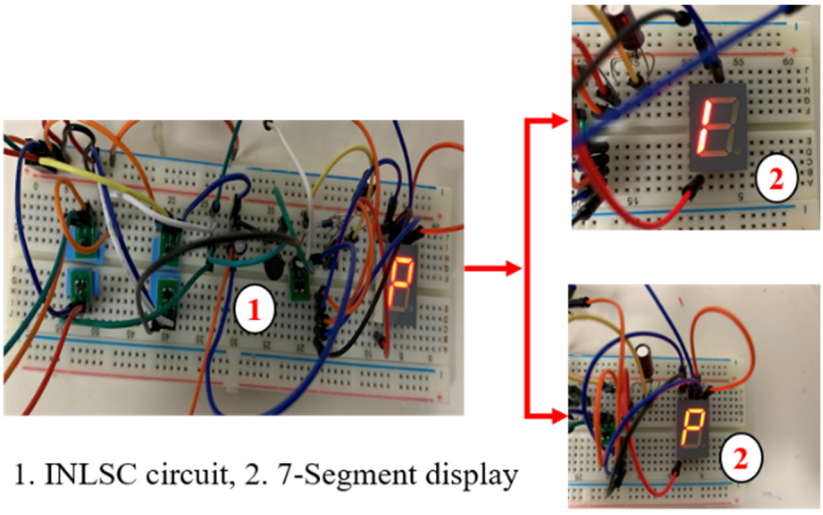


**Figure 17.** 7-segment display powered by PEH system through the proposed circuit.

Lastly, the performance of the proposed circuit was compared with some previously proposed similar circuits, and the outcome is tabulated in Table 2. The proposed circuit outperformed all previously proposed circuits/methods in terms of rectified voltage and output power.

**Table 2.** Comparison of the output of numerous circuits available in the literature.

| Methods | No of PD's | Input Voltage ($V_i$) | Output Voltage ($V_{dc}$) | Output Power (μW) | External Power Supply |
|---|---|---|---|---|---|
| [36] | 1 | 0.4 | 3.3 | - | Yes |
| [40] | 1 | 2.5 | 5.5 | 300 | No |
| [42] | 1 | 0.65 | 1.8 | 75 | Yes |
| [43] | 1 | 10 | 20 | 310 | Yes |
| [26] (Similar design) | 3 | 3.5 | - | 254 | Yes |
| [22] (Similar design) | 1 | 4.9 | - | 136 | No |
| [44] | 1 | - | 10 | - | Yes |
| [45] | 1 | 0.5 | - | 43.35 | Yes |
| [46] | 1 | 1.6 | 5.5 | 200 | Yes |
| Proposed INLSC | 1 | 0.44 | 6.5 | 469.1 | Yes |

## 7. Conclusions

An INLSC capable of extracting higher power from low voltages and reducing the ripple in rectified voltage waveform was proposed and investigated in this study. The proposed INLSC could rectify and boost the low magnitude AC voltage generated by the PD used in PEH systems. The proposed converter combines the process of synchronous rectifier boost, buck-boost, and dual-stage circuits into an improved rectifier-less switching circuit. An additional advantage of the proposed circuit is that it does not require programming or external tuning, as it can self-adjust while the PD harvests energy from ambient vibrations. The operation and performance of the proposed circuit were verified through simulation and experiment. The proposed circuit converted 0.44 $V_i$ to 6.5 $V_{dc}$ and extracted a maximum output power of 469 μW, which is superior to similar circuits in the literature. The ripples in the rectified voltage were reduced. The circuit was found to be superior to the existing circuits/methods. In addition, the proposed circuit was capable of powering a 7 segment display.

**Author Contributions:** Conceptualization, M.E.; Data curation, M.E.; Formal analysis, M.E.; Funding acquisition, Y.Y.L.; Investigation, M.E.; Methodology, M.E.; Project administration, M.E.; Resources, M.E.; Software, M.E.; Supervision, Y.Y.L., R.V.P. and D.M.; Validation, M.E.; Visualization, M.E.; Writing—original draft, M.E.; Writing—review & editing, M.E., Y.Y.L. and R.V.P. All authors have read and agreed to the published version of the manuscript.

**Funding:** The APC was paid by the first author Ricardo Vasquez Padilla.

**Institutional Review Board Statement:** Not applicable.

**Informed Consent Statement:** Not applicable.

**Data Availability Statement:** Data available on request due to privacy and restrictions.

**Conflicts of Interest:** The authors declare no conflict of interest.

## References

1. Aghamohamadi, M.; Mahmoudi, A.; Haque, M.H. Two-Stage Robust Sizing and Operation Co-Optimization for Residential PV–Battery Systems Considering the Uncertainty of PV Generation and Load. *IEEE Trans. Ind. Inform.* **2020**, *17*, 1005–1017. [CrossRef]
2. Li, S.; Zhu, G.-R.; Tan, S.C.; Hui, S.Y.R. Direct AC/DC Rectifier With Mitigated Low-Frequency Ripple Through Inductor-Current Waveform Control. *IEEE Trans. Power Electron.* **2014**, *30*, 4336–4348. [CrossRef]
3. Khezri, R.; Mahmoudi, A.; Haque, M.H.H. Optimal Capacity of Solar PV and Battery Storage for Australian Grid-Connected Households. *IEEE Trans. Ind. Appl.* **2020**, *56*, 5319–5329. [CrossRef]
4. Edla, M.; Lim, Y.Y.; Deguchi, M.; Padilla, R.V.; Izadgoshasb, I. An Improved Self-Powered H-Bridge Circuit for Voltage Rectification of Piezoelectric Energy Harvesting System. *IEEE J. Electron Devices Soc.* **2020**, *8*, 1050–1062. [CrossRef]

5. Rahman, A.; Farrok, O.; Islam, R.; Xu, W. Recent Progress in Electrical Generators for Oceanic Wave Energy Conversion. *IEEE Access* **2020**, *8*, 138595–138615. [CrossRef]
6. Liu, H.; Zhong, J.; Lee, S.-W.; Lee, L. A comprehensive review on piezoelectric energy harvesting technology: Materials, mechanisms, and applications. *Appl. Phys. Rev.* **2018**, *5*, 041306. [CrossRef]
7. Guyomar, D.; Badel, A.; Lefeuvre, E.; Richard, C. Toward energy harvesting using active materials and conversion improvement by nonlinear processing. *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **2005**, *52*, 584–595. [CrossRef]
8. Li, S.; Roy, A.; Calhoun, B.H. A Piezoelectric Energy-Harvesting System With Parallel-SSHI Rectifier and Integrated Maximum-Power-Point Tracking. *IEEE Solid-State Circuits Lett.* **2019**, *2*, 301–304. [CrossRef]
9. Edla, M.; Lim, Y.Y.; Padilla, R.V.; Mikio, D. Design and Application of a Self-Powered Dual-Stage Circuit for Piezoelectric Energy Harvesting Systems. *IEEE Access* **2021**, *9*, 86954–86965. [CrossRef]
10. Du, S.; Jia, Y.; Zhao, C.; Amaratunga, G.A.J.; Seshia, A.A. A Fully Integrated Split-Electrode SSHC Rectifier for Piezoelectric Energy Harvesting. *IEEE J. Solid-State Circuits* **2019**, *54*, 1733–1743. [CrossRef]
11. Wu, L.; Ha, D.S. A Self-Powered Piezoelectric Energy Harvesting Circuit With an Optimal Flipping Time SSHI and Maximum Power Point Tracking. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1758–1762. [CrossRef]
12. Dini, M.; Romani, A.; Filippi, M.; Tartagni, M. A Nanopower Synchronous Charge Extractor IC for Low-Voltage Piezoelectric Energy Harvesting With Residual Charge Inversion. *IEEE Trans. Power Electron.* **2015**, *31*, 1263–1274. [CrossRef]
13. Lefeuvre, E.; Badel, A.; Brenes, A.; Seok, S.; Woytasik, M.; Yoo, C.-S. Analysis of piezoelectric energy harvesting system with tunable SECE interface. *Smart Mater. Struct.* **2017**, *26*, 035065. [CrossRef]
14. Lu, D.D.-C.; Iu, H.H.-C.; Pjevalica, V. Single-stage AC/DC boost-forward converter with high power factor, regulated bus and output voltages. *IEEE Trans. Ind. Electron.* **2009**, *56*, 2128–2132. [CrossRef]
15. Kong, N.; Ha, D.S.; Erturk, A.; Inman, D.J. Resistive Impedance Matching Circuit for Piezoelectric Energy Harvesting. *J. Intell. Mater. Syst. Struct.* **2010**, *21*, 1293–1302. [CrossRef]
16. Kong, N.; Ha, D.S. Low-Power Design of a Self-powered Piezoelectric Energy Harvesting System With Maximum Power Point Tracking. *IEEE Trans. Power Electron.* **2011**, *27*, 2298–2308. [CrossRef]
17. Edla, M.; Lim, Y.Y.; Deguchi, M.; Padilla, R.V. A Novel Discontinuous Mode Piezoelectric Energy Harvesting Circuit for Low-Voltage Applications. In Proceedings of the 31st Australasian Universities Power Engineering Conference (AUPEC), Perth, Australia, 26–30 September 2021; IEEE: Piscataway, NJ, USA, 2021; pp. 1–5. [CrossRef]
18. Edla, M.; Lim, Y.Y.; Mikio, D.; Padilla, R.V. A Single-Stage Rectifier-Less Boost Converter Circuit for Piezoelectric Energy Harvesting Systems. *IEEE Trans. Energy Convers.* **2021**, 1. [CrossRef]
19. Edla, M.; Lim, Y.; Padilla, R.; Deguchi, M. An Improved Rectifier Circuit for Piezoelectric Energy Harvesting from Human Motion. *Appl. Sci.* **2021**, *11*, 2008. [CrossRef]
20. Hsieh, J.-C.; Tsai, T.-H. An AC-DC Wind Energy Harvesting Circuit with Extended Input-Voltage Range and 95% Tracking Efficiency. In Proceedings of the 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence, Italy, 30 April 2018; IEEE: Piscataway, NJ, USA, 2018; pp. 1–4. [CrossRef]
21. Ottman, G.; Bhatt, A.; Hofmann, H.; Lesieutre, G. Adaptive piezoelectric energy harvesting circuit for wireless, remote power supply. *IEEE Trans. Power Electron.* **2002**, *17*, 669–676. [CrossRef]
22. Wu, L.; Do, X.-D.; Lee, S.-G.; Ha, D.S. A Self-Powered and Optimal SSHI Circuit Integrated With an Active Rectifier for Piezoelectric Energy Harvesting. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2016**, *64*, 537–549. [CrossRef]
23. Xia, H.; Xia, Y.; Shi, G.; Ye, Y.; Wang, X.; Chen, Z.; Jiang, Q. A Self-Powered S-SSHI and SECE Hybrid Rectifier for PE Energy Harvesters: Analysis and Experiment. *IEEE Trans. Power Electron.* **2020**, *36*, 1680–1692. [CrossRef]
24. Quelen, A.; Morel, A.; Gasnier, P.; Grézaud, R.; Monfray, S.; Pillonnet, G. A 30nA quiescent 80nW-to-14mW power-range shock-optimized SECE-based piezoelectric harvesting interface with 420% harvested-energy improvement. In Proceedings of the 2018 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 30 October 2018; IEEE: Piscataway, NJ, USA; pp. 150–152.
25. Wu, L.; Zhu, P.; Xie, M. A Self-Powered Hybrid SSHI Circuit with a Wide Operation Range for Piezoelectric Energy Harvesting. *Sensors* **2021**, *21*, 615. [CrossRef] [PubMed]
26. Shareef, A.; Goh, W.L.; Narasimalu, S.; Gao, Y. A Rectifier-Less AC–DC Interface Circuit for Ambient Energy Harvesting From Low-Voltage Piezoelectric Transducer Array. *IEEE Trans. Power Electron.* **2018**, *34*, 1446–1457. [CrossRef]
27. Li, S.; Qi, W.; Tan, S.C.; Hui, S.Y.R. Integration of an Active Filter and a Single-Phase AC/DC Converter With Reduced Capacitance Requirement and Component Count. *IEEE Trans. Power Electron.* **2015**, *31*, 4121–4137. [CrossRef]
28. Li, S.; Lee, A.T.L.; Tan, S.C.; Hui, S.Y.R. Plug-and-Play Voltage Ripple Mitigator for DC Links in Hybrid AC–DC Power Grids With Local Bus-Voltage Control. *IEEE Trans. Ind. Electron.* **2017**, *65*, 687–698. [CrossRef]
29. Ravikumar, S.S.V.D.R.; Hemkumar, P. *Implementation of Direct AC-DC Boost Converter For Low Voltage Energy Harvesting*; International Journal of Engineering Science Invention: Chennai, India, 2013.
30. Nath, A.D.; Radhakrishnan, K.; Eldhose, K. Low–voltage direct ac-dc boost converter for micro generator based energy harvesting. *Int. J. Adv. Res. Electr. Electron. Instrum. Eng.* **2013**, *2*, 1045–1052.
31. Rashid, M.H. *Power Electronics Handbook*; Butterworth-Heinemann: Oxford, UK, 2017.
32. Lefeuvre, E.; Badel, A.; Richard, C.; Guyomar, D. Energy harvesting using piezoelectric materials: Case of random vibrations. *J. Electroceramics.* **2007**, *19*, 349–355. [CrossRef]

33. Du, S.; Jia, Y.; Zhao, C.; Amaratunga, G.A.J.; Seshia, A.A. A Nail-Size Piezoelectric Energy Harvesting System Integrating a MEMS Transducer and a CMOS SSHI Circuit. *IEEE Sens. J.* **2019**, *20*, 277–285. [CrossRef]
34. Xia, H.; Xia, Y.; Ye, Y.; Qian, L.; Shi, G.; Chen, R. Analysis and Simulation of Synchronous Electric Charge Partial Extraction Technique for Efficient Piezoelectric Energy Harvesting. *IEEE Sens. J.* **2018**, *18*, 6235–6244. [CrossRef]
35. Garbuio, L.; Lallart, M.; Guyomar, D.; Richard, C.; Audigier, D. Mechanical Energy Harvester With Ultralow Threshold Rectification Based on SSHI Nonlinear Technique. *IEEE Trans. Ind. Electron.* **2009**, *56*, 1048–1056. [CrossRef]
36. Das, A.; Gao, Y.; Kim, T.T.-H. A 220-mV Power-on-Reset Based Self-Starter With 2-nW Quiescent Power for Thermoelectric Energy Harvesting Systems. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2016**, *64*, 217–226. [CrossRef]
37. Liang, J.; Liao, W.-H. Improved Design and Analysis of Self-Powered Synchronized Switch Interface Circuit for Piezoelectric Energy Harvesting Systems. *IEEE Trans. Ind. Electron.* **2011**, *59*, 1950–1960. [CrossRef]
38. Lu, S.; Boussaid, F. A Highly Efficient P-SSHI Rectifier for Piezoelectric Energy Harvesting. *IEEE Trans. Power Electron.* **2015**, *30*, 5364–5369. [CrossRef]
39. Zouari, M.; Naifar, S.; Götz, M.; Derbel, N.; Kanoun, O. An optimized self-powered P-SSHI circuit for piezoelectric energy harvesting. In Proceedings of the 2017 IEEE International Instrumentation and Measurement Technology Conference (I2MTC), Torino, Italy, 22–25 May 2017; pp. 1–6.
40. Tabesh, A.; Fréchette, L.G. A Low-Power Stand-Alone Adaptive Circuit for Harvesting Energy From a Piezoelectric Micropower Generator. *IEEE Trans. Ind. Electron.* **2009**, *57*, 840–849. [CrossRef]
41. Edla, M.; Lim, Y.Y. An Improved Piezoelectric Energy Harvesting Circuit for Reducing the Internal Loss. In Proceedings of the 83rd Researchfora International Conference, New Delhi, India, 29–30 January 2020.
42. Hehn, T.; Hagedorn, F.; Maurath, D.; Marinkovic, D.; Kuehne, I.; Frey, A.; Manoli, Y. A Fully Autonomous Integrated Interface Circuit for Piezoelectric Harvesters. *IEEE J. Solid-State Circuits* **2012**, *47*, 2185–2198. [CrossRef]
43. Pollet, B.; Despesse, G.; Costa, F. A New Non-Isolated Low-Power Inductorless Piezoelectric DC–DC Converter. *IEEE Trans. Power Electron.* **2019**, *34*, 11002–11013. [CrossRef]
44. Ching, W.A.; Geotina, M.J.; Gora, N.S.; Sucayre, R.J.; Santiago, R.V.M.; Martinez, J.M. Implementation of Piezoelectric Generator for Harvesting Energy for Different Types of Staircases with Automatic Switching Mechanism. In Proceedings of the 2018 IEEE 10th International Conference on Humanoid, Nanotechnology, Information Technology, Communication and Control, Environment and Management (HNICEM), Baguio, Philippines, 29 November–2 December 2018; pp. 1–6. [CrossRef]
45. Dondi, D.; Napoletano, G.; Bertacchini, A.; Larcher, L.; Pavan, P. A WSN system powered by vibrations to improve safety of machinery with trailer. *Sensors* **2012**, 1–4. [CrossRef]
46. Lefeuvre, E.; Audigier, D.; Richard, C.; Guyomar, D. Buck-Boost Converter for Sensorless Power Optimization of Piezoelectric Energy Harvester. *IEEE Trans. Power Electron.* **2007**, *22*, 2018–2025. [CrossRef]