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Optimization Design of Packaging Insulation for Half-Bridge SiC MOSFET Power Module Based on Multi-Physics Simulation

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Abstract: With the development of power modules for high voltage, high temperature, and high power density, their size is becoming smaller, and the packaging insulation experiences higher electrical, thermal, and mechanical stress. Packaging insulation needs to meet the requirement that internal electric field, temperature, and mechanical stress should be as low as possible. Focusing on the coupling principles and optimization design among electrical, thermal, and mechanical stresses in the power module packaging insulation, a multi-objective optimization design method based on Spice circuit, finite element field numerical calculation, and multi-objective gray wolf optimizer (MOGWO) is proposed. The packaging insulation optimal design of a 1.2 kV SiC MOSFET half-bridge power module is presented. First, the high field conductivity characteristics of the substrate ceramic and encapsulation silicone of the packaging insulation material were tested at different temperatures and external field strengths, which provided the key insulation parameters for the calculation of electric field distribution. Secondly, according to the mutual coupling principles among electric–thermal–mechanical stress, the influence of packaging structure parameters on the electric field, temperature, and mechanical stress distribution of packaging insulation was studied by finite element calculation and combined with Spice circuit analysis. Finally, the MOGWO algorithm was used to optimize the electric field, temperature, and mechanical stress in the packaging insulation. The optimal structural parameters of the power module were used to fabricate the corresponding SiC MOSFET module. The fabricated module is compared with a commercial module by the double-pulse experiment and partial discharge experiment to verify the feasibility of the proposed design method.

Keywords: power module; packaging insulation; finite element method; multi-physics; multi-objective optimization

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1. Introduction

1.1. Motivation

Wide-bandgap semiconductors, including SiC and GaN, have the characteristics of high breakdown field strength, low switching loss, and high-temperature resistance, which can significantly improve the efficiency and power density of power modules [1]. Due to the wide bandgap characteristic of SiC, it is quite suitable for high-voltage applications such as high-voltage DC power transmission, automotive, and mechatronic applications [2–5]. To increase the power density of SiC power modules, their sizes are becoming smaller, and the working voltage and temperature are becoming higher, which makes the packaging insulation withstand greater electrical, thermal, and mechanical stress. This puts forward more challenges for the insulation design of packaging materials [6].

1.2. Related Works on Nonlinear Electrical Conductivity of Packaging Insulation and Its Optimization Design

With the development of SiC devices with 10 kV, 15 kV, and even higher-rated voltage, the insulation of the high-voltage module plays a key role in the reliability and should be carefully considered in the module design process. A half-bridge SiC MOSFET power modules are subjected to DC voltages with constant magnitude or unipolar square wave voltages, and the steady-state electric field distribution inside the encapsulation insulating material under the DC electric field are determined by its electrical conductivity. However, the electrical conductivity is not a constant value but a complex parameter with a nonlinear relationship to temperature and local electric fields. The current research on power module packaging insulation mainly focuses on reducing the maximum electric field at the "triple junction" in the packaging insulation by increasing the thickness of the ceramic substrate [7], adjusting the offset of the substrate metal layer [8], improving the pad size and corner curvature of the substrate [9,10]. However, the variation of electrical conductivity of insulating materials with the local electric field and temperature has not been considered in the existing studies. The nonlinear characteristic of the electrical conductivity is the key to calculating the electric field distribution in the module package and is considered in the proposed optimization design process in this paper.

For the packaging insulation optimization design of power modules, the current research mainly focuses on reducing stray parameters [11,12], reducing thermal resistance [13], and improving package reliability [14]. Most of the research is based on lumped parameters design or two-dimensional analysis for electric field and temperature. A multi-objective optimization design model with stray parameters, thermal resistance, and inelastic working energy density as the optimization goals is studied in [15]. A multi-objective model for maximizing the lifetime of a two-dimensional power module under power cycling and thermal cycling is established in [16]. A Bayesian optimization scheme is proposed to solve electric field crowding for a 10 kV SiC power module in [17]. However, there is little research on the design of high-voltage power module packaging insulation considering the coupling effect of temperature, electric field, and mechanical stress. There is no research on the effect of the nonlinear electrical conductivity characteristics of the packaging insulation material on the 3D power module packaging insulation design.

1.3. Contribution of This Paper

This paper proposes an electrical–thermal–mechanical stress coupling simulation and optimal design method based on the combination of Spice circuit simulation, finite element field numerical calculation, and multi-objective gray wolf optimizer (MOGWO) algorithm for optimal design of SiC MOSFET power module packaging insulation. The coupling relationship between electrical, thermal, and mechanical stress in power module packaging insulation and the influence of packaging structure parameters on electrical, thermal, and mechanical stress on packaging insulation are analyzed. The MOGWO algorithm is used to obtain the optimal structural parameters of the power module packaging. Finally, according to the optimal structural parameters, a 1.2 kV half-bridge SiC MOSFET power module is fabricated. Then, the double-pulse test experiment is carried out to evaluate the dynamic switching performance, and the partial discharge experiment is carried out to verify the reliability of packaging insulation. The contributions of this paper are listed below:

(1) The nonlinear electric conductivity of packaging insulation with respect to applied voltage and temperature is experimentally investigated and the nonlinear electric conductivity is used in the multi-physics simulation to determine the electric distribution in the packaging insulation.
(2) A multi-physics 3D simulation combining Spice circuit and finite element method is proposed and the effect of packaging structure parameters on the electric field, temperature, and mechanical stress distribution are investigated.

(3) A multi-objective optimization algorithm based on MOGWO is proposed to trade off the maximum electric field, temperature, and mechanical stress, providing optimized packaging structure parameters.

2. High Field Conductivity of the Packaging Insulating Materials at Various Temperatures

As mentioned in the introduction, the electric field distribution inside the packaging insulation material is jointly determined by the permittivity and conductivity, and the steady-state electric field mainly depends on the conductivity; however, the nonlinear electrical conductivity of packaging insulation materials is related to both the applied electric field and temperature, but there is no systematic research on the high field electrical conductivity characteristics of packaging insulation materials.

To this end, this paper firstly tested high field conductance at different temperatures on substrate ceramic and silicone encapsulation.

2.1. High Field Conductivity Measurement

The conductivity test system is shown in Figure 1, consisting of a high-voltage source, a Keithley 6517 ammeter, and a three-electrode holder. The protective electrode is grounded to avoid the influence of surface leakage current on the test. The electrical conductivity of 0.2 mm thick encapsulation silicone and 0.5 mm thick Al_2O_3 substrate ceramics were measured at 30, 50, 70, and 90 °C, respectively. The packaging insulation materials were polarized under each electric field for 1800 s, and the average value of the last 30 s of polarization was taken as the quasi-steady-state current density and conductivity.

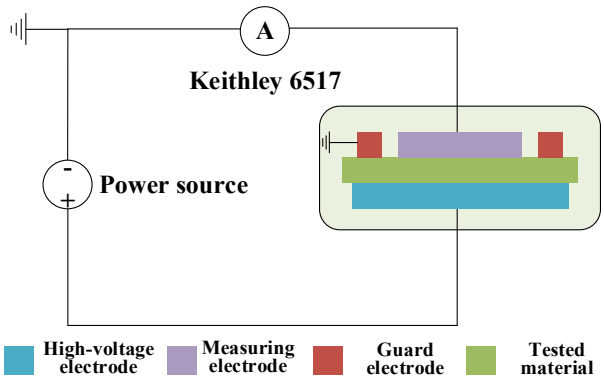

Figure 1. DC conductivity measurement system.

2.2. High Field Conductivity of Silicone Encapsulating Material

The fabrication process of the encapsulation silicone sample is as follows: firstly, the silicone matrix and the curing agent were mixed in a mass ratio of 10:1. Secondly, the mixture was placed into a vacuum oven for degassing for 30 min, and the degassed silicone was injected into a 0.2 mm thick tetrafluoroethylene mold and then placed in a press machine at room temperature to cure for 24 h to obtain a silicone film sample. Lastly, the samples were short-circuited and degassed in a vacuum oven at 60 °C for 24 h to remove byproducts and residual charges.

The conductivity test results of the encapsulation silicone are shown in Figure 2. The quasi-steady-state current density increases with the applied electric field and temperature. At 30 °C, the current density curve can be divided into two regions: the slow growth region under a low electric field and the fast-growing region under a high electric field, which match the first two stages of space charge-limited current (SCLC) theory. At 50–90 °C, the slope of the current density curve does not change and is approximately parallel to the curve of the fast-growing region under a high electric field at 30 °C. As the applied electric field increases, each segment of the curve is, respectively, defined as J_1 and J_2. At 30 °C, the current density of silicone is proportional to the applied electric field, and the slope of J_1 is close to 1, which conforms to Ohm's law. At 30 °C, the slope of J_2 is greater than 2,

indicating that the steady-state current density of silicone at this time transitions to the limited current stage by the trap-limited space charge [18]. At 50 to 90 °C, the increase in temperature enhanced the injection of charges from electrodes, which results in the formation of more carriers and increases the conductivity of the silicone. The hopping conductivity model [19] can be used to fit the conductivity in the silicone, and the fitting result is as follows:

$$\gamma = A \exp(-\frac{\varphi}{kT}) \sinh(BE) E^C \quad (1)$$

where A, B, and C are constants, T is the temperature, and k is the Boltzmann constant. By curve fitting of the data in Figure 2, A is 7.46 × 10^{-7}, φ is 0.59 eV, B is 1.87 × 10^{-8}, and C is 0.28.

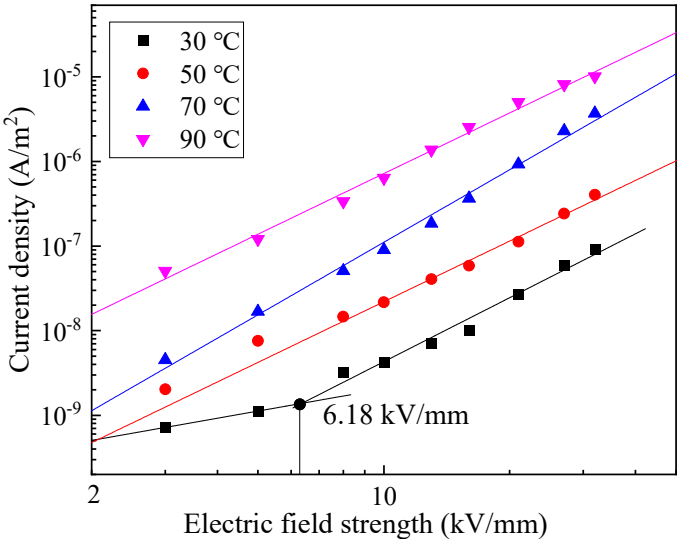

Figure 2. The quasi-steady current density of silicone at different temperatures and fields.

2.3. High Field Conductivity of Al_2O_3 Substrate Ceramic

The conductivity test results of Al_2O_3 ceramics are shown in Figure 3. The current density of the ceramic increases with the applied field strength and temperature. The DBC substrate is trigonal α-ceramic and provided by a commercial manufacturer. At low temperatures, impurity ions and local ions on the crystal lattice are the main sources of conductance. At high temperatures, when the thermal vibrational energy of the ion exceeds the binding barrier, the ion transitions away from the lattice and becomes a carrier, forming the intrinsic carrier conductance. In both cases, the ceramic conductivity and temperature satisfy the Arrhenius equation, that is, the conductivity changes exponentially with temperature. The current density curve presents a one-segment and the slopes are all approximately 1, which satisfies Ohm's law. The conductivity model obtained by fitting is

$$\gamma = A \exp(-\frac{\varphi}{kT}) \quad (2)$$

where A is a constant, φ is the activation energy, and k is the Boltzmann constant. By curve-fitting of the data in Figure 3, A is 9.01 × 10^{-11}, and φ is 0.29 eV. The DBC substrate is a trigonal α-ceramic. At low temperatures, impurity ions and local ions on the crystal lattice are the main sources of conductance. At high temperatures, when the thermal vibration energy of the ions exceeds the binding barrier, the ions transition away from the lattice and become carriers, forming the intrinsic carrier conductance. In both cases, the ceramic conductivity and temperature satisfy the Arrhenius equation, that is, the conductivity changes exponentially with temperature.

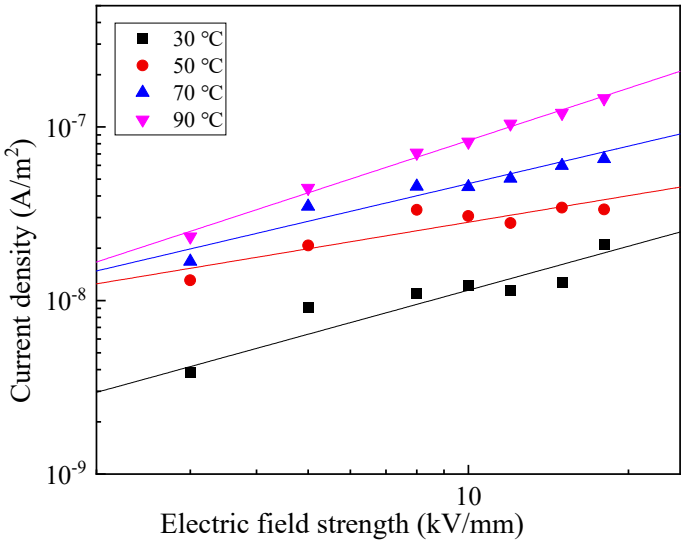

Figure 3. The quasi-steady current density of Al_2O_3 ceramic at different temperatures and fields.

3. 3D Multi-Physics Coupling Simulation of SiC MOSFET Power Module Packaging Insulation

As mentioned in the introduction, the electric field, temperature, and mechanical stress distributions in the packaging insulation are coupled and the key parameters are also determined by multi-physics. Section 3.1 theoretically analyzes the coupling relationship and all the coupling effect is considered and modeled in the proposed simulation scheme in Section 3.2. Based on the proposed scheme, Section 3.3 focuses on the effect of packaging structure parameters on multi-stress distribution, which provides the basis for the optimization in Section 4.

3.1. Multi-Physics Coupling Analysis of SiC MOSFET Power Module Packaging Insulation

3.1.1. Basic Theory of Multi-Physics Calculation

The calculation of electric field, temperature, and mechanical stress distribution in packaging insulation can be calculated using the Maxwell equation, heat conduction equation, and thermal expansion equation:

$$\begin{cases} E = -\nabla\varphi \\ \nabla \cdot J + \frac{\partial \nabla \varepsilon_0 \varepsilon_r E}{\partial t} = 0 \\ J = \gamma(E,T)E \\ \rho C_p \frac{\partial T}{\partial t} = \lambda \nabla^2 T + Q \\ \varepsilon_V = \chi \Delta T = \chi\left(T - T_{ref}\right) \\ \sigma = Y\varepsilon_V \end{cases} \tag{3}$$

where E is the electric field strength, φ is the electric potential, J is the current density, T is the temperature, ε_0 is the vacuum permittivity, ε_r is the relative permittivity, γ is the electrical conductivity, ρ is the density, C_p is the constant pressure heat capacity, Q is the heat source, that is, the power loss of the chip, λ is the thermal conductivity, χ is the thermal expansion coefficient, ε_V is the strain, σ is the stress, Y is Young's modulus, and T_{ref} is the reference temperature. It is noted that multi-physics coupling relationships will be discussed in the following section and they are also considered in Equation (3) in an implicit form.

3.1.2. Coupling Relationship between Thermal Field and Electric Field

The coupling of the electric field to thermal field is mainly reflected in the heating source. The SiC MOSFET generates power loss P_d during operation, which causes the module temperature to rise. Power loss includes two parts: conduction loss and switching loss.

Switching losses are closely related to the stray parameters of the module packaging [20]. Meanwhile, MOSFET on-state losses are mainly caused by the device's on-state resistance, which is a function of temperature. The total power loss can be expressed as

$$\begin{aligned} P_d &= P_{T(AV)} + P_{on} + P_{off} \\ &= I_{DS}^2 R_{(DS)on} + E_{on} f_s + E_{off} f_s \\ &= I_{DS}^2 R_0 \left[1 + \kappa\left(T_j - 25\right)\right] + f_s [\int_{t_{10\%}}^{t_{90\%}} v_{ds\_on}(t) i_{d\_on}(t) dt + \int_{t_{90\%}}^{t_{10\%}} v_{ds\_off}(t) i_{d\_on}(t) dt] \end{aligned} \quad (4)$$

where $R_{(DS)on}$ is the on-state resistance, E_{on} and E_{off} represent the turn-on loss and turn-off loss of the primary switch of the chip, respectively, R_0 is the on-state resistance value at 25 °C, and I_{DS} is the drain–source current of the chip during normal operation. κ is the temperature coefficient of on-state resistance, T_j is the junction temperature of the chip, f_s is the switching frequency, v_{ds} is the drain–source voltage, i_d is the drain current, and $t_{10\%}$ and $t_{90\%}$ are the transient time between the drain–source voltage at 10% and 90% of the rated voltage.

The switching loss is related to stray inductance and capacitance of the SiC MOSFET power module. The stray parameters are extracted from multi-physics simulation with the finite element method and the switching loss is evaluated from Spice simulation in this paper. $C_{\sigma+}$ and $C_{\sigma-}$ are the parasitic capacitances from the positive and negative terminals to the substrate, respectively, $C_{\sigma out}$ is the parasitic capacitance from the output terminal to the substrate, $C_{\sigma GH}$ and $C_{\sigma GL}$ are the parasitic capacitances from the gate of the upper and lower phase leg of half-bridge SiC MOSFETs to the substrate, respectively. $C_{\sigma out}$ and $C_{\sigma GH}$ are charged and discharged, respectively, by the displacement current during switching transients, while the voltages across $C_{\sigma+}$, $C_{\sigma-}$, and $C_{\sigma GL}$ are fixed, so the impedance between the output and the substrate can be expressed as $C_{\sigma out}$ and $C_{\sigma GH}$ in parallel. L_{loop} represents the equivalent inductance within the package including trace parasitic inductances and bond–wire inductance. The double pulse circuit is built in *LTspice* simulation software, as shown in Figure 4b. The stray inductance is represented as L_{loop}, C_σ represents the parallel of $C_{\sigma out}$ and $C_{\sigma GH}$. Through the Spice simulation, the switching loss E_{on} and E_{off} of every cycle can be calculated by integrating the operating voltage and current of the module with rated 1200 V voltage and 60 A current.

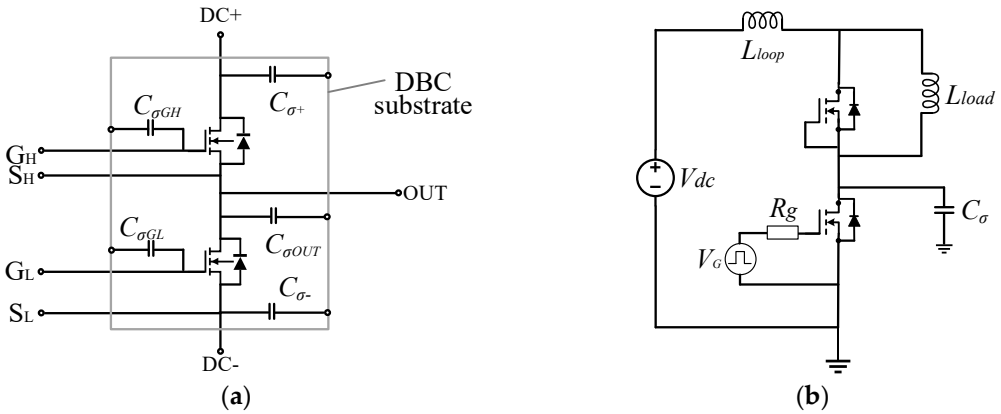

Figure 4. Stray capacitance of SiC half-bridge module (**a**) and double-pulse test simulation in LTSpice (**b**).

The coupling of thermal field to electric field is mainly reflected in the change of electrical parameters such as conductivity. The conductivity of the packaging material is a function of the local electric field and temperature, so the conductivity in Equations (1) and (2) are obtained through the experiments presented in Section 2 above. The electric field distribution is not only related to the insulating structure, but also to the temperature distribution.

3.1.3. Coupling Relationship between Thermal Field and Mechanical Stress

The coupling of thermal field to mechanical stress is mainly reflected in the thermal expansion stress. While the SiC MOSFET power module is working, due to the uneven temperature distribution inside the module and the different thermal expansion coefficients of different materials of the power module, mechanical stress is generated inside the module. As shown in Equation (3), the temperature difference is an important factor affecting the thermal stress of the power module.

The coupling of mechanical stress to thermal field is mainly reflected in the influence of interface stress on contact thermal resistance. When the two materials are in contact, there are voids between the contact interfaces due to the difference in surface roughness, resulting in an increase in thermal resistance at the interface. If the stress at the interface increases, it will reduce the size and width of the air gap, thereby affecting the thermal resistivity. At the contact interface, the contact thermal conductivity h_k is expressed as

$$\begin{cases} h_k = h_{constriction} + h_{gap} \\ h_{constriction} = 1.25 k_s \frac{m}{\delta} \left(\frac{P}{H_{mic}} \right)^{0.95} \\ h_{gap} = \frac{k_{gap}}{X + M_{gap}} \end{cases} \quad (5)$$

where $h_{constriction}$ represents the constriction conductivity, which is related to the surface properties and contact pressure; h_{gap} represents the air gap conductivity, which is related to the medium in the space. P is the contact pressure, H_{mic} is the aluminum microhardness, δ is the surface roughness, m is the roughness gradient, M_{gap} is the gas thinning parameter, k_s is the contact thermal conductivity, k_{gap} is the gap thermal conductivity, and X is the average plane microscopic spacing. The mechanical stress effect on thermal contact conduction mentioned above is also modeled in the multi-physics simulation.

3.2. 3D Multi-Physics Coupling Simulation of SiC MOSFET Power Module Packaging Insulation

A half-bridge SiC MOSFET module is taken as an example to conduct a three-dimensional multi-physics simulation of packaging insulation. The structure is shown in Figure 5. The SiC chip is soldered on the copper trace of the DBC substrate, and the electrical connection between the top surface of the chip and the DBC is realized by bonding wires. Three terminal posts (V+, V−, and AC) connect the copper trace of the DBC to the external power supply and output AC voltage. The DBC is soldered on the baseplate, and the heat generated by the chip is mainly transferred down to the heat sink through the DBC substrate. Silicone is filled as encapsulation to protect the chip and metal interconnection parts. The material parameters of the power module packaging insulation for multi-physics simulation are shown in Table 1.

Table 1. Main parameters of selected materials for multi-physics simulation.

Material	Copper	Silicone	Al_2O_3	Solder	Bond Wire	SiC
Thermal expansion coefficient (1/K)	17×10^{-6}	420×10^{-6}	6.5×10^{-6}	23×10^{-6}	23×10^{-6}	3.4×10^{-6}
Constant pressure heat capacity (J/kg/K)	385	1453	730	226	900	690
Relative permittivity	—	2.7	9.8	—	—	11.9
Density (kg/m^3)	8960	900	3780	7300	2700	3210
Thermal Conductivity (W/m/K)	400	0.145	35	50	238	501
Young's modulus (Pa)	110×10^9	5×10^6	400×10^9	40×10^9	70×10^9	501×10^9
Poisson's ratio	0.35	0.48	0.22	0.4	0.33	0.45
Conductivity (S/m)	5.998×10^7	Equation (1)	Equation (2)	8.33×10^6	3.534×10^7	—

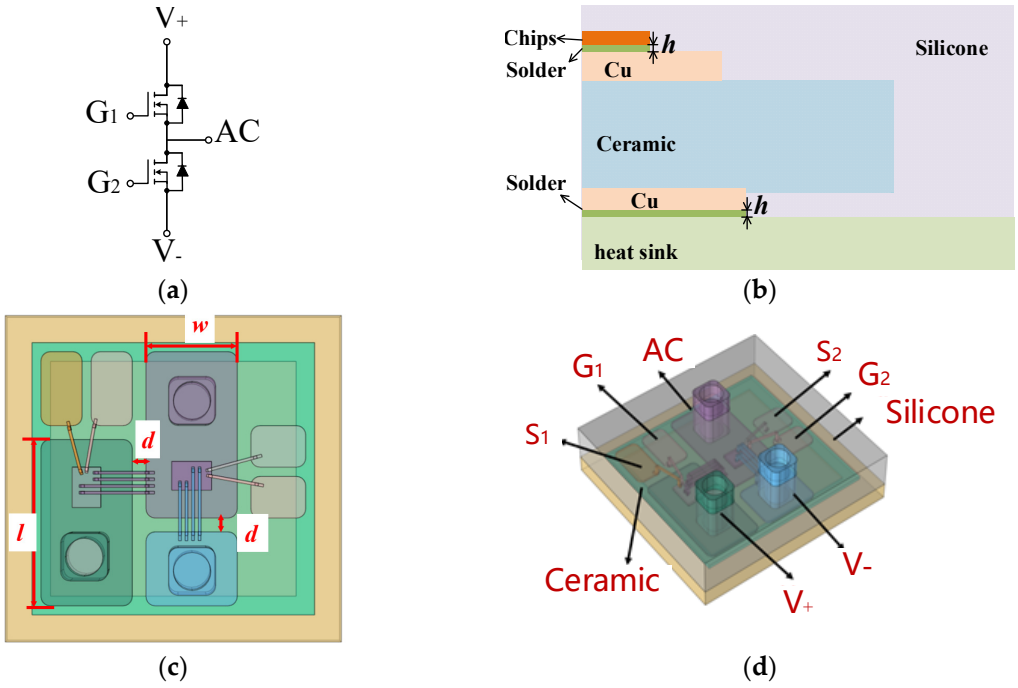

Figure 5. Packaging structure of the studied half-bridge SiC MOSFET power module: (**a**) MOSFET half-bridge circuit; (**b**) side view of the power module; (**c**) top view of the power module; (**d**) 3D structure of the power module.

The multi-physics coupling simulation flow chart is shown in Figure 6, which mainly includes four parts:

(1) The key electrical parameters of packaging insulation were obtained through the aforementioned experiments. A complete SiC MOSFET half-bridge power module was built in the multi-physics finite element software. The material parameters of the power module shown in Table 1 were imported, and the parasitic capacitance and parasitic inductance of the module package were extracted, respectively.

(2) The stray parameters were input into the double-pulse-test Spice circuit to simulate and calculate the operating loss, and the influence of the stray parameters of the module package on the switching loss of the SiC MOSFET was used in multi-physics simulation as the heat source.

(3) The multi-physics coupled finite element simulation of encapsulated module insulation was performed. The multi-physics finite element model includes an electric field calculation module, a temperature calculation module, and a mechanical stress calculation module, and the influence of multi-physics coupling factors on material parameters is also considered.

(4) According to the relationship between the packaging structure parameters and the multi-physics performance (electric field, temperature, and mechanical stress), the optimal design was applied to reduce the maximum electric field, temperature, and stress in the packaging insulation by adjusting the optimal structure parameters of the power module package.

The excitation parameters and boundary conditions are set as follows:

(1) The voltage of the drain terminal of the upper phase leg is set as 1200 V, and the source terminal of the lower phase leg and the back trace of the DBC are grounded. The ac output terminal is set as 1200 V or 0 V for the switching output.

(2) The heat source is the SiC MOSFET chip and the heat is diffused within the packaging by conduction in solids. The heat diffuses from the bottom of the module to the environment and is modeled as contacting heat sink with constant heat transfer coefficients. The heat diffuses from the top side of the silicone encapsulation to the

environment and is modeled by contacting air with constant heat transfer coefficients. The heat sources of the two SiC MOSFET chips are set according to the LTspice double-pulse simulation results, as in Equation (4). The environmental temperature is 20 °C. The heat transfer coefficients of the heat sink bottom and surrounding sides are 3000 and 20 W/m^2/K. The heat transfer coefficient of the top side of the silicone encapsulation is 5 W/m^2/K.

(3) The heat sink and surrounding sides of the silicone encapsulation are fixed. The other surfaces are free to expand and shrink. The thermal expansion stress is calculated by the thermal–mechanical coupling model.

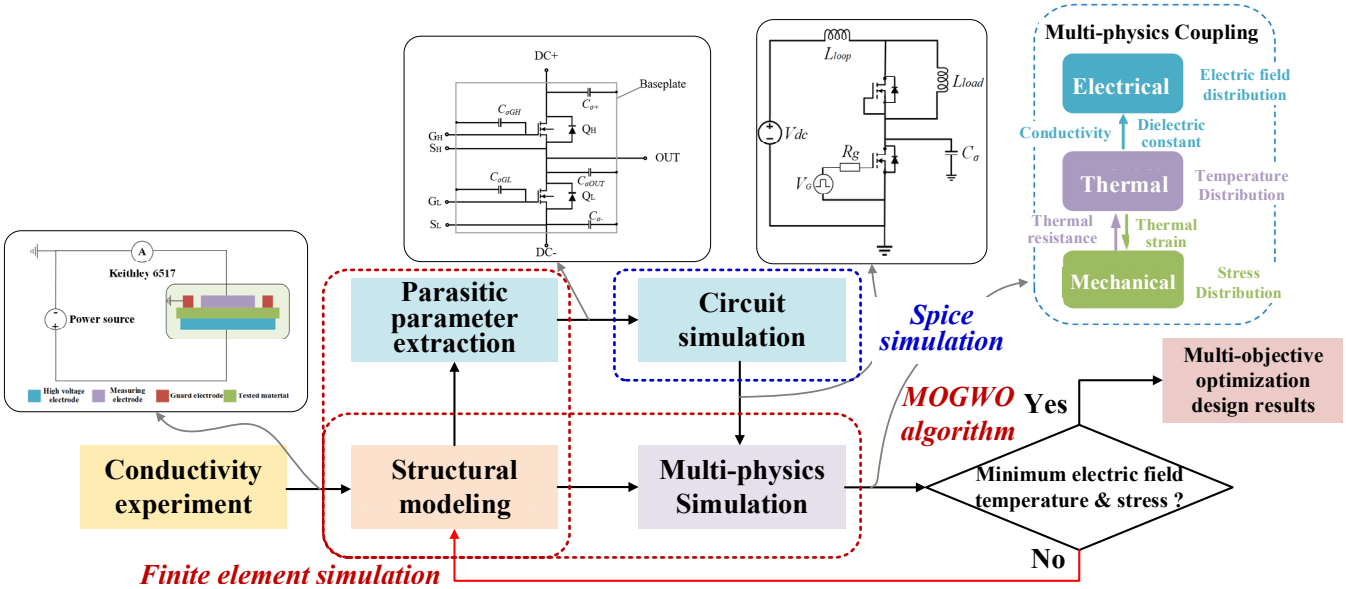

Figure 6. The flow chart of multi-physics coupling simulation.

3.3. Influence of SiC MOSFET Power Module Structure on Electrical, Thermal, and Mechanical Stress

The multi-physics simulation is performed according to the procedure shown in Figure 6. The SiC MOSFET power module structure is changed to investigate the effect of structure parameters on multi-stress distribution. The copper trace spacing d, the width w, length l, and the thickness h of the solder layer are changed from 0.5 to 2 mm, 10 to 14.5 mm, 16.5 to 21 mm, and 0.05 to 0.2 mm, as shown in Figure 5c.

The results of the electric field, temperature, and mechanical stress simulations are shown in Figure 7. The strongest electric field is at the three junction points of the DBC copper electrode, silicone, and ceramics. The temperature of the silicone at the contact position with the upper phase leg chip is the highest, and the maximum mechanical stress in the package insulation is on the contact surface of the silicone, solder, and heat sink. Figure 8 shows the effect of the packaging structure parameters on the maximum electric field, temperature, and mechanical stress in the package insulation. Since there are four variables, the curves shown in Figure 8 are, respectively, the curves obtained by changing only one variable under a set of fixed variable values (d = 0.5 mm, w = 10 mm, l = 16.5 mm, h = 0.05 mm).

3.3.1. Effect of Packaging Structure on Electric Field Distribution

The influence of the copper trace distance d on the electric field involves two aspects: on the one hand, as d increases, the thermal resistance decreases, the heat dissipation performance of the module becomes better, and the temperature at the position of the maximum electric field decreases, and the conductivity of the encapsulation silicone decreases, which in turn leads to an increase in the field strength. On the other hand, as the trace distance increases, the insulation distance increases, and the electric field decreases. The combined effect of these two factors leads to the minimum value. While the width w or

length l of the copper trace increases, the heat dissipation is enhanced, then the temperature decreases. In this way, the conductivity of the silicone decreases, and the electric field increases. With the increase of the thickness h of the solder layer, the thermal resistance increases, the heat dissipation is weakened, the conductivity of the silicone increases, and the field strength decreases.

3.3.2. Effect of Packaging Structure on Temperature Distribution

While the copper trace spacing d, the width w, and length l of the copper trace increase, the thermal resistance is reduced, and the heat dissipation of the module is enhanced. The switching power loss of the chip is slightly reduced, the conduction loss power is reduced, and the total power loss is reduced. Therefore, the maximum temperature shows a downward trend. When the thickness h of the solder layer increases, the thermal resistance increases, which weakens the heat dissipation of the module. The switching power loss of the module is almost unchanged, and the conduction loss power increases, increasing the total power loss. The cooling capacity of the module is weakened, so the maximum temperature increases.

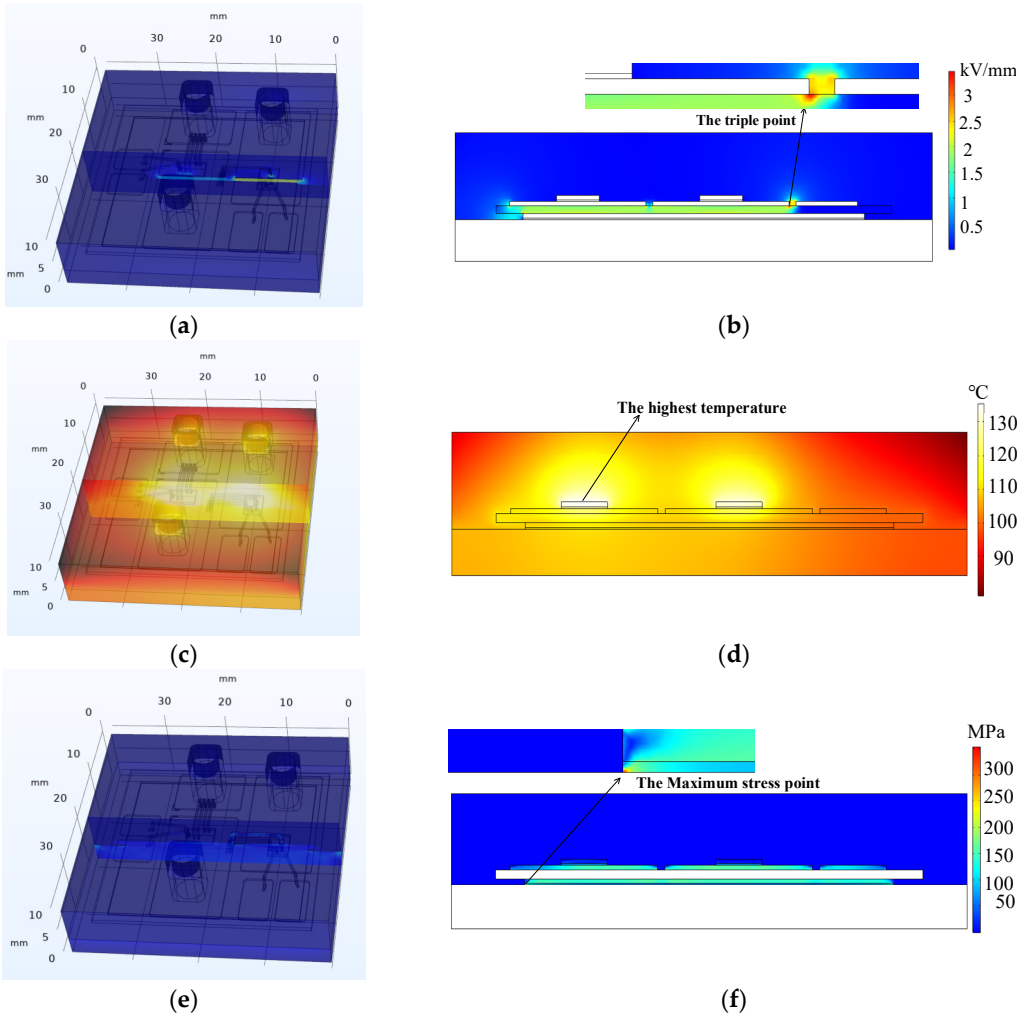

Figure 7. The distribution of the electric field, temperature, and mechanical stresses of power module packaging: (**a**) 3D view of electric field distribution, (**b**) cross-section view of electric field distribution, (**c**) 3D view of temperature distribution, (**d**) cross-section view of temperature distribution, (**e**) 3D view of mechanical stress distribution, (**f**) cross-section view of mechanical stress distribution.

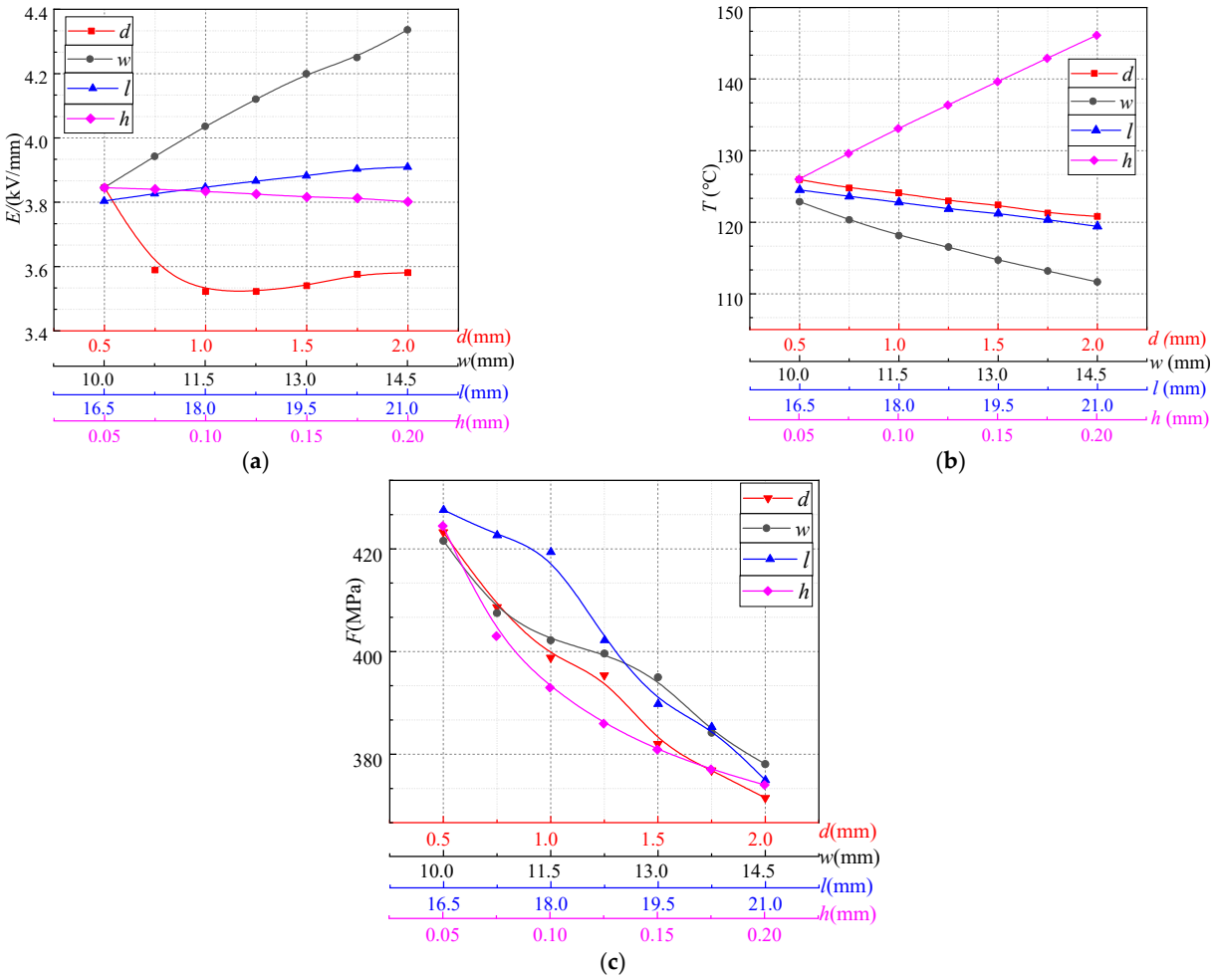

Figure 8. Effects of packaging structure parameters on the electric field, temperature, and mechanical stresses: (**a**) maximum electric field; (**b**) maximum temperature; (**c**) maximum mechanical stress.

3.3.3. Effect of Packaging Structure on Mechanical Stress Distribution

With the increase of copper trace spacing d, copper trace width w, and length l, the heat dissipation area increases, leading to a decrease in temperature and maximum mechanical stress. As the thickness h of the solder layer increases, the area of the heat sink remains unchanged. However, because the thermal resistance of the module increases, under the same temperature difference, the smaller the thickness h, the greater the deformation, and the deformation is proportional to the stress, so the mechanical stress increases.

Since the effects of structure parameters on the electric field, temperature, and mechanical stress are complicated and present coupling relationships, optimization should be performed to determine the optimized packaging parameters, which is presented in the following section.

4. Multi-Objective Optimization Design of Packaging Insulation Based on MOGWO Algorithm

4.1. MOGWO Algorithm

The gray wolf algorithm is an intelligent optimization algorithm based on group behavior. It has the characteristics of strong convergence, few parameters, easy implementation, and adaptive adjustment [21]. Therefore, the MOGWO algorithm is used to determine the optimal packaging structure parameters.

The gray wolf population has a pyramid-shaped social hierarchy, as shown in Figure 9. The first level of the pyramid is the leader of the population, called α. The second level of the pyramid is α's think tank team, called β. The third level of the pyramid is the δ, which

obeys the decision-making commands of α and β. α and β with poor fitness will also be reduced to δ. The bottom layer of the pyramid is ω, which is mainly responsible for the balance of relationships within the population.

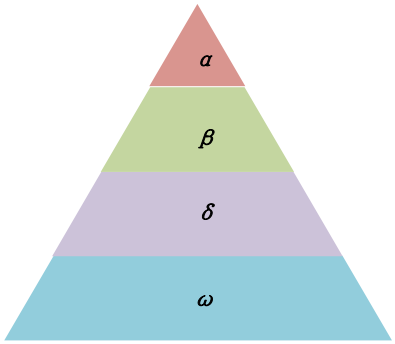

Figure 9. The hierarchy of the gray wolf population.

The hunting behavior of gray wolves mainly includes four parts [21]:

(1) Surrounding the prey: In the group of gray wolves, the distance between the individual gray wolf and the prey is

$$D = \left|C \cdot X_p(t) - X(t)\right| \tag{6}$$

where t is the current moment, C is coefficient vectors, X_p is the position vector of the prey, and X is the position vector of the gray wolf population:

$$\begin{cases} X(t+1) = X_{\mathrm{p}}(t) - A \cdot D \\ A = 2a \cdot r_1 - a \\ C = 2 \cdot r_2 \end{cases} \tag{7}$$

where a is a vector of convergence factors that decreases linearly from 2 to 0 as the number of iterations increases, and $\boldsymbol{r_1}$ and $\boldsymbol{r_2}$ are random vectors in the range [0, 1].

(2) Hunting: When the gray wolf finds the location of the prey, α leads β and δ to surround the prey. Among the positions of the three optimal solutions α, β, and δ determine the position of the prey, and at the same time, other gray wolf individuals update their positions according to the position of the optimal gray wolf individual:

$$\begin{cases} D_{\boldsymbol{\alpha}} = \left|C_1 \cdot X_{\boldsymbol{\alpha}}(t) - X(t)\right| \\ D_{\boldsymbol{\beta}} = \left|C_2 \cdot X_{\boldsymbol{\beta}}(t) - X(t)\right| \\ D_{\boldsymbol{\delta}} = \left|C_3 \cdot X_{\boldsymbol{\delta}}(t) - X(t)\right| \\ X_1 = X_{\boldsymbol{\alpha}} - A_1 \cdot D_{\boldsymbol{\alpha}} \\ X_2 = X_{\boldsymbol{\beta}} - A_2 \cdot D_{\boldsymbol{\beta}} \\ X_3 = X_{\boldsymbol{\delta}} - A_3 \cdot D_{\boldsymbol{\delta}} \\ X(t+1) = (X_1 + X_2 + X_3)/3 \end{cases} \tag{8}$$

where D_α, D_β, and D_δ represent the distances between α, β, and δ and other gray wolves, respectively; X_α, X_β, and X_δ represent the current positions of α, β, and δ, respectively; C_α, C_β, and C_δ are random vector constants, and X is the current position of the gray wolf group.

(3) Attacking the prey: In the iterative process, as the value decreases linearly from 2 to 0, the corresponding value of $|A|$ also changes in the interval $[-a, a]$. When the prey is no longer moving, the gray wolf pack will attack the prey. When $|A| < 1$, gray wolves attack their prey, that is, they fall into a locally optimal solution.

(4) Searching for prey: When $|A| > 1$ or $|A| = 1$, the gray wolf pack is separated from the prey. It leaves the local optimal solution and looks for more suitable prey, that is, the global optimal solution. To avoid the algorithm becoming stuck in the local

optimal solution instead of the global optimal solution, C is set to decrease nonlinearly to perform a global search simultaneously in the iterative process. The MOGWO solution algorithm flow is shown in Figure 10.

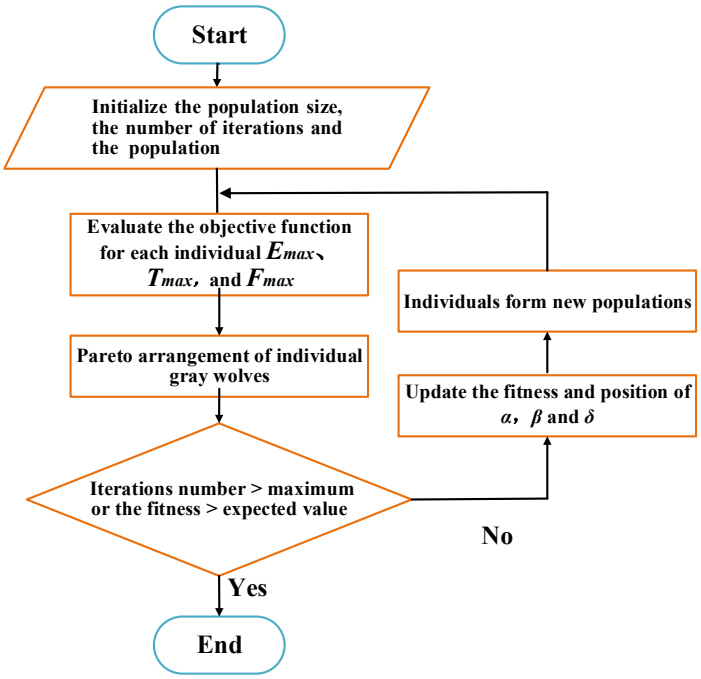

Figure 10. Flowchart of MOGWO algorithm.

4.2. Packaging Insulation Optimization Design of SiC MOSFET Power Module

The parameters of the packaging structure of the 1.2 kV SiC MOSFET half-bridge are the optimization variables and reducing the maximum electric field strength, maximum temperature, and maximum mechanical stress in the insulation of the power module package is the optimization goal. The optimization objectives are

$$\begin{cases} \min E_{\max} \\ \min T_{\max} \\ \min F_{\max} \end{cases} \tag{9}$$

The constraints are

$$\begin{cases} d_{\min} \le d \le d_{\max} \\ w_{\min} \le w \le w_{\max} \\ l_{\min} \le l \le l_{\max} \\ h_{\min} \le h \le h_{\max} \end{cases} \tag{10}$$

where the upper and lower limits are the same as those in the multi-physics simulation, as shown in Section 3.3. There are several characteristics of solving the multi-physics coupled multi-objective optimization problem for power module packaging insulation:

(1) The electrical, thermal, and mechanical stresses have a coupling relationship and influence each other. Hence, the minimum electric field, temperature, and mechanical stress cannot be obtained at the same time.

(2) The three objective functions of the maximum electric field, maximum temperature, and maximum mechanical stress have different units and orders of magnitude that cannot be directly compared. Therefore, the solution to multi-objective optimization problems is usually to obtain the Pareto optimal solution.

The MOGWO algorithm is used to solve it. The algorithm parameters are set as follows: the population size is 256, the maximum number of iterations is 5000, and the number of optimal solutions is 100. The distribution of electric field, temperature, and

mechanical stress of the gray wolf population before and after optimization is shown in Figure 11. Each point in Figure 11b represents a structural parameter optimization of the power module.

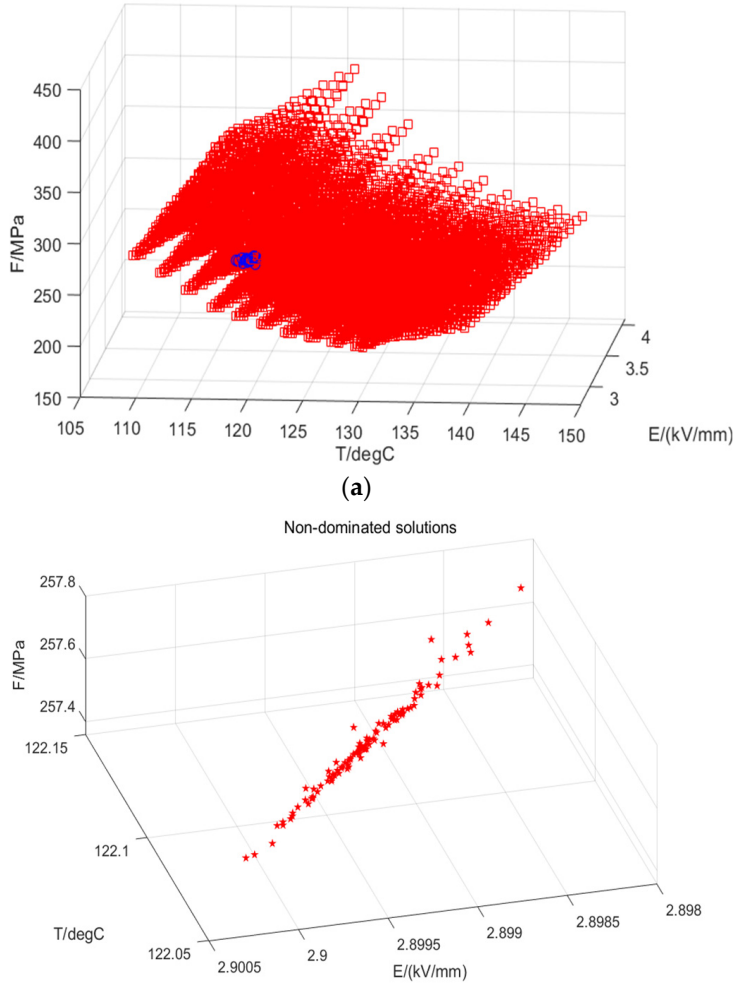

Figure 11. Maximum electric field, temperature, and mechanical stress in the original population and optimized populations: (**a**) original population (red circle) and optimized population (blue circle); (**b**) Pareto frontier of the optimized population.

Before optimization, the variation ranges of the maximum electric field, maximum temperature, and maximum mechanical stress are 2.7~4.10 kV/mm, 108.4~147.9 °C, and 110.32~342.6 MPa, respectively. After the MOGWO optimization, the variation ranges of the maximum electric, maximum temperature, and maximum stress were reduced to 2.898~2.9 kV/mm, 122.05~122.15 °C, and 257.3~257.8 MPa, respectively. For the ease of fabrication, one set of solutions is selected as the optimal structural parameters of the power module package insulation: d = 1.5 mm, w = 11.4 mm, l = 21 mm, h = 0.1 mm.

5. Experiment on the Optimal Designed SiC MOSFET

5.1. Module Fabrication

According to the half-bridge SiC MOSFET power module structure, shown in Figure 5 and the optimal structural parameters obtained by the MOGWO algorithm, the half-bridge SiC MOSFET power module is fabricated through the process shown in Figure 12. The SiC MOSFET chips are provided by the Shanghai Inventchip company with 1200 V and 60 A-rated parameters. The chips are soldered on the DBC and the DBC are soldered on

the heat sink both with SAC 305 solder paste (Sn96.5/Ag3.0/Cu0.5). Then, the connections between the top surfaces of the chips and DBC copper traces are achieved by 100 µm bonding wire. After that, the pins for gate driving and posts for the power terminals are soldered by lead-free Sn64.7/Bi35/Ag0.3 solder paste. Then, the 3D-printed frame housing is attached to the heat sink with silicone glue and the module is encapsulated with the silicone encapsulation material.

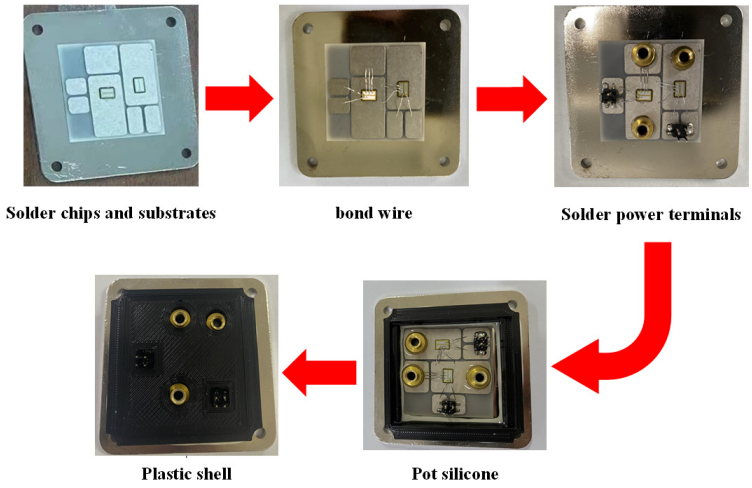

Figure 12. The fabrication process of the SiC MOSFET half-bridge power module.

5.2. Double Pulse Test

In order to evaluate the switching performance of the fabricated SiC MOSFET power module and compare the fabricated module with the commercial module, a double-pulse test circuit is built, as shown in Figure 13.

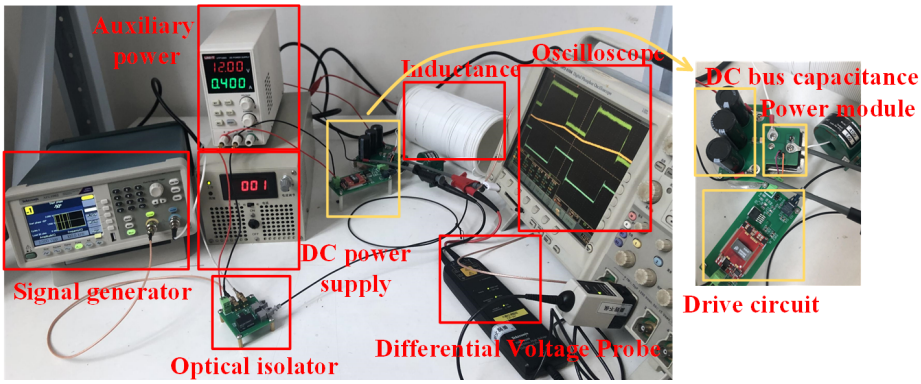

Figure 13. Double pulse test bench.

The driving circuit is composed of an optical transmitter/receiver and driving IC to isolate the driver from the high DC voltage. The DC bus voltage V_{dc} = 800 V, the DC coupling capacitance C_{dc} = 70 µF, the load inductance L_{load} = 450 µH, and the gate drive resistance R_G = 5 Ω. A signal generator is used to generate trigger pulses. To ensure that the power circuits connected externally to the power module are the same, the gate drive circuit adopts the same drive board and drive connections. The SiC MOSFET power module and the commercial SiC MOSFET power module FF45MR12W1M1 are compared at the same voltage level to test switching characteristics. The double-pulse waveform obtained through the experiment is shown in Figure 14.

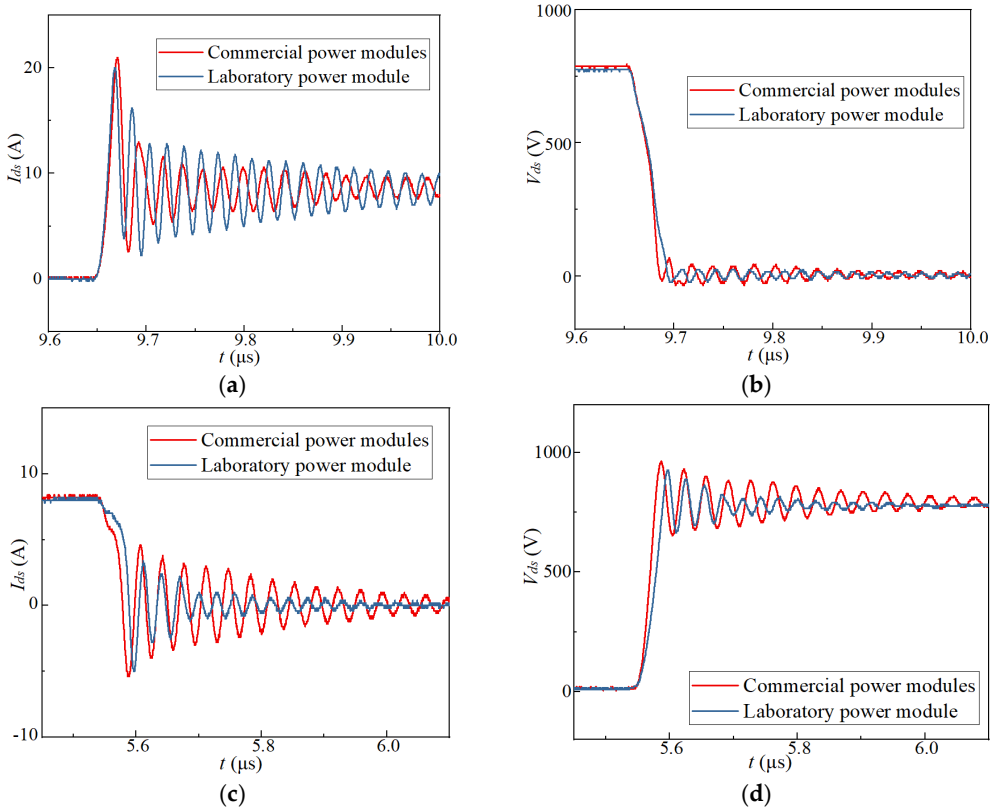

Figure 14. Double pulse test results: (**a**) drain–source current during turn-on; (**b**) drain–source voltage during turn-on; (**c**) drain–source current during turn-off; (**d**) drain–source voltage during turn-off.

Through calculation, the parasitic inductance of the obtained power module is 11.23 nH, which is smaller than the stray inductance (18 nH) of commercial power modules. The switching loss can be obtained by measuring the voltage and current curves of the SiC MOSFET power module during turn-on and turn-off and then integrating the product of the two. When calculating turn-on loss, we use the integral of the product of voltage and current in the period from 10% turn-on current to 10% turn-on voltage. The turn-off loss is calculated by using the integral of the product of voltage and current over the period from 10% turn-off voltage to 10% turn-off current [22,23]. According to the experimental results in Figure 14, the turn-on loss of the commercial power module is calculated to be 0.474 mJ and the turn-off loss is 28.64 μJ. The turn-on loss of the fabricated power module is 0.366 mJ, and the turn-off loss is 15.79 μJ. Therefore, for both the turn-on loss and the turn-off loss, the optimally designed power module is smaller than the commercial power module, indicating that the power module reduces the loss in the switching process.

5.3. Partial Discharge Test

As SiC MOSFET turn-on time shortens and operating voltage increases, dv/dt increases, resulting in extremely high transient overvoltages, which may cause partial discharges in the power module, thereby deteriorating the packaging insulation performance of the power module. Previous studies have proposed a partial discharge detection method under a square wave electric field based on the super-high-frequency (SHF)-down-mixing technology [24,25].

In this paper, the SHF mixing method was used to measure the partial discharge characteristics of the SiC MOSFET half-bridge power module packaging insulation under a square wave electric field, as shown in Figure 15. The SHF sensor horn antenna is facing the sample at a 10 cm distance from the sample. Figure 16 shows the results of the partial discharge detection of the power module package insulation under the measured 1.2 kV square waves electric field.

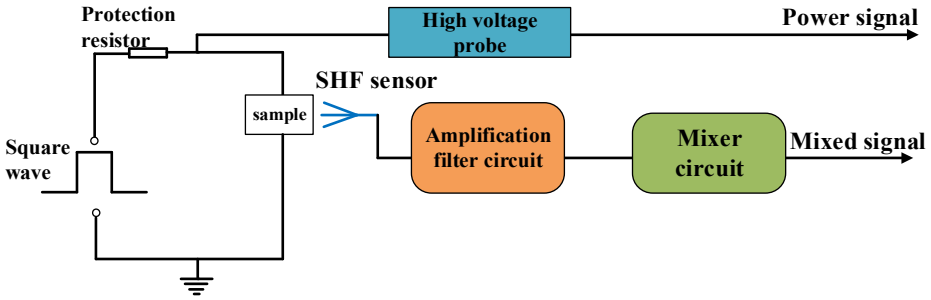

Figure 15. SHF partial discharge test system diagram.

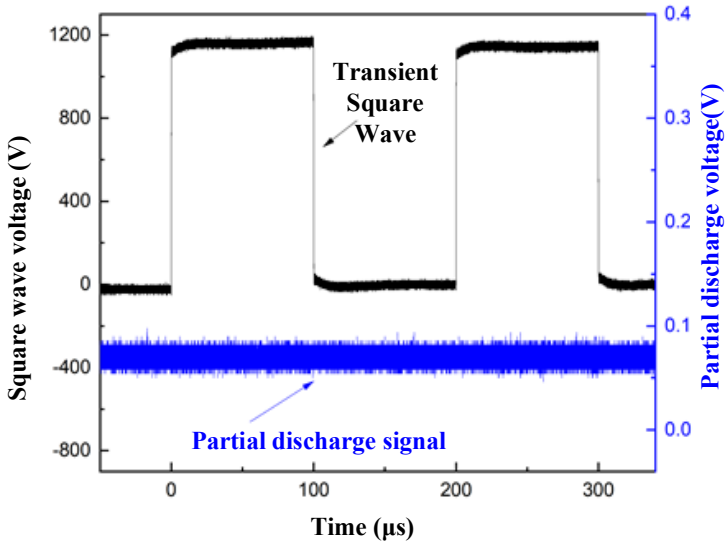

Figure 16. Partial discharge signal of power module under square waves with high dv/dt.

The results in Figure 16 show that no partial discharge signal is detected when the fabricated SiC MOSFET half-bridge power module operates at the rated square wave voltage with a fast-rising edge.

It should be noted that this paper aims to introduce a multi-physics design method for packaging insulation of SiC MOSFET modules. Due to the limited length of the paper, only the double pulse experiment (to show the dynamic performance) and partial discharge experiment (to verify the insulation performance) are presented. The continuous run experiment and thermal experiment will be performed and reported in the future.

6. Conclusions and Future Works

Aiming at solving the electrical–thermal–mechanical multi-stress problem of SiC MOSFET power module packaging insulation, this paper proposed an analyzing and optimized design method of three-dimensional electrical, thermal, and mechanical multi-physical field coupling of power module packaging insulation, which is based on Spice circuit, finite element field numerical calculation, and MOGWO optimization. Through the high field conductance characteristics of the packaging insulating substrate Al_2O_3 ceramic and encapsulation silicone at different temperatures, and the correlation between the power module loss and the packaging structure, the multi-physics numerical calculation of the packaging insulation of the 1.2 kV half-bridge SiC MOSFET power module was carried out. The effect of packaging structure parameters on the electric field, temperature, and mechanical stress of packaging insulation is studied. On this basis, the MOGWO algorithm was used to optimize the packaging structure parameters of the power module. According to the optimization results, a 1.2 kV half-bridge SiC MOSFET power module was fabricated and tested by experiments. The following conclusions can be drawn:

(1) Encapsulating silicone and Al_2O_3 ceramic substrate have different high field conductivity characteristics. Within the operating temperature range of the power module, the conductivity of the encapsulation silicone conforms to the hopping conductivity mechanism. The conductivity of the substrate Al_2O_3 ceramics varies with temperature and satisfies the Arrhenius relationship.

(2) The effect of the packaging structure parameters on the electric field, temperature, and mechanical stress in the packaging insulation is determined by a variety of factors. The maximum temperature in packaging insulation increases with solder thickness and decreases with copper pitch, width, and length. The maximum electric field in the packaging insulation first decreases and then increases with the copper trace spacing, which is positively related to the copper trace width and length. The maximum mechanical stress is inversely related to the copper trace spacing, width and length, and the thickness of the solder layer.

(3) The 1.2 kV half-bridge SiC MOSFET power module was fabricated with the optimized packaging parameters by the MOGWO algorithm and tested in comparison with a commercial module. The double-pulse test result shows that the switching loss of the fabricated power module is smaller than that of the commercial power module. The test results of the partial discharge experiment under square voltages with high dv/dt show that no partial discharge was detected during the operation of the power module, thus verifying the reliability of the packaging insulation of the fabricated SiC MOSFET half-bridge power module.

It should be noted that this paper just focuses on proposing the multi-physics simulation scheme and multi-objective optimization algorithm for the half-bridge SiC MOSFET power module. The research on other properties of the module and the inverter-level by integrating the modules will be investigated and reported in the future. Furthermore, this paper should also provide references for co-simulation and formal verification of power electronic systems in the future [26–28]. The proposed multi-physics simulation scheme and the optimization algorithm can also be applied to high-voltage power modules by identifying the packaging structure parameters and performing the multi-objective MOGWO optimization algorithm to determine the optimal structure parameters by trading off and obtaining the Pareto front [29].

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Conflicts of Interest: The authors declare no conflict of interest.

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