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An Overview about Si, Superjunction, SiC and GaN Power MOSFET Technologies in Power Electronics Applications

Edemar O. Prado [1,2,*], Pedro C. Bolsi [1,2], Hamiltom C. Sartori [2] and José R. Pinheiro [1,2]

1 Energy Efficiency Lab, LABEFEA, Federal University of Bahia, Salvador 40170-110, BA, Brazil; pcbolsi@gmail.com (P.C.B.); jrenes@gepoc.ufsm.br (J.R.P.)
2 Power Electronics and Control Research Group, GEPOC, Federal University of Santa Maria, Santa Maria 97105-900, RS, Brazil; hamiltomsar@gmail.com
* Correspondence: edemar.prado@ufba.br

Abstract: This work presents a comparative analysis among four power MOSFET technologies: conventional Silicon (Si), Superjunction (SJ), Silicon Carbide (SiC) and Gallium Nitride (GaN), indicating the voltage, current and frequency ranges of the best performance for each technology. For this, a database with 91 power MOSFETs from different manufacturers was built. MOSFET losses are related to individual characteristics of the technology: drain-source on-state resistance, input capacitance, Miller capacitance and internal gate resistance. The total losses are evaluated considering a drain-source voltage of 400 V, power levels from 1 kW to 16 kW (1 A–40 A) and frequencies from 1 kHz to 500 kHz. A methodology for selecting power MOSFETs in power electronics applications is also presented.

Keywords: comparative analysis; GaN; power MOSFET; power electronics; SiC

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1. Introduction

The increasing volumetric power density in static converters is a subject that has been highlighted in recent decades [1–7]. The expansion of the renewable energy and electric vehicle sectors increases the need for high power density and high performance in static converters [8–12]. Applications with higher switching frequencies are indicated as a possible way to reduce the volume of passive components. However, increasing switching frequency results in higher switching losses in power transistors, which may reduce the efficiency of converters and increase the volume and cost of heat transfer systems [13–16].

In order to reduce electrical losses, the industry began to develop power MOSFETs using different semiconductor structures and technologies, improving their performance at higher frequencies, powers and drain-source voltages [17–21]. For silicon-based devices, the structure was modified, resulting in the development of superjunction (SJ) devices. These devices present a significant reduction in the drain-source on-state resistance, shorter switching times and increases in the drain-source breakdown voltage capability [17,19,22–24].

The development of wide bandgap technologies, such as Silicon Carbide (SiC) and Gallium Nitride (GaN), also enable operation at higher frequencies [17–21,25]. Physical characteristics of SiC technology, such as high thermal conductivity, high electric field and wide energy gap, make its use attractive for applications where it is necessary to operate at higher temperatures, frequencies, powers and high drain-source voltages [18,26–29]. GaN technology has an electric field and energy gap similar to SiC devices, with greater electron mobility and lower thermal conductivity [26,28,30]. Electron mobility reduces switching times and output capacitance. For this reason, GaN technology tends to present an advantage in high-frequency operations. A lower thermal conductivity, on the other hand, provides disadvantages in situations where there is a need to operate at higher powers and temperatures [17,18,28,30–32].

In power electronics applications, a vertical MOSFET structure is preferable. This ensures uniform current distribution in the transistor. While GaN theoretically offers better high-frequency and high-voltage performances, the lack of good-quality bulk substrates required for vertical devices and the lower thermal conductivity of GaN give SiC the best position for high voltages. Because of this, some limitations in the vertical structures of the GaN FETs have been reported; although bearing the same previous FET structure, these devices have low blocking voltages (approximately 65 V), making their applications at higher powers unfeasible [20,21,26,31]. The GaN HEMT (high electron mobility transistor) with lateral structure is commonly used in this situation [20,21,31,32]. Although the GaN HEMT structure has a normally on behavior, several techniques have been developed to provide a modification in order to obtain a normally off behavior in the device, but intrinsic characteristics of the materials led to failures [32]. To easily apply GaN HEMT in circuit design, a low-voltage Silicon MOSFET is connected in series to provide normally off behavior. This structure is known as a cascode structure [20,21,31–33].

The development of power MOSFET technologies brings the challenge of defining which technologies and part numbers perform best in defined applications of drain-source voltage, current levels and switching frequencies. In the last decade, authors have analyzed the behavior of losses in different power MOSFET technologies [20,34–45]. Overall, losses were presented for specific operating points as in [34,36,37,40,42,43,45], specific part numbers [20,34,35,37–41] or for part numbers of different technologies and the same manufacturer [44].

In order to make a fair comparison among technologies, losses need to be estimated with accuracy. They may be calculated by analytical methods, SPICE, or finite element analysis (FEA) [16,46–49]. Due to its simplicity and processing time, the use of analytical models is preferable when reduced computational time is required [38,47,48,50]. In this work, the model proposed by [16] is used to estimate switching losses. Among the models [16,51–56], only [16,52] considered the internal gate resistance in loss calculation, while [16] also takes into account Miller capacitance variation and gate driver characteristics to determine overlap times. The DC link voltage used was 400 V. This voltage level is commonly used in literature for motor drive electric vehicle applications [11,57], in the design of step-up converters [3,13,58] and for microgrid applications [59–61].

Based on the outlined discussions, this paper presents four main contributions:

- A comparative analysis among four power MOSFET technologies: conventional Silicon (Si), Superjunction (SJ), Silicon Carbide (SiC) and Gallium Nitride (GaN) using a database with 91 part numbers from different manufacturers (Appendix A);
- A correlation of losses to physical characteristics of each technology, considering internal capacitances, internal gate resistances and drain-source on-state resistance as a function of junction temperature;
- A methodology for selecting power MOSFETs in power electronics applications;
- A definition of power and frequency ranges of the best performance for each technology, considering a drain-source voltage of 400 V, power levels from 1 kW to 16 kW (1 A–40 A) and frequency ranges from 1 kHz to 500 kHz.

2. Losses in Power MOSFETs

The equations of [16] are presented below and are used in the analysis presented in Section 4. The analytical model for obtaining the power dissipated during on-state period of MOSFETs (P_C) relates the square of RMS current with the on-state drain-to-source resistance (R_{DSon}), considering junction temperature (T_J) for a specific operation point:

$$P_C = R_{DSon(Tj)} I_{RMS}{}^2. \quad (1)$$

Switching losses are estimated by:

$$P_{SW} = \frac{1}{2}(t_{on} V_{DS} I_{on} + t_{off} V_{DS} I_{off}) F_{SW} \quad (2)$$

where F_{SW} is the switching frequency, V_{DS} is the drain-to-source voltage over the MOSFET and I_{on}, I_{off} and t_{on}, t_{off} are the respective currents and overlap times of MOSFET turn-on and turn-off.

Time periods t_{on} and t_{off} are determined as:

$$t_{on} = \frac{Q}{I_{Gon}} \tag{3}$$

$$t_{off} = \frac{Q}{I_{Goff}} \tag{4}$$

Q being the total charge, and I_{Gon} and I_{Goff} the gate currents at turn-on and turn-off:

$$I_{Gon} = (V_{GS} - V_{PL})/R_G \tag{5}$$

$$I_{Goff} = V_{PL}/R_G \tag{6}$$

in which V_{GS} and V_{PL} are the gate and plateau voltages, and R_G corresponds to the combination of external and internal gate resistances (R_G = R_{Gext} + R_{Gint}).

Q is given by the sum of gate-source and gate-drain charges, Q_{GS} and Q_{GD}:

$$Q = Q_{GS} + Q_{GD} \tag{7}$$

$$Q_{GS} = C_{ISS}(V_{PL} - V_{TH}) \tag{8}$$

$$Q_{GD} = \left(\frac{C_{GD(B)}V_{DS} + C_{GD(A)}0.135V_{DS}}{2} \right) \tag{9}$$

in which C_{ISS} is the input capacitance, and $C_{GD(A)}$ and $C_{GD(B)}$ are the gate-to-grain capacitances obtained at different points of the $C_{GD} \times V_{DS}$ curve, as explained in [16].

With these definitions, total losses are obtained by adding Equations (1) and (2):

$$P_{TOT} = P_C + P_{SW}. \tag{10}$$

3. Analytical Model Experimental Validation

The analytical model used as a basis for the comparative analysis is validated using the test circuit shown in Figure 1. It operates in steady-state and thermal equilibrium. This disregards the thermal transients of the MOSFET, and the temperature on the device may be considered uniform [62].

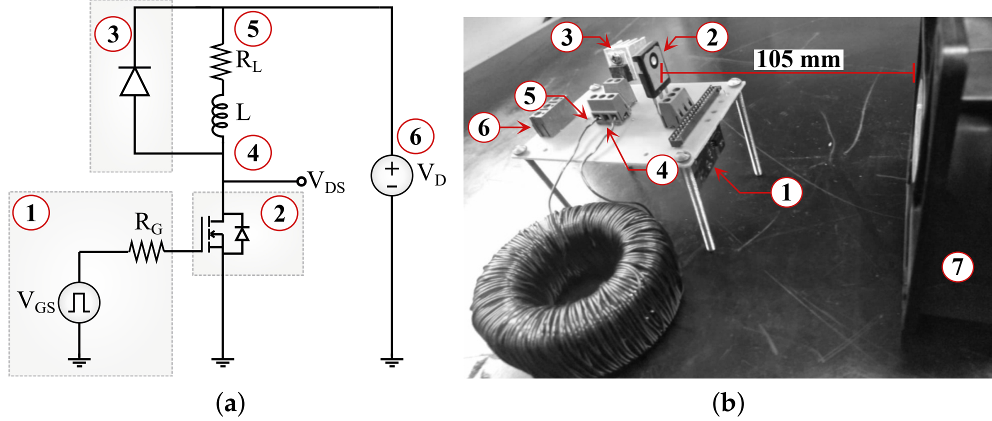

Figure 1. Test circuit: (**a**) diagram and (**b**) experimental setup; (1) Gate driver; (2) Device under test; (3) Diode with heat sink; (4) Inductor; (5) Resistive load (bottom side); (6) Adjustable voltage source V_D used to maintain V_{DS} constant; (7) Air cooler.

The tested MOSFETs were MTW20N50E (Si), IPW60R040C7 (SJ) and IMW65R072M1H (SiC). These were operated at voltages corresponding to 40%, 50% and 60% of each respec-

tive drain-source breakdown voltage (V_{DSb}). The switching frequencies used were 50 kHz and 150 kHz. Circuit parameters considered include: $R_G = 15\ \Omega$, $V_{GS} = 15$ V, $R_L = 70\ \Omega$ and $L = 1.7$ mH. In order to minimize the effects of reverse recovery, a freewheeling diode C3D10060A of SiC technology was used.

For temperature measurements, a Fluke Ti20 thermal camera was used. This thermal imaging device has a accuracy of ±2 °C or 2%, whichever is the highest [63]. The thermal camera emissivity was set to 0.9. Ambient temperature was constant for each test, and the laboratory environment was kept separate from external interference in temperature, such as wind or other nearby heat sources. Thermal results obtained in this evaluation are shown in Figure 2a–c for Si, SJ and SiC technologies, respectively, where the measured point is the package of MOSFET under test, and the scale of the thermal camera is adjusted automatically.

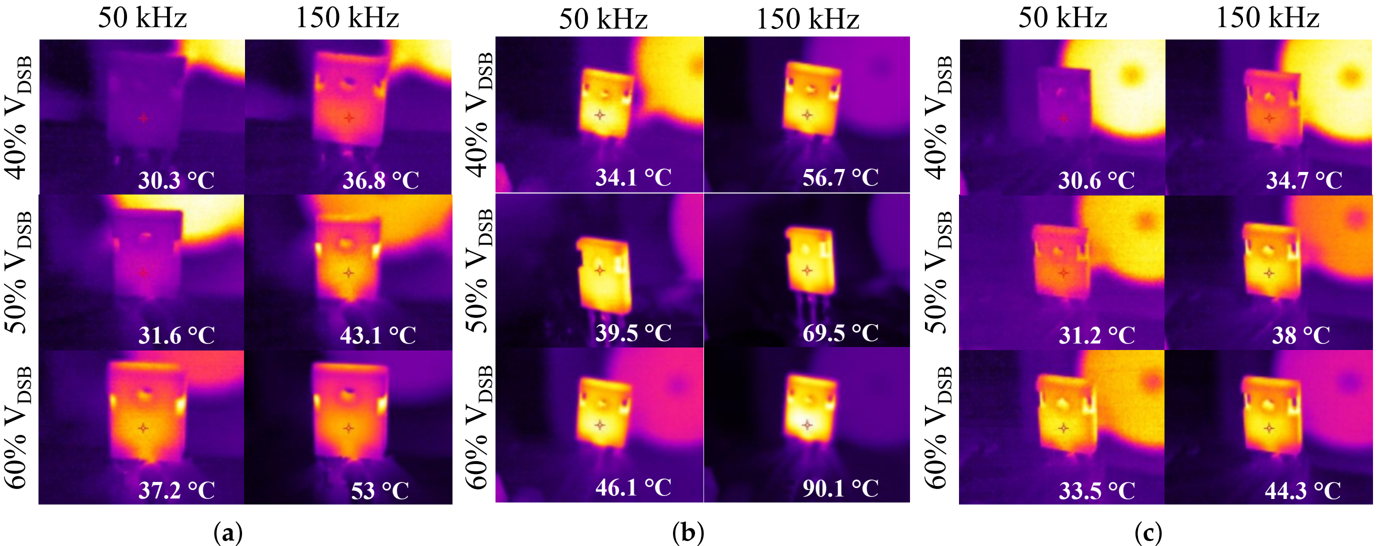

Figure 2. Measured temperatures for $F_{SW} = 50$ kHz and 150 kHz, $V_{DS} = 40\%$, 50% and 60% of V_{DSB}: (**a**) MTW20N50E, (**b**) IPW60R040C7 and (**c**) IMW65R072M1H.

From the temperature, total losses were obtained using the thermal resistances of each device. Using the data of $R_{\theta CA}$ from [16] and the measured ambient and case temperatures, losses can be found for each evaluated condition [62,64,65]:

$$P_{TOT} = \frac{T_C - T_A}{R_{\theta CA}}. \tag{11}$$

The comparison among measured and calculated losses and its associated error is shown in Table 1. The largest errors were 6.63% for Si technology, 5.65% for SJ technology and 6.9% for SiC technology. The results obtained validate the analytical model for each technology, in different voltage ratings and switching frequencies. The behavior of the Miller capacitance in GaN cascode devices is similar to the other technologies of power MOSFETs, presenting two different characteristics in the Miller capacitance curve shape. In low voltages there is a high variation of capacitance with voltage, and after that, a more linear behavior [16]. Based on this characteristic, the model represents switching losses accurately for GaN FETs as well.

Table 1. Comparison among measured and calculated losses.

	MTW20N50E								
	40%V_{DS}			**50%V_{DS}**			**60%V_{DS}**		
	Meas.	**Calc.**	**Error**	**Meas.**	**Calc.**	**Error**	**Meas.**	**Calc.**	**Error**
50 kHz	0.56	0.58	3.45%	0.86	0.92	6.52%	1.41	1.40	0.71%
150 kHz	1.43	1.41	1.42%	2.29	2.16	6.02%	3.70	3.47	6.63%
	IPW60R040C7								
50 kHz	0.50	0.51	1.96%	0.80	0.84	4.76%	1.17	1.24	5.65%
150 kHz	1.75	1.66	5.42%	2.46	2.33	5.58%	3.59	3.48	3.16%
	IMW65R072M1H								
50 kHz	0.35	0.33	6.06%	0.39	0.38	2.63%	0.54	0.58	6.90%
150 kHz	0.62	0.59	5.08%	0.82	0.83	1.20%	1.22	1.29	5.43%

4. Impact of Internal Parameters on MOSFET Losses

4.1. Conduction Loss Evaluation

As shown in Section 2, conduction losses in power MOSFETs are a function of R_{DSon} (dependent on T_J) and the RMS current. The flowchart in Figure 3 shows the methodology used to evaluate conduction losses, summarized in 5 steps:

- Step 1: The initial RMS current of 1 A and T_J of 25 °C and 125 °C are defined.
- Step 2: The algorithm searches the database, selecting transistors that meet the current capacity criteria for the specified current.
- Step 3: The losses are calculated by Equation (1).
- Step 4: In each current iteration, the part number that presents the lowest losses for each technology is selected. This procedure is executed in steps of 1 A until the RMS current reaches 100 A. Thus, it is possible to select different part numbers for the same technology along the current range.
- Step 5: As the output, the behavior of the conduction losses with current variation is obtained.

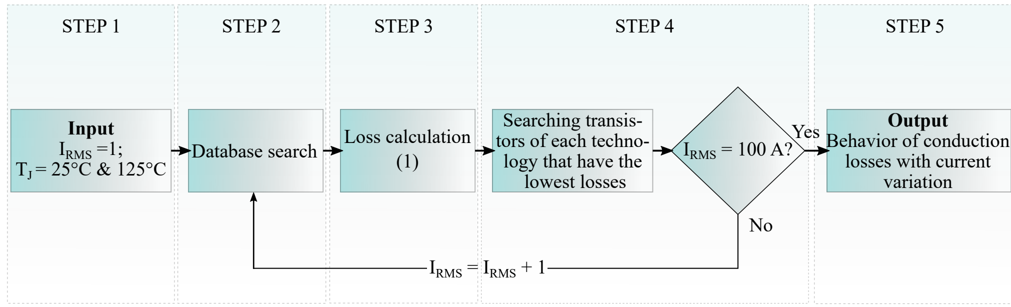

Figure 3. Flowchart: methodology for the selection of the MOSFET with lowest conduction losses for each technology.

In addition to T_J, V_{GS} has also a direct impact on R_{DSon}. Therefore, R_{DSon} is adjusted according to the applied gate voltage, following the electrical characteristics diagrams from each MOSFET datasheet. In order to operate all technologies close to saturation region, the gate voltage used was 18 V.

The results are shown in Figure 4, where solid lines represent the conduction losses at $T_J = 25$ °C and dashed lines represent the losses calculated for $T_J = 125$ °C; line colors identify each technology.

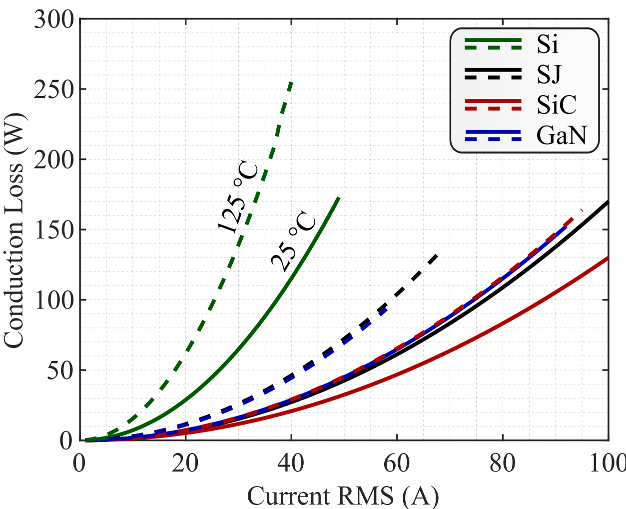

Figure 4. Conduction loss as a function of I_{RMS}.

For conduction losses in 25 °C, SiC, SJ and GaN technologies present similar losses up to the range of $I_{RMS} = 20$ A, above this value, SiC technology presents the best performance. GaN and SJ technologies presents similar losses, but higher than SiC, with the maximum rated RMS current for GaN technology being 91 A. Silicon MOSFETs present the highest losses (highest R_{DSon}), and their rated RMS current is limited to 49 A. As the temperature is increased from 25 °C to 125 °C, SiC presented the lowest losses compared to other technologies in the RMS current range above 20 A. The Si rated RMS current is limited to 40 A, GaN to 58 A, SJ to 68 A and SiC to 95 A. The rated current limits are obtained from the database presented in Appendix A.

To visualize the impact of T_J variation on R_{DSon}, in Figure 5 the averages of normalized values of R_{DSon} for each technology are shown ($R_{DSon(Norm)} = R_{DSon(Tj)}/R_{DSon(25)}$). These values are obtained by running temperature scans for all transistors in the database and averaging them for each technology. The increase in normalized values of R_{DSon} is the lowest in SiC when compared to the other technologies (around 50%). The largest variation in $R_{DSon(Norm)}$ occurs in the Si MOSFET, with an increase of 160% when varying T_J from 25 °C to 150 °C. The SJ and GaN technologies increase by about 100%. The increase in R_{DSon} by T_J variation has a significant impact on the transistor losses, as shown in Figure 4; thus, it may not be disregarded.

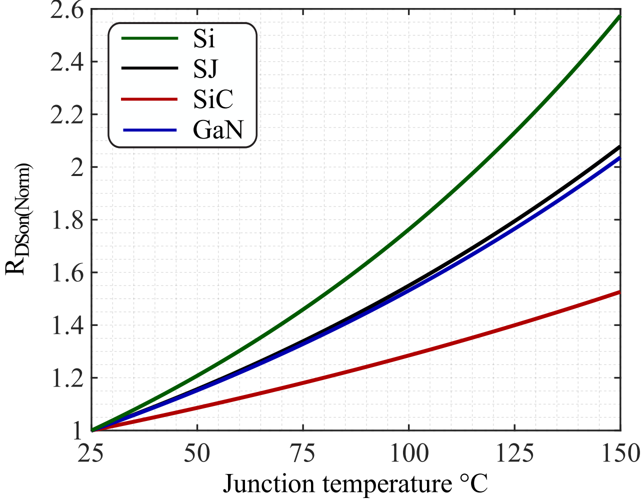

Figure 5. R_{DSon} normalized for each technology × T_J.

4.2. Switching Loss Evaluation

Switching losses are determined as defined in Section 2, being a function of R_{Gext}, V_{GS}, I_{on}, I_{off}, C_{ISS}, C_{GD}, V_{PL}, V_{TH}, R_{Gint}, V_{DS} and F_{SW}. Gate driver parameters (V_{GS} and R_{Gext}) determine the charging and discharging of a transistor's internal capacitances. From the internal parameters, C_{ISS} is responsible for the rise and fall times of the current, while C_{GD} is responsible for the rise and fall times of the voltage, which are significantly smaller than C_{ISS} and highly nonlinear. V_{PL} is the voltage at which C_{GD} starts charging and also represents the end of gate-source charging. V_{TH} is the voltage at which MOSFET enters the on-state region, and R_{Gint} is the internal gate resistance of the MOSFET. When MOSFETs are manufactured for different drain-source voltage ratings or different current levels, its characteristics are modified.

To determine the influence of the internal parameters on switching losses and to define application trends, two scenarios (evaluations) are considered. In the first scenario, (Section 4.2.1) the internal gate resistance R_{Gint} is disregarded, with the goal of demonstrating the impact of the internal capacitances in switching losses. In the second scenario (Section 4.2.2), results are obtained with R_{Gint} included. The external parameters to determine losses were considered as $V_{DS} = 400$ V, $R_{Gext} = 15\ \Omega$, $V_{GS} = 18$ V, average currents of 2.5 to 80 A and frequency range of 1 kHz to 500 kHz, as shown in the flowchart of Figure 6. The switching loss evaluation is summarized in 5 steps:

- Step 1: Input parameters are set as $I_{SW} = I_{on} = I_{off} = 2.5$ A, $V_{DS} = 400$ V and starting frequency = 1 kHz.
- Step 2: The algorithm searches the database, selecting transistors that meet the current and voltage criteria.
- Step 3: The losses are calculated by Equation (2).
- Step 4: Only the transistor of each technology that presents lowest losses (for a set of parameters) is selected. Step 4 is performed in steps of 1 kHz until the switching frequency reaches 500 kHz, for current levels of 2.5 A until 80 A. The current loop is doubled in each iteration. It is possible to select different part numbers for the same technology along the frequency and current ranges.
- Step 5: As the output, the behavior of losses with variations in the switching frequency and current levels in scenario 1 (without including R_{Gint}) and scenario 2 (using R_{Gint}) are obtained.

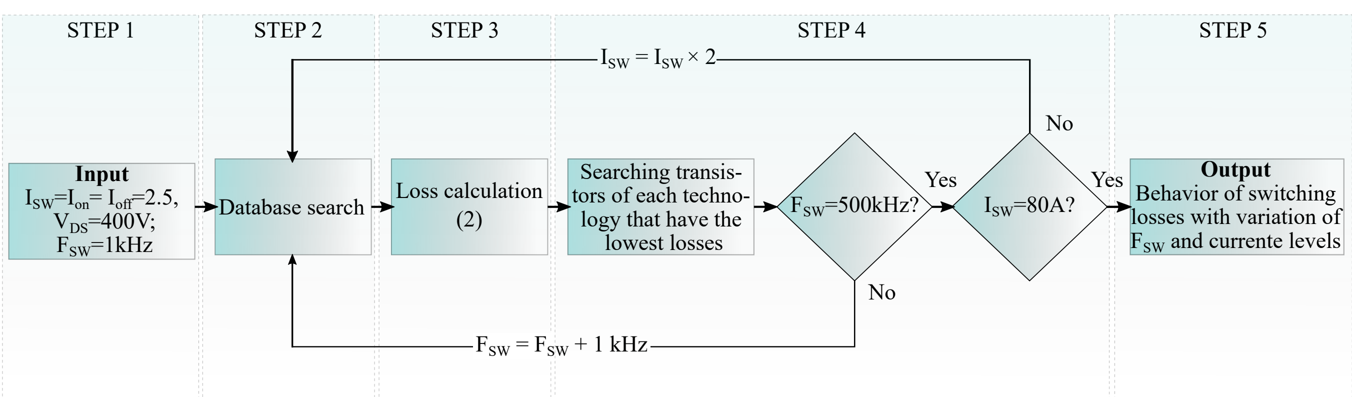

Figure 6. Flowchart: methodology for the selection of the MOSFET with lowest switching losses for each technology.

4.2.1. Scenario 1: Influence of Internal Capacitances

The results obtained for scenario 1 are shown in Figure 7 (a) for 2.5 A, (b) 5 A, (c) 10 A, (d) 20 A, (e) 40 A and (f) 80 A. In this analysis, the numerical behavior of the losses was evaluated. It disregards the junction temperature, considering only both V_{DSb} and current capability.

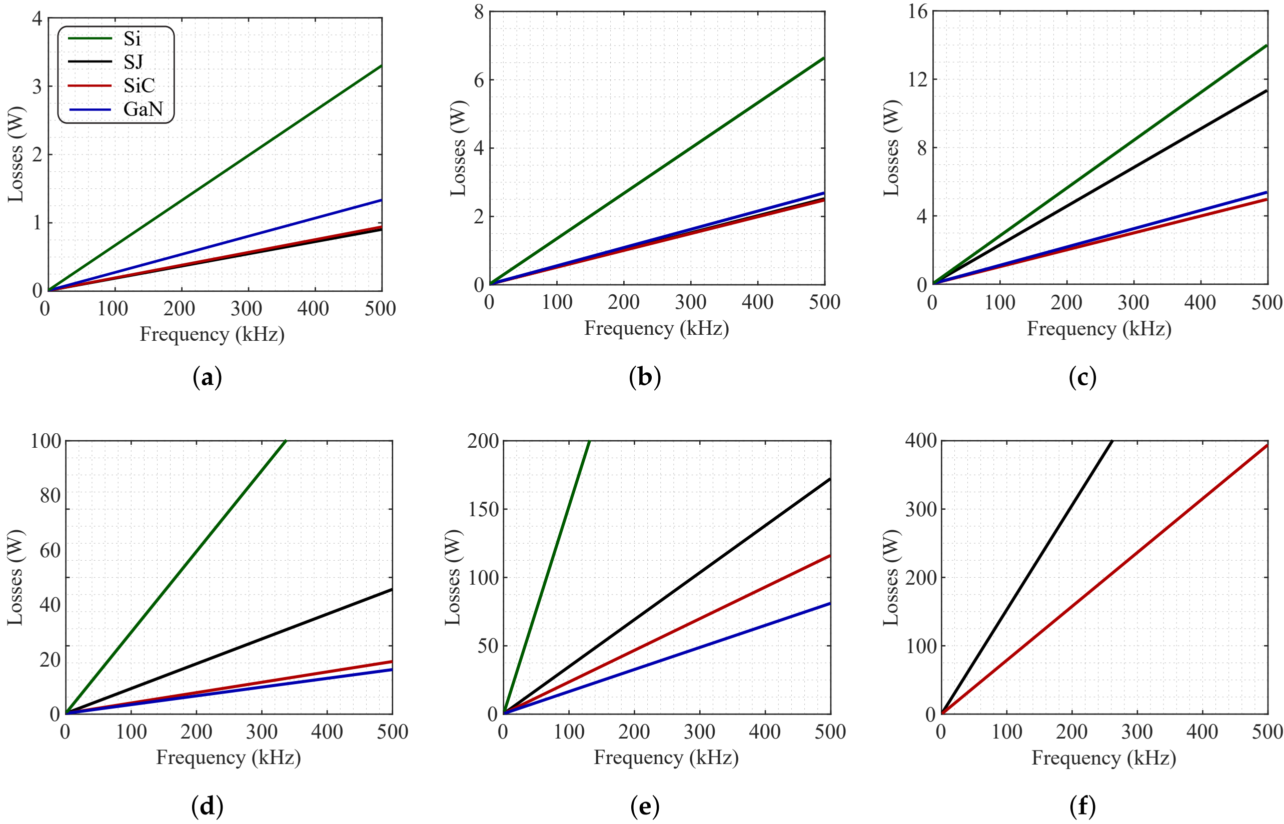

Figure 7. Switching losses: (**a**) 2.5 A, (**b**) 5 A, (**c**) 10 A, (**d**) 20 A, (**e**) 40 A and (**f**) 80 A.

Figure 7a shows a loss comparison considering $V_{DS} = 400$ V and a current of 2.5 A. In this range, SJ MOSFET presented the lowest switching losses, followed by SiC and GaN. In Figure 7b, the SiC, SJ and GaN MOSFETs present the lowest switching losses, while the Si MOSFET has the highest losses. In Figure 7c, GaN presents the best performance, as well as in Figures 7d,e. In Figure 7f, only the SJ and SiC transistors met the current capacity criteria, and SiC presents the lowest losses. The part numbers that minimize switching losses for each current level, frequency and technology are shown in Table 2.

Table 2. Part numbers that were selected by the algorithm in order to minimize switching losses.

I (A)	SJ	SiC	GaN	Si
2.5	IPU95R2K0P7	IMW120R350M1H	TP65H150G4PS	IXFP20N50P3M
5	IPA95R1K2P7	C3M0280090J	TP65H150G4PS	IXFP20N50P3M
10	IPA95R450P7	IMW120R220M1H	TP65H150G4PS	IXFH16N50P3
20	IPZ65R095C7	C3M0120100K	TP65H070L	IXFR64N50P
40	IPP60R040C7	SCT4026DE	TP65H035WSQA	IXFR80N50Q3
80	IPZ60R017C7	SCT4013DR	–	–

The behavior of losses for the selected power MOSFETs is related to the internal parameters of each part number and technology. Tables 3–6 show the characteristics of R_{DSon} at 25 °C, C_{ISS} and C_{GD}, for SJ, SiC, GaN and Si technologies, respectively, considering a drain-source voltage of 400 V.

Table 3. Characteristics of selected SJ MOSFETs.

I (A)	Part Number	C_{ISS} (pF)	$C_{GD(VDS)}$ (pF)	$R_{DSon(25)}$ (Ω)
2.5	IPU95R2K0P7	330	1.6	2
5	IPA95R1K2P7	478	2.1	1.2
10	IPA95R450P7	1053	5	0.45
20	IPZ65R095C7	2140	8	0.095
40	IPP60R040C7	4340	19	0.04
80	IPZ60R017C7	9890	40	0.017

Table 4. Characteristics of selected SiC MOSFETs.

I (A)	Part Number	C_{ISS} (pF)	$C_{GD(VDS)}$ (pF)	$R_{DSon(25)}$ (Ω)
2.5	IMW120R350M1H	182	1	0.35
5	C3M0280090J	150	2	0.28
10	IMW120R220M1H	289	2	0.22
20	C3M0120100K	350	3	0.12
40	SCT4026DE	2320	9	0.026
80	SCT4013DR	4580	10	0.013

Table 5. Characteristics of selected GaN MOSFETs.

I (A)	Part Number	C_{ISS} (pF)	$C_{GD(VDS)}$ (pF)	$R_{DSon(25)}$ (Ω)
2.5	TP65H150G4PS	307	1	0.15
5	TP65H150G4PS	307	1	0.15
10	TP65H150G4PS	307	1	0.15
20	TP65H070L	600	4	0.072
40	TP65H035WSQA	1500	14	0.035
80	–	–	–	–

Table 6. Characteristics of selected Si MOSFETs.

I (A)	Part Number	C_{ISS} (pF)	$C_{GD(VDS)}$ (pF)	$R_{DSon(25)}$ (Ω)
2.5	IXFP20N50P3M	1800	7	0.3
5	IXFP20N50P3M	1800	7	0.3
10	IXFH16N50P3	1515	7	0.3
20	IXFR64N50P	9700	30	0.095
40	IXFR80N50Q3	10,000	115	0.05
80	–	–	–	–

In Tables 3–6, it is possible to identify that in all cases, as the current levels increase, C_{ISS} and $C_{GD(VDS)}$ also increase, while $R_{DSon(25)}$ decreases. This occurs because, at higher current levels, to reduce R_{DSon}, manufacturers increase the carrier density and die size, which, as a consequence, increases the internal capacitances. Otherwise, at lower current levels, the die size is smaller, reducing the internal capacitances and increasing R_{DSon}.

4.2.2. Scenario 2: Influence of R_{Gint}

Figure 8 shows the switching losses with R_{Gint} included for currents of 5, 20 and 80 A (Figures 8a–c respectively). Solid lines represent losses without considering R_{Gint}, and dashed lines show losses considering R_{Gint}. Line colors identify the different technologies. In Figure 8, the arrows indicate the increase in switching losses resulting from the inclusion of R_{Gint}. SiC technology presents the greatest increase in losses. To highlight the characteristics that led to these results, selected part numbers and their respective R_{Gint} are shown in Table 7.

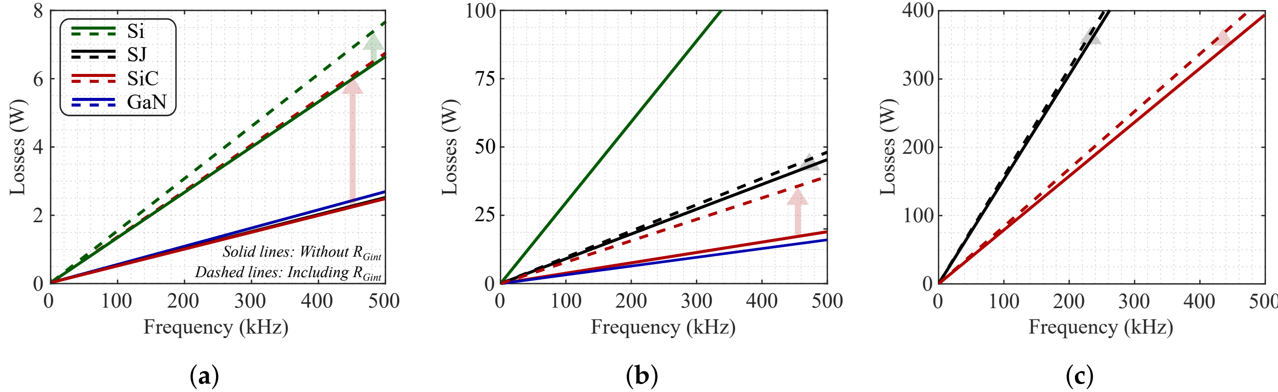

Figure 8. Switching losses evaluation: (**a**) 5 A, (**b**) 20 A and (**c**) 80 A.

Table 7. Internal gate resistance for selected MOSFETs.

I (A)	Part Number	Technology	R_{Gint} (Ω)
5	IPA95R1K2P7	SJ	1
20	IPZ65R095C7	SJ	0.9
80	IPZ60R017C7	SJ	0.45
5	C3M0280090J	SiC	26
20	C3M0120100K	SiC	9
80	SCT4013DR	SiC	1
5	TP65H150G4PS	GaN	–
20	TP65HO70L	GaN	–
80	–	–	–
5	IXFP20N50P3M	Si	2.3
20	IXFR64N50P	Si	–
80	–	–	–

Table 7 shows that the SiC MOSFETs have the highest R_{Gint}. This results in longer overlap times and increasing switching losses, as shown in Figure 8. The physical characteristics of SiC MOSFETs make their die sizes smaller when compared to other MOSFET technologies. The R_{Gint} value is inversely proportional to the die size, so that the R_{Gint} is higher for SiC devices. As the current level increase, the die size of the MOSFETs increase, and R_{Gint} is reduced. For Si MOSFETs, R_{Gint} is small because of their relatively larger die sizes. As the rated current levels increase, the die sizes increase further, making R_{Gint} smaller; thus, it is sometimes not provided in the datasheet. For GaN MOSFETs, the cascode structure makes R_{Gint} negligible, and thus it is also not provided on the datasheet. In the cases where R_{Gint} is not provided, it was not considered. Nevertheless, it is shown that in some cases, R_{Gint} may be very influencing in switching losses and may not be disregarded.

4.3. Total Losses Evaluation

The analysis used to determine total losses may be described according to flowchart shown in Figure 9 and its respective operating steps. The external parameters to determine losses were considered as V_{DS} = 400 V, R_{Gext} = 15 Ω, V_{GS} = 18 V, power levels of 1 kW to 16 kW and frequency range of 1 kHz to 500 kHz. Current ripple was considered as 30% peak-to-peak with duty cycle of 50%.

- Step 1: The input parameters are set as $F_{SW} = 1$ kHz, $T_J = 125$ °C and power level of 1 kW, which corresponds to an average current of 2.5 A.
- Step 2: The algorithm searches the database, selecting transistors that meet the current and voltage criteria.
- Step 3: The total losses are calculated by Equation (10).

- Step 4: Only the transistor of each technology that presents lowest losses (for a set of current and voltage) is selected. This procedure is performed in steps of 1 kHz for all power levels under analysis, until the switching frequency reaches 500 kHz, for power levels of 1 kW until 16 kW. The power loop is doubled in each iteration. It is possible to select different part numbers in each iteration.
- Step 5: As the output, the behavior of total losses as a function of the switching frequency and current/power levels are obtained.

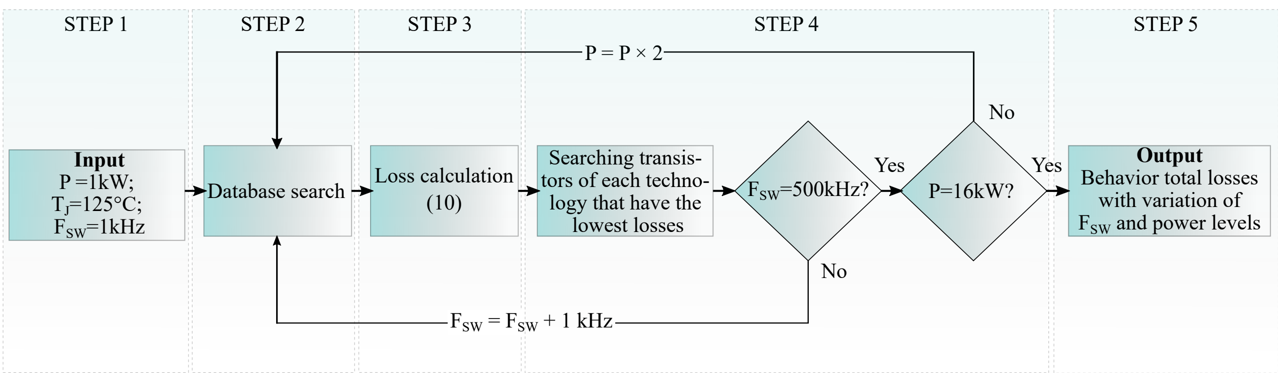

Figure 9. Flowchart: methodology for the selection of the MOSFET with lowest total losses for each technology.

Figure 10 shows the results of the methodology described in Figure 9. It is worth mentioning that the algorithm selects transistors at each frequency step, scanning for the optimal relationship between conduction and switching losses. In manufacturer datasheets, the maximum power dissipation (P_{MAX}) is given for a temperature of 150 °C. In this paper, P_{MAX} for the results shown in Figure 10 was defined so that the junction temperature does not exceed 125 °C in order to ensure a safety margin:

$$P_{MAX} = \frac{T_J - T_C}{R_{\theta JA}} = \frac{125 - T_C}{R_{\theta JA}} \tag{12}$$

where the case temperature (T_C) must be equal to ambient temperature (25 °C). The junction-ambient thermal resistance ($R_{\theta JA}$) is assumed to be close to the junction-case thermal resistance for each part number under analysis ($R_{\theta JC(\#)}$):

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \approx R_{\theta JC(\#)} \tag{13}$$

where $R_{\theta CS}$ and $R_{\theta SA}$ are the case-sink and sink-ambient thermal resistances, respectively. Thus, P_{MAX} is found for each part number ($P_{MAX(\#)}$):

$$P_{MAX(\#)} = \frac{T_J - T_C}{R_{\theta JA}} = \frac{125 - 25}{R_{\theta JC(\#)}}. \tag{14}$$

In Figure 10a, with 1 kW and an average current of 2.5 A, the SiC technology presented the best performance in the frequency range up to 9 kHz (represented by the red gradient). The GaN technology performed best from 9 kHz to 500 kHz (represented by the blue gradient). In Figure 10b, with 2 kW and 5 A, the results are similar to those of Figure 10a, with SiC presenting the best performance from 1 kHz to 17 kHz and GaN with the best performance in the remaining frequency range (17 kHz–500 kHz). In Figure 10c (4 kW and 10 A), the SiC technology expands its area of best performance to 34 kHz. Above this frequency, GaN performs better. In Figure 10d (8 kW and 20 A) the SiC technology again increases its range of best performance, reaching 68 kHz.

In Figure 10e, with 16 kW, only the SiC, SJ and GaN technologies fit the current criteria (40 A average current and 46 A peak). The SiC technology has the best performance across

the entire frequency range. In this case, the maximum switching frequency (which does not exceed power dissipation limits) is 400 kHz for SJ technology and 97 kHz for GaN technology. The SiC technology had no operating range limitations.

The best performance ranges for the evaluated powers and frequencies are summarized in Table 8 for its respectively technologies. It is possible to observe the trends in the applications of SiC technologies at higher powers, as the best performance range of the technology gradually increases with the levels of the current in the transistor, and of the GaN technology at higher switching frequencies and lower power levels.

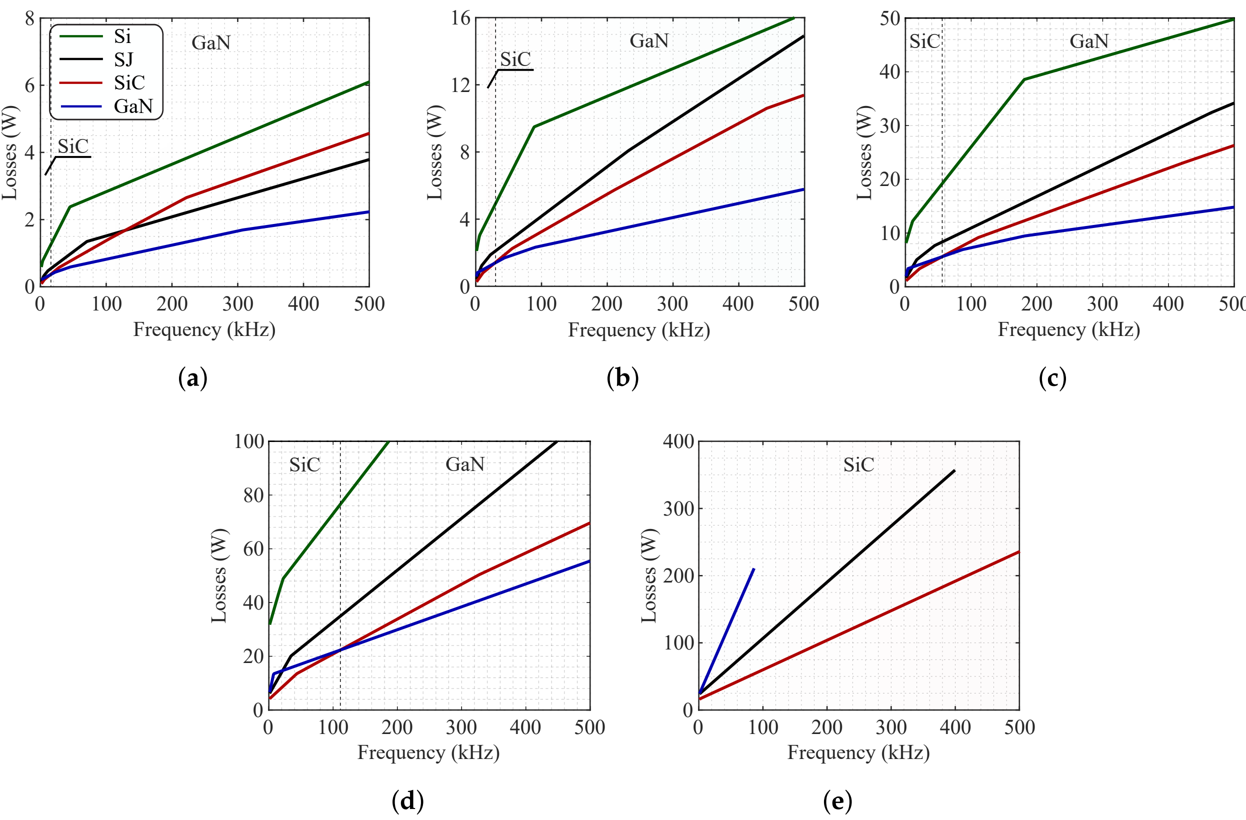

Figure 10. Total losses: (**a**) 1 kW, (**b**) 2 kW, (**c**) 4 kW, (**d**) 8 kW and (**e**) 16 kW.

Table 8. Best performance ranges for the evaluated powers and frequencies.

P (kW)	SiC	GaN	SJ	Si
1	Up to 14 kHz	14–500 kHz	–	–
2	Up to 28 kHz	28–500 kHz	–	–
4	Up to 55 kHz	55–500 kHz	–	–
8	Up to 110 kHz	110–500 kHz	–	–
16	1–500 kHz	–	–	–

In Figure 10, it is possible to identify similar results among the SiC, SJ and GaN technologies at some frequencies and power levels. At 1 kW, the SiC and SJ technologies have presented similar losses across the entire frequency range evaluated, and at 128 kHz, SJ was superior to the SiC technology. At 2 kW and 4 kW, losses among the SiC and SJ technologies were close to each other across the entire frequency range. At 8 kW, the SJ technology was superior to the GaN technology in the frequency range up to 15 kHz. For 16 kW, the SiC technology presents the best performance across the entire frequency range, followed by the SJ technology.

For the same current rating, the average cost ratio for the SJ technology is about three times that of a Si device, while SiC and GaN semiconductors cost up to six times more. For applications where the performances of the SiC, GaN and SJ technologies are similar, the cost factor has a significant impact, making SJ a replacement alternative to wide bandgap MOSFETs.

Based on this, the results presented in this section were compiled in Figure 11, where application trends for the SiC, SJ and GaN technologies are shown. For the frequency range of up to 200 kHz and power up to 8 kW, the use of SiC, GaN or SJ technology is recommended, leaving the designer to determine their own objective function for performance or cost. In applications with powers from 8 to 16 kW and frequencies up to around 200 kHz, only the use of SiC and SJ technologies is recommended, due to the lower performance of GaN MOSFETs in this power and frequency range. Above 200 kHz and above 8 kW, the use of SiC technology is recommended. Below 8 kW and at frequencies higher than 200 kHz, the use of GaN MOSFET technology is recommended.

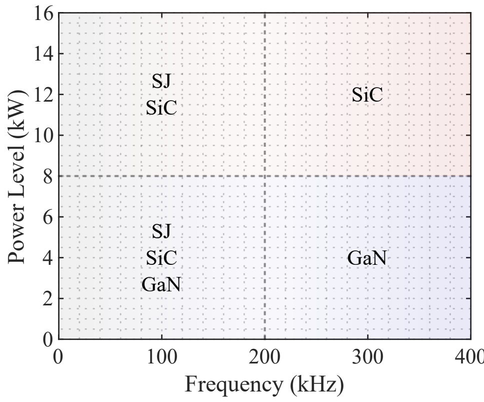

Figure 11. Application trends for SiC, SJ and GaN technologies.

It is worth mentioning that this graph shows trends, and when carrying out a particular design, all of the issues addressed in this paper must be taken into account, since these technologies are under constant development, and the cost ratio may change according to market conditions.

5. Conclusions

In this paper, the characteristics of SiC, GaN, SJ and Si MOSFETs were analyzed. A database of 91 power MOSFETs was used. Parametric evaluations of the $R_{DSon} \times T_J$ behavior for each technology were performed. The Si MOSFET showed the largest increase in the averages of the normalized values of R_{DSon} (160%) when T_J increased from 25 °C to 150 °C. In the SJ and GaN technologies, the increase was about 100%, and in the SiC MOSFETs the increase was about 50%. The increase in R_{DSon} by T_J variation has a significant impact on transistor conduction losses, as shown in Figure 4. This behavior results in advantages for SiC technologies at higher temperatures and current levels over the MOSFET.

The switching losses evaluation demonstrated the impact of constructive characteristics of MOSFETs, as shown in Tables 3–6. As current levels increase, capacitances also increase (C_{ISS} and $C_{GD(VDS)}$), and the $R_{DSon(25)}$ decreases for all technologies. When R_{Gint} was included (Figure 8 and Table 7), the SiC technology showed the greatest increase in switching losses due to the high R_{Gint} of this structure.

In Figure 10 and Table 8, the SiC technology was the best at higher powers, as the best performance range of the technology gradually increases with the levels of the current in the transistor. The GaN technology was the best at higher switching frequencies and lower power levels. The application trend ranges for the SiC, GaN and SJ technologies were shown in Figure 11. In the range up to 200 kHz and up to 8 kW, the use of SiC, GaN

or SJ technology is recommended, leaving the designer to determine the objective function for performance or cost. In applications with powers from 8 to 16 kW and frequencies up to around 200 kHz, only the use of SiC and SJ technologies are recommended, due to the worse performance of GaN MOSFETs in this power and frequency range. Above 200 kHz and above 8 kW, the use of SiC technology is recommended. Below 8 kW and at frequencies higher than 200 KHz, the use of GaN MOSFET technology is recommended.

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Appendix A

Part numbers in the database are listed: (1) AIMW120R045M1, (2) AIMW120R080M1, (3) APT70SM70B, (4) C2M0025120D, (5) C2M0045170D, (6) C2M0080170P, (7) C2M0160120D, (8) C2M0280120D, (9) C3M0015065D, (10) C3M0015065K, (11) C3M0016120K, (12) C3M0021120D, (13) C3M0030090K, (14) C3M0060065D, (15) C3M0060065J, (16) C3M0060065K, (17) C3M0065090, (18) C3M0065090D, (19) C3M0075120K, (20) C3M0120100K, (21) C3M0280090J, (22) IMW120R030M1H, (23) IMW120R045M1, (24) IMW120R060M1H, (25) IMW120R060M1H, (26) IMW120R140M1H, (27) IMW120R220M1H, (28) IMW120R350M1H, (29) IMW65R107M1H, (30) IMZ120R045M1, (31) IMZ120 R090M1H, (32) IPA60R180C7, (33) IPA65R045C7, (34) IPA65R065C7, (35) IPA65R095C7, (36) IPA80R 460CE, (37) IPA95R1K2P7, (38) IPA95R450P7, (39) IPA95R750P7, (40) IPB60R060C7, (41) IPP60R040C7, (42) IPU95R2K0P7, (43) IPU95R3K7P7, (44) IPU95R750P7, (45) IPW60R037C6, (46) IPW60R045CP, (47) IPW60R070P6, (48) IPW60R280P6, (49) IPW65R065C7, (50) IPW65R080CFD, (51) IPZ60R017C7, (52) IPZ65R019C7, (53) IPZ65R095C7, (54) IXFH16N50P3, (55) IXFP20N50P3M, (56) IXFR20N80P, (57) IXFR36N60P, (58) IXFR44N50Q3, (59) IXFR64N50P, (60) IXFR80N50P, (61) IXFR80N50Q3, (62) NTP8G202N, (63) NTP8G206N, (64) PU95R450P7, (65) SCT10N120, (66) SCT20N120, (67) SCT2120AF, (68) SCT3017AL, (69) SCT3022AL, (70) SCT3030AL, (71) SCT3060AL, (72) SCT3080AL, (73) SCT3120AL, (74) SCT4013DR, (75) SCT4018KR, (76) SCT4026DE, (77) SCT4045DE, (78) SCT4062KE, (79) TP65H015 G5WS, (80) TP65H035WS, (81) TP65H035WSQA, (82) TP65H050WS, (83) TP65H070L, (84) TP65H150 G4PS, (85) TP65H150LSG, (86) TP90H050WS, (87) TP90H180PS, (88) TPH3205WSBQA, (89) TPH3206 PSB, (90) TPH3208PS, (91) TPH3212PS.

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