energies

MDPI

Article

An Improved Down-Scale Evaluation System for Capacitors Utilized in High-Power Three-Phase Inverters under Balanced and Unbalanced Load Conditions

Yi-Hung Liao * and Yen-Lun Lin

Department of Electrical Engineering, National Central University, Taoyuan City 320, Taiwan
* Correspondence: yhungliao@ee.ncu.edu.tw; Tel.: +886-3-4227151 (ext. 35153)

Abstract: The DC-link capacitors in an electronic power system are the main constraint of the power density and lifespan of the power converters. Evaluating the load life of capacitors working in severely adverse circumstances plays an important role in the design stages of the next-generation power converters. In this article, an improved evaluation system for the capacitors utilized in high-power three-phase voltage source inverters is proposed. The purpose of this article is to reproduce the same encountered stresses when a DC-link capacitor is used in a high-power inverter with pulse-width modulation. Hence, an improved down-scale evaluation system for the DC-link capacitors used in high-power three-phase inverter systems under balanced and unbalanced load conditions is proposed. Moreover, AC and DC analyses in the proposed evaluation system are conducted. The equivalent circuit and transfer functions are derived to verify the proposed evaluation system. Finally, a prototype system is constructed to facilitate the theoretical results as the verification.

Keywords: DC-link capacitors; three-phase inverters; down-scale evaluation system; unbalanced load condition; life of capacitors

check for updates

Citation: Liao, Y.-H.; Lin, Y.-L. An Improved Down-Scale Evaluation System for Capacitors Utilized in High-Power Three-Phase Inverters under Balanced and Unbalanced Load Conditions. *Energies* **2022**, *15*, 6937. https://doi.org/10.3390/en15196937

Academic Editor: Abu-Siada Ahmed

Received: 1 August 2022
Accepted: 19 September 2022
Published: 22 September 2022

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

Due to the development of renewable energy, more and more high-power and high-density inverters are being manufactured for PVs, wind power systems and fuel cells, etc. Therefore, the system testing for high-power and high-density inverters becomes very important, especially in the limited power-rating testing field. Although the International Electrotechnical Commission (IEC) has established some testing standards for distributed systems, such as IEC 60364-7-712:2017 [1] and IEC 61000-3-3:2013 + AMD1:2017 + AMD2:2021 [2], and IEC/TS 61000-3-4 [3], etc., there still exist some issues in the testing field. If the power capacity of the testing field is smaller than that of the equipment under test (EUT), the high-power EUT cannot be tested under a full-scale power rating. Hence, some evaluation circuits and/or evaluation methods [4–11] for high-power converters were proposed. They are intended to reproduce the same encountered stresses for any components of high-power converters. However, the main constraint of the power density and lifespan of power converters is the DC-link capacitor. Generally, the life cycle of capacitors is usually shorter than that of the magnetic components and semiconductor devices. Therefore, evaluating the load life of capacitors working in severely adverse circumstances plays an important role in the design stages of the next-generation power converters, especially in the evaluation of the capacitors in terms of the power loss, ageing, and failure rate.

Nevertheless, in the past decades, only a single sinusoidal current was used to evaluate the quality of capacitors, such as 120 Hz and 1 kHz [4]. In addition, a ripple current tester and a DC bias are used to test the capacitors [5,12]. However, the current that flows from the converter to the capacitors (EUT) contains multiple frequency components. Although the frequency components can be correctly analyzed, it should be noted that the power loss

of capacitors with respect to frequencies is a non-linear characteristic [6–8,13]. In order to understand the aging characteristics, it is necessary to monitor the aging parameters of the capacitor under test in the actual scenario. Generally, there are three kinds of estimation methods, i.e., offline, quasi-online, and online methods. A quasi-online method was proposed in [14], where a specific switch is used to stop the inverter and an LC resonant network is introduced. The DC-link capacitor value is estimated by analyzing the collected current data. However, this method requires additional control design, which limits its application. In [9], a variable electrical network monitoring method was proposed. During the inverter shutdown period, the capacitors are discharged through the controlled variable electrical network, and the capacitance value and equivalent series resistance (ESR) are estimated, based on the observed discharge curve. Considering that the accelerated aging test is a long process, frequent shutdowns of the system will increase the burden of the system, and online estimation can avoid this shortcoming. In [13], a small AC voltage is injected into the DC link, and the input impedance model of the inverter is adopted to simplify the measured approaches and calculate the capacitance value to realize online monitoring, which is suitable for a long-term accelerated life test. However, with the increasing power rating of inverters used in renewable energy, it will be more difficult to create a standard field to evaluate the capacitors on-line in full-scale converters and give a certification. Therefore, a down-scale capacitor evaluation testing circuit for high-power three-phase inverters was proposed in [11]. By providing a high-voltage DC source to emulate the voltage across the capacitors in a full-scale voltage rating inverter, a down-scale voltage rating inverter is used to supply the current rating, which is the same as that of a full-scale voltage rating inverter. However, in the literature [11], the inductor ripple current flowing through the capacitor is different from that in a full-scale voltage rating inverter. In addition, in practical applications, an unbalanced load in a three-phase system is a more common condition and this condition is not considered in [11], which will cause an error estimation for the capacitor operated in a high-power inverter system.

In this paper, an improved down-scale power rating evaluation system is proposed by modifying the inductor value and adding a filter in a series with a low-voltage DC supply to precisely evaluate the current of the capacitor under the test. Moreover, AC and DC analyses of the proposed improved down-scale power rating evaluation system are conducted, and the equivalent circuit and transfer function are derived. Finally, some simulation and experimental results are provided to verify the validity of the proposed down-scale evaluation system.

The remainder of this paper is organized as follows. In Section 2, the conventional down-scale evaluation system is described. Then, an improved down-scale evaluation system for the DC-link capacitors used in high-power three-phase inverter systems under balanced and unbalanced load conditions is proposed in Section 3. In Section 4, some simulation and experimental results are given to verify the validity of the proposed evaluation system. Finally, some conclusions are offered in Section 5.

2. Conventional Down-Scale System

More and more high-power three-phase inverters are widely used in renewable energy resources. Thus, the reliability of these high-power three-phase inverters becomes more and more important. A high-power full-scale three-phase inverter is shown in Figure 1, where a DC-voltage source V_H is connected in the DC side and paralleled with a DC-link capacitor, which is a critical component for reliability in high-power three-phase inverters.

In order to evaluate the DC-link capacitor in a full-scale voltage rating three-phase inverter, a down-scale voltage rating evaluation system was proposed [11], as shown in Figure 2, where the voltage and current of the DC-link capacitor are designed to be very close to that of the DC-link capacitor in a full-scale voltage rating system. However, in an actual case, the down-scale inverter in Figure 2 will have different inductor current ripples in the line currents i_a, i_b and i_c compared with the full-scale inverter in Figure 1. In addition, although the evaluation circuit can work well in a load-balanced condition, it does not

perform well when the three-phase load is unbalanced. In the three-phase unbalanced load condition, the difference in the capacitor current i_{CT} between the full-scale VSI and the evaluation circuit proposed in [11] can be observed. The main problem is that the second-order harmonic current is not high enough for the inductor L_{Lchoke} to block it. Moreover, a LC resonant circuit loop may be formed, which makes the evaluation results become worse. Therefore, in this paper, an improved down-scale evaluation circuit for DC-link capacitors in high-power applications under balanced and unbalanced load conditions is proposed and analyzed to precisely evaluate the DC-link capacitor in a high-power three-phase inverter system.

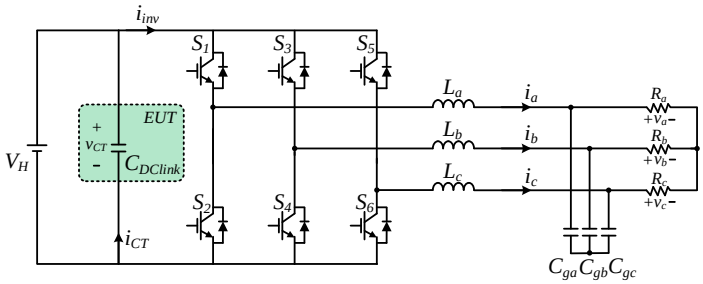


Figure 1. Full-scale voltage rating evaluation system in a high-power three-phase inverter.

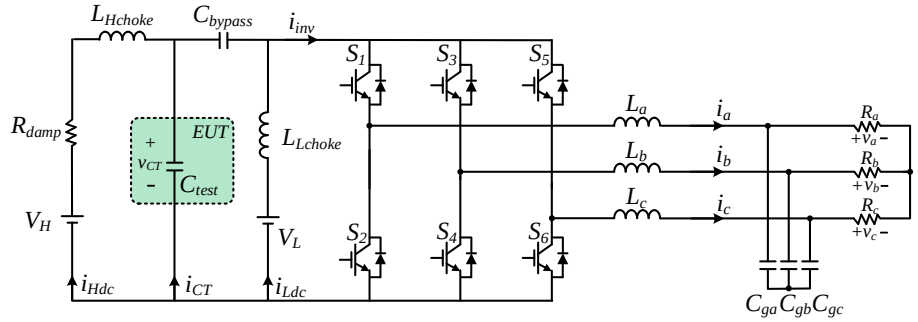


Figure 2. Down-scale voltage rating evaluation system in a high-power three-phase inverter [11].

3. Proposed System Configuration

In [11], since the current rating of the small inverter is controlled to be same as that of the full-scale inverter, the relationship between the power rating of the small inverter P_{small} and the full-scale inverter P_{FS} is given by

$$\frac{P_{small}}{P_{FS}} = \frac{V_{DClink-S}}{V_{DClink-FS}} = \frac{V_{LV}}{V_{HV}}, \tag{1}$$

where $V_{DClink\text{-}S}$ and $V_{DClink\text{-}FS}$ are the DC-link voltages of the down-scale inverter and the full-scale inverter, respectively. However, the different DC-link voltages will change the actual inductor current ripples of the three-phase currents i_a, i_b and i_c. The voltage across the output inductors in the down-scale voltage rating inverter is different from that in the full-scale voltage rating inverter. Therefore, the DC-link capacitor current in the down-scale voltage rating inverter is also different from that in the full-scale voltage rating inverter. In this paper, an improved evaluation circuit is proposed in Figure 3. To reach the same encountered amplitude of the current ripple in the line currents i_a, i_b and i_c in the full-scale inverter, the inductor value should be modified according to the down-scale voltage rating as follows.

$$v_l = L\frac{di_l}{dt}, \tag{2}$$

where the v_l is the inductor terminal voltage, and i_l is the inductor current. For example, if the low-voltage DC supply V_L is half of the high-voltage DC supply V_H, the inductance of

the down-scale voltage rating inverter must be half the inductance of the full-scale voltage rating inverter. Otherwise, the amplitude of the current ripples in the three-phase currents in the down-scale voltage rating inverter will be half of that in the full-scale voltage rating inverter. It should be noticed that the more we lower the voltage rating of the small inverter, the smaller inductance of the output inductors we should select.

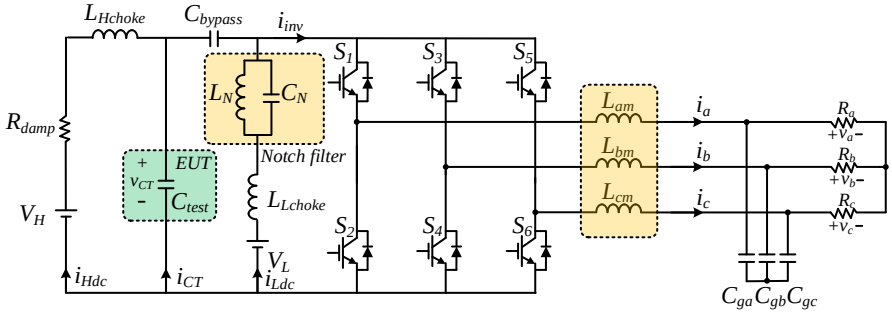


Figure 3. Proposed down-scale voltage rating evaluation system.

Therefore, an improved down-scale voltage rating evaluation system for DC-link capacitor is proposed in Figure 3. Compared with Figure 2, the three-phase inductors are changed and a notch filter is adopted in the low-voltage DC supply path. It should be noticed that, in order to block the high-frequency ripple current produced by the PWM inverter to flow through the high-voltage DC supply V_H and low-voltage DC supply V_L, the reactance of the two choke inductors must be much larger than that of C_{test} and C_{bypass}, as follows

$$\omega L_{choke} \gg \frac{1}{\omega C_{test}}, \tag{3}$$

where $\omega = 2\pi f_{sw}$, f_{sw} is the switching frequency of the inverter. L_{Hchoke} and L_{Lchoke} are the choke inductors of the high- and low-voltage DC supplies, respectively. However, under the unbalanced load condition, there exists a double-line frequency in the DC-link capacitor. The choke inductor cannot block the double-line frequency caused by the unbalanced load condition. Hence, the L_N and C_N must satisfy the following

$$\frac{1}{\sqrt{L_N C_N}} = 2\omega_l, \tag{4}$$

where $\omega = 2\pi f_l$, f_l is the line frequency.

In order to analyze the proposed evaluation system shown in Figure 3, an equivalent circuit focusing on the inverter current i_{inv} and DC side currents is introduced in Figure 4, where the low-voltage DC supply V_H and high-voltage DC supply V_L are set to zero. The current i_{inv} can be seen as the current source and expressed as the sum of the DC component I_{dc} and the AC component i_{ac}. The AC current i_{ac} includes high- and low-frequency components. The L_{Lchoke} and L_{Hchoke} are the choke inductors in the low-voltage DC side and high-voltage DC side, respectively. The R_{LV} and R_{HV} are the equivalent series resistance corresponding to the low-voltage DC side and the high-voltage DC side circuit branches, respectively. Note that the damping resistor R_{damp} is added into the R_{HV}. For the convenience of discussion, we assume Z_1 and Z_4 are the total impedance in the low-voltage DC side and the high-voltage DC side circuit branches, respectively. The Z_2 and Z_3 are the impedance of the bypassing capacitor C_{bypass} and capacitor C_{test} under test, respectively. Therefore, the impedances Z_1 to Z_4 can be written as follows:

$$Z_1(s) = \frac{\mathrm{sL}_N}{s^2 L_N C_N + 1} + sL_{Lchoke} + R_{LV}, \tag{5}$$

$$Z_2(s) = \frac{1}{sC_{bypass}}, \tag{6}$$

$$Z_3(s) = \frac{1}{sC_{test}}, \tag{7}$$

$$Z_4(s) = sL_{Hchoke} + R_{HV}, \tag{8}$$

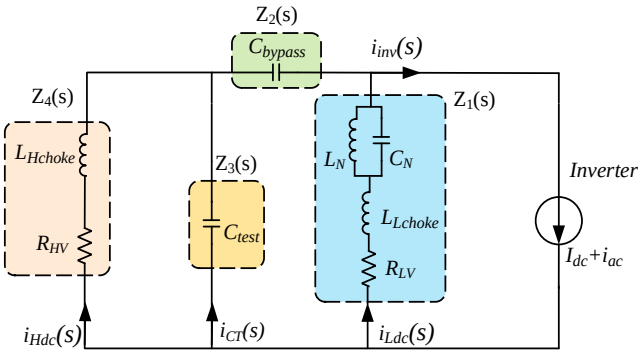


Figure 4. Equivalent circuit focusing on the current flowing into the inverter i_{inv}, capacitor current i_{CT}, high voltage DC current i_{Hdc}, and low voltage DC current i_{Ldc}.

Then the transfer functions $G_1(s)$ from i_{inv} to i_{Ldc}, and $G_2(s)$ from i_{inv} to i_{CT} can be expressed as follows

$$G_1(s) = \frac{i_{Ldc}(s)}{i_{inv}(s)} = \frac{Z_2(Z_3 + Z_4) + Z_3Z_4}{Z_3Z_4 + (Z_1 + Z_2)(Z_3 + Z_4)}, \tag{9}$$

$$G_2(s) = \frac{i_{CT}(s)}{i_{inv}(s)} = \frac{Z_1Z_4}{Z_3Z_4 + (Z_1 + Z_2)(Z_3 + Z_4)}, \tag{10}$$

Under the load-unbalanced condition, the AC component i_{ac} in the current i_{inv} contains a second-order harmonic current and a high-frequency switching current, which are greater than or equal to 120 Hz. It should be noted that, when the current frequency is 120 Hz or above, the impedance of Z_3 is much smaller than Z_4. For instance, if the current frequency is 120 Hz and the capacitor C_{test}, choke inductor L_{Hchoke}, and equivalent series resistance R_{HV} are selected as 2.2 mF, 1.6 mH and 10 ohm, respectively, the impedance Z_3 is 0.6 ohm and Z_4 is 11.2 ohm. In this condition, Z_3 is much less than Z_4. Thus, for AC components above 120 Hz in current i_{inv}, Z_4 can be approximated as an open circuit. Thus, the transfer functions from i_{ac} to $i_{Ldc,}$ and from i_{ac} to i_{CT} can be written as follows, respectively.

$$G_3(s) = \frac{i_{Ldc}(s)}{i_{ac}(s)} = \frac{Z_2 + Z_3}{Z_1 + Z_2 + Z_3}, \tag{11}$$

$$G_4(s) = \frac{i_{CT}(s)}{i_{ac}(s)} = \frac{Z_1}{Z_1 + Z_2 + Z_3}, \tag{12}$$

In order to discuss the properties of the conventional and proposed evaluation systems for capacitors utilized in high-power three-phase inverters, $G_3(s)$ and $G_4(s)$ in the evaluation system [11] can be written as Equations (13) and (14)

$$\frac{i_{Ldc}(s)}{i_{ac}(s)} = \frac{1}{s^2L_{Lchoke}C_S + sR_{LV}C_S + 1}, \tag{13}$$

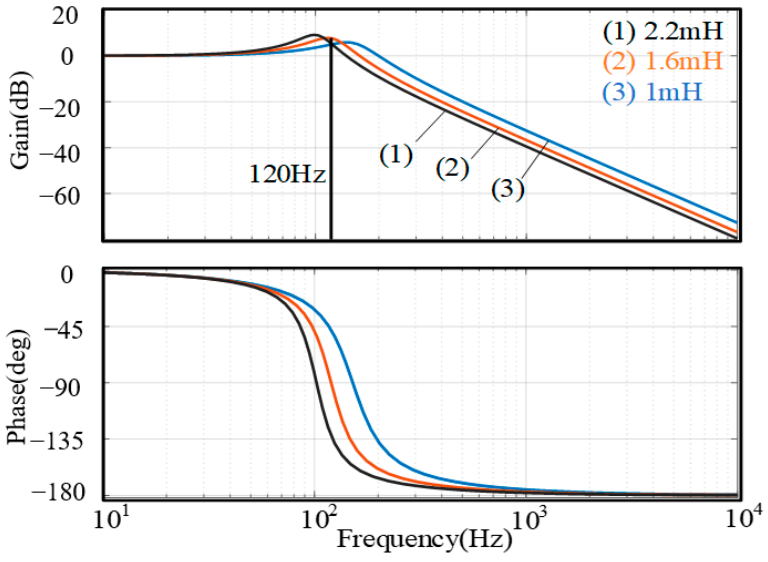
$$\frac{i_{CT}(s)}{i_{ac}(s)} = \frac{s^2L_{Lchoke}C_S + sR_{LV}C_S}{s^2L_{Lchoke}C_S + sR_{LV}C_S + 1}, \tag{14}$$

where C_S is the equivalent series capacitor in the Z_2 and Z_3 circuit branch. In the following, the choke inductor L_{Lchoke} is discussed under three different inductor values, namely 1 mH, 1.6 mH, and 2.2 mH. The bode plots of G_3 and G_4 in the conventional evaluation system are shown in Figure 5a,b, respectively. Note that, in the system, C_S and L_{Lchoke} will form an

LC resonant circuit. For the worst case, when the inductance value of the choke inductor L_{Lchoke} is 1.6 mH, the second-order harmonic current, i.e., 120 Hz, will exactly fall on the peak resonance, where the gain of the transfer function is at the maximum. In this case, it will seriously influence the current i_{CT} under test because the second-order current will not only flow into i_{Ldc}, but also be amplified due to the LC resonance. To solve this problem, a filter is adopted and added to the low DC voltage side circuit branch, shown in Figure 3, to block the second-order harmonic current and change the resonance situation. For the improved system in this paper, $G_3(s)$ and $G_4(s)$ are given as Equations (15) and (16), respectively. The bode plots of $G_3(s)$ and $G_4(s)$ in the improved evaluation system are shown in Figure 6. Different from that shown in Figure 5, the gain of the transfer function $G_3(s)$ at 120 Hz is much smaller. Thus, it can be seen from Figures 5 and 6 that, for the 120 Hz ripple current, the impedance of Z_1 is high enough to block it. Moreover, the peak resonance point is set to 66 Hz, as shown in Figure 6a. Note that, under the load-unbalanced condition, i_{ac} does not contain the ripple currents whose frequencies are below 120 Hz. Figure 6b shows the bode plot of the transfer function $G_4(s)$. No matter what inductance value of L_{Lchoke} is selected, the gain of $G_4(s)$ stays at 0 dB at 120 Hz and at the switching frequency, which indicates that the AC component of the capacitor current i_{CT} is equal to the ripple current flowing from the down-scale and full-scale voltage rating inverter under the unbalanced load condition.

$$\frac{i_{Ldc}(s)}{i_{ac}(s)} = \frac{s^2 L_N C_N + 1}{s^4 L_{Lchoke} C_S L_N C_N + s^3 R_{LV} C_S L_N C_N + s^2 (L_N C_N + L_{Lchoke} C_S + L_N C_S) + s R_{LV} C_S + 1}, \tag{15}$$

$$\frac{i_{CT}(s)}{i_{ac}(s)} = \frac{s^4 L_{Lchoke} C_S L_N C_N + s^3 R_{LV} C_S L_N C_N + s^2 (L_{Lchoke} C_S + L_N C_S) + s R_{LV} C_S}{s^4 L_{Lchoke} C_S L_N C_N + s^3 R_{LV} C_S L_N C_N + s^2 (L_N C_N + L_{Lchoke} C_S + L_N C_S) + s R_{LV} C_S + 1}, \tag{16}$$



(**a**)

Figure 5. *Cont.*

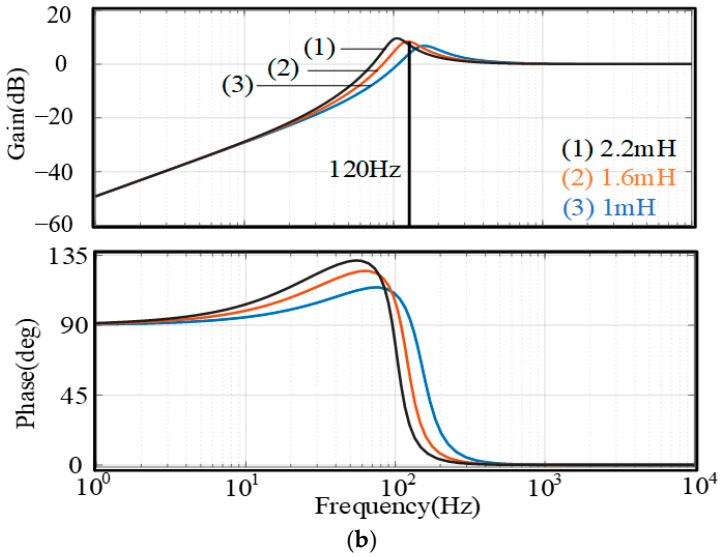


Figure 5. Bode plot of the transfer function in evaluation system proposed in [11]. (**a**) $G_3(s)$. (**b**) $G_4(s)$.

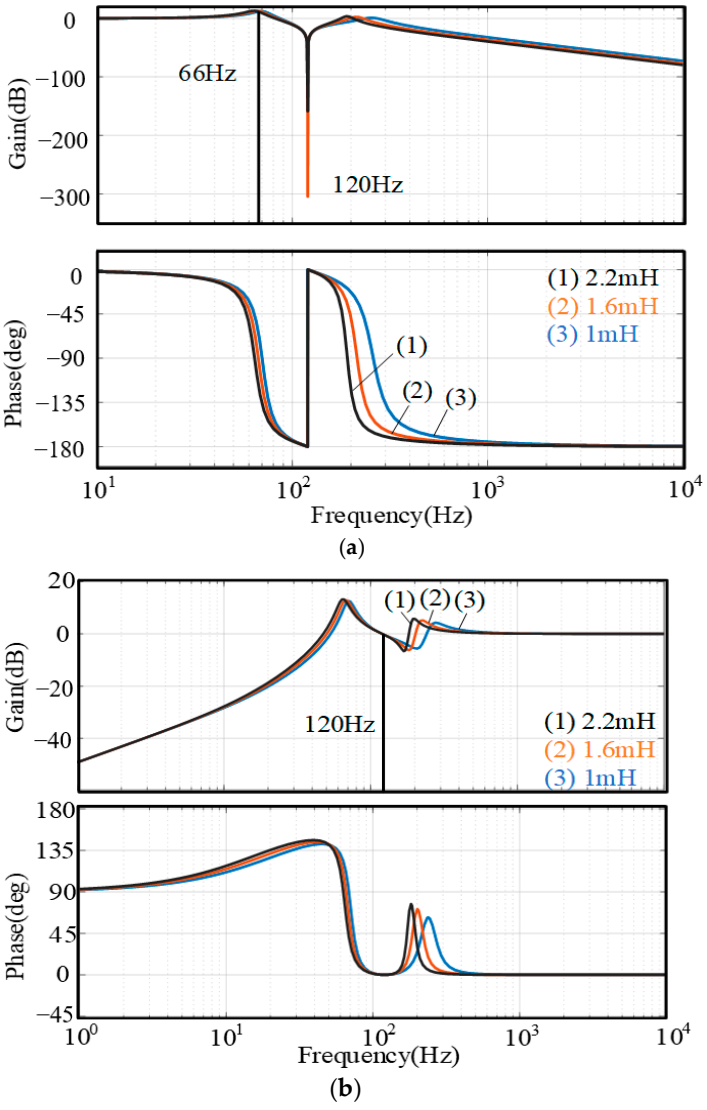


Figure 6. Bode plot of the transfer function proposed in this paper. (**a**) $G_3(s)$. (**b**) $G_4(s)$.

4. Simulation and Experimental Results

To verify the effectiveness of the proposed evaluation system, some simulation results are executed. Simultaneously, a full-scale voltage rating inverter and a down-scale voltage rating evaluation system are also constructed. Tables 1 and 2 list the circuit parameters of the full-scale voltage rating inverter and the down-scale voltage rating evaluation systems used in the simulation and experiment, respectively.

Table 1. Parameters of the full-scale voltage rating inverter used in simulation and experiment.

Name	Symbol	Parameter
Power rating	P	3 kW
DC link voltage	V_H	450 V
DC link capacitor	C_{DClink}	2.2 mF
AC line voltage (rms)	V_{line}	220 V
Switching frequency	f_{sw}	18 kHz
Output frequency	f_o	60 Hz
Output inductors	L_a L_b L_c	2 mH
Output capacitors	C_{ga} C_{gb} C_{gc}	22 uF
Balanced load resistors	R_a R_b R_c	16 Ω, 16 Ω, 16 Ω
Unbalanced load resistors	R_a R_b R_c	12 Ω, 16 Ω, 16 Ω

Table 2. Parameters of the down-scale voltage rating evaluation system used in simulation and experiment.

Name	Symbol	Parameter
Power rating of the system	P	1.5 kW
High-DC voltage source	V_H	450 V
Low-DC voltage source	V_L	225 V
High-voltage choke inductor	L_{Hchoke}	1.6 mH
Low-voltage choke inductor	L_{Lchoke}	1.6 mH
Notch filter inductor	L_N	2.43 mH
Notch filter capacitor	C_N	0.724 mF
Bypassing capacitor	C_{bypass}	2.2 mF
Capacitor under test	C_{test}	2.2 mF
Damping resistor	R_{damp}	10 Ω
AC line voltage (rms)	V_{line}	110 V
Switching frequency	f_{sw}	18 kHz
Output frequency	f_o	60 Hz
Output inductors	L_{am} L_{bm} L_{cm}	1 mH
Output capacitors	C_{ga} C_{gb} C_{gc}	22 uF
Balanced Load resistors	R_a R_b R_c	8 Ω, 8 Ω, 8 Ω
Unbalanced load resistors	R_a R_b R_c	6 Ω, 8 Ω, 8 Ω

Figures 7a–c and 7d–f shows the simulation and experimental results of the output voltages V_a, V_b, V_c, and the output inductor current i_a, respectively. Due to the power rating of the down-scale voltage rating VSI being half that of the full-scale voltage rating VSI, it can be seen from Figure 7 that the output inductor values of the down-scale voltage rating VSI must be modified to half that of the full-scale voltage rating VSI, so that the amplitude of the line current ripple in the down-scale voltage rating inverter is very

close to that in the full-scale inverter. Tables 3 and 4 show the simulated and measured peak-to-peak current ripples at the maximum phase voltage, respectively. As can be observed from Tables 3 and 4, one can see that the amplitude of the current ripple in the proposed down-scale voltage rating evaluation system has a value closer to that of the full-scale voltage rating VSI, when compared with the conventional down-scale voltage rating evaluation system.

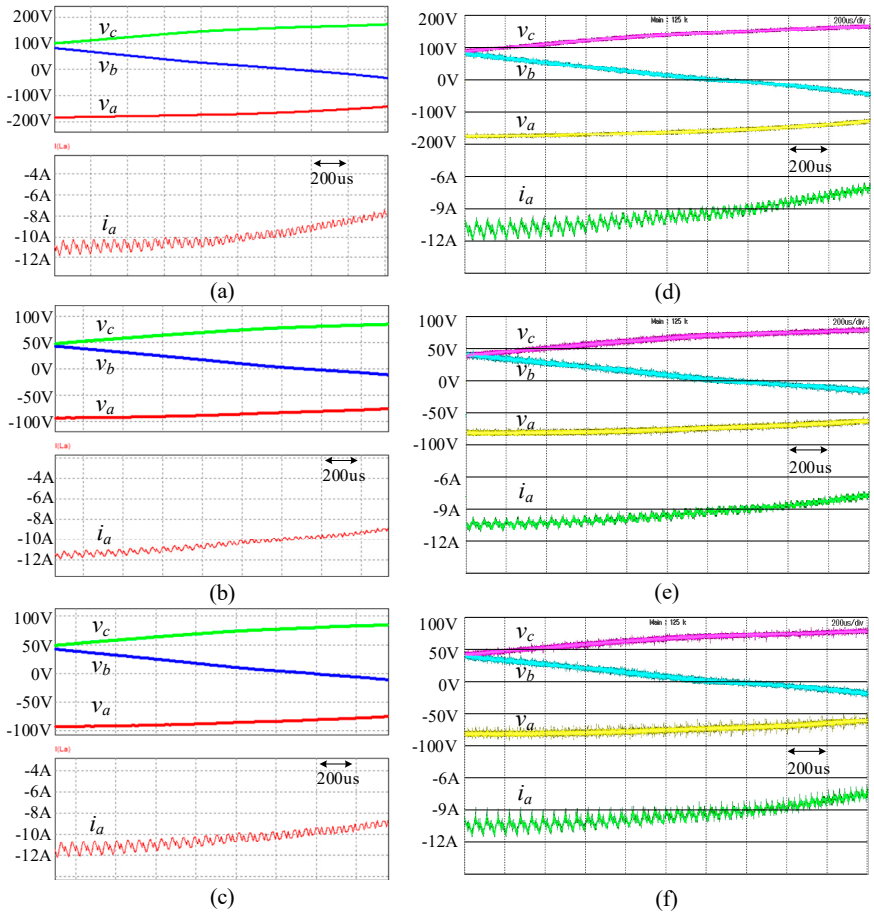


Figure 7. Simulation (**left**) and corresponding experimental (**right**) waveforms of output three-phase voltages V_a, V_b, V_c and output current i_a under (**a**,**d**) full-scale VSI with output inductor 2 mH, (**b**,**e**) conventional down-scale voltage rating evaluation system with output inductor 2 mH, and (**c**,**f**) proposed down-scale voltage rating evaluation system with output inductor 1 mH.

Table 3. Comparison of simulated line-current ripple at maximum phase voltage.

Ripple (Peak to Peak)	Full-Scale VSI	Conventional Down-Scale Evaluation System	Proposed Down-Scale Evaluation System
Maximum	~1.64 A	~0.79 A	~1.58 A

Table 4. Comparison of measured line-current ripple at maximum phase voltage.

Ripple (Peak to Peak)	Full-Scale VSI	Conventional Down-Scale Evaluation System	Proposed Down-Scale Evaluation System
Maximum	~2.23 A	~0.88 A	~2.41 A

Figure 8 shows the voltage and current simulated waveforms of the capacitor under test in the full-scale voltage rating inverter, conventional down-scale voltage rating evaluation system, and proposed down-scale voltage rating evaluation system. Figure 8a,b illustrates the simulated waveforms of the full-scale voltage rating inverter under the load-balanced and load-unbalanced conditions, respectively. As shown in Figure 8c,d, although the testing capacitor current i_{CT} of the conventional down-scale voltage rating evaluation system can be very close to that of the full-scale voltage rating inverter in the load-balanced condition, it does not perform well in the load-unbalanced condition. By comparison, the proposed down-scale voltage rating evaluation system can have a similar testing capacitor current i_{CT} compared with the conventional down-scale voltage rating evaluation system in both the load-balanced and load-unbalanced conditions, as shown in Figure 8e,f.

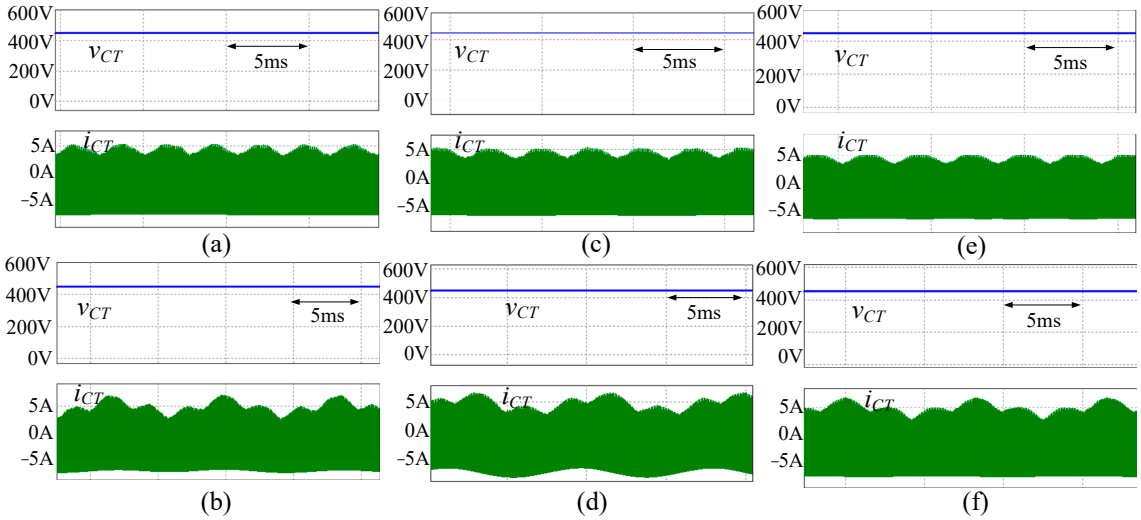


Figure 8. The simulated voltage v_{CT} and current i_{CT} of the DC-link capacitor under test for (**a**,**c**,**e**) balanced and (**b**,**d**,**f**) unbalanced load condition in the (**a**,**b**) full-scale voltage rating VSI, (**c**,**d**) conventional down-scale voltage rating evaluation system, and (**e**,**f**) proposed down-scale voltage rating evaluation system.

In order to clarify the difference in the capacitor evaluation results, the corresponding enlarged view of the simulated current i_{CT} of the DC-link capacitor under test is illustrated in Figure 9. It follows from Figure 9 that, under the balanced load condition, the conventional and proposed down-scale evaluation systems can obtain a similar DC-link capacitor current under test compared with the full-scale voltage rating VSI, but it is different under the unbalanced load condition. In addition, the corresponding close-to-120 Hz FFT results of the simulated i_{CT} of the DC-link capacitor under test are shown in Figure 10. As can be seen from Figure 10, under the balanced load condition, the amplitude of the double-line frequency in the full-scale voltage rating VSI, conventional down-scale voltage rating evaluation system, and proposed down-scale voltage rating evaluation system is very close to zero. However, under the unbalanced load condition, the amplitude of the double-line frequency in the conventional down-scale voltage rating evaluation system is much different from that in the full-scale voltage rating VSI.

Next, by analyzing the i_{Ldc} and i_{CT}, one can observe the problem of the previous system [11] in Figure 11. Figure 11b shows that, when the three phase loads are unbalanced, the double-line frequency or second-order harmonic current will flow into i_{Ldc} and be amplified by an LC resonant circuit loop. As shown in Figure 11d, the proposed down-scale voltage rating evaluation system can block the second-order harmonic current in the low-voltage DC-side i_{Ldc} circuit branch and change the LC resonant circuit loop. Figures 12 and 13 are the experimental results corresponding to the simulation results in Figures 8 and 11, respectively. As can be observed from Figures 8 and 11–13, the experi-

mental results are in very close agreement with the simulation results. Both the simulation and experimental results verify the validity of the proposed down-scale voltage rating evaluation system.

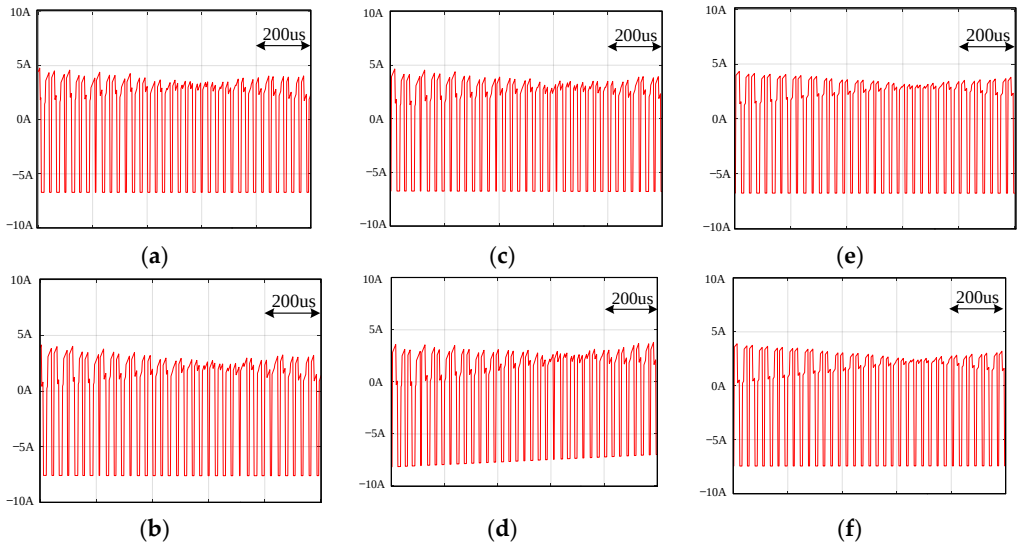


Figure 9. The enlarged view of simulated current i_{CT} of the DC-link capacitor under test for (**a**,**c**,**e**) balanced and (**b**,**d**,**f**) unbalanced load conditions in the (**a**,**b**) full-scale voltage rating VSI (**c**,**d**), conventional down-scale voltage rating evaluation system, and (**e**,**f**) the proposed down-scale voltage rating evaluation system.

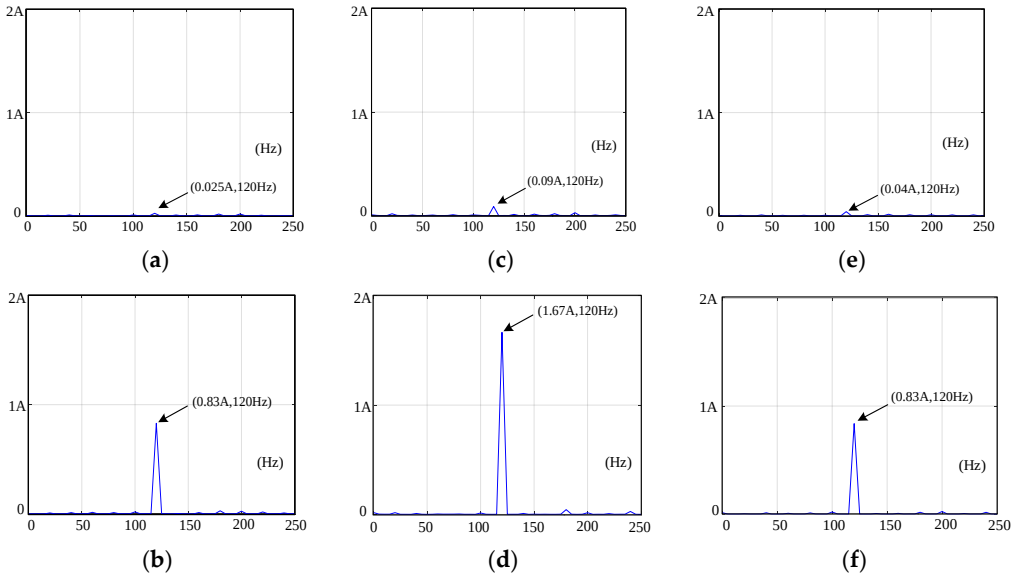


Figure 10. Close-to-120 Hz FFT results of current i_{CT} of the DC-link capacitor under test for (**a**,**c**,**e**) balanced and (**b**,**d**,**f**) unbalanced load conditions in the (**a**,**b**) full-scale voltage rating VSI, (**c**,**d**) conventional down-scale voltage rating evaluation system, and (**e**,**f**) proposed down-scale voltage rating evaluation system.

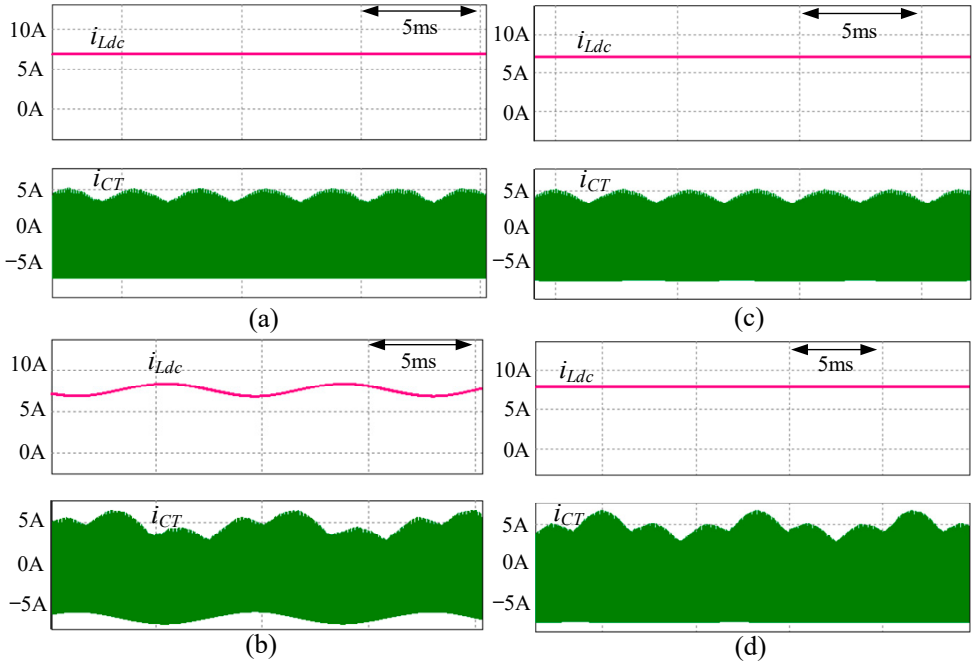


Figure 11. The simulated waveforms of the low-voltage-side dc current i_{Ldc} and the testing capacitor current i_{CT} for (**a**,**c**) balanced and (**b**,**d**) unbalanced load conditions in the (**a**,**b**) conventional down-scale voltage rating evaluation system, and the (**c**,**d**) proposed down-scale voltage rating evaluation system.

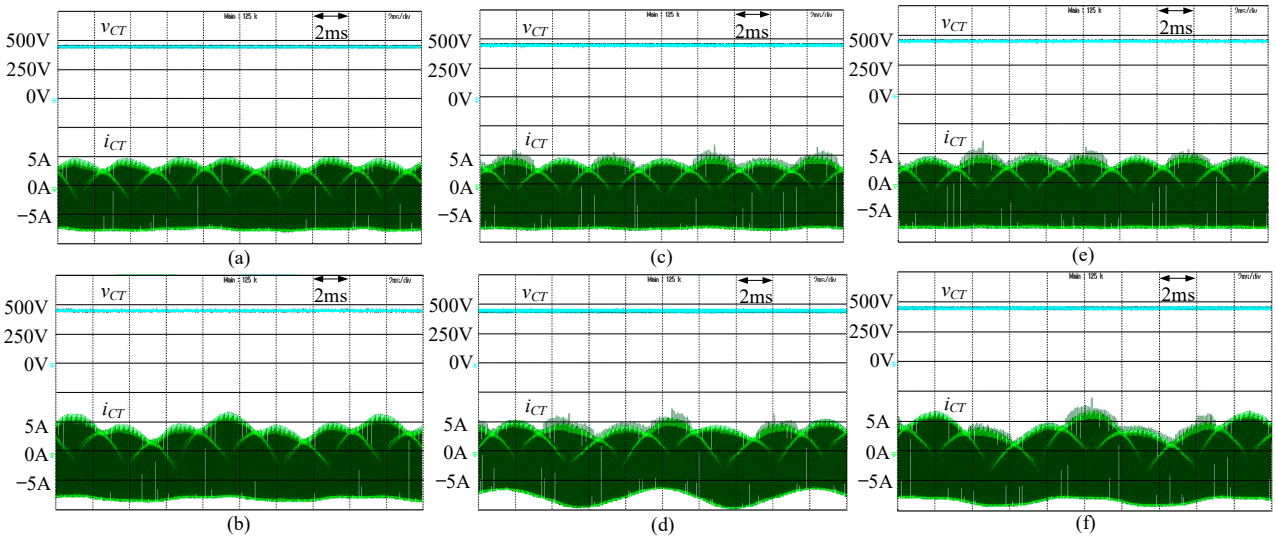


Figure 12. The measured voltage v_{CT} and current i_{CT} of the DC-link capacitor under test for (**a**,**c**,**e**) balanced and (**b**,**d**,**f**) unbalanced load conditions in the (**a**,**b**) full-scale voltage rating VSI, (**c**,**d**) conventional down-scale voltage rating evaluation system, and (**e**,**f**) proposed down-scale voltage rating evaluation system.

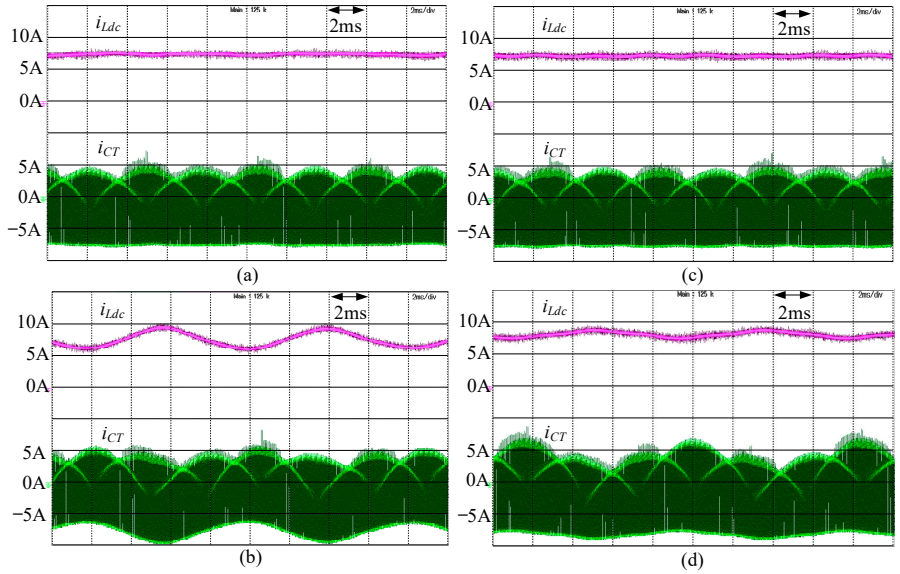


Figure 13. The measured waveforms of the low-voltage-side dc current i_{Ldc} and the testing capacitor current i_{CT} for (**a**,**c**) balanced and (**b**,**d**) unbalanced load conditions in the (**a**,**b**) conventional down-scale voltage rating evaluation system, and (**c**,**d**) proposed down-scale voltage rating evaluation system.

5. Conclusions

More and more high-power and high-density inverters are manufactured for renewable energy systems to reduce carbon emissions in the world. Therefore, the system testing and certification for high-power and high-density inverters becomes very important, especially in the limited power rating testing field. In order to reproduce the same encountered stresses when a DC-link capacitor is used in a high-power inverter with pulse-width modulation, in this article, an improved evaluation circuit for the DC-link capacitors used in high-power three-phase inverters under balanced and unbalanced load conditions is proposed. A comparison of the down-scale voltage rating evaluation systems is analyzed and some problems in the conventional evaluation systems are discovered. It was found that, under an unbalanced load condition, the conventional down-scale voltage rating evaluation system does not present very closely the testing capacitor current of the full-scale voltage rating inverter system. In order to more precisely evaluate the current of the capacitor under test, the output inductors of the conventional evaluation system are modified, and a filter is added in the low-voltage DC-side circuit branch. From the simulation and experimental results, the proposed down-scale voltage rating evaluation system presents the closest ripple current waveform and DC bias voltage of the DC-link capacitors in the full-scale voltage rating inverter system under the balanced and unbalanced load conditions. The validity of the proposed down-scale voltage rating evaluation system is verified in this article. In the future, the accelerated life testing of capacitors working in severely adverse circumstances can be utilized in the proposed improved down-scale voltage rating evaluation system.

Author Contributions: Conceptualization, Y.-H.L.; methodology, Y.-L.L.; validation, Y.-H.L. The paper was a collaborative effort among the authors. The authors contributed collectively to the theoretical analysis, modeling, simulation, experiment, and manuscript preparation. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by [the Ministry of Science and Technology of R.O.C] grant number [111-3116-F-008-003].

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. *IEC 60364-7-712:2017*; Requirements for Special Installations or Locations—Solar Photovoltaic (PV) Power Supply Systems. International Electrotechnical Commission: Geneva, Switzerland, 2017.
2. *IEC 61000-3-3:2013+AMD1:2017+AMD2:2021 CSV*; Electromagnetic Compatibility (EMC)—Part 3-3: Limits—Limitation of Voltage Changes, Voltage Fluctuations and Flicker in Public Low-Voltage Supply Systems, for Equipment with Rated Current $\leq$16 A Per Phase and Not Subject to Conditional Connection. International Electrotechnical Commission: Geneva, Switzerland, 2021.
3. *IEC/TS 61000-3-4*; Electromagnetic Compatibility (EMC)—Part 3-4: Limits—Limitation of Emission of Harmonic Currents in Low-Voltage Power Supply Systems for Equipment with Rated Current Greater Than 16 A. International Electrotechnical Commission: Geneva, Switzerland, 1998.
4. Amaral, A.M.R.; Cardoso, A.J.M. A simple offline technique for evaluating the condition of aluminum–electrolytic–capacitors. *IEEE Trans. Ind. Electron.* **2009**, *56*, 3230–3237. [CrossRef]
5. Amaral, A.M.R.; Cardoso, A.J.M. Estimating aluminum electrolytic capacitors condition using a low frequency transformer together with a DC power supply. In Proceedings of the 2010 IEEE International Symposium on Industrial Electronics, Bari, Italy, 4–7 July 2010; pp. 815–820.
6. Wang, H.; Blaabjerg, F. Reliability of capacitors for dc-ink applications in power electronic converters—An overview. *IEEE Trans. Ind. Appl.* **2014**, *50*, 3569–3578. [CrossRef]
7. Ondel, O.; Boutleux, E.; Venet, P. A decision system for electrolytic capacitors diagnosis. In Proceedings of the 2004 IEEE 35th Annual Power Electronics Specialists Conference, Aachen, Germany, 20–25 June 2004; pp. 4360–4364.
8. Makdessi, M.; Sari, A.; Venet, P. Metallized polymer film capacitors ageing law based on capacitance degradation. *Microelectron. Reliab.* **2014**, *54*, 1823–1827. [CrossRef]
9. Wu, Y.; Du, X. A VEN Condition Monitoring Method of DC-Link Capacitors for Power Converters. *IEEE Trans. Ind. Electron.* **2019**, *66*, 1296–1306. [CrossRef]
10. Zhou, W.; Wang, M.; Wu, Q.; Xi, L.; Xiao, K.; Bhat, K.P.; Chen, C.C. Accelerated Life Testing Method of Metallized Film Capacitors for Inverter Applications. *IEEE Trans. Transp. Electrif.* **2021**, *7*, 37–49. [CrossRef]
11. Hasegawa, K.; Omura, I.; Nishizawa, S.I. Design and Analysis of a New Evaluation Circuit for Capacitors Used in a High-Power Three-Phase Inverter. *IEEE Trans. Ind. Electron.* **2016**, *63*, 2679–2687. [CrossRef]
12. Chroma ATE Inc. Ripple Current Tester Model 11800/11801/11810. 2022. Available online: https://assets.testequity.com/te1/Documents/pdf/11800-ds.pdf (accessed on 18 September 2022).
13. Makdessi, M.; Sari, A.; Venet, P.; Bevilacqua, P.; Joubert, C. Accelerated ageing of metallized film capacitors under high ripple currents combined with a DC voltage. *IEEE Trans. Power Electron.* **2015**, *30*, 2435–2444. [CrossRef]
14. Li, H.; Xiang, D.; Han, X.; Zhong, X.; Yang, X. High-accuracy capacitance monitoring of DC-link capacitor in VSI systems by LC resonance. *IEEE Trans. Power Electron.* **2019**, *34*, 12200–12211. [CrossRef]