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Abstract: Multilevel inverters (MLIs) consist of a wide range of power converters. They have many designs and have been introduced with different circuit topologies such as neutral point clamped, diode clamped, cascaded H-bridges, and flying capacitors. Some of these MLIs have disadvantages, including design complexity, size, and losses due to the large number of switching devices required when they produce many output voltage levels. They are also bulky in size and may require several DC power sources. This paper presents a review of the various topologies of single-phase T-Type MLIs (T-MLIs). These MLIs are used to convert DC power from renewable energy sources (RESs) into AC with a near-sine waveform and low total harmonic distortion (THD). Simple and complex MLI designs are discussed. The major types of modulation techniques are discussed, including sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE), and preprogrammed PWM. Various methods of output voltage control are taken into consideration as well. The aim of this comprehensive survey is to identify T-MLIs for researchers and those interested in the power conversion field, as well as to discuss the many topologies, identifying designs with superior characteristics that can be efficiently implemented with RESs to obtain better AC voltage with enhanced power quality.

Keywords: inverter; multilevel; PWM; SHE; SPWM; topology; T-type

1. Introduction

Recently, solar and wind energy have been considered the most important renewable energy systems (RESs) [1,2]. A wind turbine converts the force of the wind that moves the blades into electrical energy by rotating a generator. Photovoltaic (PV) modules convert solar energy directly into electrical energy [3]. In most cases, it is difficult to power electrical equipment directly from RESs without using power conditioning circuits such as inverters or DC/DC converters. The power converted from RESs is usually in the form of DC voltage and DC current. It was determined that the DC voltage and current should be converted to AC voltage using an inverter [4,5]. A common type of single-phase inverter produces three levels of output voltage: \( \pm V_{dc} \) and 0 volts. These inverters are known as 2-level or 3-level inverters, depending on whether 0 is considered a voltage level [6]. These inverters use a high switching frequency with the use of “pulsed width modulation (PWM)” technology to minimize ripple and achieve a nearly sinusoidal waveform of the output voltage. Furthermore, at high voltages, switching elements such as BJTs, IGBTs, or MOSFETs are subjected to high voltage stress in various modes of operation [7–9]. During switching, power transistors can be exposed to high voltage spikes. Therefore, soft-switching techniques should be used to overcome these problems. This can increase losses and reduce inverter efficiency. In addition, the filter requirements for these types of
inverters are high because the shape of the output voltage at the inverter output terminals is either square wave or quasi-square wave. To overcome these problems, multilevel inverters were introduced [10]. The purpose of MLI is to synthesize an approximately sinusoidal waveform in the output voltage. Its output voltage is therefore formed from several parts of the supplied DC voltage. Increasing the number of voltage levels reduces harmonic distortion, filtering requirements, and voltage stress on each switching element. However, the design topologies of multilevel inverters, PWM, and their voltage control are more complex, resulting in higher inverter costs [11,12]. Therefore, researchers in this field have long worked to balance the cost, complexity, and size of multilevel inverters [13].

The advantages of single-phase MLI over two-level inverters (2LI) contribute to RES integration in low-, medium-, and even high-voltage grids, eliminating bulky power transformers [14–16]. Many PWM techniques are possible to properly use MLI. The main types of PWM techniques are selective harmonic rejection (SHE), sinusoidal PWM (SPWM), and variants thereof. The purpose of such a PWM scheme in MLI is to reduce the harmonic content of the output voltage and reduce filtering requirements [17,18]. The choice of PWM technology depends on the specific MLI topology and the number of output voltage levels on its terminals [19,20]. ML can be used for both high-power and low-power applications. Diode-clamped flying-capacitor, neutral-point-clamped (NPC), and cascaded H-bridge (HB) MLIs can be used for high-power applications [21,22]. For low-power applications, T-MLI can be used. The purpose of the current work is to comprehensively review single-phase T-type MLI (T-MLI) used for RES, considering their topology, PWM technology, and output voltage regulation method. This document is organized as follows: an introduction is given, then MLI topologies, modulation techniques, output voltage control, connecting T-MLIs to RES, output voltage filter design, list of challenges of using T-MLIs, and conclusions.

2. Similarity between Neutral Point Clamped (NPC)

A T-type MLI is similar to a three-level NPC MLI. In a three-level T-type MLI, a zero-voltage level is added, which in turn improves harmonic performance over a typical 2LI. Compared to an NPC MLI, a T-MLI MLI has fewer components since only one switching device is utilized instead of two in a series. This eliminates clamp diodes and reduces conduction losses in external switching devices. [23]. The disadvantage is that the external switching device is no longer connected in series, so the reverse voltage is reduced compared to the NPC MLI [24,25]. The trends for NPC inverters have been published previously [26]. A three-level NPC inverter is shown in Figure 1a [27], whereas the same number of levels of a T-MLI is shown in Figure 1b.

![Figure 1. Single-phase three-level (a) NPC MLI (b) T-MLI.](image)

In both NPC and T-MLIs, only a single DC source is used. Increasing the number of levels requires several DC-linked capacitors that are normally connected in series. All these capacitors are mounted in parallel with the inverter switching devices [28–30].
3. Topologies of T-Type MLIs

3.1. Simple Designs

T-MLIs are considered simplified NPC MLI. Per phase, a T-MLI consists of two conventional switching devices and one bidirectional switching device, as shown in Figure 1b. Figure 2 shows how a T-MLI single-phase MLI is originated from a traditional two-level full-bridge inverter. This is performed by substituting the two-level switching device arm with a three-level T-type arm. The T-branch consists of S1, S2, S3, and S4 IGBTs. Switching is performed at high frequency to perform SPWM modulation, and the two-stage branch (S5 to S6) switches at the fundamental frequency, which is either 60 or 50 Hz, to change the polarity of the output voltage. Since the structure is symmetric, only the positive half-wave of the power supply is analyzed [31].

![Figure 2. A single-phase T-type five-level inverter.](image)

C1 and C2 should be balanced in capacitance and voltage. Thus, usually, they are selected with high values. Each capacitance is responsible for feeding the full or an equal portion of the supplied DC voltage to the load. S2 and S3 are responsible for the $\pm \frac{1}{2} V_{dc}$ levels, where S2 is ON for the positive part and S3 is ON for the negative part. S1 and S5 are responsible for the $\pm V_{dc}$ levels, where S1 is ON for the positive part and S5 is ON for the negative part. S4 and S6 can be ON or OFF when supplying $\pm \frac{1}{2} V_{dc}$ or $\pm V_{dc}$, where S6 is ON for the positive part and S4 is ON for the negative part of the full or half DC voltage. The MLI in Figure 2 is a five-level inverter since the voltage levels are arranged as $(+ V_{dc}, + \frac{1}{2} V_{dc}, - V_{dc}, - \frac{1}{2} V_{dc})$. For a seven-level type, the number of DC side capacitors is increased to three. Also, there will be two S2 and S3 branches, or (T-branches) where each is connected between two capacitors. The HB side remains the same. Thus, the number of switching devices is increased by two. The voltage levels for the seven-level T-MLI are $(+ V_{dc}, + \frac{2}{3} V_{dc}, + \frac{1}{3} V_{dc}, 0 V_{dc}, - \frac{1}{3} V_{dc}, - \frac{2}{3} V_{dc})$ and $- V_{dc}$.

A small modification of the seven-level T-MLI was previously performed, where five levels were proposed by [32,33]. In this design, blocking diodes D5 to D8 are added to secure unwanted current flow and reduce the output voltage ripple as well as its harmonics, as shown in Figure 3. The operation modes are illustrated in Figure 4.

For a seven-level T-MLI, another design is shown in Figure 5 [34,35]. This design is similar to the five-level inverter in Figure 1. The difference is that the HB portion is connected to the S3 and S4 branches. In this scheme, only two capacitors on the DC bus are needed instead of three as compared to [32]. Both designs have the same number of switching devices.

The T-branch of the five-level inverter of Figure 2 can be replaced with a bidirectional switch known as a transistor-clamped inverter. The switch is constructed from a single switching device bounded by four diodes [36,37]. This type of inverter was formerly known as a modified HB MLI [38]. In this design, the number of switching devices is reduced by 16.66%. In the case of a seven-level inverter, the number of IGBT switches is decreased by 25% since only six will be needed instead of eight.
Figure 3. T-type seven-level inverter with blocking diodes.

Figure 4. Modes of operation of a seven-level inverter for the modes: (a) $+ V_{dc}$ mode, (b) $+ \frac{2}{3} V_{dc}$ mode, (c) $+ \frac{1}{3} V_{dc}$ mode, (d) $0 V_{dc}$ mode, (e) $- V_{dc}$ mode, (f) $- \frac{2}{3} V_{dc}$ mode, (g) $- \frac{1}{3} V_{dc}$ mode, (h) $0 V_{dc}$ mode.
A modified converter similar to the structure of the MLI in Figure 3 was proposed [39]. This MLI has two isolated DC sources or capacitors and uses eight bidirectional conduction switching devices. A bidirectional conduction scheme is used for switching devices, but due to the presence of an anti-parallel diode, it only blocks voltage in one direction. The proposed topology allows the use of two separate DC sources, either from PV systems, battery banks, or rectifier circuits. An improved five-level T-MLI was developed based on the method of hysteresis current (HC) to control the inverter [40]. The hysteresis levels are used to provide switching signals for the transistors in T-MLIs. This design is similar to those in Figures 2 and 6, but the T-branch contains only one bidirectional switch consisting of two IGBTs connected at their gates. This inverter has only two balancing capacitors on its DC link side. The switches in the T-branch of a five-level inverter can be replaced by a short circuit and are not connected to the HB [35]. There are two switching transistors connected in parallel to the HB, and the T-branch is connected to both switching transistors. Also, there are two transistors connected in series with the DC source at their ends. In this inverter, the number of switching devices is increased by 33.33% for the MLI in Figure 2 and by 60% for the MLI in Figure 6.

The topology of the three-level inverter includes an HB inverter and two bidirectional switching devices, as shown in Figure 7. Its five-level version is included as well [41]. The bidirectional switches are linked to the HB to generate the third stage of the inverter output. Other IGBTs are incorporated into the inverter circuit to increase the number of levels. The two portions of this MLI operate at high and low frequencies, resulting in a multi-level hybrid switching frequency T-MLI. Here, the switching devices in the HB work at a 50 Hz switching frequency. The bidirectional switching devices can work at frequencies up to 10 kHz [42].

**Figure 5.** Another Seven-level inverter topology.

**Figure 6.** Five-level inverter with a bidirectional switch.
A five-level inverter structure is illustrated in Figure 8. This inverter includes four capacitors (C1–C4), eight power switches, and two diodes (D1, D2) [43]. The mechanism of this topology is according to the switched capacitor principle. The T-structure of the inverter topology has four switches (S1, S2, S1, and S22). Output voltage polarity is determined through switches S1 and S2. SU1, SU2, SL1, and SL2 are responsible for increasing the number of levels of the output voltage from three to five. In comparison with the inverter in Figure 2, the number of switching elements is increased by 33.33%.

Another modified T-MLI topology is presented in Figure 9 [43]. The basic module is illustrated in Figure 9a, whereas the construction of a five-level inverter is shown in Figure 9b. There are four DC sources, which can be substituted by balancing capacitors, and the number of switching devices is eight. From this design, the neutral is located at point N. Point (A) represents the output side, which is connected to the load when the switching devices SH, S0, or SL are in the ON state. The performance of this five-level inverter modification is due to the SH1 and SL1 switches. When SH2 or SL2 are in the ON state, they must tolerate negative voltages.
Another modified T-MLI topology is presented in Figure 9 [43]. The basic module is illustrated in Figure 9a, whereas the construction of a five-level inverter is shown in Figure 9b. There are four DC sources, which can be substituted by balancing capacitors, and the number of switching devices is eight. From this design, the neutral is located at point N. Point (A) represents the output side, which is connected to the load when the switching devices $S_{H_1}, S_{0},$ or $S_{L_1}$ are in the ON state. The performance of this five-level inverter modification is due to the $S_{H_1}$ and $S_{L_1}$ switches. When $S_{H_2}$ or $S_{L_2}$ are in the ON state, they must tolerate negative voltages.

3.2. Complex Designs

Normally, the complex designs of T-MLIs are accompanied with an increase in the number of levels of the MLI output voltage to more than seven. Generally, most of the simple topologies of Section 3.1 can be maximized as nine-level inverters or even more levels [44]. A nine-level inverter is proposed in [45] and shown in Figure 10. It is based on the cascading modules of a T-type switched capacitor. The switched capacitors are enabled by a step-by-step charging method to attain voltage gain and high levels of output voltage. Furthermore, the inversion process is achieved without using an HB portion, which greatly decreases the number of switches. The proposed topology of this nine-level inverter can be constructed using only ten switches. Voltage gain is increased by two times. The nine levels of the output voltage are arranged as $(+2 V_{dc}, +1.5 V_{dc}, + V_{dc}, +0.5 V_{dc}, 0 V_{dc}, -0.5 V_{dc}, -V_{dc}, -1.5 V_{dc}$ and $-2 V_{dc})$.

A basic segment is formed by a back-to-back (BTB) connection with a modified T-shaped and half-bridge inverter (BBTHB), as shown in Figure 11a [46]. The HB portion of an inverter is linked to points A and B, which are shown in Figure 11b. There are five DC power sources at different voltage levels. The concept of this topology is to fabricate a new MLI structure with more output voltage levels but utilizing fewer switching devices. The proposed power circuit of the BBTHB module is shown in Figure 11c. This inverter topology can generate up to 31 voltage levels with five DC power sources using 12 power switches. It can provide negative levels without involving an HB. Table 1 illustrates the possible ON and OFF states of this T-type inverter. This topology exhibits both the negative and positive voltage levels through switches $S_1, S_{1_1}, S_2$ and $S_{2_2}$. Simply, the voltage drop at the switches is due to a conduction process. Unidirectional switches $S_1, S_{1_1}, S_2, S_{2_2}, S_3, S_{3_3}, S_4, S_{4_4}, T_1, T_{1_1}, T_2,$ and are activated in the reverse modes to avoid shorting the DC power supply.

The topology proposed by [47] introduces a hybrid T-Type (HT) type MLI. This topology consists of 12 diodes and switching devices and five DC power sources. Eleven voltage levels can be generated by this MLI, which are (one zero-level, five negative-levels, and five positive-levels) in a symmetric configuration with no HB module.

The concept of this topology utilizes different sides of the DC power sources to create different routes that are coupled with the other DC sources, as shown in Figure 12. The switch set $(S_5, S_6, S_7, S_8)$ is coupled with the (VC3M) DC source. Nearby switches $(S_1 - S_4, S_9,$ and $S_{10})$ work together for different levels of voltage generation. $S_9$ and
S10 are bidirectional switches mounted in both T-type modules at each side to prevent short-circuiting between the four DC sources (VDC1L, VDC2L, VDC1R, and VDC2R).

In [48], there is an MLI that shows some structural similarity to the proposed topology in [47], but using three modules. T-type modules are located at each end of the topology, denoted as T and T’. Switching devices, Sti and Sti’, where (i = 1...5), are utilized in these modules. Other modules, or switching devices, are positioned between the T-type configurations using interconnecting structures for scalable topologies. To step up the MLI AC voltage N times, several DC sources are required, [(N/2)−1], with a cross module for each module and two capacitors.

**Figure 10.** A nine-level inverter based on cascading of T-Type modules.

**Figure 11.** A modified T-MLI, (a) modified T-type converter, (b) modified T-type inverter, and (c) BBTHB proposed structure.
Table 1. Output voltage and switch status for a modified 15-level T-MLI.

<table>
<thead>
<tr>
<th>Level of the Output Voltage</th>
<th>S1</th>
<th>S2</th>
<th>S3</th>
<th>T1</th>
<th>T1_1</th>
<th>T2</th>
<th>T2_2</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{dc1} + V_{dc2} + V_{dc3})</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(V_{dc2} + V_{dc3})</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(V_{dc1} + V_{dc3})</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(V_{dc3})</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(V_{dc1} + V_{dc2})</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(V_{dc2})</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(V_{dc1})</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(V_{dc2})</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(V_{dc3})</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>(-V_{dc1} + V_{dc2})</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>(-V_{dc3})</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>(-V_{dc1} - V_{dc3})</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>(-V_{dc2} - V_{dc3})</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>(-V_{dc1} - V_{dc2} - V_{dc3})</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 12. A single-phase 11-level HT-type multilevel inverter.

The work of [49] presents a new and different module for asymmetric MLI inverters with fewer elements. This involves a square arrangement of two BTB T-MLIs with other switching devices. A square T-type (ST-type) portion creates seventeen levels using twelve switching devices and four different DC supplies having two voltage levels (three VDC and one VDC). The two strategies can also be expanded in a cascading arrangement to achieve even more levels. ST-type modules can be formed by connecting two T-connectors BTB from points A, B, and C. This means one bidirectional switch from point B, and two unidirectional switching devices should be added from points C and A, as shown in Figure 13. The intermediate circuits are assumed to have respective voltages of one VDC and three VDC for the first and second T-connections. This design is used for an MLI (with different ratios of intermediate circuits) to produce various numbers of output voltage levels and fewer switching devices.
In [48], there is an MLI that shows some structural similarity to the proposed topology in [47], but using three modules. T-type modules are located at each end of the topology, denoted as T and T’. Switching devices, St i and St i’ where (i = 1...5), are utilized in these modules. Other modules, or switching devices, are positioned between the T-type configurations using interconnecting structures for scalable topologies. To step up the MLI AC voltage N times, several DC sources are required, [(N/2) – 1], with a cross module for each module and two capacitors.

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Table 2 represents a comparison among the different T-Type MLIs that are discussed. A comparison is made between the number of switching devices for each MLI topology, the number of DC sources, the number of DC-link capacitors, the availability of switching modules, and blocking diodes. Some of the topologies can be extended for a higher number of levels (N) as in [31,32,34,36,41], but others are intended for the proposed number of levels [43–47,49]. Also, most of them have to balance the voltage across DC capacitors connected with a single DC source. In the rest of the topologies, DC capacitors are replaced by several DC sources. Few of them have switching modules, which are a combination of two opposite switching devices triggered by a single pulse at the same time. Each switch is an IGBT connected with an anti-parallel diode. Blocking diodes are also employed in most of the topologies to control the current path for the required instantaneous voltage level. The efficient inverter topology is that which has a low number of components and provides a possibly high number of levels for its output voltage. The selection of the efficient inverter topology is tied to that which has a low number of components and provides a possibly high number of levels for its output voltage.

Table 2. Comparison between different T-Type MLI topologies.

<table>
<thead>
<tr>
<th>Ref. No.</th>
<th>Number of Switching Devices</th>
<th>Number of Voltage Sources</th>
<th>Number of DC-Link Capacitors</th>
<th>Switching Modules</th>
<th>Blocking Diodes</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31]</td>
<td>1 + N</td>
<td>1</td>
<td>(\frac{N-1}{2})</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[32]</td>
<td>1 + N</td>
<td>1</td>
<td>(\frac{N-1}{2})</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>[34]</td>
<td>1 + N</td>
<td>1</td>
<td>(\frac{N-1}{2})</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[36]</td>
<td>2.5 + 0.5 N</td>
<td>1</td>
<td>(\frac{N-1}{2})</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>[41]</td>
<td>3 + N</td>
<td>(\frac{N-1}{2})</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[42]</td>
<td>8 for five-level</td>
<td>1</td>
<td>2</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>[43]</td>
<td>8 for five-level</td>
<td>4 for five-level</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>[45]</td>
<td>10 for nine-level</td>
<td>1</td>
<td>4 for nine-level</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[46]</td>
<td>12 for fifteen-level</td>
<td>4 for fifteen-level</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>[47]</td>
<td>12 for eleven-level</td>
<td>4 for eleven-level</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>[49]</td>
<td>12 for seventeen-level</td>
<td>4 for seventeen-level</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

4. Modulation Techniques

The essential aim of a modulation technique is to provide synchronized pulses for each switching device of an MLI [50]. Also, they are used to decrease the harmonic content of the output current and voltage waveforms. Normally, the application of modulation techniques is made to every class of MLIs, not only T-MLIs. Figure 14 presents the modulation
techniques that most researchers and manufacturers have followed in their MLI designs for many years [51–54].

Figure 14. Modulation techniques of single-phase MLIs.

4.1. SPWM by Multi-Carriers

Sinusoidal PWM or SPWM is the modulation technique most used for single- and three-phase inverters. SPWM can be used for MLIs in many ways. In this section, the SPWM is used based on a comparison among several saw-tooth or triangular carriers at high frequency and one sine wave as a reference (modulating) signal at a fundamental frequency. Normally, for a three-level MLI, two carriers are required. For a five-level inverter, four carriers are needed, and for a seven-level inverter, six carriers are required, i.e., for an N-level inverter, N−1 carriers are required [55,56]. Then the number of carriers can be reduced to \( N - \frac{1}{2} \) if a sine wave reference signal is replaced by its absolute function, i.e., a reference signal of \(|\sin(x)|\). SPWM by multiple carriers can be classified as follows.

4.1.1. PD, POD, and APOD

In the phase disposition (PD) technique, all the triangular waveform carriers have the same phase, frequency, and waveform amplitude but they are set at different locations, as shown in Figure 15a. The major harmonic contents are induced at the carrier frequency [57,58]. In this method, only odd harmonics result [10]. Modulation in the PD technique can be used for an MLI with asymmetric topology as well [59,60]. In the phase opposition disposition (POD) technique, all the triangular waveform carriers are out of phase by \((180^\circ)\). The frequency and waveform amplitude are the same for all carriers, but they are at different locations, as shown in Figure 15b [61]. In the alternative phase opposition disposition (APOD) technique, the carrier’s waveform is alternatively displaced in phase by \(180^\circ\), as shown in Figure 15c.

4.1.2. PSPWM

The phase-shifted (PSPWM) is an SPWM technique that uses multicarrier modulation. In this technique, each triangular carrier waveform has the same peak amplitude and frequency, but between any two adjacent carrier waves, there is a phase shift given by \( \Phi_c = \frac{360}{N} \) where \( N \) is the voltage level of an MLI [62–64]. For a five-level inverter, there is a phase displacement of \(90^\circ\) for any two adjacent carriers since four triangular carriers are required, as shown in Figure 15d.
Figure 15. SPWM modulation techniques for five-level inverter: (a) PD, (b) POD, (c) APOD, (d) PSPWM, (e) RPWM, and (f) multi references PWM.

4.1.2. PSPWM

The phase-shifted (PSPWM) is an SPWM technique that uses multicarrier modulation. In this technique, each triangular carrier waveform has the same peak amplitude and frequency, but between any two adjacent carrier waves, there is a phase shift given by $\Phi_{cr} = \frac{\pi}{2(N-1)}$ where $N$ is the voltage level of an MLI [62–64]. For a five-level inverter, there is a phase displacement of 90° for any two adjacent carriers since four triangular carriers are required, as shown in Figure 15d.

4.1.3. RPWM

Random pulse width modulation (RPWM) is an SPWM technique that has become an essential tool for the mitigation of the harmonic effects of PWM inverters. This is a major improvement in the electromagnetic and acoustic noise from the output of RPWM inverters [65–68]. In this technique, a random number is compared with the sine wave signal or its absolute function, as shown in Figure 15e.

4.2. SPWM by Multi Reference Signals

In this modulation technique, there are only one or two triangular carrier waveforms and multi-reference signals that have the same frequency and phase, but their position is displaced. For a five-level inverter, there are two required sine wave references. For $N$-levels of the output voltage, $\frac{N-1}{2}$ sine wave reference signals are required, as shown in Figure 15f [69,70].

4.3. Selective Harmonics Elimination (SHE)

The PWM by SHE technique is made using a selective harmonic suppression scheme that relies on voltage waveforms in Fourier analysis. SHE determines an interval of the switching process that filters out unwanted output voltage harmonics and at the same time leaves the switching frequency unchanged.

For $N$-levels of the output voltage, the mathematical expression of the eliminated harmonics is $\frac{N-3}{2}$. For instance, to control a seven-level cascaded HB to reject the 5th and 7th harmonics, set the output phase voltages of each harmonic order to zero. A typical odd harmonic component and output phase voltage are expressed mathematically by Equations (1) and (2), respectively, and the odd harmonics and switching angles are as follows [71]:

$$\text{Odd Harmonic Component}$$

$$\text{Switching Angle}$$
For general output voltage,

$$V(\omega t) = \sum_{n=1,3,5,...}^{\infty} V_n \sin(n\omega t)$$  \hspace{1cm} (1)

The odd harmonic components,

$$V_n = \frac{4V_{dc}}{n\pi} \sum_{l=1}^{n} \cos(n\theta_l)$$  \hspace{1cm} (2)

For a seven-level inverter, the PWM by conventional SHE includes three switching angles. So, the nonlinear mathematical expressions are as follows:

$$\begin{align*}
\cos \alpha_1 + \cos \alpha_2 + \cos \alpha_3 - \frac{3\pi}{4} M &= 0 \\
\cos 5\alpha_1 + \cos 5\alpha_2 + \cos 5\alpha_3 &= 0 \\
\cos 7\alpha_1 + \cos 7\alpha_2 + \cos 7\alpha_3 &= 0
\end{align*}$$  \hspace{1cm} (3)

Also, the condition that the switching angles must fulfill is as follows:

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2}$$  \hspace{1cm} (4)

The optimal solutions of Equation (3) are found by taking into the consideration the constraints of Equation (4) through minimization of the objective function $F_1$ as follows:

$$F_1 = \sqrt{\frac{V_5^2 + V_7^2}{V_1}}$$  \hspace{1cm} (5)

where $\alpha_1, \ldots, \alpha_3$ are the switching angles, $V_1$, $V_5$, and $V_7$ represent the fundamental component, fifth component, and seventh component of the output voltage, respectively.

In comparison with the other modulation schemes, the use of SHEPWM technology in MLIs provides a higher-quality output voltage. In the output voltage waveform, tight control and a high output harmonic voltage are achieved while keeping the frequency of switching devices at a minimum. The projected drawback of SHE is the high amplitude of the first set of unwanted harmonics \cite{72–75}. The usage of numerical analysis for SHE for MLIs with a high number of levels is inefficient \cite{76–78}. Optimization techniques using artificial intelligence (AI) techniques have been used directly to solve these problems. The primary reason for using these algorithms is that they do not have long ranges and do not rely on any initial assumptions. Thus, they can reduce computational effort. Moreover, these optimization techniques easily work on low-cost DSPs. Some of the bioinspired algorithms include the genetic algorithm (GA), bee algorithm (BA), particle swarm optimization (PSO), and differential evolution (DE), among other techniques \cite{79}.

Nonlinearities in low-order harmonic equations can originate using objective functions. Typically, researchers utilize various objective functions to reduce harmonics. Various methods have been proposed to solve harmonic suppression problems \cite{80,81}.

### 4.4. Pre-Programmed PPPWM

The PPPWM formulation usually depends on certain waveform characteristics, such as unipolar, bipolar, step, multistep, symmetric, and asymmetric waveforms \cite{82–87}. All of these properties play the same significant role in analyzing and determining the shape and difficulty of a specific solution space. Figure 16 illustrates the common classification of PPPWM-type solutions. The SHE technique can be framed as a minimization function that seeks to eliminate the selected harmonics. The problem of selective harmonics mitigation (SHM) is often expressed as a minimization function that attempts to discover a global or local minimum rather than eliminating selected harmonics. It is sometimes formulated as a minimization function that provides a solution to create harmonic values and volt-
age/current so that the total harmonic distortion (THD) is below the limits of the applicable grid code [88–94].

Figure 16. PPPWM common classification types and formulations.

5. Output Voltage Control

The role of any modulation technique is to form the shape of the inverter output voltage so that it is as nearly a sinusoidal waveform as possible. However, these techniques and control methods can be merged to regulate the MLI output voltage. For MLIs, it is required that their output voltages have a constant root mean square (RMS) value at any load condition.

In most cases where an MLI is connected to a RES, during the normal operation of a wind turbine or PV system, the RES is variable in nature. Thus, maximum power point tracking (MPPT) methods [95–97] are employed to extract the maximum power from a RES, as depicted in Figure 17.

Figure 17. Voltage control for a T-MLI with a RES system.
To reach the maximum power point (MPP) during changes in weather conditions, the $V_{dc}$ of the MLIs is not fixed at a single value. To overcome this issue, voltage control methods are employed to regulate the MLI output voltage and achieve a constant-rated RMS voltage [98]. The common type of voltage control is performed using a proportional-integral (PI) controller. The value of the PI controller output ($u(t)$) is fed to a boost converter circuit, and an error signal, $e(t)$ is employed as follows [99]:

$$e(t) = SP - PV \quad (6)$$

$$u(t) = e(t) \times KP + \frac{KI}{T} \int e(t) dt \quad (7)$$

where $PV$ and $SP$ are the process variable and set point, respectively. $u(t)$ represents the controlling signal which is resulted from the operation of the PI controller. $KP$ represents the proportional gain, $KI$ is the integral gain, and $T$ represents the integration time constant. As shown in Figure 18, control of the output voltage ($Vo$) is performed by the feedback of $Vo$, load current ($I_{load}$), and inverter current ($IL$). A reference voltage signal is set and compared to $Vo$ [100]. The error produced from the comparison is sent to the first PI controller. This PI controller is tuned, and its gain is set. Then, it sends a conditioned signal and adds it to the $I_{load}$. The collected signal is compared with the $IL$ to produce the output current error. This error is sent to a second PI controller. The produced control signal is added with the $Vo$ feedback signal to produce the main modulated signal.

Another method of controlling the $Vo$ of an MLI is a sliding mode control (SMC). This was first presented in the 1950s by Russian engineers. It is a nonlinear controller primarily designed for the control of systems with variable geometry [101]. Its switching system time-dependent equation is as follows:

$$\dot{x}(t) = g(x(t)) + \varphi(x(t)) \times u(t) \quad (8)$$

where $x(t)$ is a state variable, $u(t)$ is the controller input variable, $g(x(t))$ and $\varphi(x(t))$ are smooth vector fields in the same space [102]. In the case of a state-space environment, SMC can slide state variables of the system on a particular sliding surface. There are many kinds of slide mode controllers such as first order, second order, integral, and super-twisting, among others [101]. In the case of a first order SMC, the sliding surface is identified as follows:

$$\sigma = x_1 + c x_1 \quad (9)$$

where $\sigma$ is a sliding variable, $x_1$ and $x_2$ are state variables, and $c$ is a constant, where $c > 1$.

In a first order SMC, the controlling variable ($u$) is determined as follows:

$$u = -\rho \text{sign}(\sigma) \quad (10)$$

where

$$\text{sign}(x) = \begin{cases} 1 & \text{if } x > 0 \\ -1 & \text{if } x < 0 \end{cases}$$

In a second order SMC, the sliding variable ($\sigma$) is calculated via the following formula:

$$\sigma = \dot{x}_1 + c |x_1|^\frac{3}{2} \text{sign} (x_1) \quad (11)$$

There is a new curved sliding surface for single-phase UPS. This rotary sliding-mode controller is a combination of a traditional SMC and fuzzy logic controllers. The main advantages of the proposed technique are lower THD and better dynamic response of inverter output voltage and current compared to a conventional SMC [102]. A variant of SMC of a trinary hybrid MLI was implemented [103,104]. Figure 19 is a diagram of a trinary hybrid MLI. A dynamic performance investigation was performed in which the MLI output current almost instantly reached the reference current. In a second test, input
voltages from 130 V to 170 V were used. The output current did not vary from the reference current, but the voltage changed occasionally. The results of this SMC are compared with those of a PI controller. SMC has a significantly lower relative error, better SMC tuning response, and a larger perturbation clearance than a PI controller.

Another voltage control method was presented [105] for a five-level inverter. The stand-alone control scheme is separated into the following two parts: a power circuit and a control circuit. The former circuit consists of five power switches (S1-S5) and a power switch (D1) acting as a diode. The modulation technique is SPWM for power switching in the control circuit. A control circuit utilizes a reference sinusoidal signal and the actual signal from a voltage sensor. A reference signal is subtracted from the actual signal to generate an error signal. The error signal is input to a PI controller to generate a PI signal. Multiplying the PI signal by \(-1\) produces a minimum signal shifted by 180°. The reference PI and minimum signals are modulated using a carrier signal employing a comparator circuit in a control circuit that generates an SPWM signal for each power switch. A schematic of the power supply and control is shown in Figure 20.

**Figure 18.** Output voltage control of an MLI by PI controller.

**Figure 19.** Block diagram of a closed-loop variant of SMC of a trinary hybrid MLI.

**Figure 20.** Control circuit of a five-level inverter.
AI methods are used to control the voltage of an MLI either with the integration of multiple control methods or individually, such as a fuzzy logic controller (FLC), interval type 2 FLC (IT2FLC), neural networks, PSO, or GA, among others [106–112].

6. Connecting T-MLIs to RES

As discussed above, the RES may be wind or solar energy, where electrical energy can be extracted by wind turbines or PV panels, respectively. Recently, the use of thermoelectric generators (TEG) in conjunction with solar PV panels has attracted interest in using infrared waves in the solar spectrum that are converted to heat in solar panels. They convert this heat into electricity by the Seebeck effect. TEG modules can operate autonomously or be integrated with solar panels, which leads to an increased system efficiency and reduced environmental impact [113–115]. The T-MLIs can be connected to RES to either supply loads or grids with AC voltage. In both cases, an MPPT method should be employed due to the intermittent nature of RES. There are the following two kinds of MPPT implementation: either by adding a DC/DC converter such as a boot, buck, or SEPIC converter, among others [116–120], or directly using an inverter, as shown in Figure 21. If DC/DC converters are involved, then the role of the inverter is to provide a constant AC voltage to loads or a grid. In this way, control of the inverter voltage is simple. However, if they are not involved, it is crucial to perform MPPT as well to control the inverter output voltage, and the control technique will be more complex [121–125].

Figure 21. Connection of T-MLI to RES by: (a) two stages (b) a single stage.

7. Output Voltage Filter Design

It is well established that the output voltage of MLIs has a staircase shape that is not a sinusoidal waveform. The role of an output voltage filter is to smooth the stairs and to produce a sinusoidal or semi-sinusoidal waveform. There are many kinds of passive filters that perform this function, such as LC, LCL, PI, or LLCL, among others. Their purpose is to reduce the THD % from the output voltage [126,127]. There are many ways to design filters. The design itself depends on the selection of the filter type, the modulation process, and the number of output voltage levels [128–130]. For the LC filter design, an inductor L
is used to filter current harmonics, and a capacitor C is used to filter voltage harmonics. For L and C calculation purposes, the peak output voltage value is selected depending on the number of levels appropriate for the DC source voltage [128]. The cutoff frequency $f_c$ should be 10% of the switching frequency $f_s$ where:

$$f_c = 10\% f_s$$

$$L = \frac{0.03 V_{dc}}{2\pi f_c I_{L \text{ max}}}$$

$$C = \frac{1}{(2\pi f_c)^2 L}$$

Before practical implementation, the design should be checked using a simulation software package to determine if slight modifications are required.

8. Challenges of Using T-MLIs

There are the following several challenges when using T-MLIs:

1. The main challenge of using T-MLI is in selecting their voltage-balancing capacitors on the DC link side. With an increasing number of output voltage levels, it is difficult to have the same voltage for all capacitors. In the case of unbalanced voltage levels of DC link capacitors, the output voltages will not be similar at all levels, which may lead to increased harmonics;

2. DC link capacitors should be of the type that is charged on both sides since the current can flow in either direction by changing the voltage from a positive value to one that is negative. Using unidirectional charging of capacitors or DC capacitors should be avoided since negative charging may overheat the capacitors and cause them to explode;

3. Selecting a proper voltage controller to regulate output voltage is important since, in most cases, these MLIs are supplied from a RES through DC/DC converters employing MPPT methods. Due to the variable nature of RES voltage, the DC link voltage should be sufficiently high, i.e., more than 1.5 times the rated DC link value. If the inverter provides 220 V AC, its DC link voltage is 311 V so, the DC link voltage should be 1.5 times this value. This is to allow flexible voltage control to regulate the output voltage level;

4. To increase the efficiency of a T-MLI, fewer switching devices should be used, which reflects the proper design topology of an MLI. Also, each switching device must be selected for low $\frac{dv}{dt}$ and $\frac{di}{dt}$ properties;

5. The reliability of power converters is highly dependent on the reliable operation of semiconductor components. For each MLI topology, the switching device voltage and current stresses should be tested and analyzed during switching transients under different load conditions. Peak device current, peak device voltage, peak rate of change of device current $\frac{di}{dt}$, and peak rate of change of device voltage $\frac{dv}{dt}$ during turn-on and turn-off transients are measured over a wide range of operating conditions. To reduce the heavy $\frac{di}{dt}$ and $\frac{dv}{dt}$, it is helpful to design a damping circuit suitable for this purpose;

6. Since these MLIs are practically implemented to reduce their size, microcontrollers can be inserted into their circuitry to perform modulation techniques and regulate output voltage without depending on ICs and sub-circuits that could, in turn, increase losses and hence increase device temperature, as well as increase its size. For higher numbers of levels and at high switching frequencies, the MLIs will suffer from several thermal issues due to switching losses. Also, during normal operation, MLIs are subject to many variations in electrical loadings, which, through the Joule effect, create cyclic thermal stresses within the assembly. Thermally induced failure modes are the main causes of power inverter reliability issues. Due to the fact that the module contains a stack of various materials, cyclic thermal variations may drive mechanical
strains, which are reduced by the mechanical cohesion of the assembly. Through the aging of the switching modules, these thermal effects may cause failure to it. The analysis of the thermal cycling frequency for the IGBT switching modules of the specific MLI topology can extend the time to failure by providing adequate cooling to the IGBT power modules [131–133]. Thus, the design of a good cooling and ventilation system is required where thermal cycling and ripples of temperature in low-frequency applications should be taken into consideration in the practical implementation of T-type MLIs.

9. Conclusions

A comprehensive survey of T-MLI topologies, modulation techniques, and their output voltage methods is presented. The aim of the present paper is to explore and compare the topologies of various simple and complex designs. For such MLIs, the selection of topology should be according to the system voltage (low or medium), types of loads, and whether the system is stand-alone or connected to the grid, as well as design complexity, as these impact physical size and cost. It is important to address the problems that face T-MLI for voltage balancing at DC link capacitors, the nature of the RES employed, the number of required levels, output voltage filtering requirements, PWM switching frequency, modulation techniques, and output voltage control method. From all the topologies, it can be concluded that T-MLIs with five or seven levels can be used for low-power applications, while nine levels and more can be used for higher-power applications. Under these scenarios, the MLI power losses will be low compared with the output loading power, which in turn increases its efficiency. The selection of a modulation technique is related to the design topology. Researchers must examine a variety of modulation techniques and compare them to determine which have low THD values.

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