Article

Hardware-in-the-Loop Testing for Protective Relays Using Real Time Digital Simulator (RTDS)

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Abstract: With the increasing size and complexity of power systems, it is crucial to have an effective protection system in place to ensure its reliability. One of the important components of the protection system are relays. It is important for a relay to operate dependably and securely so that any fault can be cleared in time to minimize damages to the power network. However, it is important to test a relay in a realistic environment before commissioning it to the network. Testing a relay in the actual network can be expensive with limited fault scenarios. Hence, Hardware-in-the-Loop (HIL) testing is an efficient method to perform closed-loop testing of a relay since numerous fault cases can be simulated to provide a realistic operating environment for the relay under test. This paper sheds light on the HIL testing done for protective relays using a sample distribution system using RTDS. Two SEL-351 relays have been used in this experiment, and proper settings for the relays are calculated for coordination. The paper also describes the procedure of configuring the relay and other RTDS components crucial for interfacing of the relay with RTDS. After test setup, a pre-fault, fault, and post-fault analysis was done for the system. The results obtained from these analyses are cross-checked with the event history of the two SEL-351 relays, obtained with AcSELerator Quickset software. This paper provides thorough information for researchers to replicate the presented study or to develop new HIL experiments. It can also help in developing a fundamental understanding of the HIL testing setup that can be further applied to a more complex power system.

Keywords: Hardware-in-the-Loop test; real time digital simulator; protective relay; overcurrent protection

1. Introduction

The power system in the modern era has evolved into large and complex interconnected systems which is composed of nonlinear and dynamic elements. The development of smart grids has led to wide-scale integration of numerous elements at different operation levels of the grid. This has created complexities in the system and operational challenges that can be resolved using real-time digital computation, and advanced sensors and communication technologies [1–3]. With the increased sophistication in the methods and equipment for testing, power system simulation tools can play a major role in the testing and analysis of the system.

Power system simulation methods are mainly classified in two types: offline simulation and real-time simulation. Offline simulation methods have limited ability to provide an accurate simulation for the behavior of real-life equipment and practical systems [4]. The real-time simulation technology can perform numerous complex operations on the power system as they consist of high-speed processors and can provide higher efficiency and performance. Recently, Hardware-in-the-Loop (HIL) simulation has gained popularity, as it can wedge the gap between the behavior of the simulated and real system. In HIL testing, the power system under study is represented by a simulation model on a real-time simulation platform, and the equipment under test is outside of the model but is linked to the simulation model through special Digital to Analog and Analog to Digital
cards and necessary sensors and amplifiers [4,5]. One of the biggest advantages of HIL is that it can reduce the risk of field errors in actual scenarios [6]. HIL testing allows for simulating a real scenario of the power system, such as a fault situation, and provides accurate data on handling such situations in the real world [7]. HIL simulation platform performs time domain simulation to generate transient waveforms that are encountered in many protection applications [8–10].

With the increased energy demand, it has become crucial to procure the demand in an economically and environmentally sustainable way. Due to this, the stability and safety limit of modern power grids are being pushed. To handle the surge and the pressure, utilities are adding sophisticated new schemes and devices to their networks [11]. Whenever a new equipment and controller is added to the system, it needs to be tested and tuned before adding it to the network. In this situation, HIL simulation can be used for analyzing the new equipment in the simulated model before commissioning in the field [4,5,12].

Over the years, real-time simulation has become popular among manufacturers and utilities to assist them in the study of behavior and operation of the power system, performing the closed-loop testing of new equipment, and developing new protection and control functions [11].

Out of all the functions performed by a real-time simulation system, this paper is concerned with performing closed-loop testing of directional overcurrent relays using RTDS. Closed-loop testing of equipment in a model power system can mimic the characteristics of the system in a realistic scenario. Hence, readily decipherable information can be obtained on the performance of the equipment. In closed-loop testing of the relay, the RTDS outputs voltage and currents signals that are fed to the relay, and the relay provides an output, i.e., a tripping signal to the RTDS to open the circuit breaker in the RTDS model to disconnect the faulted section, and the simulation continues with the updated model [13]. The closed loop setting is ideal for testing the coordination between multiple relays.

A directional overcurrent relay is one of the primary safety equipment used in a networked, non-radial electrical distribution system to ensure the reliable and efficient operation of the power system. This relay monitors the current flowing through the protected element and generates a trip signal to the circuit breaker in the case of an occurrence of a fault, i.e., when the current exceeds the value of pickup current in the relay [14].

Numerous studies have been conducted in the field of HIL testing. These studies have been performed for various power system equipment using different real-time simulation software. F. R. Adegbobun et al. conducted a HIL testing for a grid-connected PV system consisting of SEL-421 relay, to test the hardware compatibility and model reliability [7]. A performance analysis of relays was done by M. Afshar et al. for detection of high impedance faults using a RTDS. A 15-bus system was modeled in RSCAD with an arc model for the high impedance fault [15]. The authors of [16] proposed an improved numerical algorithm based on PSCAD/EMTDC simulation to eliminate the overreach issue in distance relay caused due to transients of the coupling capacitor voltage transformer. The authors proposed a prototype for distance relay that was tested using RTDS. The proposed relay had a faster operation speed and higher reliability. Y. S. Cho et al. designed a RSCAD model containing multi-function relay and mimic board to improve the understanding of the technology associated with the protection and operation of the power system [17]. K. H. So et al. performed a closed-loop testing for differential and distance relay using EMTP [18]. O. Dias et al. [19] and T. Ledwaba et al. [20] focused on the HIL testing of transmission network. In [19], a 500 kV Brazilian transmission network was protected using SEL-421 distance relays. The simulation was performed for two fault cases: permanent and transient faults. The results were also cross-checked with the available field data. The HIL testing using ABB RED 670, a differential relay for a 400 kV, 50 Hz transmission network was performed in [20]. They also studied the system dynamics with additional equipment, such as series capacitor. A non-linear programming based adaptive protection scheme for coordination of directional overcurrent relays in a 7-bus system was proposed in [21]. The
A three-phase fault (F) has been introduced in the system for the relays under study. The lengths of feeders are in miles, and the load ratings are given in kVA. A power factor of 0.9 is assumed for all the loads.

The rest of the paper is organized as follows: Section 2 describes the RSCAD model developed in RTDS for a five-bus system selected for this experiment. Section 3 describes the procedure to configure the SEL-351 relays before they are used for HIL testing. Section 4 explains the different relay schemes used in the HIL testing. Section 5 discusses the key components and procedures in interfacing of the relays with the RTDS. Section 6 presents the findings achieved for the work carried out in Sections 2–5. Section 7 concludes the methodology used for this research.

2. Development of a RTDS Model for the Five-Bus System

This section describes the development of an RTDS model of a five-bus system. The model is developed in power mode. Additionally, crucial components for interfacing relays under testing conditions with the model simulated with the RTDS will be shown.

2.1. Five-Bus System

Figure 1 depicts a five-bus system considered for protection. R1 and R2 are the two SEL-351 relays (i.e., directional overcurrent relays under study). SEL-351 relays can protect lines and equipment using phase, negative sequence, residual-ground, and neutral-ground overcurrent elements with directional control. The modeled system is a sample 12.47 kV (L-L RMS) overhead power distribution system. The lengths of feeders are in miles, and the load ratings are given in kVA. A power factor of 0.9 is assumed for all the loads. A three-phase fault (F) has been introduced in the system for the relays under study.

![Figure 1. System considered for protection.](image)

2.2. RTDS Model

The five-bus system shown in Figure 1 has been modeled for RTDS using the RSCAD software, as shown in Figures 2 and 3. The model has been divided into two modules for

...
Module 1 shows the RSCAD model developed for the five-bus system, and module 2 shows how the RTDS model interfaces with the relays. In reality, it is a single model containing both modules to perform the HIL testing.

The feeder lines shown in Figure 2 are labelled using the pi-section element in RSCAD. The feeder line impedances between each bus have been provided as input to the relevant pi-section model connecting them. A three-phase sinusoidal source of rating 12.47 kV line-to-line RMS voltage has been selected for the model. Four grounded R-L loads were connected to buses 2, 3, 4, and 5. A circuit breaker was added between source and bus 1 and another between bus 1 and bus 4. The feeder impedance matrix in ohms/mile was as follows:
Figure 3. Module 2 of the RSCAD model.

The feeder lines shown in Figure 2 are labelled using the pi-section element in RSCAD. The feeder line impedances between each bus have been provided as input to the relevant pi-section model connecting them. A three-phase sinusoidal source of rating 12.47 kV line-to-line RMS voltage has been selected for the model. Four grounded R-L loads were connected to buses 2, 3, 4, and 5. A circuit breaker was added between source and bus 1 and another between bus 1 and bus 4. The feeder impedance matrix in ohms/mile was as follows:

\[
\begin{bmatrix}
0.3465 + j1.0179 & 0.1560 + j0.5017 & 0.1580 + j0.4236 & 0.1560 + j0.5017 & 0.3375 + j1.0478 & 0.1535 + j0.3849 \\
0.1580 + j0.4236 & 0.1535 + j0.3849 & 0.3414 + j1.0348 \\
\end{bmatrix}
\]

The pre-fault rms current at R1 was 60.2 A, and fault current was 1770.0 A. The pre-fault rms current at R2 was 30.6 A, and the fault current was 1758.7 A.

The instantaneous overcurrent relay settings were calculated as follows. At R1, the tripping current was set as three times the pre-fault current: \(60.2 \times 3 / 120 = 1.51\) A secondary, where 120:1 was the CT ratio when using a CT tapped at 600:5. The fault current will be \(1770 / 120 = 14.75\) A secondary.

At R2, the tripping current was set as three times the pre-fault current: \(30.6 \times 3 / 120 = 0.77\) A secondary, where 120:1 was the CT ratio for a CT tapped at 600:5. The fault current will be \(1758.7 / 120 = 14.66\) A secondary, which will be used in setting the time dial for the inverse-time overcurrent protection elements, to achieve a proper coordination.

3. SEL-351 Relay Configuration

To configure the SEL-351 relay, SEL’s AcSELerator Quickset software was used. In this study, two SEL-351 relays were chosen. The configuration was done as follows. First, the communication between the computer and the relay was established. Then the as-found relay settings were read to the computer. In the ‘General settings’, the CT and PT ratio were set to 120 and 60 (12,470 / 60 = 207 V secondary L-L), respectively, for both the relays. The parameters in ‘Line Settings and Fault locator’ section, as shown in Figure 4, needed to be calculated as follows:

\[
Self \ impedance \ (Z_s) = \frac{average \ of \ the \ diagonal \ elements \ of \ feeder \ impedance \ matrix}{3} \quad (1)
\]

\[
Mutual \ impedance \ (Z_m) = \frac{average \ of \ non-diagonal \ elements \ of \ feeder \ impedance \ matrix}{6} \quad (2)
\]

where

\[
Z_{11} + Z_{22} + Z_{33}
\]

\[
Z_{12} + Z_{21} + Z_{13} + Z_{31} + Z_{23} + Z_{32}
\]
Elements’ can also be set as shown in Figure 5. Settings have been provided for R1, shown operating under instantaneous overcurrent scheme. In this case) as R2 is supposed to act first. 67P1D level for R2 will be set to zero as R2 is operating under instantaneous overcurrent scheme. R2 can be set in a similar way. The 50P1P level for R2 will be less than R1 (0.77 in this case) as explained in later sections. The Trip logic equation for R1 and R2 was set to 51PT under the IDMT overcurrent scheme in Figure 6. For R2, 50P1 was used under the instantaneous overcurrent scheme, and 67P1T was used for R1 under the definite-time overcurrent scheme.

\[
\text{Zero sequence primary impedance } (Z_{0p}) = Z_s + (2 \times Z_m) \quad (3)
\]

\[
\text{Positive sequence primary impedance } (Z_{1p}) = Z_s - Z_m \quad (4)
\]

\[
\text{Zero sequence secondary impedance } (Z_{0s}) = Z_{0p} \times \frac{\text{CT ratio}}{\text{PT ratio}} \quad (5)
\]

\[
\text{Positive sequence secondary impedance } (Z_{1s}) = Z_{1p} \times \frac{\text{CT ratio}}{\text{PT ratio}} \quad (6)
\]

The pickup current of 50P1P level 1 in the ‘Phase Instantaneous Overcurrent Elements’ and the value of ‘67P1D level 1’ in the ‘Phase Definite-Time Overcurrent Elements’ can also be set as shown in Figure 5. Settings have been provided for R1, shown in Figure 5. R2 can be set in a similar way. The 50P1P level for R2 will be less than R1 (0.77 in this case) as R2 is supposed to act first. 67P1D level for R2 will be set to zero as R2 is operating under instantaneous overcurrent scheme.

Another setting is the Trip logic equation, which will be 67P1T, 50P1, 51PT—to be explained in later sections. The Trip logic equation for R1 and R2 was set to 51PT under the IDMT overcurrent scheme in Figure 6. For R2, 50P1 was used under the instantaneous overcurrent scheme, and 67P1T was used for R1 under the definite-time overcurrent scheme.

After entering the desired relay settings, the settings were written to the relay.
4. Relay Schemes

This paper focuses on the following three different relay schemes.

4.1. Instantaneous Overcurrent Scheme

Under this scheme, there was no intentional time delay in operation of the relay. The relay acts as soon as the current exceeds the pickup current setting of the relay. Relay R2 in this experiment works on this scheme. The results shown for relay R2 in case 1 of Section 6.2 of this paper were obtained using the aforesaid scheme. The 50P1P level 1 element in the Phase Instantaneous Overcurrent Elements was set to three times the value of the pre-fault current as calculated in Section 2.2.

The Trip Logic Equation was set to 50P1.

4.2. Definite Time Overcurrent Scheme

The relay R1 used the definite time scheme. Under this scheme, a pick-up setting was selected for the relay R1 as done in the instantaneous overcurrent scheme. In addition to the pickup setting, a time-setting was also provided for R1. When the current exceeded the pickup setting, R1 was supposed to wait for the specified time setting before it could issue the trip signal. A time delay of 4 cycles was set for R1, i.e., 67P1D level 1 in the Phase Definite-Time Overcurrent Elements was set to 4.0 cycles. The results for R1 using this scheme can be seen in case 2 of Section 6.2 of this paper.

The Trip Logic Equation was set to 67P1T.

4.3. Inverse Definite Minimum Time (IDMT) Overcurrent Scheme

In inverse time scheme, the relay operation time was inversely proportional to the fault current, i.e., a faster operation for a bigger fault current. In this paper, this scheme was applied to both R1 and R2 in addition to the aforementioned two schemes. A coordination was done between the two relays, where the protected feeder had a primary protection (R2) and secondary protection (R1).

The following steps were required to set up a coordination scheme for the relays under study:

Step 1—When setting up coordination, start with the device that will be closest to the fault within the zone of protection, i.e., relay R2 in this study.

Step 2—Select the appropriate relay settings for both relays as shown in Table 1.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Relay R1</th>
<th>Relay R2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pickup current setting (51PP)</td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td>IDMT curve (51PC)</td>
<td>U3</td>
<td>U3</td>
</tr>
</tbody>
</table>

Table 1. Relay settings for coordination scheme.
Step 3—Calculate the operating time and time dial setting (51PTD) for both relay R1 and R2. Initially, the operating time of R2 will be calculated. The equation used to calculate the operating time is selected as per the IDMT curve (51PC) chosen for the relay. Since curve U3 has been selected for R2, the following formula (given in SEL-351’s instruction manual) will be used to calculate the operating time:

\[
t_{\text{operate}}^{R2} = 51PTD_{R2} \times \left(0.0963 + \frac{3.88}{M^2 - 1}\right)
\]  

(7)

where, M is a multiple of the pickup current setting, and 51PTD_{R2} is the time dial setting of R2. In this experiment, for R2, the value of M is 29.32 (14.66 / 0.5, where 0.5 is the pickup current setting of R2) (see Section 2.2), and the value of 51PTD is 1. Hence, the operating time of relay R2 will be as follows:

\[
t_{\text{operate}}^{R2} = 1 \times \left(0.0963 + \frac{3.88}{29.32^2 - 1}\right) = 0.101 \text{ seconds}
\]  

(8)

Step 4—To calculate the operating time of R1, determine the operating time of R2 and a Coordination Interval (CI) between both relays. CI is required to ensure proper coordination with upstream devices (R1 in this case). It ensures that R2 has enough time to operate before R1 begins to operate.

A CI typically consists of relay/element operate time (pickup/tolerance), relay output operate time, breaker operate time, and a safety margin. Generally, CI ranges between 0.2 and 0.5 s for a distribution system. For this experiment, CI was taken as 0.3 s. Thus, the operating time of R1 was given as follows:

\[
t_{\text{operate}}^{R1} = t_{\text{operate}}^{R2} + CI = 0.101 + 0.3 = 0.401 \text{ seconds}
\]  

(9)

Step 5—Using the parameters in step 3 and 4, calculate 51PTD of R1 as follows:

\[
51PTD_{R1} = \frac{t_{\text{operate}}^{R1}}{0.0963 + \frac{3.88}{M^2 - 1}} = \frac{0.401}{0.0963 + \frac{3.88}{14.75^2 - 1}} = 3.51
\]  

(10)

where M is 14.75 (14.75/1, where 1 is the pickup current setting of R1), as calculated in Section 2.2.

The IDMT curve (i.e., operating time v/s fault current for relay R1 and R2 for a U3 curve setting) can be plotted as shown in Figure 7.

Different curve types, pickups, or time dials can be chosen to adjust the curves shapes to achieve different coordination margins.
Figure 7. Relay operating time v/s Fault current for the inverse time scheme.

5. Interfacing Relays with RTDS

Figure 8 illustrates the setup for Hardware-in-the-Loop testing of SEL-351 relay using RTDS for the five-bus system. Figure 9 shows the functional block diagram for the HIL setup.

As it can be observed from Figure 9, two circuit breakers, CB1 and CB2, were used in the power system under study. CB1 was used for relay R1, and CB2 was used for R2. To
connect both relays, R1 and R2, with RTDS, we required the Giga-Transceiver Analogue Output (GTAO) card and Gigabit-Transceiver Front Panel Interface (GTFPI) card provided in the RTDS. The GTAO provided analog signals, which could then be fed to a relay through an amplifier or through the low-level interface of the relay. In this study, we performed experiments using both the low-level interface method and CMS 356 (i.e., the amplifier). For successful implementation, one must consider the relay’s low-level interface scales, the current and potential transformer turns ratio, and the GTAO voltage and current scales. The GTAO provided the modeled system output to the relay, and when a fault was simulated, the relay sent a trip signal to the GTFPI card that in turn signaled the circuit breaker, which modified the simulation model, thus forming a closed-loop system. R1 here was to serve as a backup relay for faults within the protection zone of R2. When the fault occurs, R2 was supposed to act first to clear the fault. However, in case of failure of R2, R1 must act after a specified coordination delay, e.g., 4 cycles.

![Figure 9. Block diagram for HIL setup.](image)

In Figure 9, the Amplifier refers to external devices, such as the Omicron CMS 356, which can convert RTDS low current and voltage signals (0–5 V rms) to higher current and voltage signals (0–5 A, 0–120 V rms) that are at the same level of actual CT and VT signals that can be fed to the tested relays’ current and voltage input terminals on the backside without using the relay’s low-level signal interface.

Sections 5.1 and 5.2 provide a detailed description about the configuration of GTA0 and GTFPI card, respectively, to perform their assigned operations shown in Figure 9.

5.1. GTA0 Card

The GTA0 card can be modelled in the RSCAD software using the GTA0 element as shown in Figure 10. A GTA0 card has 16 input ports. For our experiment, we needed 14 ports. In Figure 10, port 1 to 7 were the current and voltage inputs for relay R2, and port 8 to 14 were the current and voltage inputs for relay R1. The GTA0 card took these inputs and provided analogue outputs to the relay input port. In Figures 9 and 10, Ia, Ib, and Ic were the input phase currents for R2, and Ia_R1, Ib_R1, and Ic_R1 were the input phase...
currents for R1. In and In_R1 were the neutral currents for R2 and R1, respectively. At bus 1, ‘phase1Asamp’ (Va), ‘phase2Asamp’ (Vb) and ‘phase3Asamp’ (Vc) were the phase voltages.

![GTAO element in the RSCAD model](image)

Figure 10. GTA0 element in the RSCAD model.

The connections shown in Figure 10 were determined as per the highlighted connections given on the relay low-level test interface as shown in Figure 11. The rightmost parameter ‘IA’ given on the relay panel was considered as the connection on the input port 1 on the GTA0 element shown in Figure 10 for relay R2 and so on. As observed from highlighted area in Figure 11, the first four parameters were for currents, and the rest were for voltages. Not following the given connection pattern will result in errors in values on the relay front panel.

![Low–level test interface for SEL–351 relay](image)

Figure 11. Low–level test interface for SEL–351 relay.

The above-mentioned parameters were sampled using a sampling frequency of 7.68 kHz before being provided as an input to the GTA0 card. This can be done using the sampler element provided in the RSCAD library as shown in Figure 12.
5.1.1. GTAO Scaling When Using Relay’s Low-Level Interface

The input parameters shown in Figure 10 needed to be scaled to a value within ±5 V before being sent as input to the GTAO card. These values were internally scaled in the GTAO element. This section discusses the process of obtaining the scaling factor for input currents and voltages for GTAO. When providing the output of the GTAO card to the relay, it is also important to consider the scaling factors of the relay. The scaling factors available for SEL-351 relay can be seen in Table 2. Initially, the required GTAO output voltages were calculated using the relay scaling factors, Current Transformer Ratio (CTR), and Potential Transformer Ratio (PTR). Then, these voltages were used to calculate the current and voltage scaling factors for the GTAO card.

Figure 13 shows the connection on the relay end between the GTAO card of the RTDS and relay. J1 was the terminal connector for input module of the relay, and J10 was the terminal for the processing module of the relay. J10 received the input secondary current and voltage parameters from the GTAO. After receiving the input secondary values, the processing module converted these values to primary values as per the relay scaling factor, CTR and PTR. These primary values could be verified on the relay front panel. Figure 14 shows the connection made on the GTAO card to provide output current and voltage values to the relay. The bottom most port of the card was the first output port of the card. The connections shown here were made as per the connection diagram shown in Figures 10 and 11. Port 1 to 7 were the output values provided to relay R2, and port 8 to 14 were the output values provided to relay R1.
Connections shown in Figures 13 and 14 were done for both relays shown in Figure 15. We also tested using the CMS 356 to power Relay R2, as shown in Figure 8.

Table 2. Scaling factors for SEL-351 relay.

<table>
<thead>
<tr>
<th>Input Channels (Relay Rear Panel)</th>
<th>Input Channel Nominal Rating</th>
<th>Input Value</th>
<th>Corresponding J1 Output Value</th>
<th>Scale Factor (Input/Output) (A/V or V/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IA, IB, IC, IN</td>
<td>1 A</td>
<td>1 A</td>
<td>100 mV</td>
<td>10</td>
</tr>
<tr>
<td>IA, IB, IC, IN</td>
<td>5 A</td>
<td>5 A</td>
<td>100 mV</td>
<td>50</td>
</tr>
<tr>
<td>IN</td>
<td>0.2 A</td>
<td>0.2 A</td>
<td>114.1 mV</td>
<td>1.753</td>
</tr>
<tr>
<td>IN</td>
<td>0.05 A</td>
<td>0.05 A</td>
<td>50 mV</td>
<td>1</td>
</tr>
<tr>
<td>VA, VB, VC, VS</td>
<td>150 V</td>
<td>67 VLN</td>
<td>1313.7 mV</td>
<td>51</td>
</tr>
<tr>
<td>VA, VB, VC, VS</td>
<td>300 V</td>
<td>134 VLN</td>
<td>1313.7 mV</td>
<td>102</td>
</tr>
<tr>
<td>Power (+, −)</td>
<td>48/125 Vdc or 125/120 Vdc</td>
<td>125 Vdc</td>
<td>1.25 Vdc</td>
<td>100</td>
</tr>
</tbody>
</table>

For the relays used in this study, a scaling factor of 50 for current and 102 for voltage in the relay was adopted.
Calculating Required Voltage Output from GTAO Card for Input Current Parameters

As an example, assume a fault current of 4000 A and follow the steps given below to calculate the required output from the GTAO card.

Step 1—Calculate the secondary side value of the fault current. In this case, the CTR is 120 (i.e., 120:1). Therefore,

\[
\text{Secondary relay current} = \frac{\text{Primary Current}}{\text{CTR}} = \frac{4000\, \text{A}}{120} = 33.33\, \text{A} \quad (11)
\]

This secondary relay current is then stepped down within the relay and converted to a mV signal used by the relay’s processor based upon the scale factors shown in Table 2.

Step 2—To calculate the required output voltage from the GTAO card, divide the secondary current by the scaling factor of the relay. In our case, the scale was 50, as shown in Table 2. Therefore,

\[
\text{GTAO output for current} (V_{\text{GOUTI}}) = \frac{\text{Secondary relay current}}{\text{Relay current scale factor}} = \frac{33.33}{50} = 0.67 \, \text{V} \quad (12)
\]

Calculating Required Output from GTAO Card for Input Voltage Parameters

For a pre-fault voltage of 10 kV, the required GTAO voltage output can be calculated as shown below.

Step 1—Calculate the value on the secondary side of the relay by dividing fault current by PTR. In our case, the PTR was 60 (i.e., 60:1). Therefore,

\[
\text{Secondary relay voltage} = \frac{10000\, \text{V}}{60} = 166.67 \, \text{V} \quad (13)
\]
This secondary relay voltage is then stepped down within the relay to a mV signal used by the relay’s processor based upon the scale factors shown in Table 2.

Step 2—To calculate the required output voltage from the GTAO card, divide the secondary voltage by the scaling factor of the relay. In this case, the scale factor was 102, as shown in Table 2. Therefore,

\[
\text{GTAO output for current (V_{GOUTI}) = \frac{\text{Secondary relay voltage}}{\text{Relay voltage scale factor}}} = \frac{166.67}{102} = 1.63V
\] (14)

After obtaining the required GTAO outputs, calculate the scaling factor for the GTAO card to ensure that the above calculated GTAO outputs are obtained at the output of the GTAO card. The following formulas can be used to calculate the scaling factor for the voltage and current signal:

\[
\text{GTAO output for voltage (V_{GOUTV})} = \frac{5}{V_{sf} \times 1000} \times V_{\text{actual (in volts)}} \quad (15)
\]

\[
\Rightarrow V_{sf} = \frac{5}{V_{GOUTV} \times 1000} \times V_{\text{actual (in volts)}} = \frac{5}{1.63 \times 1000} \times 10000 = 30.6
\]

or a more general equation is shown below that can be used to calculate \(V_{sf}\):

\[
\frac{5}{V_{sf} \times 1000} \times V_{\text{actual (in volts)}} \times S_V \times PTR = V_{\text{actual (in volts)}}
\] (16)

where \(S_V\) is the relay voltage scale factor, which is 102. Therefore, we have

\[
\frac{5}{V_{sf} \times 1000} \times V_{\text{actual (in volts)}} \times 102 \times 60 = V_{\text{actual (in volts)}}
\]

from which \(V_{sf}\) can be derived.

\[
\text{GTAO output for current (V_{GOUTI})} = \frac{5}{I_{sf} \times 1000} \times I_{\text{actual (in amperes)}} \quad (17)
\]

\[
\Rightarrow I_{sf} = \frac{5}{V_{GOUTI} \times 1000} \times I_{\text{actual (in amperes)}} = \frac{5}{0.67 \times 1000} \times 4000 = 30
\]

or a more general equation is shown below that can be used to calculate \(I_{sf}\):n

\[
\frac{5}{I_{sf} \times 1000} \times I_{\text{actual (in amperes)}} \times S_I \times CTR = I_{\text{actual (in amperes)}} \quad (18)
\]

where \(S_I\) is the relay current scale factor, which is 50. Therefore, we have

\[
\frac{5}{I_{sf} \times 1000} \times I_{\text{actual (in amperes)}} \times 50 \times 120 = I_{\text{actual (in amperes)}}
\]

from which \(I_{sf}\) can be derived.

Here, \(V_{sf}\) and \(I_{sf}\) are the scaling factors in the GTAO card for the voltage and current, respectively.

5.1.2. GTAO Scaling When Using CMS 356

The GTAO scaling was calculated differently when using CMS 356 in contrast with when using relay’s low-level interface.

In this study, the voltage amplification factor was 60 V/V, and the current amplification factor was 6.4 A/V for the CMS 356.
The GTAO scaling was calculated as follows. We have the following relationship between the GTAO output and the actual voltage and current:

\[
GTAO \text{ output for voltage } (V_{GOUT V}) = \frac{5}{V_s f \times 1000} \times V_{actual} \tag{19}
\]

\[
GTAO \text{ output for current } (V_{GOUT I}) = \frac{5}{I_s f \times 1000} \times I_{actual} \tag{20}
\]

The actual voltage is also expressed as:

\[
V_{actual} = V_{GOUT V} \times AMP_V \times PTR \tag{21}
\]

The actual current is expressed as:

\[
I_{actual} = V_{GOUT I} \times AMP_I \times CTR \tag{22}
\]

Here, PTR is Potential Transformer Ratio, and CTR is Current Transformer Ratio.

The GTAO scaling factor for voltage can be obtained by substituting Equation (3) in Equation (5).

\[
V_{actual} = \frac{5}{V_s f \times 1000} \times V_{actual} \times AMP_V \times PTR
\]

Therefore,

\[
V_s f = \frac{5 \times AMP_V \times PTR}{1000} \tag{23}
\]

Equation (7) can be used to calculate the GTAO scaling factor for voltage. For a PTR equal to 60 and \(AMP_V\) of 60, the \(V_s f\) will be as follows:

\[
V_s f = \frac{5 \times 60 \times 60}{1000} = 18
\]

The GTAO scaling factor for current can be obtained by substituting Equation (4) in Equation (6).

\[
I_{actual} = \frac{5}{I_s f \times 1000} \times I_{actual} \times AMP_I \times CTR
\]

Therefore,

\[
I_s f = \frac{5 \times AMP_I \times CTR}{1000} \tag{24}
\]

Equation (8) can be used to calculate the GTAO scaling factor for the current. For a CTR equal to 120 and \(AMP_I\) of 6.4, the \(I_s f\) will be as follows:

\[
I_s f = \frac{5 \times 6.4 \times 120}{1000} = 3.84
\]

5.2. Obtaining Readings on the Relay Front Panel

After getting the required output from the GTAO card, to show the reading on the relay front panel, i.e., the primary side value, multiply the GTAO output by the current or potential transformer ratio and the scaling factor of the relay. In case of using relay’s low-level interface, the formulae are shown below:

\[
\text{Relay voltage reading} = V_{GOUT V} \times \text{Relay scaling factor} \times PTR \tag{25}
\]

\[
\text{Relay current reading} = V_{GOUT I} \times \text{Relay scaling factor} \times CTR \tag{26}
\]

Table 3 shows the voltage output and scaling factors obtained for GTAO for our experiment. The current and voltage values shown in Table 3 were the pre-fault values.
obtained on the relay front panel using the GTAO scales shown in the table. The calculations were verified by the actual readings on the relay.

Table 3. Parameters for GTAO card.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Magnitude (RMS)</th>
<th>CTR</th>
<th>PTR</th>
<th>Relay Scale</th>
<th>GTAO Output</th>
<th>GTAO Scale</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current</td>
<td>30 A</td>
<td>120</td>
<td>-</td>
<td>50</td>
<td>0.67 V</td>
<td>30</td>
</tr>
<tr>
<td>Voltage</td>
<td>7133 V</td>
<td>-</td>
<td>60</td>
<td>102</td>
<td>1.63 V</td>
<td>30.6</td>
</tr>
</tbody>
</table>

When using CMS 356, the Relay reading would be calculated as the product of GTAO output and the CMS 356 amplification factor and the PT and CT ratio.

5.3. GTFPI Card

The GTFPI card was used to transmit the trip signal from the relay to the circuit breaker in the RSCAD model, as shown in Figure 16. The relay trip signal is transmitted from the relay to the RTDS digital interface panel, as shown in Figures 17 and 18.

![GTFPI element in RSCAD.](image1)

![Connection on relay back panel with digital interface panel of RTDS.](image2)

In Figure 16, ‘OUT 101’ and ‘OUT102’ are the trip signals from R1 and R2, respectively. ‘Inp_GTFPI’ is the input signal being provided from the GTFPI element. The input signal is a single word that can be converted into multiple logic outputs using a word/bit converter. The outputs of this converter are digital trip signals, i.e., logical outputs. These trip signals are then provided as an input to the digital interface panel provided on the front panel of RTDS, as shown in Figure 18. If there is only one trip signal, the converter is not required as only one port of the digital interface panel is needed. In the case of multiple trip signals, this converter is required as only one GTFPI element can be used in a RSCAD model, and this experiment required more than one port of the digital interface panel. Here, each port
was considered as one bit. Two input ports will capture the two trip signals. Hence, two bits were obtained using the converter.

Figure 17 shows the connections done on the relay back panel for providing input signals to the digital interface panel of RTDS. It can be observed from the figure that ‘OUT101’ terminal of the relay has two connections (i.e., one for trip signal and another for ground). However, in general, the first terminal of the relay was the input signal, and the second terminal was ground, unlike the relay shown in Figure 17.

![Figure 17. Connection on relay back panel with digital interface panel of RTDS.](image)

The connections coming from ‘OUT 101’ shown in Figure 17 were provided to the digital interface panel, as shown in Figure 18. As mentioned previously, two ports of the panel were used, i.e., one for relay R1 and one for relay R2. The input trip signal coming from relay was connected to the digital input channel on the panel, and the ground signal coming from relay was connected to the ground input on the panel.

5.4. Applying Faults to the System

Figure 19 shows the fault logic developed in RSCAD for the system. ‘SW1’, ‘SW2’, and ‘SW3’ were the switch elements in RSCAD, which denoted phases of the system. Each switch needed to be turned on to introduce the fault on the corresponding phase. For example, to apply a three-phase fault, all three switches must be turned on. Each fault type in RSCAD was assigned a binary value, which had a corresponding decimal value, as shown in Table 4. The three switches shown in Figure 19 were assigned a decimal value of 1, 2, and 4, respectively. The switch positions shown in Figure 19 indicate that a three-phase fault were introduced in the system. Alternatively, a three-phase fault can also be introduced by using a single switch having a decimal value of 7.

![Figure 18. Digital interface panel of RTDS receiving signal from relay.](image)

<table>
<thead>
<tr>
<th>Binary Value</th>
<th>Fault Type</th>
<th>Decimal</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>A-G</td>
<td>1</td>
</tr>
<tr>
<td>010</td>
<td>B-G</td>
<td>2</td>
</tr>
<tr>
<td>100</td>
<td>C-G</td>
<td>4</td>
</tr>
</tbody>
</table>
As shown in Figure 1, relay R1 is connected between the source and bus 1, and relay R2 is connected between bus 1 and bus 4. Thus, the phase voltages on bus 1, phase currents on the sending end of the feeder between bus 1 and bus 4, and bus 4 are of particular interest. The results have been obtained for the system for pre-fault, during fault, and post-fault period. The x-axis in Figures 21–29 (excluding Figure 23) represents time in seconds, and the multiple y axes represent different signals, which have been explained in the previous sections.

### 5.5. Circuit Breaker Logic

Figure 20 shows the circuit breaker logic, where ‘XCBR1open’ and ‘XCBR1close’ were the push buttons used to open and close the circuit breaker contacts, respectively. The initial status of the breaker was ‘closed’, which was assigned a logical input of 1. ‘OUT101’ was the trip signal coming from relay R1. The first OR-gate was assigned for opening the circuit breaker and, hence, had two inputs, which were ‘XCBR1open’ and ‘OUT101’. The output of the first OR-gate served as the input (S) to the S-R flip flop. The second OR-gate was assigned for closing circuit breaker contacts. Since this experiment was not concerned with the reclosing of the circuit breaker after the occurrence of a fault, the control signal ‘PROTIED_Reclose_R1’ was assigned a zero value. The output of the second OR-gate served as the second input (R) to the flip flop. The output (Q) of the flip flop passed through a timer block, which determined the duration of the operation of the circuit breaker.

The final output of the circuit breaker logic for relay R1, i.e., ‘BRK_R1’, was provided as an input to the circuit breaker element assigned for R1 in the model. Similar logic was used for relay R2 with its corresponding trip signal and breaker signal.

### Table 4. Cont.

<table>
<thead>
<tr>
<th>Binary Value</th>
<th>Fault Type</th>
<th>Decimal</th>
</tr>
</thead>
<tbody>
<tr>
<td>110</td>
<td>AB-G</td>
<td>6</td>
</tr>
<tr>
<td>011</td>
<td>BC-G</td>
<td>3</td>
</tr>
<tr>
<td>101</td>
<td>AC-G</td>
<td>5</td>
</tr>
<tr>
<td>111</td>
<td>ABC-G</td>
<td>7</td>
</tr>
</tbody>
</table>

The fault can be applied to the system using the push button titled ‘ApplyFLT’ as shown in Figure 19. The duration of the fault can be determined using a slider titled ‘FDUR’. The output of this logic system was a control signal ‘FLT’, which was provided as an input control signal to the fault block in the RSCAD model.

**Figure 19.** Fault logic.

**Figure 20.** Circuit breaker logic for relay R1.
6. Results

As shown in Figure 1, relay R1 is connected between the source and bus 1, and relay R2 is connected between bus 1 and bus 4. Thus, the phase voltages on bus 1, phase currents from the source, and the phase currents on the sending end of the feeder between bus 1 and bus 4 are of particular interest. The results have been obtained for the system for pre-fault, during fault, and post-fault period. The x-axis in Figures 21–29 (excluding Figure 23) represents time in seconds, and the multiple y axes represent different signals, which have been explained in the previous sections.

Figure 20. Circuit breaker logic for relay R1.

Figure 21. Current waveforms for pre-fault condition.

Figure 22. Voltage at bus 1 preceding the fault.
Figure 22. Voltage at bus 1 preceding the fault.

Figure 23. Applying fault to the system in RTDS environment.

Figure 24. Waveforms for fault condition when R2 operates—case 1.
Figure 25. Waveforms for fault condition when R1 operates—case 2.

Figure 26. Waveforms for post-fault condition when R2 operates—case 1.
Figure 27. Waveforms for post-fault condition when R1 operates—case 2.

Figure 28. Waveforms when relay R2 operates to clear the fault.

Figure 29. Waveforms when relay R1 operates to clear the fault.

6.1. Pre-Fault Period

Figure 21 depicts the waveforms for the pre-fault condition. The first y-axis shown in Figure 21 shows the sampled phase currents from source. The second y-axis denotes the
sampled phase currents between bus 1 and bus 4. The third y-axis shows the status of the circuit breaker for relay R1. The initial status of the signal is ‘high’, as the circuit breaker is initially closed. The fourth y-axis shows the trip signal of relay R1, whose initial status is ‘low’ as there is no fault present in the system. Axes 5 and 6 show the circuit breaker status of relay R2 and trip signal of relay R2, respectively.

Figure 22 shows the line-neutral voltage (in kV) at bus 1 during pre-fault period. ‘phase1Asamp’, ‘phase2Asamp’, and ‘phase3Asamp’ are the sampled voltages for phase A, B, and C, respectively, at bus 1.

6.2. Fault Period (Instantaneous and Definite Time Scheme)

A three-phase fault with fault resistance of 0.1 ohms for a duration of 8 cycles has been applied to the system. The fault is applied in the runtime module of RTDS using a red push button shown in Figure 23. The switches shown in Figure 23 are used to select the fault type as explained in Section 5.4.

The waveforms have been obtained for two cases. In case 1, R2 operates to remove the fault. For case 2, R2 is in open loop, and R1 is in closed loop. Case 2 is simulating the scenario where R2 has failed to trip for the fault.

Figure 24 shows the current waveform and trip signal for case 1. The first y-axis in Figure 24 shows the phase current between source and bus 1 during the fault period. It can be observed that the fault current is very high for the fault duration. The second y-axis shows the phase currents between bus 1 and bus 4 during the fault. As R2 operates to remove this fault, the circuit breaker signal of R1 is high and trip signal of R1 is low as shown in third and fourth y-axis, respectively. Conversely, as observed from the sixth y-axis, the trip signal for R2 goes from low to high when the fault occurs, giving the command to the circuit breaker to open its contact. The fifth y-axis shows the breaker signal status for R2 switching from high to low when the trip signal for R2 goes from low to high.

Figure 25 depicts the current waveforms and trip signal for case 2. As the relay R1 operates to remove this fault, the circuit breaker signal of R2 is high, and the trip signal of R2 is low, as shown in fifth and sixth y-axis of Figure 25, respectively. As observed from the fourth y-axis, the trip signal for R1 goes from low to high when a fault occurs, giving the command to the circuit breaker to open its contact. The third y-axis shows the breaker signal status for R1 switching from high to low when the trip signal for R1 goes from low to high. It can be observed from Figures 24 and 25 that when the relay sends the trip command, the circuit breaker opens immediately, but there is a small delay between opening of the circuit breaker and the current dropping to zero, which is characteristic of a real system.

6.3. Post-Fault Period

Figure 26 depicts the post-fault condition for case 1. The high-frequency components in the current waveforms are due to numerical chatter of RTDS simulation. As shown in the second y-axis in Figure 26, the post-fault values for sampled currents are approximately zero as the contacts of the circuit breaker for R2 are opened and does not reclose, as the reclose control signal has been set to zero in the circuit breaker logic. In the first y-axis, the phase source currents are reduced in comparison to the pre-fault condition as the feeder where the circuit breaker for relay R2 was deployed is now open, thus the source is now only supplying load on the remaining feeder. The trip signal of R2 remains high, and correspondingly, the status of circuit breaker of R2 is low because the breaker is still open.

Figure 27 shows the post-fault condition for case 2. In Figure 27, the trip signal of R1 remains high, and correspondingly, the status of the circuit breaker of R1 is low as the breaker is still open. Both phase currents are almost reduced to zero in this scenario as the breaker near the source is open.
6.4. Coordination between R1 and R2 (IDMT Scheme)

Given the operating times of R1 and R2 obtained in Section 4.3, the fault duration and the relay trip logic in this case has been modified from the one chosen for the instantaneous and definite time schemes. The fault duration has been changed to 0.637 s using the fault slider shown in Figure 19. The relay trip logic equation used in this case for both relays is 51PT. In the occurrence of a fault (three-phase fault in this case), R2 is supposed to act as per its operating time. In case of R2 failure, R1 will wait for the time duration specified by the coordination interval (CI) and then will act as per its operating time.

Case 1—When R2 operates

Figure 28 shows the waveforms when relay R2 operates to clear the fault. The first y-axis shows the phase currents between bus 1 and the source, and the second y-axis shows the phase currents between bus 1 and bus 4. When a three-phase fault occurs, the digital trip signal for R2 shown in the sixth y-axis goes from low to high, which in turn causes the circuit breaker signal for R2 on fifth y-axis to switch from high to low. It is observed that after a certain period, the trip signal again switches to a low value even though there is no reclosing performed in this experiment. It is because of the SELogic equations defined for R2 (referred to SEL-351’s instruction manual) which causes R2 to deenergize the trip output after a certain period. In the post-fault period, the phase currents between bus 1 and bus 4 shown in the second y-axis are zero as the breaker for R2 remains open. However, as seen in the first y-axis the post-fault currents between source and bus 1 are lower than the pre-fault period because even though breaker between bus 1 and bus 4 are open, the remaining feeder lines between bus 1, 2, and 3 are still operating.

Case 2—When R1 operates

When relay R2 fails to operate, R1 operates after specified CI to clear the fault. Figure 29 depicts the waveforms when R1 operates to clear the fault. It can be observed from Figure 29, the digital trip signal for relay R1 in the fourth y-axis switches from low to high while the trip signal of R2 still remains low as shown in the sixth y-axis. Correspondingly, the circuit breaker signal for R1 goes from high to low, shown in the third y-axis. In the post-fault period, all the phase currents between the source and bus 1 are zero as the breaker for R1 near the source remains open. In fourth y-axis, it can be observed as well that R1 is deenergized after some time, bringing the signal back to the ‘low’ state.

6.5. Relay Events

The software AcSElErator Quickset is used to retrieve the fault events from the two relays. Figures 30–32 depict the current, voltage, and trip signals, respectively, from R2 during the instantaneous scheme. Figures 33–35 show the current, voltage, and trip signals, respectively, from R1 during definite-time scheme. This section presents waveforms actually recorded by the relays to corroborate with RTDS simulation waveforms.

Figure 30 shows the phase currents for pre-fault, fault, and post-fault between bus 1 and bus 4 obtained from relay R2 when deployed in instantaneous scheme. The pre-fault event shown in Figure 30 is similar to the pre-fault period for R2 shown in Figure 21. The fault event obtained from Figure 30 matches the fault period for R2 shown in Figure 24 and similar post-fault event can be seen in Figure 26. These observations indicate that RTDS and relays operate correctly as expected from the model.

The phase voltages seen in relay event for R2 in Figure 31 are similar to the phase voltage waveforms shown in Figure 22 which confirms the voltage waveforms obtained from RTDS.

Figure 32 shows the trip signal generated by R2 as per the specified trip logic equation. When comparing the trip signals in Figure 32 with Figures 21 and 24, it can be noticed that they are similar and thus verified.

Figure 33 shows the phase currents for pre-fault, fault, and post-fault between bus 1 and bus 4 obtained from relay R1 when deployed in the definite-time scheme. The pre-fault event shown in Figure 33 aligns with the pre-fault period for R1 shown in Figure 25. The
fault event shown in Figure 33 matches the fault period for R1 shown in Figure 25 and similar post-fault event can be seen in Figure 27. This verifies the waveforms obtained for R1 from RTDS.

Figure 34 shows the voltages obtained at bus 1 when R1 is active. When compared with the voltage waveforms shown in Figure 22, it can be observed that they are similar, which verifies the waveforms obtained for R1 from RTDS.

The trip signal generated by R1 under definite-time scheme can be seen in Figure 35. When compared with the digital trip signals shown in Figures 21 and 25, a similar operation of R1 can be observed in pre-fault and fault condition.

Figure 36 shows the phase currents recorded for R2 when deployed under IDMT scheme. When compared with the waveforms shown in Figure 28, the waveforms match, which validates the current waveforms achieved for R2 from RTDS.

![Figure 30. Phase currents recorded by R2 under instantaneous scheme.](image1)

![Figure 31. Phase voltages recorded by R2 under instantaneous scheme.](image2)

![Figure 32. Trip logic and trip signal recorded by R2 under instantaneous scheme.](image3)

![Figure 33. Phase currents recorded by R1 under definite-time scheme.](image4)
Figure 33. Phase currents recorded by R1 under definite-time scheme. 

Figure 34. Phase voltages recorded by R1 under definite-time scheme. 

Figure 35. Trip logic and trip signal recorded by R1 under definite-time scheme. 

Figure 36. Event obtained for phase currents recorded by R2 under IDMT scheme. 

Under IDMT scheme, the relay operates as per the operating time set for it while relay configuration. The relay is supposed to trip after the specified fault duration. The aforesaid functioning can be observed in Figure 37. The similar functioning can also be observed in Figure 28 where R2 operates the clear the fault using IDMT scheme. This validates the waveforms obtained for R2 under IDMT scheme.

Figure 37. Trip signal generated by R2 under IDMT scheme. 

In case when R2 fails to operate, R1 will act as per its operating time calculated in Section 4.3. Figure 38 shows the event for phase currents obtained for R1. When compared with Figure 29, similar current waveforms can be seen for R1, which validates the phase current waveforms obtained for R1 in RTDS.
Figure 38. Event obtained for phase currents recorded by R1 under IDMT scheme.

Figure 39 shows the trip signal generated by R1 under IDMT scheme, which when compared with digital trip signal for R1 in Figure 29 verifies the RTDS waveforms.

Figure 39. Trip signal generated by R1 under IDMT scheme under IDMT scheme.

7. Conclusions

Hardware-in-the-Loop (HIL) testing plays an increasingly critical role in system design and deployment. There is a lack of literature for providing guidance on how HIL tests can be setup including the connection of various HIL platform components, external power amplifiers, and the equipment under test and how critical parameters, such as scaling factors are calculated.

This paper presents the Hardware-in-the-Loop (HIL) testing done for a five-bus system. This paper thoroughly illustrates the procedure and steps for performing HIL test using RTDS platform, Omicron amplifiers, and SEL 351 protective relays as examples. Different tripping schemes including the Instantaneous overcurrent, Definite time, and Inverse Definite Minimum Time (IDMT) scheme have been implemented. The test results obtained by the testing platform RTDS and those recorded by the relays are compared, and the comparison confirms that the experiments are correct, and the testing platform and setup are suitable for testing protective relays. It is expected that the test setup is generally suitable for testing other equipment, such as power inverters, controllers, and machines, and such transients-based testing provides a realistic environment to better design and test the equipment under test.

The procedure and framework presented in this paper will be useful for designing HIL experiments for research, education, and training purposes. In particular, the paper will provide guidance not only for students at universities, but also for professional engineers that intend to adopt and implement HIL tests.

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References


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