Article

A Voltage Doubler Boost Converter Circuit for Piezoelectric Energy Harvesting Systems

Abdul Haseeb 1,*, Mahesh Edla 2, Mustafa Ucgul 1, Fendy Santoso 1 and Mikio Deguchi 3

1 Faculty of Science and Engineering, Southern Cross University, East Lismore, NSW 2480, Australia
2 Department of Research and Development, Electronics Engineer, MYRA Corporate, Wollongbar Industrial Area, Alstonville, NSW 2477, Australia
3 Department of Electronics and Control Engineering, National Institute of Technology, Niihama College, Niihama 790-8570, Japan
* Correspondence: a.haseeb.10@student.scu.edu.au

Abstract: This paper describes the detailed modelling of a vibration-based miniature piezoelectric device (PD) and the analysis modes of operation and control of a voltage doubler boost converter (VDBC) circuit to find the PD’s optimal operating conditions. The proposed VDBC circuit integrates a conventional voltage doubler (VD) circuit with a step-up DC-DC converter circuit in modes 1–4, while a non-linear synchronisation procedure of a conventional boost converter circuit is employed in modes 5–6. This integration acted as the voltage boost circuit without utilising duty cycles and complex auxiliary switching components. In addition, the circuit does not require external trigger signals to turn on the bidirectional switches. This facilitates the operation of VDBC circuit at very low AC voltage ($V_{ac} \geq 0.5$ V). Besides this, the electrical characteristics of VDBC circuit’s input (i.e., PD) perfectly concurs with the studied testing scenarios using impedance power sources (mechanical shaker). Firstly, the proposed circuit which can rectify the PD’s output was tested at both constant input voltage with varying excitation frequency and constant excitation frequency with varying input voltage. Next, a small-scale solar battery was charged to validate the feasibility of the performance of the proposed VDBC circuit. The proposed circuit achieved a maximum output voltage of 11.7 V$_{dc}$ with an output power of 1.37 mW. In addition, the rectified voltage waveform is stable due to the sminimization of the ripples. In addition, the performance of VDBC circuit was verified by comparing the achieved results with previously published circuits in the literature. The results show that the proposed VDBC circuit outperformed existing units as described in the literature regarding output voltage and power. The developed rectifier circuit is suitable for various real-life applications such as energy harvesting and battery charging.

Keywords: piezoelectric energy harvesting; voltage doubler; boost converter; self-powered voltage boost converter; ripple reduction; rectifier

1. Introduction

A piezoelectric device [1–3] (PD) transforms the mechanical energy (ME) [1,4], which is available in the environment, into electrical energy (EE) [5,6] in the form of an alternating current (AC). Scientific researchers have had a surge in interest in piezoelectric energy harvesting (PEH) systems during the last decade [1,3,7,8]. However, the PD’s are constrained to limited power applications, usually on the scale of milliwatts and microwatts [9–14]. This is mainly due to its internal properties, namely internal capacitance and resistance [1,3,7,15]. They can resist high pressure but are small devices compared to the other electrical devices, which produce high amounts of current and voltage [16]. In addition, another concern is that high-frequency vibrations are required to efficiently exploit these PD’s, as they generate very low power and voltage due to their internal characteristics. However, most vibrations are expected to be in the range of 0.1–1 KHz [8], whereas a PD can function at...
several hundred kilohertz. Despite that, the primary objective of the PEH field is to power miniature electronic devices. However, the PD generates AC in the PEH system due to ambient vibrations in the environment.

Nevertheless, to operate electronic devices, the AC generated from the PD has to be transformed into direct current/voltage (DC) [3,7,15]. Consequently, the PEH entails a power converter circuit (i.e., rectifier circuit) for rectification, facilitating AC-DC conversion. Thus, the rectifier circuit plays a crucial role between the vibrating PD and the storage device in the PEH field.

A conventional full-bridge rectifier (FBR) circuit is the simplest technique for AC to DC conversion [13,14,17–23]. However, the FBR circuit exhibits inefficient conversion efficiency because of forward voltage [24,25] and $V_f$ losses across the diodes [17,26,27], while most power electronic devices require 3.3 V$_{dc}$. As a result, effective electronic circuits and active materials must be involved to overcome forward voltage issues and maximise the PD’s outcomes.

Various single [15,28–31] and two-stage [3,29,32,33] power conversion circuits have been described in the previous literature to overcome this issue. A single-stage circuit converts AC generated by the vibrating PD into DC, whereas a two-stage circuit confines two processes, such as AC to DC and DC to DC. A framework that explains the operation of PEH in both scenarios, termed single and two-stage power conversion circuits, is depicted in Figure 1.

![Figure 1](image.png)

Figure 1. A framework of PEH power-conversion circuits: (a) a single stage, (b) two-stage.

To attain effective optimisation and achieve maximum power at the output, Edla et al. [1,7,34] attempted to use minimal power electronic components in the H-Bridge rectifier (HBR) circuit. This research involved the congregation of high and low frequencies. Besides, the output voltage and power of the HBR circuit are higher than the conventional FBR circuit. This originates from the fact that the FBR circuit embodies diodes with forward voltage and $V_f$ losses of 0.6 V and 0.15 V. In addition, the rectified voltage waveform from the HBR circuit had fewer ripples. However, the rectified voltage output of the HBR circuit remained low, and the proposed research has not discussed the issue of ripple reduction in the rectified output voltage waveform in detail.

Later, Hsieh et al. [35] proposed a two-stage rectifier circuit to attain maximum output power at load. The proposed circuit comprised a maximum power extraction (MPE) circuit and a regulator for dual-stage circuit operations. To attain maximum power output across the battery, the proposed circuit controlled the switching frequency of the step-down
converter circuit by using a controller. Nevertheless, the switching losses were higher than the output power due to the switching frequency.

One other approach to attain maximum power at the output is employing a non-linear system and using external switches, namely, metal-oxide-semiconductor-field-effect-transistor (MOSFET), switching frequency, duty cycles, and passive electronic components, such as inductors and capacitors. A range of non-linear approaches was proposed by [17,22,36–42]. However, the preceding circuits were incorporated with auxiliary circuits, transformers, diodes, and bulky inductors. Thus, the power consumption in the used power electronic components is high, which is unsuitable for PEH applications.

Later, Shareef et al. [26] proposed a power electronic circuit to attain a rectifier-less AC-DC conversion by employing the synchronous process using an inductor. In addition, a cold-startup feature was also included in the proposed circuit to achieve the optimised output from the proposed circuitry. It achieved a gleaning output power of 254 µW at 0.65 mV ac input voltage. However, the proposed methodology was adamant, as it demanded subsidiary components, such as three capacitors, three PDs, a digital logic controller, a polarity detector, and an inductor of milli-range. Thus, the proposed circuit utilised high power and inflexibility in the PEH applications.

In addition, synchronised switching harvesting techniques were proposed by [17,27,43]. In comparison to the FBR circuit, the testing results significantly improved and boosted the input AC into high DC (i.e., output). Nevertheless, the method conceded additional components: an oscillator, polarity detector, controller, diodes, logic gates, and transformers. Consequently, the AC-DC conversion losses and power consumption of the proposed circuit were higher than the power generated by a PD. Additionally, it required high voltage to kickstart the conversion process.

Recently Jeong et al. [44,45] proposed an efficiency-based multi-output charging system to improve the overall conversion efficiency by adaptably dividing the input power across different PV cells based on their power level. This proposed methodology was useful when PV cells are partly shaded. In addition, the proposed system is implemented by adopting CMOS technology.

Edla et al. [1,19] recently conducted an experimental study where they facilitated an HBR circuit to a self-powered dual-stage HBR rectifier (DSHBR) circuit. Numerous high-frequency and high-voltage applications were carried out using the DSHBR circuit. The results verified that the DSHBR circuit successfully enhanced the output voltage and power compared to the HBR circuit. However, the proposed method incorporated an additional DC-DC converter and Zener diode, resulting in increased power losses, complex design, and high cost. In general, the DSHBR circuit generated low output power at load. However, the problems with ripples in the rectified voltage waveform are not fully covered.

Edla et al. [31] recently conducted an experimental study on HBRJT circuit to achieve high voltage gain by employing the Joule thief topology. The proposed HBRJT circuit congregated the HBR and Joule thief circuit for effective AC-DC power conversion with minimal circuit components. The circuit achieved a gleaning output of 13.5 V O with 0.51 mW output power. However, this topology ignored the issues of ripples in the gained output voltage. Besides, the winding losses in the transformer are not discussed.

Later, Zhao et al. [46] conducted an experimental study on developing an impedance model for a dual stage photovoltaic (PV) inverter. The proposed model was developed to achieve the impedance characteristics of PV as well as provide a solution for the potential stability of an inverter linked to a poor grid. The proposed model comprised of PV arrays, a boost converter and a backend inverter circuit, along with LCL output filter. The proposed study was also validated using PSCAD based simulation results.

Later, Yang et al. [47] proposed a conventional neural network based sub-dictionary predictor to optimise the conventional atomic decomposition algorithm for power quality disturbance signals. It is verified that the proposed methodologies successfully sminimised the need for additional computation sources while improving the accuracy of sub-dictionary predictor power quality signals.
It is worth emphasising that the vibrating PD generates a very low AC voltage. However, most power electronic devices require a minimum of 3.3 V\text{dc} with a stable DC voltage waveform. Nevertheless, the previous researchers [1,7,17,48–50] and in the abovementioned literature focused on size reduction, power optimisation, and minimising conversion losses, while fewer attempts have been made on ripple reduction and AC-DC conversion without employing external operating circuits and complex IC’s. Thus, there is a need for a more suitable power-conversion circuit that can minimise the usage of multiple diodes and employ a non-linear switching process that can boost the low AC voltage generated by the vibrating PD to high DC voltage with minimised ripples.

To overcome the abovementioned issues, the authors adopted a traditional voltage doubler (VD) circuit described in the literature [51,52] and extended it with the abovementioned features, such as boosting the low AC voltage to a high DC voltage, self-powered switching process. Therefore, the voltage doubler boost converter (VDBC) circuit is proposed, which is depicted in Figure 2b.

![Figure 2. Existing and proposed circuits: (a) VD and (b) VDBC. (M\textsubscript{1}–M\textsubscript{2}: MOSFET switches, D: Drain, G: Gate, S: Source).](image)

The proposed VDBC circuit minimises the usage of additional diodes to limit the forward voltage losses. It can increase the PD’s low input AC voltage to a high DC output voltage at different vibration frequencies. In addition, the proposed circuit also reduces the ripples in the rectified output voltage waveform and charges the solar battery continuously without employing the additional switching circuits.

The proposed VDBC circuit possesses six modes of operation. Modes 1–4 garnered the combination of a conventional VD circuit for the AC-DC conversion process with a step-up DC-DC converter for effective power conversion, while modes 5–6 include an improved non-linear synchronisation procedure of a conventional boost converter circuit [51,52], to mitigate ripples in the rectified voltage waveform. Besides, the proposed VDBC circuit is a self-powered switching approach, eliminating the need for additional switching components. Consequently, the losses are improved due to high power consumption and stress between the switches and parasitic components.

As this study reports to be an extension of a VD circuit [53] and previously published literature switching circuits [52], the proposed circuit is unique in the way that it implements the VDBC circuit to enhance the power flow towards the load capacitor, C\textsubscript{L3} with minimum
power consumption, less stress across switches and using zero parasitic components during the switching process. Herein, the proposed VDBC circuit is implemented by using the methods described in [22,26,27,54], conventional boost converters in [37,55], and switching rectifier circuits in [1,7,17,56,57].

Despite the proposed circuit employing existing methodologies, there has been no attempt to combine the VD circuit and the standard DC-DC approach with application in charging garden lights. As a general rule of energy harvesting, the VDBC circuit makes no attempt to use external switching circuits to reduce conversion losses and costs. As the VDBC circuit comprises a simple power electronic circuit that operates without needing active logic controllers, it is expected that the VDBC circuit minimises the necessity for external switching circuits while increasing the overall system’s performance. Additionally, due to the irregular behaviour of vibration, charging a battery and continually powering LED lights is quite challenging [3,58]. As a result, the proposed VDBC can also resolve this issue when LED bulbs refer to solar battery lights. Other key benefits of the VDBC circuit are highlighted below:

1. The proposed VDBC circuit implemented MOSFET switches. This reduced stress in the switching process, thus achieving higher output voltage (Vdc) and power.
2. As highlighted in the literature, it is developed without employing complex, extraneous circuits and polarity indicators, which leads to lower conversion losses and complexity.

This paper is divided as follows: Section 2 discusses the internal characteristics of PD and PEH circuits, while experimental results and discussion are described in Section 3. The conclusion is described in Section 4.

2. PD Internal Characteristics and PEH Circuits

This section reveals the internal features of PD’s circuit and frequently employed rectifier circuits in the PEH field. The VDBC circuit is also illustrated, in detail, in the following paragraphs.

2.1. PD Circuit Model

A typical PD may exhibit both current and voltage sources when it is mechanically exciting [3,26,27,59], as depicted in Figure 3a. However, the internal capacitor, \( C_p \), is parallel when it is considered a current source. While in series, it is regarded as a voltage source.

![Figure 3. (a) PD representation as a current source; (b) the current and voltage outputs of a vibrating PD.](image-url)
The harvested current and voltage deviate from the mechanical vibrations in each half-cycle, as depicted in Figure 3b. Initially, the current generated by the PD due to the mechanical excitation has to charge its internal capacitor, \( C_P \). The charging duration of the internal capacitor is shown in interval 1 in Figure 3b. During this period, the rectifier circuit does not operate and charge the load capacitor, as there is no current flow from the PD. This process endures until the PD’s magnitude voltage, \( V_{ac}(t) \), and load capacitor becomes identical.

Once the \( C_P \) is charged completely, then interval 2 begins. During interval 2, the magnitude of the PD’s voltage and load capacitor voltage becomes equal, and the rectification process begins. A similar trend is also predicted in the negative half-cycle [60]. In particular, the internal capacitor charging period occurs in intervals 1 and 3, while the rectification occurs in intervals 2 and 4. In other words, intervals 1 and 3 are referred to as non-harvesting regions, while intervals 2 and 4 are referred to as harvesting regions. During this process, the current harvested by a PD can be written as [1,3,61]:

\[
i_{ac}(t) = \hat{I}_{ac} \sin(\omega t)
\]

where \( \hat{I}_{ac} \) is the magnitude of harvested current, \( \omega \) is the angular frequency, while \( t \) represents the time period.

2.2. VD Circuit

Figure 2a comprises a VD circuit in shunt with the PD, and its corresponding current and voltage waveforms are delineated in Figure 4. As depicted in Figure 2a, the current generated by the PD must charge its internal capacitor, \( C_P \). At this instant, the PD voltage lags behind the total forwarding and rectified voltage (i.e., \( V_{PD} \leq V_D + V_{dc} \)), where the \( V_D \) represents the forward voltage losses across diodes. As a result, the VD circuit does not conduct, and the capacitor \( C_{L1} \) remains uncharged. This occurs in both half-cycles of input voltage [3,62]. Intervals 1 and 3 are referred to as non-harvesting regions (i.e., PD charging the internal capacitor, \( C_P \)). The VD circuit starts conducting when the PD’s magnitude equals the rectified voltage (i.e., \( V_{PD} \geq V_D + V_{dc} \)). Consequently, the capacitor, \( C_{L1} \), starts charging. Intervals 2 and 4 are referred to as harvesting regions (i.e., PD charges the load capacitor, \( C_{L1} \)). The process of energy accumulation across \( C_{L1} \) in both half cycles is represented as follows.

Figure 4. The current and voltage outputs generated by PD. (\( u \): polarisation current used to charge the internal capacitor of PD).

Mode 1: Positive half-cycle

During interval 1 (\( t_0 < t \leq t_1 \)):
- \( C_P \) = Charging (PD delivers no output to load)
- \( C_{L1} = \text{Not charging} \)
- \( D_1 - D_2: \text{OFF} \)

During interval 2 \( (t_1 < t \leq t_2) \):
- \( C_P = \text{Discharging (PD delivers output to load)} \)
- \( D_1: \text{ON} \)
- \( D_2: \text{OFF} \)
- \( V_{PD} = V_{dc} (C_{L1}: \text{Charged}) \)

**Mode 2: Negative half-cycle**

During interval 3 \( (t_2 < t \leq t_3) \):
- \( C_P = \text{Charging (PD delivers no output to load)} \)
- \( C_{L1} = \text{Not charging} \)
- \( D_1 - D_2: \text{OFF} \)

During interval 4 \( (t_3 < t \leq t_4) \):
- \( C_P = \text{Discharging (PD delivers output to load)} \)
- \( D_1: \text{OFF} \)
- \( D_2: \text{ON} \)
- \( V_{PD} = V_{dc} (C_{L1}: \text{Charged}) \)

The capacitor, \( C_{L1} \), is charged during both half-cycles of the PD. The output power of the VD circuit varies with the changing in rectified voltage \[1,27,63\], and the high output power turns out, when

\[
V_{dc} = \frac{\overline{I_{ac}}(t)}{2 \omega C_P} \tag{2}
\]

In addition, the current output across the capacitor, \( C_{L1} \), can be depicted as \[8,63\]:

\[
\left\{ \begin{array}{ll}
0, & 0 \leq t \leq u \\
\frac{C_{L1}}{C_{L1} + C_P} \overline{I_{ac}} \sin(\omega t) \approx, & u \leq t \leq \pi
\end{array} \right.
\tag{3}
\]

Given that \( C_{L1} \geq C_P \), then most of the current will be output:

\[
\frac{C_{L1}}{C_{L1} + C_P} \overline{I_{ac}} \approx i_{ac} \tag{4}
\]

The rectified output power, \( P_O(t) \), can be stated as a function of the rectified voltage, \( V_{dc} \):

\[
\langle P_O(t) \rangle = \frac{2 V_{dc}}{\pi} - (I_{ac} - V_{dc} \omega C_P) \tag{5}
\]

### 2.3. Voltage Doubler Boost Converter Circuit

Herein, a VDBC circuit is proposed and studied, one which boosts the low rectified voltage, operates at low AC voltage from PD, and reduces ripples in the rectified voltage output. The proposed VDBC circuit is depicted in Figure 2b. It is designed to work in 6 modes of operation.

Modes 1–2 comprise a VD circuit for AC-DC conversion, while modes 3–4 consist of a step-up DC-DC converter for effective power conversion. Modes 5–6 include an improved non-linear synchronisation procedure of a conventional boost converter circuit. It is worth noting that modes 1–2 of the VDBC circuit are similar to the exact operation of the VD circuit since the proposed VDBC circuit is stated to be an extension of the VD circuit \[53\] and literature circuits \[17,52,55\].

When the rectified voltage from the VD circuit is collected across the capacitor, \( C_{L1} \), modes 3–4 (i.e., DC-DC conversion) start conducting. Mode 3 begins when the inductor, \( L_1 \), charges, while mode 4 initiates when \( L_1 \) discharges. The complete working operation of both modes 3–4 is depicted in Figure 5.

**Mode 3:** (Charging process of inductor \( L_1 \))
The stored voltage in the capacitor, $C_{L1}$, charges the inductor, $L_1$. From here, it flows to the base, B of the transistor, $Q_1$, via a capacitor, $C_4$. $Q_1$ behaves as a voltage amplifier that amplifies the low voltage at the base, B, and generates a high output at the collector, C. Thus, the collector output activates the MOSFET switch, $M_1$, and it starts conducting. Consequently, the inductor starts charging and increases its current. During this time, the voltage accumulated across $C_{L1}$ starts charging the inductor, $L_1$, slowly from zero to peak, as the inductor prevents a sudden change in current. During this, the diode, $D_4$, is OFF, and no output flows towards the capacitor, $C_{L2}$.

![Image](image_url)

**Figure 5.** Working operation of VDBC circuit in modes 3 and 4: (a) mode 3 (inductor $L_1$ is charging) and (b) mode 4 (inductor $L_1$ is discharging). (B: Base, C: Collector, E: Emitter).

**Mode 4:** (Discharging process of Inductor $L_1$)

During this mode, when $L_1$ gets saturated, the current flow to the transistor, $Q_1$ is terminated, and $M_1$ is turned OFF. Thus, the current stored in $L_1$ freewheels via a diode, $D_4$, and charges the capacitor, $C_{L2}$. As the capacitor prevents a sudden change in voltage, it charges slowly from zero to peak voltage level. A detailed working principle of both modes 3 and 4 is depicted in Figure 5a,b.

Once the rectified voltage fully charges the capacitor $C_{L2}$, modes 5–6 begin to operate. In these modes, an improved non-linear synchronisation procedure of a conventional boost converter circuit is implemented to alleviate the ripples in the rectified output voltage stored in $C_{L2}$. This converter circuit is utilised to sustain a stable and fixed rectified output voltage at the load capacitor, $C_{L3}$.

Considering the ideal DC-DC converter (modes 5–6) circuit having zero losses, the same rectified current and voltage, which was stored in $C_{L2}$ must be passed through it and stored in the load capacitor, $C_{L3}$. Consequently, the rectified voltage and current are regarded as constant because they are DC. Therefore, the output power, $P_O$, at the load capacitor, $C_{L3}$, can be determined by the product of the voltage ($V_O$) across the load capacitor, $C_{L3}$, and the current ($I_{CL3}$) flowing from the load resistor, $R_L$.

$$P_O = V_O \times I_{CL3} \quad (6)$$

The DC-DC converter comprises 2 modes, namely modes 5 and 6. Mode 5 starts working when the MOSFET switch, $M_2$, is turned ON, while mode 6 begins when $M_2$ is turned OFF. A similar gate signal is employed to turn ON the MOSFET switch, $M_2$ in mode...
5, as used in Modes 3–4. The complete working operation of both modes 5 and 6 is depicted in Figure 6.

**Figure 6.** (a) Circuit diagram of modes 5–6, (b) mode 5 (M$_2$ switch is on), (c) mode 6 (M$_2$ switch is off) and linked waveforms. ($V_{L2}$: Inductor current, $T_{SW}$: time period of the switching process, $d_1T_{SW}$, $d_2T_{SW}$: ON and OFF period of the control circuit, $i_{D5}$: diode.)

**Mode 5:** (When MOSFET switch M$_2$ turns ON)
During this period, the MOSFET switch M$_2$ turns on. Thus, the stored rectified output voltage in the load capacitor, C$_{L2}$, envelopes through C$_{L2}$–L$_2$–M$_2$–C$_{L2}$ to charge the inductor, L$_2$. During this period, the diode, D$_5$, is reverse biased, and no current flows towards the load capacitor, C$_{L3}$.

**Mode 6:** (When MOSFET switch M$_2$ turns OFF)
During this period, the switch M$_2$ turns off. Thus, the accumulated current across the inductor L$_2$ during mode 5 is freewheeled via the diode D$_5$ to charge the load capacitor, C$_{L3}$.

It should be worth emphasising that the proposed VDBC circuit does not entail an external power source to trigger the MOSFET switches across any of the six modes. Thus, switching pulses, logic gates, and integrated circuits [54] are not required to operate the proposed circuit’s MOSFET switches (M$_1$ and M$_2$).

This study assumes that the inductor and capacitors are ideal semiconductor devices. The subsequent equations are stated when the MOSFET switches are conducting (Figure 6) [8].

**ON Period** ($t_0 < t < d_1T_w$):
When the switch is in a conduction state:

\[
V_{L2}(t) = V_{dc} \quad (7)
\]

\[
i_{CL3} = -\frac{V_O(t)}{R} \quad (8)
\]

Small ripple approximation for $V_O(t)$:

\[
V_{L2} = (t) \approx V_{dc} \quad (9)
\]

\[
i_{CL3} \approx -\frac{V_O(t)}{R} \quad (10)
\]
OFF Period \((d_1 T_w < t < (d_1 + d_2) T_{sw})\): When the switch is in a conduction state:

\[
V_{L2}(t) = V_{dc} - V_O(t)
\]

(11)

\[
i_{CL3} = i_{dc}(t) - \frac{V_O(t)}{R}
\]

(12)

Small ripple approximation for \(V_O(t)\):

\[
V_{L2}(t) \approx V_{dc} - V_O(t)
\]

(13)

\[
i_{CL3} \approx i_{dc}(t) - \frac{V_O(t)}{R}
\]

(14)

Empowering the load resistances \(((d_1 + d_2) T_{sw} < t < T_{sw})\):

\[
V_{L2}(t) = 0, \quad i_{dc}\left|_{\delta \to 0}\right. = 0
\]

(15)

\[
i_{CL3} = -\frac{V_O(t)}{R}
\]

(16)

Small ripple approximation for \(V_O(t)\):

\[
V_{L2}(t) = 0
\]

(17)

\[
i_{CL3} \approx -\frac{V_O(t)}{R}
\]

(18)

where \(d\) represents the duty cycle, \(T_w\) refers to the time period of the switching process, \(V_{L2}\) is the inductor current, \(i_{CL3}\) is the current flowing through the load resistor, and \(V_o\) is the voltage across the load capacitor.

During the switching interval, the MOSFET switch is turned on, while the diode, \(D_5\), is turned off with zero current. Thus, a negligible switching loss can be anticipated. As the result of the above assumptions, diode and inductor waveforms, capacitor charge balance and inductor voltage-sec balance, and the output voltage through modes 5–6 can be stated as follows [56]:

\[
\frac{V_O}{V_{dc}} = 1 \pm \sqrt{1 + \frac{4d_1^2}{K}}
\]

(19)

where \(V_O\) represents the generated output voltage of the VDBC circuit, \(V_{dc}\) is the rectified output voltage stored in the capacitor, and \(C_{L2}\) is the operation of modes 1–4.

3. Experimental Results and Discussions

A conventional piezoelectric cantilever beam consists of an aluminium beam (dimensions: 205 × 20 × 1 mm), with the first end attached to the mechanical vibration shaker (APS—113), and the opposite end carries two permanent magnets. The magnets were utilised as proof mass coupled at the nook of the aluminium beam. A microfiber composite (MFC) patch (M2814-P2, 37 mm × 17 mm × 0.180 mm, \(C_P = 33.90\) nF) was glued at the fixed end of the aluminium beam, facing the maximum strain occurrence. A function generator (Agilent 33210A, The Agilent Technologies, Santa Clara, California, USA) was employed to provide a sinewave signal to a power amplifier (2706, B&K Agilent). This amplifier boosted the sinusoidal signal before triggering the mechanical shaker. This shaker operated on input amplitude and vibrational frequency to produce mechanical vibrations to excite the piezoelectric cantilever beam. An inductive sensor can be applied to track the acceleration of the base excitation beam. Thus, due to these mechanical vibrations, the patched PD generated an AC signal, \(V_{ac}\), which was taken as an input for the proposed VDBC circuit.

To validate the applicability of the VDBC circuit, three different testing scenarios were implemented. In Test 1, the proposed VDBC circuit was tested at constant excitation frequency under varying input voltage. In Test 2, the proposed circuit was analysed at constant input voltage under varying excitation frequencies, as highlighted in Table 1.
However, in Test 3, the proposed circuit was used to charge a solar-powered battery. The generated output voltage, $V_O$, through the VDBC circuit was stored in $C_{L3}$ in both Test 1 and Test 2. In addition, each load resistor, $R_L$, was connected in parallel with $C_{L3}$ and outputs were measured using a multimeter.

### Table 1. Testing Scenarios.

<table>
<thead>
<tr>
<th>Sources of Excitation</th>
<th>Test Scenarios</th>
<th>Frequency (Hz)</th>
<th>Input Voltage (V$_{ac}$)</th>
<th>Load Capacitor ($\mu$F)</th>
<th>Types of PD</th>
<th>Load Resistors (K$\Omega$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mechanical Shaker</td>
<td>Test 1</td>
<td>5, 10, 15, 20</td>
<td>5</td>
<td>10</td>
<td></td>
<td>$R_1 = 100$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MFC</td>
<td>$R_2 = 300$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$R_3 = 620$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$R_4 = 910$</td>
</tr>
<tr>
<td>Test 2</td>
<td>100</td>
<td>0.5, 0.7, 1.0, 1.25</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Test 3</td>
<td>5</td>
<td>5</td>
<td>(solar battery) 1.2 V$_{dc}$, 4 mA</td>
<td>100</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### 3.1. Varying Excitation Frequency at Fixed Input Voltage

The output voltage and power attained from Test 1 are depicted in Figure 7a,b, respectively. Here, the output voltage and power obtained from the VDBC circuit are compared at different input frequencies (5–20 Hz) under varying load resistances ranging from (100–910 K$\Omega$).

![Figure 7. Outcomes of Test 1 at 5V$_{ac}$, (a) output voltage and (b) output power.](image)

According to Figure 7, regardless of applied input voltage and frequency, the output voltage is boosted with the increase in load resistances. It is prominent that the VDBC achieves the maximum output voltage at a higher load resistance of 910 K$\Omega$.

Firstly, a 5 V$_{ac}$ input voltage is given to the VDBC circuit at a 5 Hz excitation frequency. Taking a positive half-cycle, mode 1 started working and conducted the AC-DC conversion process. Consequently, the rectified output voltage is stored in the capacitor, $C_{L1}$ (Figure 7). A similar operation happened in the negative half-cycle. Once $C_{L1}$ is fully charged, it initiates the current flow in modes 3–4 (i.e., DC-DC converter).

The rectified voltage stored in $C_{L1}$, as the consequence of modes 1–2, stimulates the current flow towards the base of the transistor, Q$_1$, after passing through the inductor, L$_1$ and coupling capacitor, C$_4$. The transistor, Q$_1$, acted as a common emitter voltage amplifier, amplifying the base input voltage to a higher collector output voltage. The collector output activated the MOSFET switch, M$_1$’s gate and allowed the drain to source current flow, resulting in charging the L$_1$ (mode 3).

Once L$_1$ is fully saturated, it blocks the current flow towards Q$_1$. As a result, the M$_1$ stopped conducting. Thus, the stored current in L$_1$ initiated the current flow towards the capacitor, $C_{L2}$, via forwarding biased diode, D$_4$ (Mode 4). Once $C_{L2}$ is completely charged, modes 5–6 begin to operate.

In mode 5, the stored rectified voltage in capacitor $C_{L2}$, $V_{dc}$, as the result of modes 3–4, causes a magnetic field across the inductor, L$_2$. It is to be noted that the MOSFET switch,
M_2_, is turned on and off during this time duration. Thus, the V_{dc} acted as a short circuit, causing an increased magnetic field across L_2. The prime factor behind this boosted magnetic field across L_2 is that the quicker the magnetic field variates, the higher the potential difference it causes. The magnetic field through L_2 is enveloped as M_1 is switched on. However, when M_2 is switched off, the stored charge across L_2 forward biased the diode, D_5 and charges the load capacitor, C_{L3}. Later, each load resistance is connected in parallel, and output is captured using a multimeter.

Later, the remaining input frequencies were applied under a similar input voltage. The resulting output voltage was measured, as depicted in Figure 7a. Once the output voltage was stored in C_{L3}, the current and voltage across R_L were measured. Using Equation (6), the output power was calculated, depicted in Figure 7b.

Another observation revealed that the excitation frequency considerably impacts the overall performance of the VDBC circuit. Higher output voltage and power values were achieved at higher excitation frequencies. This is because the capacitive inductance of PD drops at higher switching frequencies [2]. Thus, the PD generates a higher AC voltage, V_{ac}, which leads to increased output voltage and power. Figure 8 represents the output voltage and power under constant input voltage and at varying excitation frequencies.

![Figure 8. Outcomes of Test 1 at various excitation frequencies (a) output voltage and (b) output power.](image)

It is worth noting that the main goal of the proposed study is to validate the performance of the VDBC circuit by minimising power conversion, the diode’s forward voltage, and ripple losses in the rectified voltage waveform, thus achieving a high output voltage and power. The peak output voltage of 11.7 V_{dc} is achieved at a frequency of 20 Hz. However, the least voltage of 5.66 V_{dc} is accumulated across the load resistor at a 5 Hz input frequency.

3.2. Varying Input Voltage at Fixed Excitation Frequency

The performance of the VDBC circuit was tested under a fixed excitation frequency at a varying input voltage. Here the excitation frequency was kept constant at 100 Hz, and the VDBC circuit was subjected to the PD’s variable input AC voltage (Table 1). The resulting output voltage and power from Test 2 are depicted in Figure 9a,b.
Initially, 0.5 V\text{ac} input voltage was applied across the VDBC circuit at 100 Hz excitation frequency. As the applied input voltage, V\text{ac} exceeded the threshold voltage of both MOSFET and transistor switches, the proposed circuit started conducting in modes 1–6, as discussed in Section 3.1. This achieved 0.28 V\text{dc}, which was stored across the load capacitor, C_{L3}. Later, the remaining input voltages were applied, and the resulting output voltage and power were calculated and plotted in Figure 9a,b.

To further understand the behaviour of the VDBC circuit, the relation between the output voltage and power with the increasing load resistances was observed (Figure 9). Figure 9 shows that output voltage is enhanced with the increase in the load resistance, regardless of the applied excitation frequency. The highest output voltage was observed at 910 K\text{Ω}; however, the least was obtained at 100 K\text{Ω}. This behaviour was consistent with all applied input voltages and followed Ohm’s law [3,7].

Further examination of Figure 9 reveals that the magnitude of applied input voltage considerably influences the overall performance of the VDBC circuit. The higher-output voltage and power were obtained at a higher input voltage, V\text{ac}. This is because, at higher input voltages, V\text{ac}, the drain to source resistance path in the MOSFET switch, is reduced. Thus, the output voltage and power are increased. Figure 9 represents the output voltage and power at various input voltages over 100 Hz excitation frequency.

3.3. VDBC Application: Solar Battery Charging

To validate the real-world application of the proposed circuit, the power generated by the VDBC circuit was utilised to charge a solar battery (1.2 V\text{dc}, 4 mA battery used as solar cell-powered garden lighting). This battery was powered at a 5 Hz input frequency with an input voltage of 5 V\text{ac}, under similar experimental circumstances.

The solar battery was charged up to 1.078 V\text{O} in 32 min at 5 V\text{ac}, 5 Hz input parameters. A 1 cm × 1.5 cm solar panel and a DC-DC converter typically charge a similar battery in 4–5 h. It is noted that electronic components of low threshold voltage are chosen for effective power conversion. However, the parameter rating must be set carefully for safe experimental operation. Figure 10 depicts the experimental illustration of the solar battery while turned off and on.
3.4. Comparison of VDBC with the Conventional VD Circuit

The output voltage waveform of the VDBC circuit acquired from the oscilloscope at 5 Hz, at 5 V\textsubscript{ac} input voltage, is summarised in Figure 11. Figure 11 shows that the VDBC circuit eliminated a majority of the ripples at the given frequency.

The rectified voltage waveforms from the VDBC were also compared with those rectified by VD. Both circuits were tested under similar scenarios (5 V\textsubscript{ac} at 5 Hz frequency). It should be noted that the VD circuit possesses only the rectifier circuit (i.e., AC-DC conversion). The VD circuit charged the capacitor, C\textsubscript{L1}, which was discharged at the load resistor. Thus, a high number of ripples are observed in the rectified output voltage waveform. These ripples were reduced by the VDBC circuit, which incorporates both AC to DC and DC to DC conversion processes, before the rectified voltage is stored in a load capacitor, C\textsubscript{L3}.

Consequently, the VDBC circuit outperforms the VD circuit regarding the stability of the rectified output voltage waveform. Thus, the secondary objective of minimising ripples in the rectified output voltage waveform was proved in this chapter.

Recalling that the main objective of this study is to rectify and boost the low AC voltage which is generated by PD to a higher DC output voltage and power, this has been achieved by the proposed VDBC circuit at both low and higher excitation frequencies.
Besides, the output voltage waveform generated from the VDBC circuit is stable compared to the circuits described in the existing literature.

In addition, the results demonstrated that the proposed VDBC circuit outperformed the existing literature circuits in terms of output voltage and power. For the sake of comparison, Table 2 lists the generated output power of similar circuits published in the literature.

Table 2. Comparison to previously published literature circuits.

<table>
<thead>
<tr>
<th>Circuit Sources</th>
<th>Input Voltage ($V_{ac}$)</th>
<th>DC Voltage ($V_{dc}$)</th>
<th>Output Power ($\mu$W)</th>
<th>External Power Supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>[27]</td>
<td>8</td>
<td>-</td>
<td>0.8 W</td>
<td>YES</td>
</tr>
<tr>
<td>[3]</td>
<td>5</td>
<td>-</td>
<td>22 $\mu$W</td>
<td>NO</td>
</tr>
<tr>
<td>[64]</td>
<td>0.65</td>
<td>1.8</td>
<td>75 $\mu$W</td>
<td>NO</td>
</tr>
<tr>
<td>[26]</td>
<td>3.5</td>
<td>-</td>
<td>254 $\mu$W</td>
<td>YES</td>
</tr>
<tr>
<td>[57]</td>
<td>0.4</td>
<td>3.3</td>
<td>54.4 $\mu$W</td>
<td>YES</td>
</tr>
<tr>
<td>[65]</td>
<td>0.4</td>
<td>3.3</td>
<td>40 $\mu$W</td>
<td>YES</td>
</tr>
<tr>
<td>[66]</td>
<td>1.2</td>
<td>-</td>
<td>30 $\mu$W</td>
<td>YES</td>
</tr>
<tr>
<td>[8]</td>
<td>3</td>
<td>-</td>
<td>364.5 $\mu$W</td>
<td>NO</td>
</tr>
<tr>
<td>VDBC</td>
<td>5</td>
<td>11.7</td>
<td>1.368 mW</td>
<td>NO</td>
</tr>
</tbody>
</table>

4. Conclusions

This study focuses on extracting higher output voltage by taking the benefits of MOSFETs, which have low threshold voltage, and mitigating ripples in the output voltage waveform of miniature vibrating PEH, which converts ME into EE for charging solar batteries. The proposed VDBC circuit rectified and boosted the low AC voltage, $V_{ac}$, generated by vibrating PD in the PEH system. The proposed VDBC circuit integrated a previously established VD with a step-up boost converter (modes 1–4) for both AC to DC and DC to DC conversions, while an extended switching circuit using a DC-DC converter in modes 5–6 stabilised the rectified voltage generated from modes 1–4. The feasibility of the proposed VDBC circuit was verified through a series of experimental analyses at both a fixed excitation frequency and a fixed input voltage. In Test 1, the proposed VDBC circuit converted a 5 Vac and 20 Hz input AC voltage to 11.7 Vdc and achieved a output power of 1.368 mW. However, the proposed prototype converted a 1.25 Vac and 100 Hz input AC voltage to 1.11 Vdc with an output power of 12.321 $\mu$W. It is noted that proposed circuit is limited to low voltage applications only. For ultra-low voltages, the proposed prototype is not suitable as the input voltage will be dissipated across circuit components and there will be no output at the load. For future work, modification of the VDBC circuit to incorporate the non-linear process is recommended.

Author Contributions: Conceptualization, A.H.; methodology, A.H.; software, A.H.; validation, A.H.; formal analysis, A.H.; investigation, A.H.; resources, A.H.; data curation, A.H.; writing—original draft preparation, A.H.; writing—review and editing, A.H., M.E. and M.U.; visualisation, A.H.; supervision, M.E., F.S., M.U. and M.D.; project administration, A.H.; funding acquisition, Not applicable. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no funding.

Data Availability Statement: Data is available on request due to privacy and restrictions.

Acknowledgments: The work is supported by Southern Cross University, Faculty of Science and Engineering, Lismore, NSW, 2480.

Conflicts of Interest: The authors declare no conflict of interests.
**Symbols and Abbreviation**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_f$</td>
<td>Diode Forward Voltage</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>DC Voltage</td>
</tr>
<tr>
<td>$V_o$</td>
<td>Output Voltage</td>
</tr>
<tr>
<td>$t$</td>
<td>Time Period</td>
</tr>
<tr>
<td>$V_D$</td>
<td>Diode Forward Voltage Losses</td>
</tr>
<tr>
<td>$C_1, C_2, C_{L1}, C_{L2}$</td>
<td>Capacitor</td>
</tr>
<tr>
<td>$P_o$</td>
<td>Rectified Output Power</td>
</tr>
<tr>
<td>$D_1$–$D_5$</td>
<td>Diodes</td>
</tr>
<tr>
<td>$M_1$–$M_2$</td>
<td>MOSFET Switches</td>
</tr>
<tr>
<td>$B$</td>
<td>Base</td>
</tr>
<tr>
<td>$E$</td>
<td>Emitter</td>
</tr>
<tr>
<td>$T_{sw}$</td>
<td>Time Period of Switching Process</td>
</tr>
<tr>
<td>$G$</td>
<td>Gate</td>
</tr>
<tr>
<td>$S$</td>
<td>Source</td>
</tr>
<tr>
<td>$C_{L3}$</td>
<td>Load Capacitor</td>
</tr>
<tr>
<td>$C_P$</td>
<td>Internal Capacitor of PD</td>
</tr>
<tr>
<td>$\omega$</td>
<td>Angular Frequency</td>
</tr>
<tr>
<td>$i_{ac}$</td>
<td>AC Current</td>
</tr>
<tr>
<td>$V_{PD}$</td>
<td>Voltage Across PD Electrodes</td>
</tr>
<tr>
<td>$u$</td>
<td>Polarization Current used to Charge the PD</td>
</tr>
<tr>
<td>$V_{ac}$</td>
<td>AC Voltage</td>
</tr>
<tr>
<td>$R_1$–$R_2$</td>
<td>Resistors</td>
</tr>
<tr>
<td>$L_1$–$L_2$</td>
<td>Inductors</td>
</tr>
<tr>
<td>$C$</td>
<td>Collector</td>
</tr>
<tr>
<td>$R_L$</td>
<td>Load Resistor</td>
</tr>
<tr>
<td>$d_1$–$d_2$</td>
<td>Duty Cycles</td>
</tr>
<tr>
<td>$D$</td>
<td>Drain</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Explanation</th>
</tr>
</thead>
<tbody>
<tr>
<td>PD</td>
<td>Piezoelectric Device</td>
</tr>
<tr>
<td>ME</td>
<td>Mechanical Energy</td>
</tr>
<tr>
<td>EE</td>
<td>Electrical Energy</td>
</tr>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>PEH</td>
<td>Piezoelectric Energy Harvesting</td>
</tr>
<tr>
<td>FBR</td>
<td>Full Bridge Rectifier</td>
</tr>
<tr>
<td>PSCAD</td>
<td>Power System Computer Aided Designs</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Field Effect Transistor</td>
</tr>
<tr>
<td>DSHBR</td>
<td>Dual Stage H-Bridge Rectifier Circuit</td>
</tr>
<tr>
<td>VDBC</td>
<td>Voltage Doubler Boost Converter</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>MPE</td>
<td>Maximum Power Extraction</td>
</tr>
<tr>
<td>HBR</td>
<td>H-Bridge Rectifier</td>
</tr>
<tr>
<td>LCL</td>
<td>Latching Current Limiter</td>
</tr>
</tbody>
</table>

**References**


25. Teo, J.; Tan, R.H.; Mok, V.; Ramachandaramurthy, V.K.; Tan, C. Impact of bypass diode forward voltage on maximum power of a photovoltaic system under partial shading conditions. *Energy* 2020, 191, 116491. [CrossRef]


29. Li, D.; Wang, C.; Cui, X.; Chen, D.; Fei, C.; Yang, Y. Recent progress and development of interface integrated circuits for piezoelectric energy harvesting. *Nano Energy* 2022, 94, 106938. [CrossRef]


**Disclaimer/Publisher’s Note:** The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.