A Bridge-Level Junction Temperature Estimation Method for SiC MOSFETs Combining Transient Voltage and Current Peaks

Shuo Wu, Pengju Sun *, Xu Huang and Kaiwei Li

State Key Laboratory of Power Transmission Equipment and System Security and New Technology, Chongqing University, Chongqing 400044, China; wushuo@cqu.edu.cn (S.W.); huangxutongxue@163.com (X.H.); kaiwei_li@cqu.edu.cn (K.L.)

* Correspondence: spengju@cqu.edu.cn

Abstract: Accurate measurement of the junction temperature $T_j$ is crucial for ensuring safe operation and evaluating the performance of silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs). In this paper, the junction temperature of a half-bridge is monitored by combining transient voltage and current peaks across the lower device. Both theoretical analysis and switch tests validate that the peak induced voltage and peak reversed current during the commutation transient exhibit a linear relationship with the temperature of the corresponding devices. The impact of load current and bus voltage on the measurement results is also investigated. Moreover, the effectiveness of the proposed method is confirmed by carrying out tests at different temperatures, and the feasibility of online implementation is discussed. The experimental results show that the proposed method has high linearity and sensitivity and can simultaneously provide temperature information for both devices of a half-bridge.

Keywords: junction temperature; SiC MOSFET; temperature-sensitive electrical parameter

1. Introduction

The silicon carbide metal–oxide–semiconductor field-effect transistor (SiC MOSFET), as a typical representative of wide-bandgap semiconductor devices, has superior properties, such as high switching frequency, high voltage withstanding capability, and low on-resistance. With the widespread application of silicon carbide devices in fields such as rail transportation, aviation and aerospace, automotive, and new energy generation in recent years [1,2], the requirements for their reliability are increasing. Temperature is one of the main causes of power device failure [3], so temperature measurement is of great significance for the safe and reliable operation and thermal management of power electronic devices [4,5].

At present, temperature measurement methods mainly comprise thermal network, physical contact, optical, and temperature-sensitive electrical parameter (TSEP). The accuracy of the thermal network method has been improved [6,7]; based on the power loss of the device under testing and the transient thermal impedance model, the junction temperature can be calculated. However, obtaining the real-time loss of SiC MOSFET can be challenging. Additionally, the thermal impedance network is subject to the effects of device aging and environmental factors, which can influence the accuracy of the calculated junction temperature. The physical contact and optical methods require the decapsulation of power devices, which reduces system reliability [8,9]. Conversely, the TSEP method is advantageous due to its low cost, fast response, and ability to measure junction temperature without causing damage to the package. It is currently the most widely used temperature measurement method.

The temperature-sensitive electrical parameters of SiC MOSFET devices can be categorized into static and dynamic parameters based on different measure timings. The static electrical parameters include internal gate resistance [10], on-state voltage drop [11],...
on-state resistance [12], and body diode voltage drop [13]. The sensitivity of the internal gate resistance is relatively low, making its measurement difficult. The on-state voltage drop shows a positive correlation with temperature under a high current, although it requires high-resolution voltage clamp circuits during switching transients. The voltage drop across the body diode is also sensitive to temperature changes and remains stable during device aging; however, online application of this parameter is challenging, since its measurement requires injecting a small current into the source-drain.

The dynamic temperature-sensitive electrical parameters consist of dynamic threshold voltage [14], turn on/off delay [15,16], and peak gate current, et cetera. A measurement scheme proposed in [16] enables online measurement of the device’s turn-on delay during inverter operation. However, the sensitivity is at the picosecond level, thus necessitating intelligent driving circuits for improved accuracy. Reference [17] obtains the gate peak current by measuring the voltage across the external drive resistor, which can be easily measured online and integrated, as it is not affected by the load current. Nonetheless, this method is not suitable for gate drive topologies with inductors or push–pull structure.

Regarding bridge-level TSEPs, reference [18] utilized the voltage oscillation on the DC bus caused by the current change rate to extract the temperature of the half-bridge. This method needs to combine the switching timing of the upper and lower switches and cannot simultaneously reflect the bridge temperature in one switching period. Furthermore, real-time digital acquisition of the transient process requires the use of high-precision ADC and signal-processing circuits.

In summary, the existing TSEP methods for SiC MOSFET devices have certain limitations, such as difficult measurement, low linearity, and low sensitivity. Furthermore, research on the dynamic TSEPs of SiC MOSFET devices has typically only focused on device-level parameters, instead of using bridge- or system-level parameters to estimate temperature. The conventional single-TSEP can be influenced by the temperature of other devices in practical applications [19]. Additionally, multiple floating grounds at bridge midpoints bring common mode interference issues [20], requiring additional isolation design of the measurement circuit to monitor the upper switch.

In contrast to traditional device-level TSEPs, this paper proposes a novel method for measuring junction temperature at the bridge level, using the transient reverse recovery current peak and the voltage peak induced by the current change rate as combined TSEPs. The proposed method overcomes the need for measurement circuits at floating grounds, as it only requires one measuring unit at the lower switch of the phase leg. Moreover, it can reflect the temperature of the phase leg simultaneously within one same switching period. The switching process of each SiC MOSFET device during the commutation stage is explained specifically, and the correlation between the proposed TSEPs and the corresponding device temperature is analyzed. Subsequently, a dynamic switching characteristics platform is established to calibrate the peak induced voltage and peak reverse recovery current at different temperatures. The effects of load current and bus voltage on the temperature calibration curve are also evaluated, and the online feasibility of the proposed method is discussed. This method utilizes the inherent parasitic inductance of the SiC MOSFET discrete device itself, without the need for external sensors, making it non-intrusive and suitable for bridge-level temperature estimation of the SiC MOSFET device.

2. Theoretical Analysis of Combining Transient Peaks as a Bridge-Level TSEP

2.1. Commutation Process of SiC MOSFETs in a Phase Leg Structure

The schematic diagram of the half-bridge test circuit considering parasitic parameters is shown in Figure 1a. $S_1$ is the upper switch, which is actively controlled by a double-pulse drive to the gate, and $S_2$ is the lower switch, with a constant negative bias on the gate to ensure the channel is completely turned off. The body diode of $S_2$ is used to provide a freewheeling loop for the load current. The main parasitic parameters in the circuit include: external and internal gate resistance $R_g$, external and internal gate loop parasitic inductance $L_{g}$, drain-source parasitic inductance $L_d$, power source drain parasitic inductance $L_{sp}$,
Kelvin source drain parasitic inductance $L_{sk}$, and the sum of the parasitic resistance in series between the power source drain and Kelvin source drain, $R_s$.

![Image](image_url)

**Figure 1.** (a) Half-bridge circuit considering parasitic parameters; (b) Main theoretical waveforms during commutation process.

The main switch waveforms of $S_1$ and $S_2$ are shown in Figure 1b, and the specific commutation process analysis is as follows:

1. ($t_0$–$t_1$): This stage is the delay period for $S_1$ to turn on. The gate voltage $v_{gs1}$ rises from the negative voltage $V_{EE}$ to the threshold voltage $V_{th}$ with a time constant of $R_s(C_{gs} + C_{gd})$. During this stage, $v_{gs1} < V_{th}$, and the load current flows through the body diode of $S_2$.

2. ($t_1$–$t_2$): In this stage, the load current is commutated from the body diode of $S_2$ to the channel of $S_1$. After the gate voltage $v_{gs1}$ rises to the threshold voltage $V_{th}$, the channel current $i_{d1}$ of $S_1$ rises to the load current $I_L$ at a rate of $di_{d1}/dt$, and $i_{d2}$ decreases to zero at the same rate.

At this time, $v_{ds1} > (V_{GG} - V_{th})$, $S_1$ is in a saturation region, and the drain-source current $i_{d1}$ can be expressed as:

$$i_{d1} = \frac{\beta}{2}(v_{gs1} - V_{th})^2$$

(1)

$$\beta = \frac{W_{CH}\mu_{CH}C_{OX}}{L}$$

(2)

where $\beta$ is the gain coefficient, $W_{CH}$ is the channel width of the inversion layer, and $\mu_{CH}$ is the effective carrier mobility of the channel.

The current change rate during this commutation stage can be calculated as:

$$\frac{di_{d1}}{dt} = \beta(v_{gs1} - V_{th})\frac{V_{GG}}{R_s(C_{gs} + C_{gd})e^{-\frac{t}{\tau_{gs1} + \tau_{gd}}}$$

(3)

3. ($t_2$–$t_3$): This stage is the charge storage stage. The current of $S_1$ continues to rise from $I_L$ to $I_L + I_{rrm}$, while the current of $S_2$ continues to decrease from zero to a negative value. During this process, the free carriers in the drift region are swept away. At $t_2$, the free carriers are zero, and the depletion region begins to form. At $t_3$, the reverse recovery current reaches the negative peak value $I_{rrm}$. 

$$i_{d1} = \frac{\beta}{2}(v_{gs1} - V_{th})^2$$

$$\beta = \frac{W_{CH}\mu_{CH}C_{OX}}{L}$$

$$\frac{di_{d1}}{dt} = \beta(v_{gs1} - V_{th})\frac{V_{GG}}{R_s(C_{gs} + C_{gd})e^{-\frac{t}{\tau_{gs1} + \tau_{gd}}}$$

(3)
The peak reverse recovery current has the following relationship with the distribution of free carrier concentration [21]:

\[ I_{rrm} = 2qD_a \frac{dn}{dx} = 2qD_a \frac{n_a}{h} \]  

(4)

where \( D_a \) is the bipolar diffusion coefficient, \( q \) is electron charge, and \( h \) is defined as the distance between the maximum and minimum carrier concentrations.

The carrier concentration \( n_a \) can be expressed as:

\[ n_a = \frac{I_L \tau_{HL}}{2q d} \]  

(5)

where \( \tau_{HL} \) is the minority carrier lifetime, and \( d \) is half of the drift region width.

4. \((t_3 \sim t_4)\): This stage is the reverse recovery stage. \( S_2 \) begins to withstand voltage, and at the same time, the parasitic capacitance of \( S_1 \) begins to discharge, while the parasitic capacitance of \( S_2 \) begins to charge. The current of \( S_2 \) during this stage consists of two parts: the actual reverse recovery current caused by the formation of the depletion region and the current charging the parasitic capacitance.

5. \((t_4 \sim t_5)\): In this stage, the reverse recovery process of \( S_2 \) ends, and \( S_1 \) enters the linear ohmic region.

2.2. Temperature Dependence Analysis

2.2.1. Peak Induced Voltage

From Figure 1a, it is evident that there exist a parasitic inductance \( L_{sk} \) and a parasitic inductance \( L_{sp} \) between the power source \( s \) and the auxiliary source \( s' \) of the discrete SiC MOSFET device with a Kelvin package. The induced voltage \( v_{ss'} \) at the two source terminals can be utilized to reflect the current change rate \( \frac{di}{dt} \). In the commutation process as depicted in Figure 1b, the channel of \( S_2 \) is completely turned off; the induced voltage \( v_{ss'} \) is only influenced by the power loop and can be given by:

\[ v_{ss'} = L_{sp} \left( \frac{di_{d2}}{dt} \right) + R_s i_{d2} \]  

(6)

As analyzed in Section 2.1, during \( t_1 \) to \( t_3 \), the current of \( S_2 \) drops from the load current at a speed of \( \frac{di_{d1}}{dt} \), and the induced voltage at this time can be further expressed as:

\[ v_{ss'} = -L_{sp} \left( \frac{di_{d1}}{dt} \right) + R_s i_{d2}, \quad t_1 < t < t_3 \]  

(7)

Owing to the wide bandgap property of SiC MOSFET devices, \( \frac{di_{d1}}{dt} \) exhibits a positive temperature coefficient under the dominating influence of the device threshold voltage \( V_{th} \) [22].

The induced voltage peak \( V_{ss'_{max}} \) appears at the moment when the current change rate reaches its maximum value. From Equations (1) and (3), during \( t_1 \) to \( t_2 \), the drive voltage rises approximately linearly, and the drain-source current increases in a quadratic function form, indicating that the maximum current change rate occurs at \( t_2 \). At this moment, the peak induced voltage can be expressed as:

\[ V_{ss'_{max}} = -L_{sp} \left( \frac{di_{d1}}{dt} \right)_{max} + R_s i_{d2} \]  

(8)

According to the device datasheet and manufacturer Spice model, the typical value of the source parasitic resistor \( R_s \) is usually in the range of 3 to 5 m\( \Omega \), while the parasitic inductance \( L_{sp} \) is about a few nH, and the switching current change rate of SiC MOSFET devices is around 0.5–3 A/ns. Therefore, \( v_{ss'} \) is mainly composed of induced voltage drop caused by parasitic inductance, and the changes caused by the temperature drift of
parasitic resistance $R_s$ is negligible. Upon determining the internal factors, such as the doping process and the physical size of the device during manufacturing, the parasitic parameter $L_{sp}$ can be considered a fixed value [14]. Thus, under the influence of the positive temperature characteristic of $(di/dt)_{max}$, $V_{ss\prime \max}$ has a positive correlation with temperature and is only affected by the temperature of $S_1$.

### 2.2.2. Peak Reverse Recovery Current

Based on Equations (4) and (5), it is apparent that the peak reverse recovery current of a SiC MOSFET device is affected by the minority carrier recombination rate in the drift region, which is closely related to the minority carrier lifetime $\tau_{HL}$ and the bipolar diffusion coefficient $D_a$, with $D_a$ exhibiting a negative temperature coefficient [21]. Furthermore, the relationship between the minority carrier lifetime and temperature can be described mathematically, as given by Equation (9) [21]. The minority carrier lifetime in the drift region increases exponentially with temperature, causing an increase in $I_{rrm}$. Thus, $I_{rrm}$ is affected by the temperature of $S_2$.

$$\tau_{HL} = \tau_0 \left(\frac{T_j}{300}\right)^k$$

In the current commutation process, the body diode of $S_2$ is turned off by active controlling of the complementary switch $S_1$. When the external switch speed $di_{d1}/dt$ is decreased, the gradient of the minority carrier concentration in the drift region is reduced, causing a decline in the peak reverse recovery current of the body diode. Additionally, $di_{d1}/dt$ is also impacted by the temperature of the upper switch $S_1$, as discussed in Section 2.2.1. Therefore, the temperature of $S_1$ also has an impact on $I_{rrm}$.

The positive peak voltage $V_{ss\prime \max}$ and the negative peak current $I_{rrm}$ both occur at the same switching transient. While $V_{ss\prime \max}$ is affected independently by the junction temperature of $S_1$, $I_{rrm}$ is affected by the temperature of $S_1$ and $S_2$. Consequently, it is possible to establish the two electrical parameters as functions of $T_{j1}$ (junction temperature of $S_1$) and $T_{j2}$ (junction temperature of $S_2$), as shown in Equations (10) and (11), if the correlation is highly linear, which would be calibrated in later experiments.

$$V_{ss\prime \max} = f_{ss\prime \max}(T_{j1}) = aT_{j1} + b$$

$$I_{rrm} = g_{rrm}(T_{j1}, T_{j2}) = cT_{j1} + dT_{j2} + e$$

By carrying out offline calibration experiments under fixed operating voltage and current, and various junction temperatures, the values of $V_{ss\prime \max}$ and $I_{rrm}$ can be determined. Subsequently, the functions of the two TSEPs with respect to device temperatures can be established using mathematical tools such as MATLAB. This approach offers a feasible solution for determining the temperature of devices in a phase leg configuration simultaneously, by only sampling the electrical parameters of the lower switch.

### 3. Experimental Results

#### 3.1. Temperature Dependence

The double-pulse test platform shown in Figure 2 is built to verify the temperature characteristics of the proposed TSEPs. The test is performed under the operating conditions of a bus voltage of 300 V and a load current of 10 A, with both upper and lower switches in the phase leg being Wolfspeed’s discrete SiC MOSFET devices C2M0045170P (Wolfspeed, Durham, NC, USA), rated for a voltage and current level of 1700 V/72 A.

Due to the switching speed of SiC MOSFET devices being in the nanosecond range, high-bandwidth measuring equipment is required to ensure accurate measurements. Specifically, the bandwidth margin should be designed to be three to five times greater than the...
calculated value. According to signal theory, the effective bandwidth of the signal rise time \( t_r \) or fall time \( t_f \) should be [23]:

\[
f_{BW} = \frac{0.35}{\min(t_r, t_f)}
\]

(12)

For instance, as calculated by Formula (12), a 3dB bandwidth of at least 35 MHz is required to measure the turn-on current during a ten-nanosecond period. Considering a margin of five times, the measuring equipment should have a bandwidth of at least 175 MHz. Therefore, device voltage and current measurements in this paper are conducted using a 500 MHz passive voltage probe and a 1 GHz shunt resistor, respectively, and the oscilloscope used is Tektronix’s DPO7104C (Beaverton, OR, USA).

![Figure 2. Double-pulse test experimental platform.](image)

The transient experimental waveforms are illustrated in Figure 3. As the current change rate of \( i_{d2} \) in the commutation process begins to drop, a voltage with a peak value of approximately 3 V is generated at the parasitic inductance \( L_{sp} \) of the lower switch. Considering the propagation delay of about three to five nanoseconds between the voltage waveform measured by the passive probe and the current waveform measured by the coaxial shunt resistor [24], the peak induced voltage appears around the moment when the load current crosses zero, which is the \( S_2 \) temperature insensitive region, and is consistent with the theoretical analysis.

![Figure 3. Experimental waveforms of the double-pulse test.](image)

During the test, a PID temperature controller is utilized to control the device under testing. The temperature of the heating pad is set to 30 °C, 50 °C, 70 °C, 90 °C, 110 °C, and 130 °C to observe \( i_{d2} \) and \( v_{ss'} \) waveforms. Figure 4a displays the waveform when \( S_1 \) is heated and \( S_2 \) is maintained at room temperature. In contrast, Figure 4b shows the waveform with \( S_2 \) heated and \( S_1 \) at room temperature.
The transient experimental waveforms are illustrated in Figure 3. As the current
load current crosses zero, which is the
moment when the upper and lower switches operate at different temperatures, as shown in Figure 5. It is apparent that
I_{rrm} is dependent on both S_1 and S_2 and increases with the rising temperature, owing to
the impact of the device carrier lifetime and the switch speed of the complementary device.

Figure 4. Experimental v_{ss'} waveforms when (a) S_1 is heated; (b) S_2 is heated.

As illustrated in Figure 4, under the same operating conditions, V_{ss'max} rises with the
increasing temperature due to the positive correlation between (di_{dt}/dt)_{max} and T_1. The
temperature change of T_2 does not impact the current change rate before its body diode
does not enter the reverse recovery process. Hence, V_{ss'max} remains unaffected within the tested
temperature range of S_2. The experimental results align with the theoretical analysis.

The same testing approach is employed to capture i_{dq} waveforms when the upper and
lower switches operate at different temperatures, as shown in Figure 5. It is apparent that
I_{rrm} is dependent on both S_1 and S_2 and increases with the rising temperature, owing to
the impact of the device carrier lifetime and the switch speed of the complementary device.

Figure 5. Experimental i_{dq} waveforms when (a) S_1 is heated; (b) S_2 is heated.

3.2. Operating Conditions Dependence

The relationship between V_{ss'max} and I_{rrm}, with junction temperature obtained under
different load currents and a fixed bus voltage, is shown in Figure 6. The results demonstrate
that both V_{ss'max} and I_{rrm} exhibit high temperature sensitivity at any load current. The
increase in load current results in a greater number of free charge carriers in the drift region,
leading to a larger reverse recovery process. Therefore, the temperature sensitivity of I_{rrm}
increases with increasing load current and is approximately −53 mA/°C, −62 mA/°C, and
−86 mA/°C for load currents of 10 A, 15 A, and 20 A, respectively.

Figure 7 displays the relationship between V_{ss'max} and I_{rrm} with the junction temperature
different bus voltages. The depletion layer of the device widens with an increase
in bus voltage, which decreases the depletion layer capacitance C_{dep} and accelerates the
switching transient. Meanwhile, the device needs to produce a wider space charge region
at higher bus voltages. The value of the combined TSEPs will thereby be affected by bus
voltage. The fitted results in Figure 7 indicate that the temperature characteristic displays
a similar trend under the tested bus voltage of 100 V, 200 V, and 300 V, and the absolute
values of V_{ss'max} and I_{rrm} increase with an increase in bus voltage.
To validate the universality of the proposed method, a different discrete SiC MOSFET device C3M0030090K from Wolfspeed (Durham, NC, USA), rated at 900 V/73 A, is selected for the same experimental verification. The junction temperature calibration curves for the two different types of devices are shown in Figure 8. The experimental results demonstrate that the combined TSEPs exhibit a similar temperature variation trend for different devices.

Based on the obtained experimental results, it can be observed that the device junction temperature $T_j$ peak induced voltage $V_{ss'\text{max}}$ and peak reverse recovery current $I_{rrm}$ exhibit a nearly linear relationship, with a fitting coefficient $R^2$ square over 0.97. Specifically, at a bus voltage of 300 V and a load current of 10 A, an increase of 1 °C in $T_{j1}$ leads to a rise of approximately 10 mV in $V_{ss'\text{max}}$, while a temperature rise of 1 °C in $T_{j2}$ results
in an absolute value increase of 44 mA in $I_{\text{rrm}}$. The combined TSEPs demonstrate high sensitivity and linearity. In addition, since the sensitivity of $I_{\text{rrm}}$ increases with a larger load current, the accuracy of the proposed method will be further improved in higher current applications. The calibrated relationship between $I_{\text{rrm}}$ and the junction temperature of $S_1$ and $S_2$ is presented in Figure 9.

![Figure 9. Calibrated $I_{\text{rrm}}$-$T_{j1}$-$T_{j2}$ relationship. ($V_{\text{dc}} = 300$ V, $I_L = 10$ A).](image)

By substituting the experimental data into Equations (10) and (11) and employing MATLAB for linear fitting, the value of the coefficients $a$, $b$, $c$, $d$, and $e$ can be mathematically obtained:

$$V_{\text{ss'}\text{max}} = f_{V_{\text{ss'}\text{max}}}(T_{j1}) = 0.007895T_{j1} + 2.822$$

$$I_{\text{rrm}} = f_{I_{\text{rrm}}}(T_{j1}, T_{j2}) = -0.028957T_{j1} - 0.05317T_{j2} + 12.24594$$

The function between the phase leg temperature and the combined TSEPs under given working conditions can be derived as:

$$\begin{align*}
T_{j1} &= 126.6624V_{\text{ss'}\text{max}} - 357.4414 \\
T_{j2} &= -68.9656V_{\text{ss'}\text{max}} - 18.8076I_{\text{rrm}} - 35.6959
\end{align*}$$

where in Equations (13)–(15), the units of voltages, currents, and temperatures are given in volts, amperes, and Celsius degrees, respectively.

4. Temperature Verification and Online Measurement Discussion

To validate the accuracy of the proposed method, experimental verification is conducted by heating both $S_1$ and $S_2$ to another temperature of 130 °C. At this time, the peak reverse recovery current and the peak induced voltage are 23 A and 3.85 V, respectively, as shown in Figure 10. The derived Equation (12) is then utilized to calculate the temperature of the upper and lower switches, which are found to be 130.2 °C and 131.4 °C, with an error of less than 1.5 °C.

When the proposed method is applied to actual systems, offline calibration of the SiC MOSFET device is performed beforehand. According to the experimental results, the variation in bus voltage affects the combined TSEPs. Hence, the proposed method is best suited for applications where the bus voltage remains constant. When extracting the junction temperature in the actual converter, only the current sensor needs to capture the specific load current $I_{\text{set}}$ to trigger the temperature monitoring unit. Subsequently, the measurement circuit can be employed to extract $V_{\text{ss'}\text{max}}$ and $I_{\text{rrm}}$ at the lower switch, and the bridge temperature could be obtained based on the established lookup model.

The peak induced voltage $V_{\text{ss'}\text{max}}$ can be directly obtained by using a peak detection circuit. Similarly, the peak reverse recovery current $I_{\text{rrm}}$ can be obtained by sampling $v_{\text{ss'}}$ and applying an integrator to the s and s’ lead [25]. The complete measurement flowchart is illustrated in Figure 11.
It is worth noting that both parameters, $V_{ss'max}$ and $I_{rrm}$, can be obtained with the help of parasitic inductance. The accuracy of the method is solely dependent on the measurement accuracy of voltage $V_{ss'max}$ and current $I_{rrm}$. However, accurate determination of parasitic inductance can just as well avoid the repetitive offline calibration process for different devices in the same circuit, which can be realized by the methods suggested in [26,27]. As a result, the proposed method is non-intrusive and can ensure the normal operation of the system.

Device degradation is a common challenge for the majority of the existing TSEPs utilized for SiC MOSFETs [28]. Specifically, the reliability of gate oxide affects the peak induced voltage $V_{ss'max}$ as bias temperature instability (BTI) stress can cause a shift in $\frac{di}{dt}$ [29]. Additionally, device package degradation has an effect on both peak induced voltage $V_{ss'max}$ and peak reverse recovery current $I_{rrm}$. To mitigate estimation errors resulting from device degradation, it is necessary to periodically recalibrate the TSEP of the SiC MOSFET with respect to temperature.
5. Conclusions

This paper proposes a novel bridge-level junction temperature measurement method for SiC MOSFETs by combining the transient voltage and current peaks across the lower switch. It is found that in a half-bridge commutation process, the peak induced voltage has a positive temperature coefficient with the upper switch, and the peak reverse recovery current has a positive temperature coefficient with both upper and lower devices.

A DPT platform is used for switching characteristic analysis. Both peak induced voltage \( V_{ss'}^{\text{max}} \) and peak reverse recovery current \( I_{rrm} \) demonstrate a desirable linear relationship with temperature at a steady state. The temperature sensitivity of \( V_{ss'}^{\text{max}} \) to the upper switch is about 8 mV/°C, while that of \( I_{rrm} \) to the lower switch is about \(-53 \, \text{mA/°C}\) when the bus voltage is 300 V and the load current is 10 A.

The accuracy of the proposed method is verified by testing at another temperature point through the DPT platform, where the bridge temperature can be independently monitored with an error margin of less than 1.5 °C. All the parameters required for this method can be extracted through the parasitic inductance \( L_{sp} \) between the source and auxiliary source of the device with a Kelvin connection, making it non-intrusive and online feasible. Moreover, only a temperature measurement circuit at the lower switch is necessary, which simplifies the design of the circuit isolation stage and reduces the number of measurement circuits.

Future work includes the development of an online temperature monitoring unit for the proposed temperature-sensitive parameters in practical converters and aging compensation strategies.

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