

Article

Modelling of Bidirectional Three-Phase Four-Wire Three-Level NPC MLC under Single-Loop Current Sensorless Control

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Abstract: Single-loop current sensorless control allows for abolishing of the instantaneous current measurement in the control system using only a single control loop with voltage feedback to stabilise the DC-bus voltage. This approach eliminates current sensors in the control circuit, benefiting from saving space on the printed circuit board and minimising power dissipation in the current measurement circuitry. This paper focuses on the single-loop current sensorless control applied to bidirectional three-phase four-wire three-level NPC MLC by simulation analysis and demonstrates the performance of the proposed current control algorithm in the rectifier and inverter modes and the step response with power direction change and grid-voltage change. In capacitor voltage balancing, an additional controller is applied, which is capable of compensating for the voltage asymmetry caused by adding a 2.5 kOhm resistor in parallel to one of the DC-bus capacitors. Our results demonstrate good performance of the proposed control method both in the inverter and rectifier modes, showing stable current shape in the low power and full power modes with acceptable harmonics content, meeting the requirements of the IEC 61000-3-2 standard for Class A devices. The analysis showed that the proposed control approach is suitable for industrial application.



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Keywords: AC/DC converter; rectifier; inverter; bidirectional power control; current control; sensorless control

1. Introduction

Developments in power electronics follow different directions. Novel ideas in material science provide for switching elements with close to ideal switch parameters. The module-type packaging allows designing of industrial types of converters based on various topologies packed in the module. Among those most frequently used in the industry are half-bridge and full-bridge topologies; however, module-type packaging for T-type, multi-level neutral-point clamped and matrix topologies that have appeared on the market are becoming the industry standard topology. Development of the module packaging allows for the use of most of the benefits of technologies such as SiC [1] and GaN [2] switches, resulting in higher efficiencies and more compact design of the end product.

Researchers are also focusing on new control approaches applied to the mitigating issues of the power electronics converters introduced by new applications of switching converters. The Green Deal or Energy Transition pushes industry to develop power converters with high reliability for such applications as e-mobility, photovoltaics, etc. For this reason, the converters should have redundancy to basic faults [3] or should be equipped with condition monitoring by using dedicated measurement circuitry and/or special data processing techniques to estimate degradation of the main components. The importance of device reliability in PELS converters is well discussed in [4], providing arguments in favour of condition monitoring and a review on corresponding techniques. Condition monitoring of MOSFET and the IGBT module based on a modified PWM strategy and measurement routine capable of detecting bond-wire lift-offs due to increased voltage drops

at semiconductor terminals is reported in [5]. Another approach based on short-circuit current monitoring to detect bond-wire problems is described in [6]. End of life estimation of power electronics converters using multiple approaches to obtain confident results has been studied in [7]. Some other researchers explain techniques for online parasitic component estimation, such as equivalent serial resistance of the capacitor [8–10], inductor active resistance [10], etc.

Traditionally, a double-loop control method has been used for most of AC/DC converters where the outer (slow) control loop stabilises the DC-bus voltage, and the internal (fast) control loop controls the current sinking or sourcing to the grid [11–13]. The PID regulator is used mainly due to its simplicity. This approach, however, does not always cover the requirements for dynamic and steady-state performance; as a result, new control methods, such as model predictive pulse pattern control [14] and deadbeat control [15], are proposed in the literature.

In single-loop control approaches, only a single voltage control loop is used to stabilise the DC-bus voltage. This control method type has been approved in various single-phase power-factor correction topologies: boost-type [16–18], full-bridge [19], half-bridge [20], totem-pole [21], bridgeless [22], dual-boost [23], and five-level NPC MLC [24,25]. Recent research papers have described the mentioned control approach applied to three-phase converter topologies, such as the full-bridge three-wire converter [26–29], full-bridge four-wire converter [30], and four-switch full-bridge three-wire converter [31].

This paper studies the single-loop current sensorless control (SL, CSC, SL-CSC) approach applied to the three-phase four-wire three-level NPC MLC (see Figure 1) that could run without current sensors operating both in the rectifier and inverter modes. The paper is organised as follows: Section 2 describes the methods of the research, mainly focusing on the implementation of the SL CSC; Section 3 presents the results of the simulation analysis of the SC CCSC applied to the three-phase MLC. The conclusions are drawn at the end of the paper.

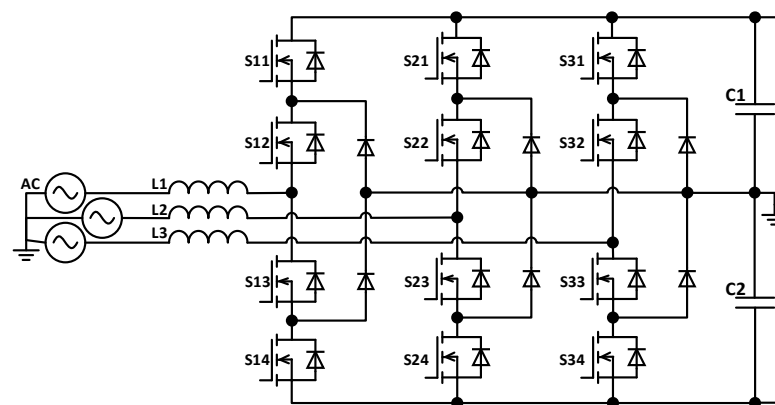


Figure 1. Three-phase four-wire three-level NPC inverter topology.

2. Methods

The single-loop controller uses only a single control loop with voltage feedback to stabilise the DC-bus voltage, while the current controller is replaced with the math block responsible for the duty cycle calculation based on the reference current value and acquired grid and DC-bus voltage values.

2.1. Switching State Table

The selected topology contains three L-type input filters, three legs of 3-level NPC block available in an “off-the-shelf” solution with standard module-type industrial packaging, as well as two DC link capacitors connected in series, while the middle point is connected to the diode’s middle point of all three NPC modules and also to the common neutral potential. Considering that the NPC MLC topology has four-wire connection, the analysis of the

three-phase converter could be reduced to three identical and independent single-phase NPC MLCs with the capacitor middle point connected to the neutral wire. The current paths for different switching states are shown in Figure 2.

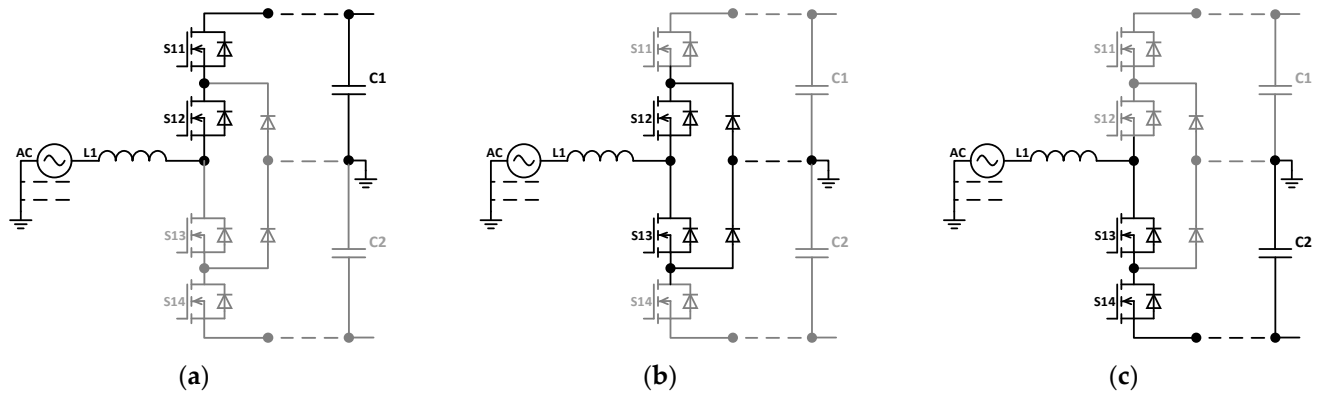


Figure 2. Commutated current paths according to the selected voltage pole: (a) level 1 (voltage pole $+V_{DC}/2$), (b) level 0, and (c) level -1 (voltage pole $-V_{DC}/2$).

Different operation scenarios are possible during inductor's current zero crossing: (1) bipolar voltage switching during the whole switching period that allows maintaining of the continuous current mode (CCM) and (2) bipolar voltage switching with a high-Z state period after the current drops to zero value. The latter considers the discontinuous current mode (DCM) in the inductor and thus is preferable. The reason is that the proposed CSC method inherits an accumulated volt-second error effect, resulting in current shape degradation during the CCM period [32]. Instead, the DCM operation allows resetting of the volt-second error during the current zero crossing, ensuring the current starts from the zero point in the following switching cycle, which helps to maintain a sinusoidal shape of the grid current (see Figure 3). It is obvious that the shorter the CCM period, the smaller is the accumulated volt-second error; as a result, the impact on the sinusoidal shape of the inductor's current is negligible.

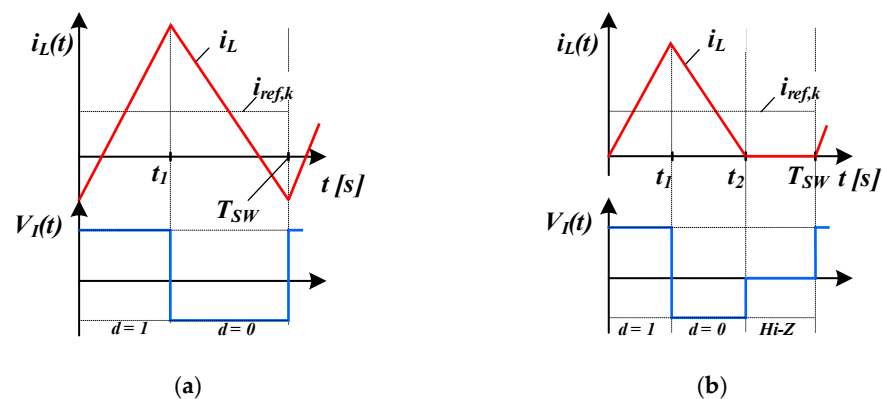


Figure 3. Preview of current control approaches during zero crossing: (a) bipolar switching where the inductor current operates in CCM and (b) bipolar switching with Hi-Z state where the inductor current operates in DCM.

In case a converter operates in a wide range of power, including less than 10% of the nominal power, a higher efficiency is expected to be obtained by using DCM during zero crossing. The reason is that, depending on the input inductor size, the DCM period of the grid-side inductor could share a noticeable part of the grid period.

The switching table below (see Table 1) contains the corresponding inductor voltages and their impact on the capacitor voltages, where I_M is the amplitude value of the reference

current value ($I_M > 0$ —rectifier mode, $I_M < 0$ —inverter mode), $d(t)$ is the control signal applied to transistors (1—inductor magnetisation state, 0—inductor demagnetisation state).

Table 1. Switching states of the bidirectional 3-phase 4-wire 3-level NPC MLC for phase A.

Power Mode	Grid Polarity	Voltage Level	Voltage Pole	PWM Output $d(t)$	Transistor Conduction State				Simplified Inductor Voltage	dVc1	dVc2
					Sx1	Sx2	Sx3	Sx4			
Rectifier ($I_M > 0$)	Positive ($V_a > 0$)	0	0	1	-	-	1	-	$V_L = V_a$	0	0
		1	$+V_{dc}/2$	0	1	1	-	-	$V_L = V_a - V_{C1}$	$+\Delta$	0
	Negative ($V_a > 0$)	1	$+V_{dc}/2$	1	-	1	-	-	$V_L = V_a$	0	0
		0	0	0	-	-	1	1	$V_L = V_a + V_{C2}$	0	$+\Delta$
High-Z ($I_M = 0$)	-	-1	$-V_{dc}/2$	-	-	-	-	-	$V_L = 0$	-	-
Inverter ($I_M < 0$)	Positive ($V_a > 0$)	Z	-	1	1	1	-	-	$V_L = V_a - V_{C1}$	$-\Delta$	0
		1	$+V_{dc}/2$	0	-	1	-	-	$V_L = V_a$	0	0
	Negative ($V_a > 0$)	0	0	1	-	-	1	1	$V_L = V_a + V_{C2}$	0	$-\Delta$
		-1	$+V_{dc}/2$	0	-	-	1	-	$V_L = V_a$	0	0

2.2. Current Sensorless Control

As mentioned previously, the main idea of the current sensorless control is to maintain a proper volt-second balance applied to a grid-side inductor to ensure that the average value of the inductor current can follow the reference value. In other words, the controller modulates the inverter's output voltage by proper calculation of the magnetisation and demagnetisation periods to ensure the average inductor current follows a sinusoidal shape of the reference signal without the current feedback. For that purpose, the CSC block should be aware of the voltage levels to be applied to the inductor for the upcoming switching period.

In order to minimise the number of inductor voltage equations from Table 1, the single switch model can be applied to each phase of the converter that uses Boolean functions to track the voltage-source component changes in the current path as well as the polarity of the capacitors. In this relation, $gtz(x)$ (greater than zero) is defined as follows:

$$gtz(x) = \begin{cases} 1, & \text{if } x \geq 0 \\ 0, & \text{if } x < 0 \end{cases} \quad (1)$$

This function allows reduction of the number of equations of the converter output voltage down to two for the magnetisation ($V_I^{d=1}(t)$) and demagnetisation states ($V_I^{d=0}(t)$):

$$V_I^{d=1}(t) = gtz(-I_M) \cdot (gtz(v_g(t)) \cdot v_{C1}(t) - gtz(-v_g(t)) \cdot v_{C2}(t)), \quad (2)$$

$$V_I^{d=0}(t) = gtz(I_M) \cdot (gtz(v_g(t)) \cdot v_{C1}(t) - gtz(-v_g(t)) \cdot v_{C2}(t)) \quad (3)$$

where $v_g(t)$ is the grid voltage, $v_{C1}(t)$ and $v_{C2}(t)$ are DC-bus capacitor voltages.

Depending on the grid voltage polarity and the direction of converter power flow (rectifier or inverter), the final values from the above-defined equations are visualised in Figure 4.

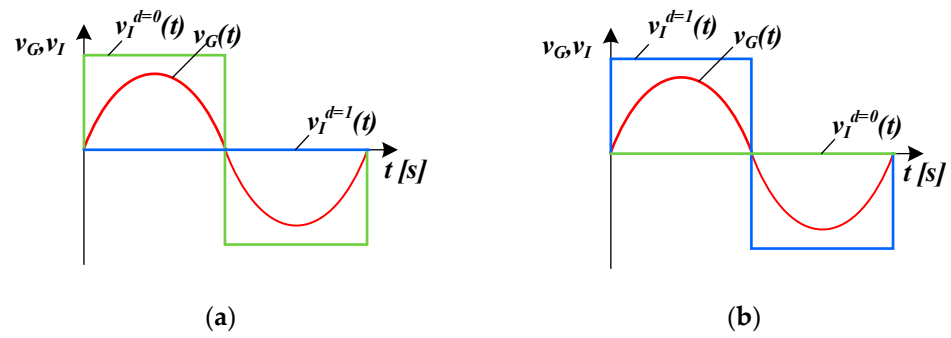


Figure 4. Analytical shapes of converter modulated voltages: (a) rectifier mode and (b) inverter mode.

It is assumed that grid and capacitor voltages remain constant during a single switching cycle; thus, the inductor's current rises and falls linearly, as shown in Figure 5.

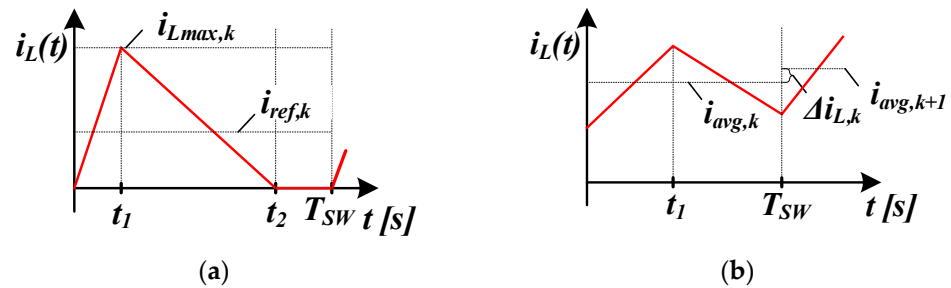


Figure 5. Simplified current shapes and corresponding parameters during (a) DCM and (b) CCM.

Moreover, the time-variant inductor current can be transformed to discrete values by mathematical averaging in order to simplify the calculations within a single switching cycle:

$$I_{ref,k} = I_{avg,k} = 1/T_{sw} \int_{k \cdot T_{sw}}^{(k+1) \cdot T_{sw}} I_M \cdot \sin(t) dt = 1/T_{sw} \int_{k \cdot T_{sw}}^{(k+1) \cdot T_{sw}} i_L(t) dt \quad (4)$$

where $I_{ref,k}$ is the average reference value for the k -th switching period, $I_{avg,k}$ is the average inductor current for the k -th switching period, T_{sw} is the switching period, I_M is the amplitude of the reference signal.

The same average inductor current can be defined from the basic inductor equation, where the current depends on the applied voltage:

$$I_{avg,k} = 1/T_{sw} \left(\int_{k \cdot T_{sw}}^{k \cdot T_{sw} + t_{1,k}} \frac{v_G(t) - v_I^{d=1}(t)}{L} dt + \int_{k \cdot T_{sw} + t_{1,k}}^{k \cdot T_{sw} + t_{2,k}} \frac{v_G(t) - v_I^{d=0}(t)}{L} dt \right) \quad (5)$$

where $v_G(t)$ is the grid voltage, $v_I^{d=1}(t)$ is the converter's voltage during the magnetisation period, $v_I^{d=0}(t)$ is the converter voltage during the demagnetisation period, L is the inductor's inductance, the time slot from $(k \cdot T_{sw})$ to $(k \cdot T_{sw} + t_{1,k})$ is the magnetisation period, the time slot from $(k \cdot T_{sw} + t_{1,k})$ to $(k \cdot T_{sw} + t_{2,k})$ is the demagnetisation period.

As we assumed previously that the grid voltage and capacitor voltages stay almost constant within a single switching cycle, it is reasonable to replace the time-variant voltage variables with discrete constant values, with the index k representing the number of the switching period.

Thus, Equation (5) can be rewritten as follows:

$$I_{avg,k} = 1/T_{sw} \left(\frac{V_{G,k} - V_{I,k}^{d=1}}{L} \cdot t_{1,k} + \frac{V_{G,k} - V_{I,k}^{d=0}}{L} \cdot (t_{2,k} - t_{1,k}) \right). \quad (6)$$

The following equation defines the maximum inductor current during the magnetisation period:

$$I_{Lmax,k}^{dcm} = \frac{V_{G,k} - V_{I,k}^{d=1}}{L} \cdot t_{1,k} \quad (7)$$

where $i_{Lmax,k}^{dcm}$ is the inductor's maximum current during the k -th switching period.

The average current value during DCM can be also defined using the peak current value as follows:

$$I_{avg,k} = \frac{I_{Lmax,k}^{dcm} \cdot t_{2,k}}{2 \cdot T_{sw}} \quad (8)$$

In addition, it is possible to define the ratio between the total current flowing period (t_2) and the magnetisation period (t_1):

$$t_{2,k} = \left(1 - \frac{V_{G,k} - V_{I,k}^{d=1}}{V_{G,k} - V_{I,k}^{d=0}} \right) \cdot t_{1,k} \quad (9)$$

Finally, it is possible to define the equation for the inductor's magnetisation period to get an average current to follow the reference value during DCM by substituting the variable from Equation (8) for definitions from Equations (7) and (9):

$$D_{dcm,k} = \frac{t_{1,k}}{T_{SW}} = \sqrt{\frac{2 \cdot I_{avg,k} \cdot L / T_{sw} - V_{G,k} + V_{I,k}^{d=0}}{(V_{G,k} - V_{I,k}^{d=1}) \cdot (V_{I,k}^{d=1} - V_{I,k}^{d=0})}} \quad (10)$$

The magnetisation period during CCM can be calculated from Equation (6), where t_2 is replaced with T_{sw} . The integration of the inductor's voltage within a single switching period during CCM allows estimation of the end value of the current with respect to the starting point. Taking into account that the peak-to-peak value of the current remains almost constant between neighbouring switching cycles, the difference between the end value and the starting value is almost equal to the difference in the reference current between the neighbouring switching cycles ($\Delta I_{avg,k}$). Then the transistor's control signal can be defined as follows:

$$D_{ccm,k} = \frac{t_{1,k}}{T_{SW}} = \frac{\cdot I_{avg,k} \cdot L / T_{sw} - V_{G,k} + V_{I,k}^{d(t)=0}}{V_{I,k}^{d(t)=0} - V_{I,k}^{d(t)=1}} \quad (11)$$

The minimal value of the two control equations should be finally applied to the transistors to implement CSC.

2.3. Controller Design

A PI controller is used to stabilise the DC-bus voltage that has positive and negative output value ranges, where positive values correspond to the rectifier mode, while the negative range activates the inverter mode (see Figure 6).

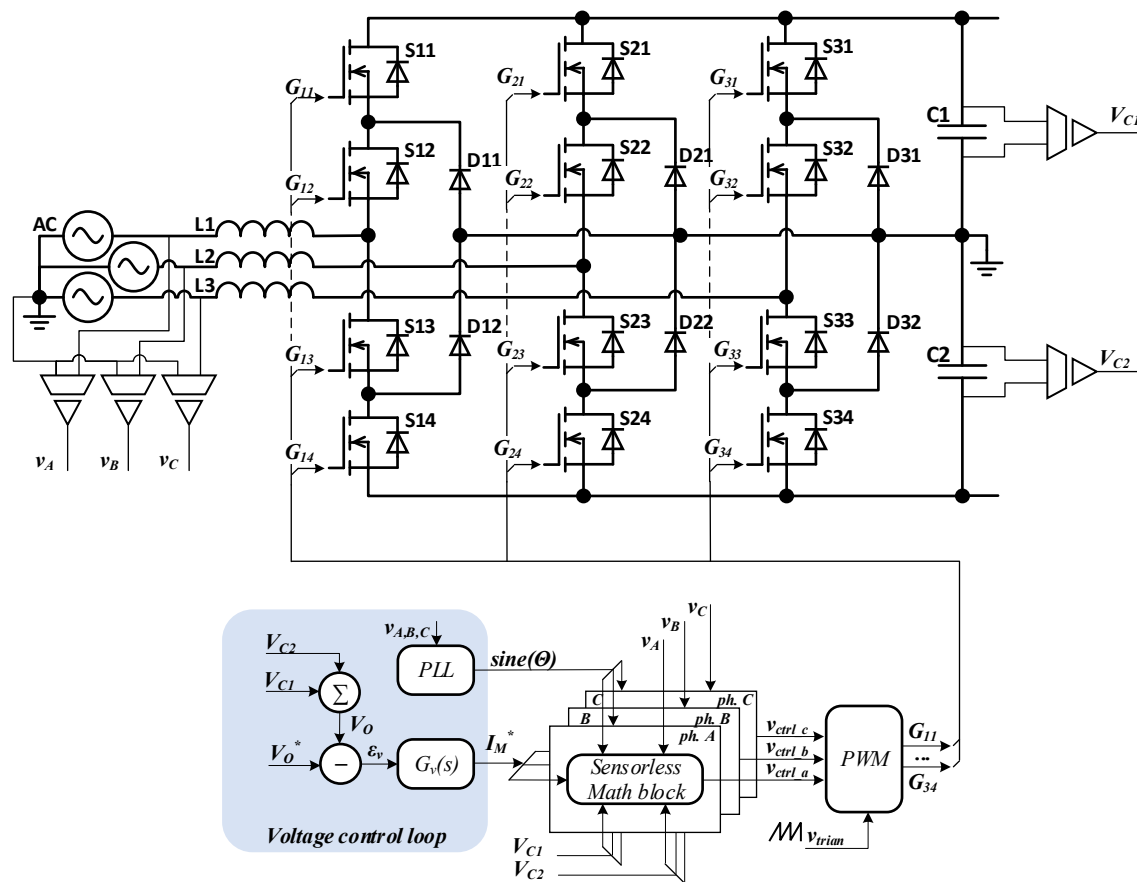


Figure 6. Block diagram of the single-loop CSC algorithm.

As can be seen from the figure above, each phase is provided with individual current control. Figure 7 shows a detailed block diagram of the sensorless math block.

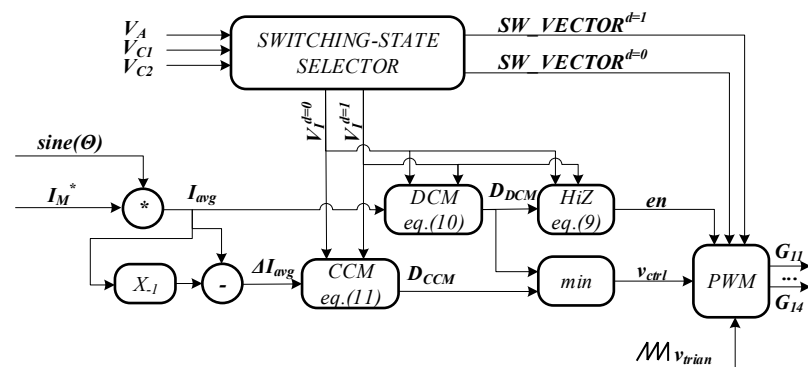


Figure 7. Block diagram of the “sensorless math-block” for phase A.

It is worth mentioning that the table data (in the block diagram above) contain the switching states, and also the corresponding inductor voltage equation (in the form of a mask of used measurements presented in the inductor’s voltage equation), as well as the capacitor voltage differential. The CSC algorithm is not influenced by the table data, which means that by changing only the table data it is possible to apply the proposed algorithm to another multilevel topology. An example is the 9-level ANPC MLC topology [33].

2.4. Capacitor Voltage Balancing

In ideal conditions, capacitor voltages fluctuating with triple grid frequency have voltage level crossing each $\pi/3$ angle starting from $\pi/6$. Nevertheless, due to the foreseen small imprecisions of CSC and manufacturer tolerances of the DC-link capacitors, capacitor voltage imbalance occurs in real world applications. Thus, an additional P-controller is implemented to adjust the reference current amplitude of phase A (see Figure 8).

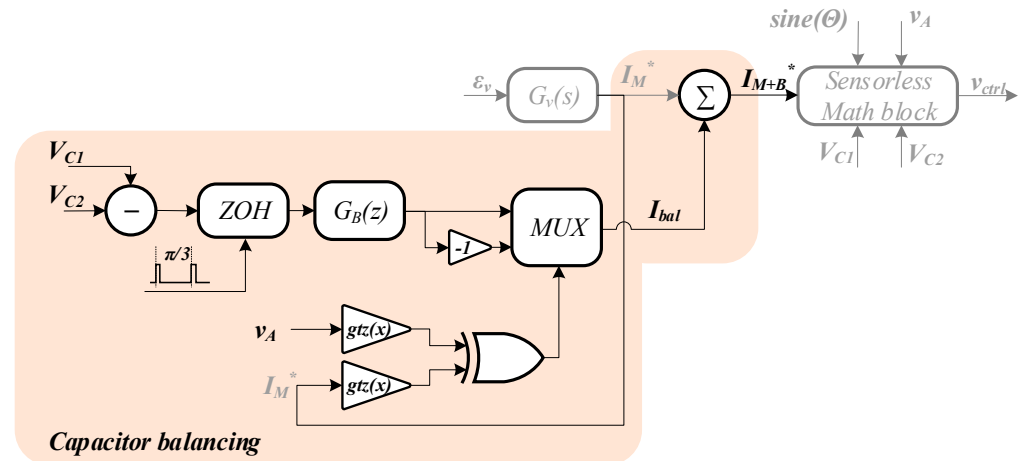


Figure 8. Block diagram of the capacitor balancing controller added to phase A CSC.

The voltage difference of the two capacitors is applied to the PI-controller ($k_p = 0.1$, $k_I = 0.1$), whereas the output value is interpreted as an extra amplitude to the reference current of phase A. Since capacitor charging or discharging depends on the polarity of the input voltage and the power flow direction, an additional multiplexer that selects the sign of the balancing current amplitude is introduced. Finally, the summation of the balancing amplitude and the reference signal takes place and the result is supplied to the CSC math block.

3. Results

The proposed control method was evaluated by simulation analysis using the PSIM software. In the control algorithm, a simplified C-code block available from built-in PSIM control blocks was used.

The simulation parameters are as follows: grid voltage (RMS) $V_G = 230$ V; grid frequency $f_{AC} = 50$ Hz; capacitor nominal voltages $V_{C1}, V_{C2} = 400$ V; inductance $L_{a,b,c} = 1$ mH; capacitance $C_1, C_2 = 4.7$ mF; switching frequency $f_{sw} = 20$ kHz.

3.1. Rectifier Mode

The rectifier mode was evaluated at two reference values: 1 A and 10 A. The first case (see Figure 9a) has DCM during the full input voltage period, shown by the bottom graph, where the DCM control signal has a lower value than the CCM control signal within the full grid period. Nevertheless, the average inductor current seen on the top graph perfectly matches the reference sinusoidal signal.

The second case (see Figure 9b) corresponds to 90% of the nominal power, where DCM takes place for a very short period near the zero crossing of the reference signal. The inductor operates mostly in CCM, which can be noticed by comparing the two control signals in the bottom graph of Figure 9b. An average current value follows the reference signal with minor deviation.

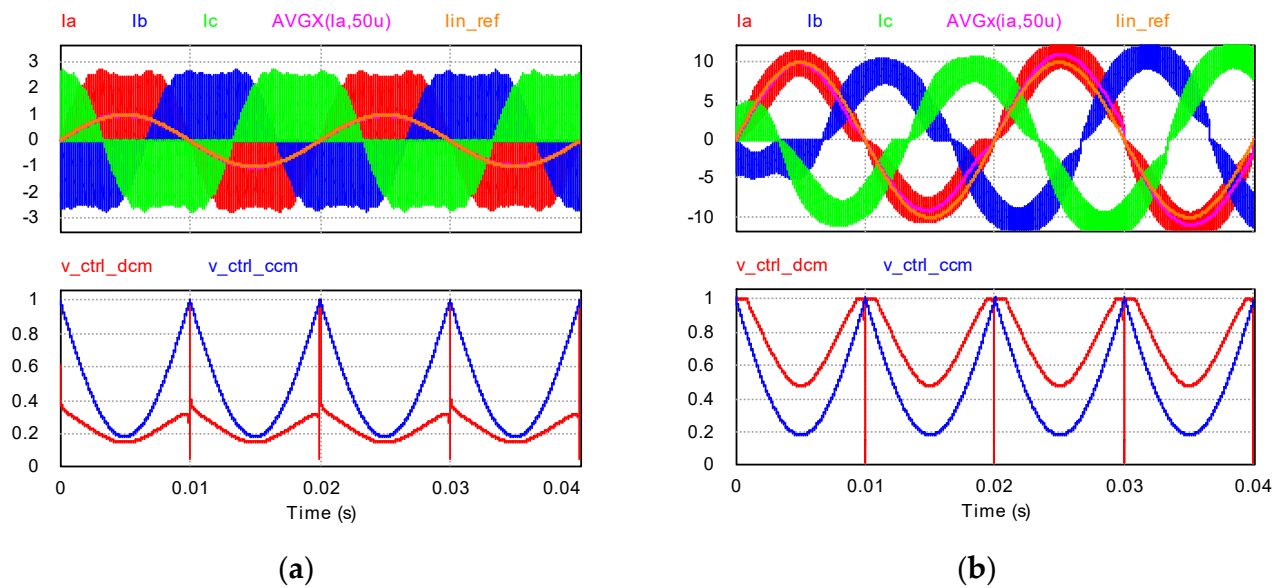


Figure 9. Simulation results of the rectifier mode: (a) reference value $I_M = 1$ A and (b) reference value $I_M = 10$ A (x-axis is time [s], top graph y-axis is current [A], bottom y-axis is duty ratio [%]).

3.2. Inverter Mode

The inverter mode was simulated at two power points: -1 A and -10 A (see Figure 10). In both cases, the average current follows the reference value without any noticeable difference.

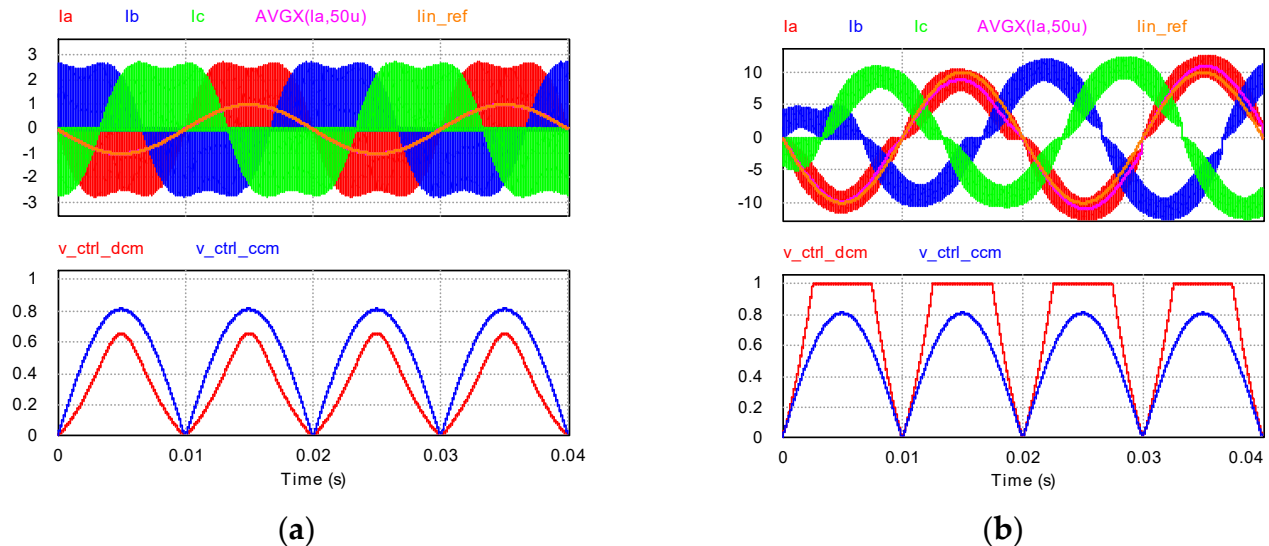


Figure 10. Simulation results of the inverter mode: (a) reference value $I_M = -1$ A and (b) reference value $I_M = -10$ A (x-axis is time [s], top graph y-axis is 3-phase current, average A-phase current and A-phase reference current [A], bottom y-axis is SL-CSC calculated duty ratio for DCM and CCM [%]).

The current harmonic analysis is presented in the Table 2 for the inverter and rectifier modes at full power. The simulation results show that the harmonic distortion of the proposed controller meets the requirement of the IEC-61000-3-2 standard for a Class A device.

Table 2. Harmonic analysis of input current.

Order of Current Harmonics		Class A Limit	Phase A Current	
			Rectifier (4 kW)	Inverter (−4 kW)
Fundamental		-	10.1	10.1
Even	3	2.3	0.11	0.07
	5	1.14	0.11	0.1
	7	0.77	0.092	0.082
	9	0.4	0.075	0.069
	11	0.33	0.056	0.052
	13	0.21	0.05	0.046
$15 \leq h \leq 39$		0.15	<0.05	<0.04
Odd	2	1.08	0.147	0.131
	4	0.43	0.014	0.02
	6	0.3	0.031	0.033
	$8 \leq h \leq 40$	0.23	<0.03	<0.02

3.3. Capacitor Balancing

The capacitor balancing controller was tested by adding a 2.5 k resistor in parallel with capacitor C2 at time 0.1 s and activated at time 0.2 s. As can be seen from the figure, the two capacitor voltages are equalised 0.15 s after the balancing controller is activated (see Figure 11).

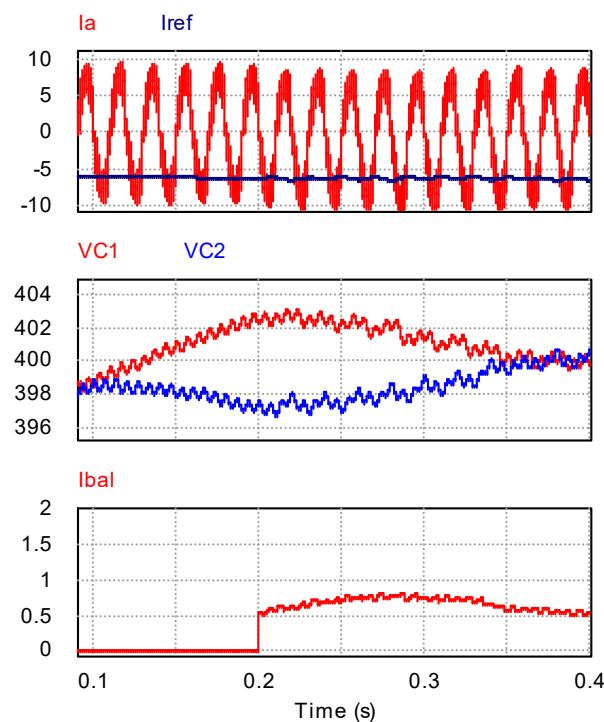


Figure 11. Simulation result of the capacitor balancing controller (x-axis is time [s], top graph y-axis is phase A current [A], middle y-axis is capacitor voltages [V], bottom y-axis is balancing current [A]).

3.4. Step Response with Conversion Mode Change

The step response simulation with the power flow direction change was performed by adding a 5 A controlled DC current source to the DC-bus driven by control pulses at 3 Hz, which resulted in 4 kW power sourcing or sinking from the DC-bus. The results of the simulation (see Figure 12) demonstrated good performance of the proposed SL-CSC that can stabilise the DC-bus voltage within 0.1 s. This performance is comparable to similar

control system settling times found in the literature. For instance, a 100–150 ms settling time has been demonstrated in [28,31] at a load step change from 50% to 100%.

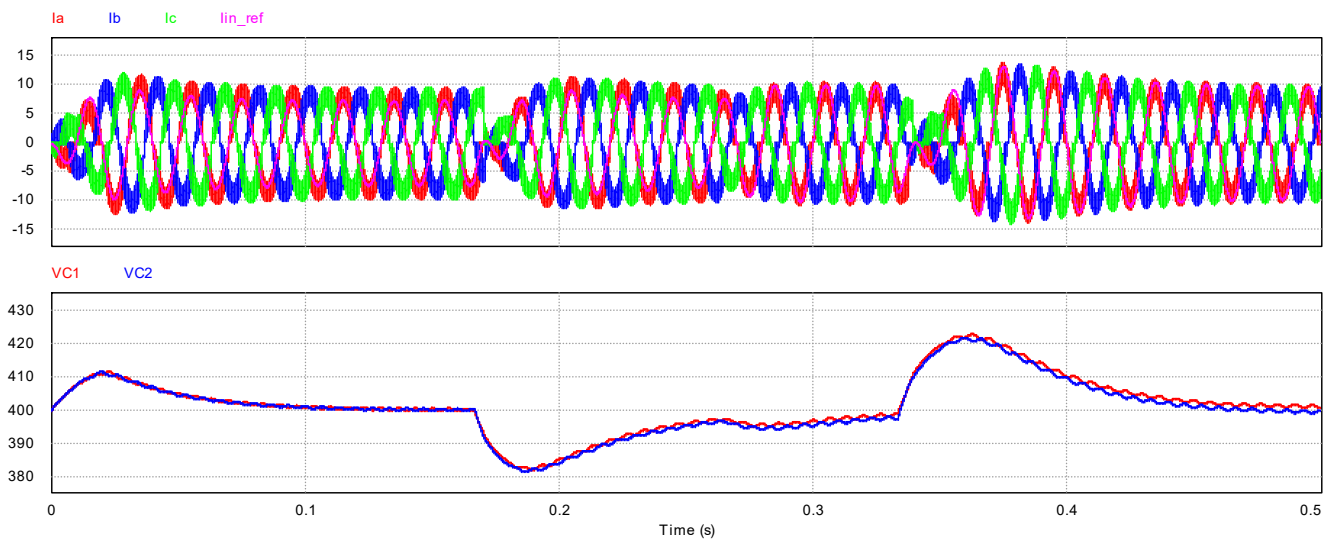


Figure 12. Simulation results of step response with the bidirectional power flow (x-axis is time [s], top graph y-axis is 3-phase current and A-phase reference current [A], bottom y-axis is capacitor voltages [V]).

3.5. Grid Voltage Step Response

The grid voltage step response was simulated as well (see Figure 13). The proposed converter was operating at nominal power (4 kW) when the input voltage amplitude was changed from 292 to 357 V at time 0.1 s, which corresponds to the voltage step from 90% to 110% of the nominal amplitude (325 V). Some slight increase of the DC-bus voltage could be observed right after the step event. The reaction of the PI regulator resulted in the reduction of the grid current amplitude. The new equilibrium point was reached in 0.1 s after the voltage step event. Meanwhile, the CSC mathematical block reacted at the next switching period by recalculating the duty cycle signal that corresponds to the new grid voltage. Thus, the current shape of the inductor was not influenced.

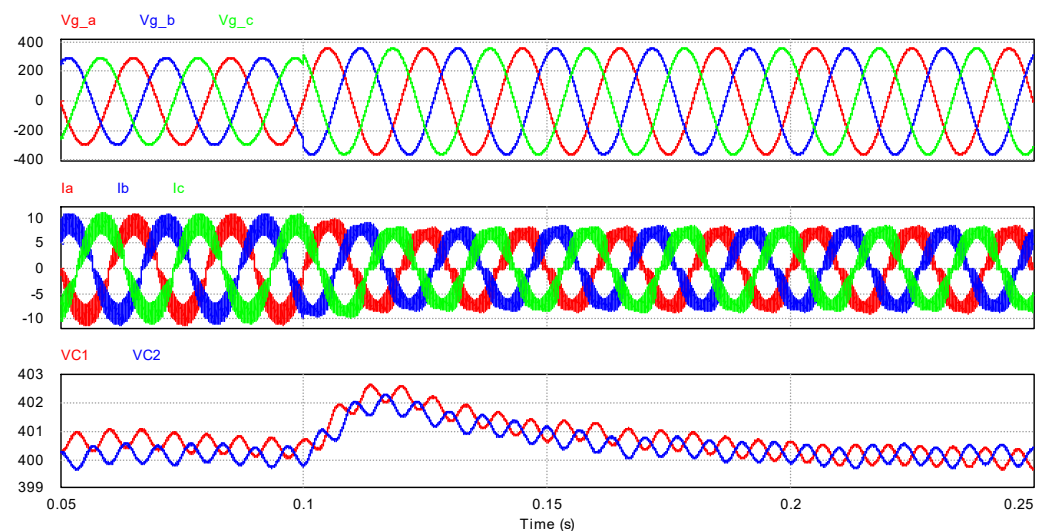


Figure 13. Simulation results of grid voltage step response (x-axis is time [s], top graph y-axis phase voltages [V], middle graph y-axis phase currents [A], bottom graph y-axis capacitor voltages [V]).

4. Discussion and Conclusions

The single-loop current sensorless control (SL-CSC) algorithm was applied to a three-phase four-wire three-level neutral-point clamped multilevel converter (NPC MLC). This is the first application of the proposed sensorless approach to the mentioned topology. The paper gives a detailed analytical description of main operation modes with key equations describing the mathematical basis of the proposed control algorithm. It is based on a few simple equations intended for the estimation of the inductor's voltage during the magnetisation and demagnetisation periods, which are used to calculate the corresponding duty ratio for the transistors. As a result, the average inductor current follows the reference value without the feedback from the current sensor, which allows for abolishing of the instantaneous current measurement in the control system and also the internal current control loop. Thus, only a single control loop with voltage feedback is finally used to stabilise the DC-bus voltage. This approach allows exclusion of the power losses related to shunt-based current sensors and an increase of the power density of the power electronics converter in the case where galvanically isolated current sensors are excluded.

The proposed algorithm suffers from an accumulated error effect during CCM of the inductor, which appears as a slowly increasing deviation from the reference value. This disturbance relates to the simplified mathematical equations used to estimate the inductor's voltage where the conduction losses caused by parasitic circuit elements are neglected. Consequently, a small volt-second error takes place in each switching period, resulting in an increasing deviation of the inductor's current from the reference value. Nevertheless, the paper describes the option of how to mitigate the described problem. The authors propose to use bipolar switching with high impedance state near the zero crossing that would ensure the DCM for the inductor. This helps to reset the accumulated error arising from the inductor's current that starts from zero each new switching period during DCM. However, if the inductor operates in DCM during the whole grid voltage period, there is no noticeable deviation from the reference value.

The capacitor voltage balancing was implemented by means of an additional PI controller. It monitors the voltage difference six times per grid period, when the capacitors' voltages should have identical values in the balanced condition. In the case of voltage error, it passes through the PI controller and the resulting extra current amplitude is added to the main reference value. The sign of the balancing current amplitude is modified according to the power direction flow and grid voltage polarity. Finally, the simulation analysis, where a 2.5 kOhm resistor was connected in parallel to capacitor C2, demonstrated an ability to compensate for the voltage asymmetry equal to 5 V in 0.15 s.

The simulation analysis demonstrated good performance of the proposed algorithm within a wide power range. The dynamic performance of the SL-CSC showed good results during the step response simulation with power direction change switching between a 4 kW source and 4 kW load connected to the DC-bus. The capacitor voltage overshoot stayed within 5% of the reference value with a settling time of 0.1 s, which is comparable to other similar control approaches mentioned in the literature. Moreover, the harmonic distortion of the proposed controller meets the requirements of the IEC 61000-3-2 standard for Class A devices.

Finally, it should be mentioned that the proposed current control algorithm could be easily modified for application to higher-level NPC MLC or even any other MLC topology. The mathematical block implementing the sensorless current control function is based on an invariant code written in the C programming language, while a specific description of the switching vectors is defined in the header file.

Further research is planned to include the experimental analysis and implementation of a hybrid (sensed and sensorless) control algorithm, demonstrating the benefits from both approaches.

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Abbreviations

ANPC	asymmetric neutral point clamped
GaN	gallium nitride
Hi-Z	high ohmic input state
IGBT	Insulated Gate Bipolar Transistor
MOSFET	metal oxide semiconductor field effect transistor
MLC	multilevel converter
NPC	neutral point clamped
PELS	power electronics
PID	proportional integral regulator
PWM	pulse width modulation
SiC	silicon carbide

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