

Article

Influence of Water Ingress on Surface Discharges Occurring on the Silicone Gel Encapsulated Printed Circuit Boards Developed for Deep-Sea Applications

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Abstract: This paper discusses the influence of water ingress on the electrical discharges that arise on the surface of printed circuit boards that are developed for deep sea applications. The primary concern is the electrical discharges arising on the surface of the PCB bridging localized spots/areas between conductive traces, high voltage terminal, mounting hole options, and so on. The current literature focuses on electrical discharges arising on the surface of PCB at low-pressure environments emulating aircraft and space applications. Extending the same approach to deep-sea environments is not feasible since the pressure is very high and the temperatures are very low. In all, a meager attempt has been made to investigate the possible application of such gel-encapsulated PCBs in adverse high-pressure, salt/sea water, low-temperature, deep-sea environments. This experimental study focuses on studying the influence of deionized and sea water on electrical discharges arising on the surface, between conductive tracks of PCB. A group of PCBs with different gaps between the conductive tracks was produced and immersed in deionized and seawater for a specific duration at standard pressure. Afterward, the discharge characteristics were measured the using partial discharge (PD) test method and the respective phase-resolved PD pattern was studied and analyzed. Pertinent experiments revealed that the PD process and eventual failure manifests as a typical and substantial pattern. The apparent charge measured during the PD inception and near-by failure condition, influenced by deionized and seawater, reveals a regular trend. Naturally, a simple observation of the PD pattern might help to identify the intricacy and to initiate a preventive measure well before the complete system suffers a premature failure. Also, based on these results, making slight structural modifications on the PCB at crucial locations might help in retaining the dielectric integrity of the material.

Keywords: printed circuit boards; dielectric gel; water ingress; high voltage; partial discharge; PRPD pattern; breakdown voltage



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1. Introduction

Modern electrical, and electronic systems developed for maritime applications use dielectric gel materials to encapsulate electrical, electronic, and high-voltage components along with the printed circuit board (PCB) to provide better insulation and gain a pressure-neutral solution. Printed circuit boards (PCB) employed in high-voltage and high-power electrical and electronic systems are more vulnerable to damages caused by surface electrical discharges [1]. The adverse environmental conditions such as low pressure, deep-sea

conditions, hydrolysis of seawater, and steep variations in temperature, aggravate these changes even under a reduced level of stress conditions which eventually lead to a tracking failure [2–4]. In this case, if these tracking failures are detected in an early stage, then it is easy to retain the condition of the PCB and circuitry; however, if unnoticed they may result in aging, permanent damage, and degradation [4]. Exercising preventive measures requires sensitive data that describe the intensity of surface electrical discharges occurring on the PCB and its circuitry. In this context, an experimental study that focuses on identifying discharges occurring on the surface of a PCB is initiated and the same is quantified and analyzed using a pattern-based approach. The adopted pattern-based approach is popularly known as phase-resolved partial discharge or briefly as PRPD and is invariably employed in ascertaining the dielectric integrity of high-voltage and high-power apparatuses in electric power transmission, distribution, and utilization networks [5].

The direct exposure of the electrical and electronic systems and their respective PCBs must withstand the effects of water ingress, pressure, and salt water, which may lead to material corrosion. Certain applications make use of corrosion-resistant pressure tolerant vessels, whereas a novel approach utilizes a silicone compound embedded in the components [6]. This silicone compound material is expected to serve as insulation and neutralize the mechanical forces uniformly to the enclosed components. It is known that silicone rubber is permeable to many gasses and that it can become saturated by water to some extent [7,8]. Pertinent water in the silicone encapsulation may penetrate components embedded and on the surface of the PCB, resulting in increased leakage currents causing corrosion [7]. As part of a multifaceted study, the suitability of using silicone rubber compounds in water absorption and their adequacy in encapsulating PCB, high voltage circuits and employing polyoxymethylene as enclosures have been investigated and the effect of water saturation has been experimentally determined [4,7–9]. In the present context, the influence of seawater and subsequent interactions on surface discharges is investigated.

The basic physics and deduced mechanisms of surface discharges and space-charge behavior that cause tracking failures and eventual dielectric breakdown in PCB have been intensively studied for more than four decades [10–19]. It is well-proven that external factors such as pollution, moisture, pressure, water ingress, and so on initiate electrical discharges between tracks, mounting holes, connectors, etc., and have significant impacts on the dielectric integrity of the PCB material [15–17,20]. In the case of multi-layered PCB, the discrepancy between the layers causes interior discharges, eventually resulting in permanent damage to the material [21]. Most of these investigations focus on conditions related to ambient, aircraft, and space applications [2,3,22]. In addition, the influence of moisture and water invasion while being operated in a humid environment has been studied and the failure mechanisms and probability of failure, and estimation of the lifetime of PCBs and electronic components are currently available [23]. Naturally, these investigations have resulted in design improvements and the development of better materials with moisture and discharge resistance. On the contrary, deploying the same under deep-sea conditions are entirely different. During this, the PCB boards, components, and circuitries require a pressure-neutral solution capable of handling water ingress, and material conductivity due to salt diffusion and higher pressure [4,8,9,24]. Despite all, there are very few data available, or at least in the public domain. The available data focuses on breakdown phenomena, tracking failures, related failure causes, and so on. This study analyzes electrical discharges arising on the surface of the PCB, encapsulated in silicone gel at standard pressure. The adopted silicone gel is capable of handling higher pressures of up to 600 bars [4,5].

2. Literature and Motivation

Literature works relevant to the present study were grouped into four categories and are discussed below.

2.1. Partial Discharges in Liquid and Gel Materials

Recent literature works report that the weaker spots in high-power semiconductor modules are the trenches in between the metallization edges and ceramic substrates [5,25–27]. These physical defects can be easily identified using a modern PD detection method and PRPD-based pattern analysis [5]. This is feasible since these defect conditions produce unique patterns specific to the defect condition. In addition, the humid environment may introduce moisture into the semiconductor modules which may cause deviations in the dielectric properties of the insulating materials [25]. These conditions are inadequate as the modules and converters are applied in lower- or higher-pressure environments. In this context, the application of liquid- and gel-based dielectric materials become a necessity to provide electrical insulation and to offer a pressure-neutral solution [4,24,26,27]. Experiments on specific dielectric materials have indicated that their application increases the breakdown and partial discharge characteristics of the modules and power converters [2,4]. The same has been extensively studied on low-pressure conditions to emulate their application on aircraft and space applications while they have yet to be investigated for deep-sea environments [4].

2.2. Dielectric Breakdown on PCB

The currently available literature works focus on correlating the influence of lower pressures on the dielectric breakdown between tracks in PCB boards. Recently, an attempt has been made to study the effect of water saturation on the breakdown strength of standard PCB with dielectric encapsulation developed for deep-sea applications [4]. It appeared that the water ingress reduced the breakdown strength of the material as well as an anomalous breakdown on the rear surface. It is also noted that the breakdown behavior did not change significantly during rear surface breakdown over the evaluation period for the sample immersed in seawater [8]. Pertinent reasons might be due to the weak bonding between surfaces and the deposition of salts in the outer layer of the test specimens [18].

2.3. Reasons for a Failure and Material Degradation

The reasons and types of failures in PCB may not only depend on the material structure/arrangement but also on environmental factors [2,21]. For instance, the literature reveals that the common failures in PCB are due to surface discharges while the same for multi-layered arrangements are due to the weak spots such as the interface between layers, gaseous or metallic inclusions in the materials, and metal-coated drill holes, respectively [2,21]. The reason for such failures in multiple layers and metallic/gaseous inclusions and metallic holes is influenced by the stronger and divergent electric fields. In addition, external factors such as lower pressure, deep-sea conditions [2,4,21], etc., initiate situations conducive to the development of electrical discharges on the surface of the PCB boards and in between circuitry. It has been identified that the lower pressure increases the endurance level insulation breakdown on the surface of the PCB boards and is very different from that of the same occurring in ambient pressures [21]. As the pressure decreases, the failure due to surface tracking on the PCB board emerges slowly [2].

2.4. Impact of Water Ingress of Moisture on PCB

Moisture ingress on the PCB material and its encapsulation can alter its dielectric properties [4,6–8]. In particular, exposure to adverse humid environmental conditions can induce electrochemical corrosion on the materials [28]. In all, the insulation resistance of the material is relatively more sensitive while ascertaining DC material properties [28]. Alternatively, frequency domain spectroscopy can ascertain the same and quantify the AC material properties with more sensitivity and accuracy [4,6–8]. Recent research work has resulted in PCB laminates with moisture-resistance properties that can be developed and applied in a real-time scenario [29]. During this, the base materials can be purely renewable so that they are environmentally friendly, however are more sensitive to water or moisture absorption. Alternately, in addition to a renewable base, non-toxic composite materials such as epoxidized linseed oil, melamine polyphosphate, and flax fibers can be used in

developing PCB boards. Experiments reveal that the water/moisture absorption can be reduced from 4.87% to 1.15% and the electrical properties of the PCB improved by means of chemical treatment [28,29]. However, it has also been reported that these alternate materials are not a wise choice, since they tend to absorb moisture which reduces their dielectric integrity [30] and interferes with the performance of electronic devices [30].

In summary, it emerges from the existing literature that the current ‘know-how’ on the occurrence of surface discharges on PCB boards focuses on their application in low-pressure environments. There is literature that discusses the influence of moisture on laminates, the impact of pollution layer on PCBs, failure reasons, and material degradation due to discharges, and so on. However, there are very few literature works that focus on PCBs and laminates that are developed and deployed for deep-sea applications, where the pressure is very high (e.g., 600 bar at 6000 m deep) and the temperature is lower than room temperature. The current practice is to use silicone gel encapsulation for achieving a pressure-neutral solution. So, naturally, it is necessary to understand the permeation of salt constituents of seawater during its invasion into materials and characterize the discharges arising on the surface of the PCB.

3. Materials and Methods

High voltage and high-power modules and electrical circuits in deep-sea environments require pressure-tolerant and/or pressure-neutral solutions. The pressure tolerant approach employs an enclosure that can withstand high pressure, while the pressure-neutral solution (equal pressure on all sides) utilizes ductile or flexible encapsulations (in some cases, contains an intermediate liquid) that neutralizes the pressure reaching the electrical electronic components, thereby protecting them [6]. The current practice is to employ a silicone gel that encapsulates the complete circuit, including the PCB. Electrical discharges may be initiated on the surface of the PCB at all places where higher electric fields prevail, such as the edges of conductive tracks, mounting holes, high-voltage terminals, etc. At the same time, the ingress of water might worsen the situation, aggravating the intensity of electrical discharges. To understand this, a group of PCBs with two conductive tracks, facing each other and encapsulated in silicone gel, was prepared and submerged in deionized and salt/sea water (at standard pressure), to study the effect of water absorption and saturation on electrical discharges that arise on its surface.

3.1. Test Samples

The adopted PCBs were prepared with flame retardant (identified as ‘FR’), NEMA class, and glass-reinforced epoxy resin laminate material, briefly identified as FR-4 material. The chosen FR-4 laminate material is hydrophobic and immune to water absorption. In addition, the FR-4 material manifests higher dielectric breakdown voltage (i.e., more than 55 kV). The permittivity of the FR-4 laminate is close to 4.7, and the surface and volume resistivities are $2 \times 10^{11} \Omega\text{-m}$ and $2 \times 10^{13} \Omega\text{-m}$, respectively. The FR-4 material was chosen since this laminate material manifests excellent dielectric and mechanical properties in dry and humid conditions and is popularly used for preparing PCBs. After selecting the laminate, several PCBs, each with two conductive copper tracks, physically separated with a definite intermediate gap, were printed. This arrangement also electrically separates the facing copper tracks with a definite spacing. The electrically separated ends of the copper tracks are semicircular to create a quasi-uniform field in the XY plane and emulate a proper high-voltage electrode. The XY plane was considered since the surface discharges occurring between the semi-circular ends of the tracks were studied. Figure 1 shows a schematic representation of a PCB sample without gel encapsulation. Later, the copper conductive tracks were coated with nickel to minimize, or if possible, to avoid oxidation problems that might occur during water ingress. This complete arrangement of FR-4 laminates with conductive tracks electrically isolated with a gap is herein called a PCB sample.

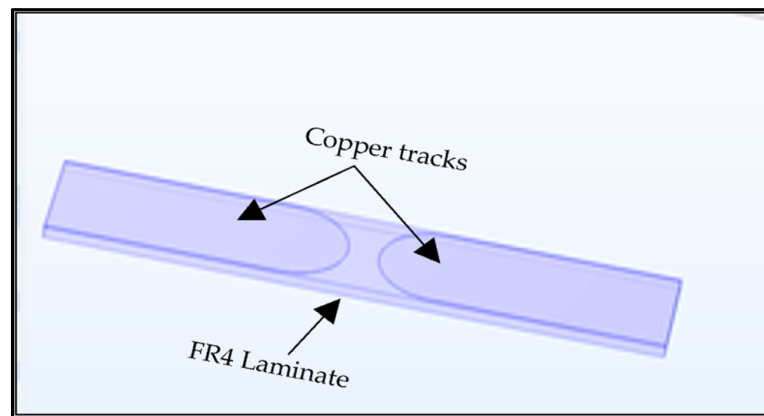


Figure 1. Schematic representation of a PCB sample prepared on FR-4 laminate material with two conductive tracks with intermediate gaps, to create a quasi-uniform electrode arrangement.

Several PCB samples with different spaces between their tracks viz., 3 mm, 5 mm and 10 mm were prepared. Another set of PCB samples was prepared with 5 mm intermediate spacing between their tracks, in which the FR-4 laminate between the tracks is cut open to form a slit. All these prepared PCB samples are then encapsulated in silicone gel and grouped as per their spacing, method of aging, test conditions, and so on.

Figure 2 shows typical specimens of the PCB samples used in this experimental study. Figure 2e shows a PCB specimen encapsulated with silicone gel. Table 1 shows the list of samples, the gap distance between the tracks, and test/aging conditions, respectively. The PCBs are developed using photoresist and galvanically applied using tin etch resist, followed by ammoniacal etching of the copper and stripping of the polymerized photo-Galvano resist. The thickness of the copper layer is approximately maintained at 35 μm . Since the chemical etching by nature will create a parabolic profile on the edges, the thickness would not be uniform throughout the electrode. No solder mask was applied, and no tinning layer was added, however, the surfaces are plated with a thin (2 μm to 5 μm) layer of nickel to avoid oxidation due to water ingress. All specimens are cleaned with isopropyl alcohol, rinsed, and soaked in de-ionized water for three days, and then further dried for three days in an oven at 50 $^{\circ}\text{C}$ before encapsulating them in silicone gel. The silicone gel was prepared at room temperature and consisted of an admixture of vulcanizing (RTV-2) siloxane elastomers (silicone gel and rubber). The encapsulation is done under a vacuum in two steps: a base layer of silicone is poured into a container to a height of approximately 8 mm, evacuated, and left to cure in a dry atmosphere (50 $^{\circ}\text{C}$, 20% RH). The PCBs are then placed on top of the base layer and filled in a further step, followed by vacuum degassing, up to a total height of 16 mm, and thereafter left to cure in a dry atmosphere for three days. After the test samples were adequately prepared, they were sorted into five groups with the first and second retained as new or virgin for the purpose of reference measurements. The third group was immersed in deionized water at 90 $^{\circ}\text{C}$, the fourth group was immersed in deionized water at 25 $^{\circ}\text{C}$ and the fifth group was immersed in sea water at 25 $^{\circ}\text{C}$. The samples were immersed in water for a period of 26 days after which they were retrieved and subjected to PD measurements.

During these measurements, it is not a feasible idea to deploy real-time sea water for aging studies since the same contains not only salts but also life forms and several other additional constituents that worsen the situation. This may result in complete corrosion of the test sample, test cell, pressure tank, contamination, life forms, etc. Consequently, the number of variables that influence the factors of measurement sensitivity and accuracy are highly erratic and cannot be used to understand the phenomena. In the present context, the influence of seawater ingress (i.e., water and salt depositions) on discharges was studied. So, the presence of other constituents, although forms a worst-case scenario, would max out

the failure condition. In this context, synthetic seawater (as recommended by the standard DIN 50905-4:2018-03 [31]) was adopted and used as a sea environment for testing purposes.

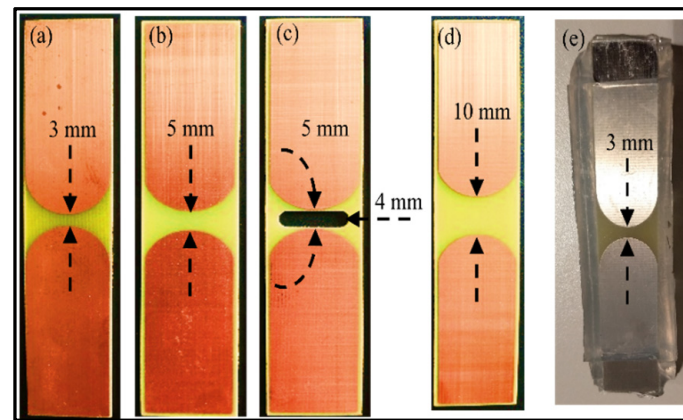


Figure 2. Specimens of the PCBs with two copper tracks spaced at different distances: (a) Gap of 3 mm; (b) Gap of 5 mm; (c) Gap of 5 mm with a slit of 4 mm wide and 1 mm in length; (d) Gap of 10 mm; (e) A sample of PCB with 3 mm gap between conductive tracks encapsulated in dielectric gel.

Table 1. Test samples and their respective aging conditions adopted.

Group	Test Samples	Gap between Tracks	Test Conditions
1	Virgin PCB ¹	5 mm	Without gel encapsulation
2	Virgin PCB ²	5 mm	With gel encapsulation
3	PCB ³	3 mm 5 mm 5 mm with 4 mm slit 10 mm	Deionized water at 90 °C
4	PCB ³	3 mm 5 mm 5 mm with 4 mm slit 10 mm	Deionized water at room temperature (RT)
5	PCB ³	3 mm 5 mm 5 mm with 4 mm slit 10 mm	Sea water in room temperature

¹ Reference: PCB is not encapsulated in silicone gel, not immersed in oil during PD testing. ² Reference: Samples encapsulated in silicone gel and tested while immersed in silicone oil. ³ FR4 laminate with copper tracks coated with nickel, PCB encapsulated in silicone gel.

3.2. Test Setup and Test Cell

The experimental study focuses on understanding electrical discharges arising on the surface of the chosen PCB samples conditioned/aged in deionized and salt or synthetic seawater. For this purpose, a partial discharge (PD) test method popularly used for measuring discharges on dielectric materials, power apparatus, and other conventional/non-conventional test objects, was adopted. The test circuit adapted for PD measurements was exactly the same as that recommended by the standard IEC 60270. In all, the PD test circuit comprises of high voltage AC source, a wide-band PD signal decoupling unit and a digital PD measuring circuit. The high voltage is produced by a 6.6 kVA, 100 kV, 50 Hz transformer, the PD measuring circuit contains a blocking impedance (L , 40 mH), coupling capacitor (C_c , 0.3 nF), and an RLC impedance (Z_m) which decouples PD signals, functions as a low-pass filter and electrically connected to a digital PD detector (Omicron, MPD 600). Figure 3a shows the schematic diagram of the high voltage and PD test circuit while the actual picture

of the setup is shown in Figure 3b. The partial discharge tests were performed in a shielded room with a noise level of less than 3 pC. Prior to PD measurements, the samples that were immersed in deionized and seawater, were retrieved, cooled to room temperature, and later dried adequately. Subsequently, the silicone gel at the ends of the PCB samples is removed to access the copper tracks for making an electrical connection. Following this, the PCB samples were housed in a test cell connected to the electrodes at both ends.

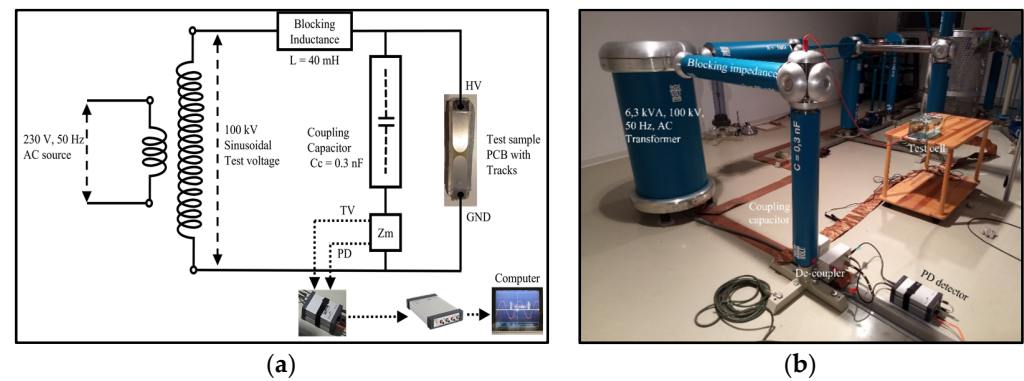


Figure 3. The setup used for generating and applying high voltage to the test samples and measuring PD arrangement: (a) Schematic; (b) Pictorial description.

Figure 4a,b shows the test cell with samples positioned appropriately. The test cell chosen is a rectangular glass container with two horizontal electrodes. The electrodes are made of brass material and are of the adjustable feed-through type with hemi-spherical electrodes facing each other inside the container. The high-voltage source is connected to the electrodes, which make contact with the PCB tracks of the specimen placed on top. Figure 4b shows the electrode arrangement with a specimen positioned accordingly. The glass container is filled with silicone oil (AK 1000) to evade field enhancements, and the voltage is raised at a rate of 1 kV/s until the insulation fails. Pertinent discharge pulses are decoupled from the measuring impedance and the respective pattern formed after correlating to the phase of applied AC sinusoidal voltage is recorded and analyzed. Also, the ambiguities that might arise due to the coupling of other PD sources, possible noise and interference are sorted out and repeatability is ensured.

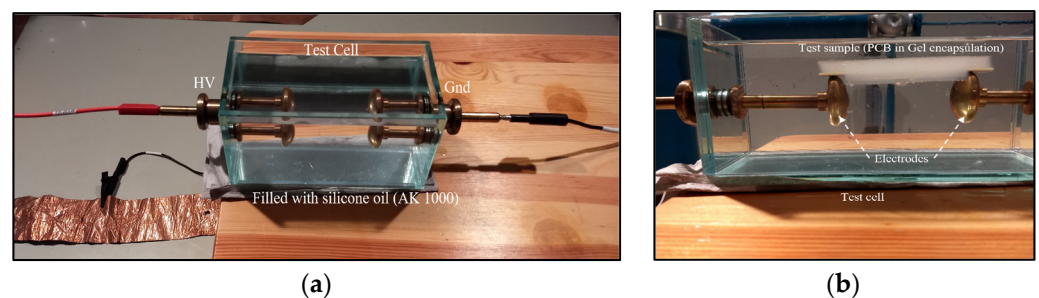


Figure 4. A pictorial description of test cell with the sample placed and electrically connected to the high voltage electrodes: (a) Test cell; (b) Sample connected to the high voltage electrodes.

4. Results

4.1. Simulation

Prior to measurements, a simulation study was performed to determine the possible locations of electric stress that might cause discharges in the gaps of the quasi-uniform electrode assemblies or PCB samples. In the present context, the edges of the semicircular conductive tracks in the samples that are facing each other are considered to be the electrodes. This assumption is quite reasonable since the applied voltage would cause a high electric field at these locations and therefore, a simulation was performed to determine

and observe the field at these edges for the chosen PCB track. The geometry of the PCB samples with gel encapsulation (see Figure 5a) was captured into a three-dimensional CAD model, and the electrostatic equation was solved using COMSOL Multi-Physics Simulation software 6.0. Under static conditions, the electric potential V is defined by $\vec{E} = -\nabla V$ and the electric displacement field $\vec{D} = \epsilon' \vec{E} + \vec{P}$, where $\vec{E}$ is electric field, $\vec{P}$ is the polarization density and $\epsilon' = \epsilon_0 \epsilon_r$ (a relative permittivity $\epsilon_r = 2.55$, is used for the encapsulation material). This is reasonable since the silicone oil and the gel encapsulant used have similar permittivity. The primary focus is on surface discharges and in this context, the factor of polarization ($\vec{P}$) was considered negligible and was henceforth ignored so that the field can simply be described by $\vec{E} = \frac{\vec{D}}{\epsilon_0 \epsilon_r}$ after solving the differential equation $\vec{D} = -\epsilon' \nabla V$. The current scenario reflects a condition of a capacitance (over surface), henceforth simulating the electric displacement field ($\vec{D}$) over a closed area implies calculating the charges on the surface that diverges from the electrode curvature influenced by the electric field.

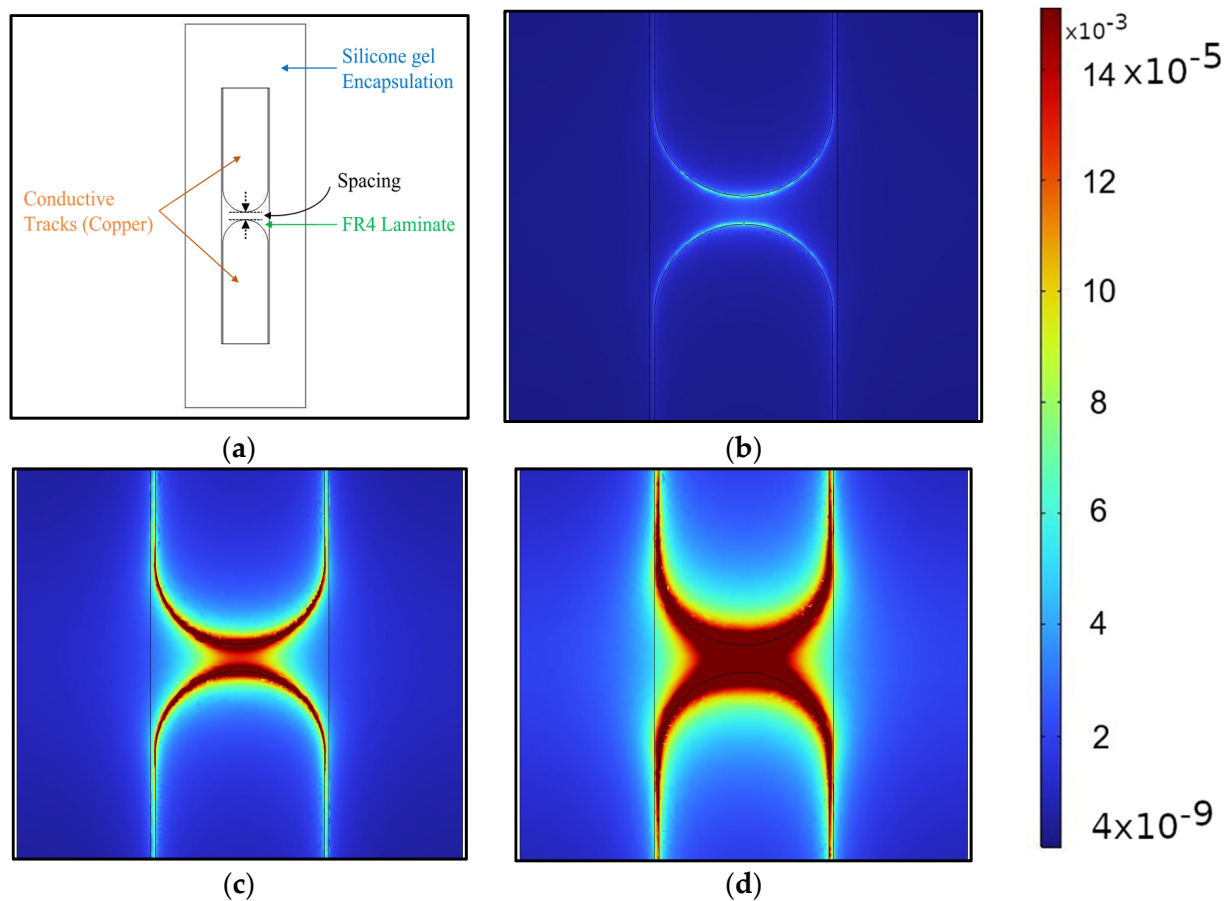


Figure 5. Simulation of electric displacement field ($\vec{D}$) (or charges built-up over the surface area) at the 3 mm spacing between the tracks of chosen PCB sample: (a) 2D CAD model; (b) Displacement field ($\vec{D}$) at 5 kV; (c) Displacement field ($\vec{D}$) at 30 kV; (d) Displacement field ($\vec{D}$) at 60 kV.

Figure 5a–d shows the electric displacement field ($\vec{D}$) simulation results of PCBs with 3 mm gaps at different voltages. A two-dimensional CAD view of the model adopted for simulation is shown in Figure 5a. The region surrounding the PCB samples are silicone material, henceforth the pertinent dielectric parameters are calculated with relative permittivity of 2.55 to simulate the actual test conditions. With all these conditions, it is expected that the electric field intensity is higher at the semicircular area of the electrode. The same can be observed in the simulation. The facing edges of the semicircular electrodes

experience higher electric displacement fields ($\vec{D}$). One of the electrodes is always set to 0 V while the potential of the opposing electrode is set to increasing voltages. At a simulation voltage of 5 kV, a notable level of electric displacement field ($\vec{D}$) appears at the curvature, while the intensity is higher at the tips of the electrodes. Table 2 provides the numerical value of maximum charges that appears at the curvature of the electrodes for the 3 mm, 5 mm and 10 mm gaps. It becomes clear from Figure 5 and Table 2 that the intensity of maximum charges increases substantially as the simulation voltage is increased to 30 kV, which indicates a higher electric field intensity. As this condition prevails, the gap between the electrodes or the conductive tracks would eventually breakdown causing a surface failure. The maxima, as presented in Table 2, increase with the applied voltage and decrease with the gap spacing, as expected. Charge accumulation can be found at the sides of the conductive tracks, which may result in surface breakdown.

Table 2. Charges simulated at the electrode curvature of the PCB sample with different spacings.

Spacing between the Tracks	Electric Displacement Field $\vec{D} = \epsilon_r \vec{E}$, $\frac{C}{mm^2}$		
	Maximum Value Simulated at 5 kV	Maximum Value Simulated at 30 kV	Maximum Value Simulated at 60 kV
	C/mm ²	C/mm ²	C/mm ²
3 mm	192×10^{-12}	1.15×10^{-9}	2.3×10^{-9}
5 mm	151×10^{-12}	908×10^{-12}	1.89×10^{-9}
10 mm	110×10^{-12}	662×10^{-12}	1.32×10^{-9}

Thus, it appears from the simulation study that the geometry of the tracks on the surface of the laminates and their proper encapsulation are very important. Any inadequacies like geometric deviations or surface irregularities would eventually cause higher displacement fields, thereby resulting in charge build-up. Further increases in charge accumulation may initiate discharges, thereby weakening the insulation locally, which may result in permanent failure. Likewise, any flaws in the silicone gel encapsulation might result in failures at these locations, respectively.

4.2. PD Measurements

The primary objective of this experimental study was to find out the breakdown voltage of the surface of the PCBs with gel encapsulation. This was achieved by conducting tests to determine the breakdown voltage coupled with PD measurements. During this, the applied voltage is increased at a steady rate until the sample suffers a breakdown failure. In tandem, the PD level and applied voltage were recorded and the subsequent PRPD pattern related to PD inception, nearing a failure and at the time of failure, were recorded and analyzed. The same was verified on a group of samples to ensure their repeatability. The PD measurements focus on identifying the dependencies of the PRPD pattern on two factors viz., geometrical spacing and water ingress into the material. The preceding analysis focused on the geometric properties only with the gap as a parameter whereas the following section will investigate the influence of water ingress on the encapsulation and the PCB surface. Prior to each measurement, the measuring system comprising the PD detector, the test and measuring circuit along with the test object was calibrated to a known PD pulse. Afterwards, it is ensured that the baseline noise level remains below an acceptable level (≈ 3 pC). Initially, measurements on virgin samples without and with encapsulation (Groups 1 and 2—see Table 1) are made, that can be used as a ‘signature’ for comparative analysis. Further experiments were conducted on aged samples and the apparent charge ($Q_{IEC} = I_{PD}(t) \times dt$) were measured, recorded, and tabulated. The adopted PD detector is highly sensitive in revealing the inception of electrical discharges close to the noise floor. Thus, a PD threshold of more than three times the baseline noise

($Q_{IEC} \geq 3 \times Q_N$ pC) was set as a necessary condition for measuring data expecting that the set value qualifies the discharge level as high enough to produce significant change (or in the long run) on the material.

4.2.1. Influence of Spacing and Geometry

Figure 6a,b shows the PRPD pattern of electrical discharges arising on the surface of virgin (without gel encapsulation) PCB samples of group 1, tested under oil with increasing test voltage. The measured values of apparent charge and the magnitude of applied voltage are given in Table 3. It becomes clear from Figure 6a that as the test voltage reaches a certain value, notable discharges are initiated on the surface of this PCB sample (without gel encapsulation). These discharges appear as pulses correlated to the phase (phasor notation) of the applied voltage, manifesting a specific pattern typical of corona discharges. As expected, further increases in the applied test voltage raised the number of discharge events with higher intensity, eventually reaching a near-by failure condition (not a failure but prior to that), as shown in Figure 6b. As the nearby failure condition is reached, even a small increase in applied voltage (in this example, from 31.27 to 31.95 kV—see Table 3) forces the samples to suffer a PD failure. The gap between the conductive tracks is bridged, and the localized area is degraded due to higher discharge energy. For comparison purposes, the PRPD pattern is measured for the virgin PCB sample without gel encapsulation (Group 1) as it is undergoing surface failure. Similar observations can be made during experiments on gel-encapsulated PCB samples in silicone oil in Group 2. At first glance, it seems that the presence of gel encapsulation increases the operating voltage and manifests a specific pattern distinguishable from other conditions.

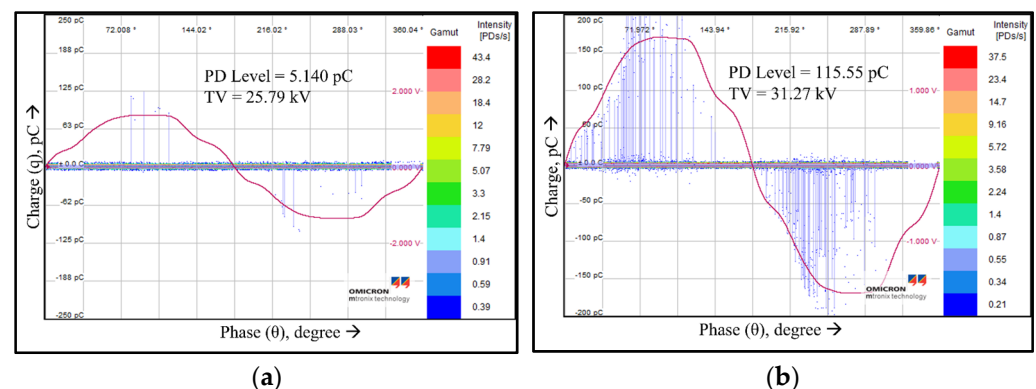


Figure 6. PRPD pattern of electrical discharges arising on the surface of virgin PCB samples at the space between conductive tracks: (a) Inception of discharges (Group 1); (b) Nearby failure (Group 1).

Table 3. Measurement of electrical discharges arising on the surface of virgin PCB samples.

Test Condition	Spacing mm	Discharge Inception		Nearing Failure		Failure Due to Discharge	
		App. Charge C	Voltage kV	App. Charge C	Voltage kV	App. Charge C	Voltage kV
¹ Air	5	9.1×10^{-12}	26.94	178×10^{-12}	31.95	195×10^{-12}	32.23
² Sil. oil	5	10.6×10^{-12}	27.41	317.5×10^{-12}	40.6	1.2×10^{-9}	40.61

Virgin samples: ¹—Without gel encapsulation (Group 1); ²—With gel encapsulation (Group 2) in Silicone oil.

Figure 7a,b shows the corresponding PRPD pattern, and the values of apparent charge and test voltage can be seen in Table 3. It becomes clear from Figure 7a that the inception of discharges manifests as pulses predominantly at the peak value of the applied voltage and is further extended in discrete steps to the first and third quadrants, respectively. As the applied voltage is raised, the number of discrete pulses and their intensity are increased,

retaining the phase correlation to the first and third quadrants of the applied voltage. If the test voltage is increased, the PCB sample reaches a nearby failure condition. In the case of the encapsulated PCB samples, the regular PRPD pattern disappears and a new one emerges, as is evident from the occurrence of stronger discrete pulses, while stable repetitive pulses are distributed in the first and third quadrants near each other. This pattern describes brush discharges appearing in micro-voids.

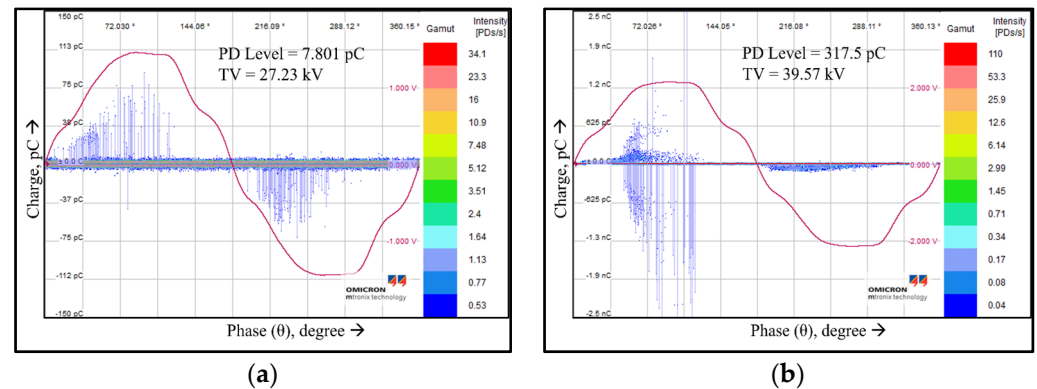


Figure 7. PRPD pattern of electrical discharges arising on the surface of virgin PCB samples at the space between conductive tracks: (a) Inception of discharges (Group 2); (b) Nearby failure.

Figure 8a,b show the PRPD pattern of virgin (group 1) and gel encapsulated samples (group 2) as they suffer PD failure. It becomes clear from the PRPD pattern shown in Figure 8a that the discharge pulses are strong and intensive and remain distributed throughout the phase of the applied voltage, possibly indicating multiple discharge zones as compared to the localized discharge behavior of the encapsulated sample shown in Figure 8b. The applied voltage collapses in both cases, indicating bridging of the dielectric gap between the conductive tracks since the bridging arcs have a resistance that varies from a few hundred ohms to a few kilohms. So, it is a momentary short-circuit with a specific value of varying resistance. During PD failure, the charges accumulated are discharged; henceforth, the value of apparent charges measured is lower than in the previous case.

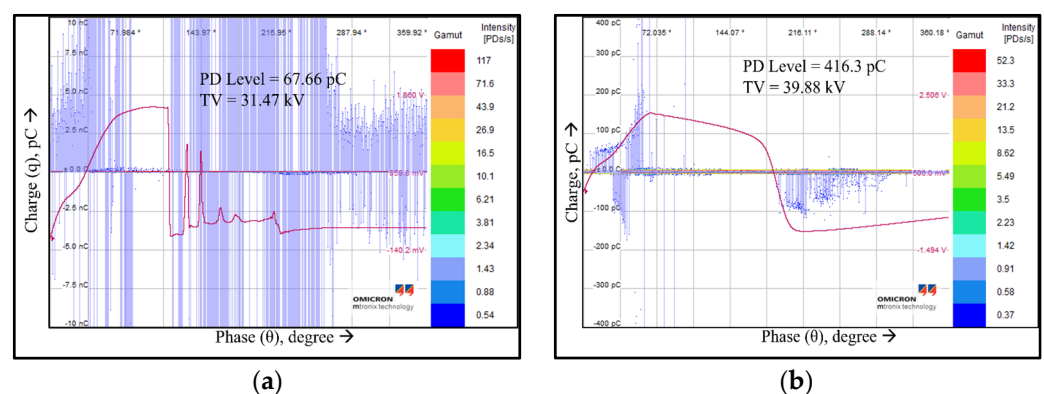


Figure 8. PRPD pattern of electrical discharges arising on the surface of virgin PCB samples at the space between conductive tracks: (a) PD failure (Group 1); (b) PD failure (Group 2).

4.2.2. Influence of Deionized Water on PD Phenomena

Figure 9a–d shows the PRPD pattern of inception of electrical discharges arising on the surface of several PCB samples (Group 3), each with different gaps (i.e., 3 mm, 5 mm, 5 mm with an intermediate slit, and 10 mm), immersed in deionized water at 90 °C for a specific duration. The maximum value of apparent charges measured and the test voltage applied to the samples are shown in Table 4. Two observations can be made from these figures: first,

the intensity and magnitude of discharges, and second, the pattern formed by the same after correlating them to the phase of the applied AC sinusoidal voltage. In comparison with the virgin samples, the inception of discharge events in the water-conditioned samples becomes observable at a much lower applied test voltage. The reason for the pulses appearing at a much lower test voltage might be the ingress of the water into the encapsulation material and, finally, the collection of water onto the surface of the PCB tracks (at the boundary). This boundary effect can be further illustrated by the improvement when introducing a small slit between the tracks, as shown in Figure 9b (5 mm, no slit) and 9c (5 mm, 4 mm slit). In this case, the inception voltage increases from 3.884 kV to 12.91 kV. The absence of a water collection boundary, therefore, seems to provide better insulation. The second observation is related to the pattern formed by the discharge events. The discharge events in the first and third quadrants of the applied AC voltage are discrete, and their intensity is not correlated to the voltage course as is typical for surface discharges. This is in contrast to the virgin samples, which initially correlated to the applied voltage. This confirms the hypothesis that water ingress initiates surface discharges at the tips of the conductive tracks on the PCB with different spacing.

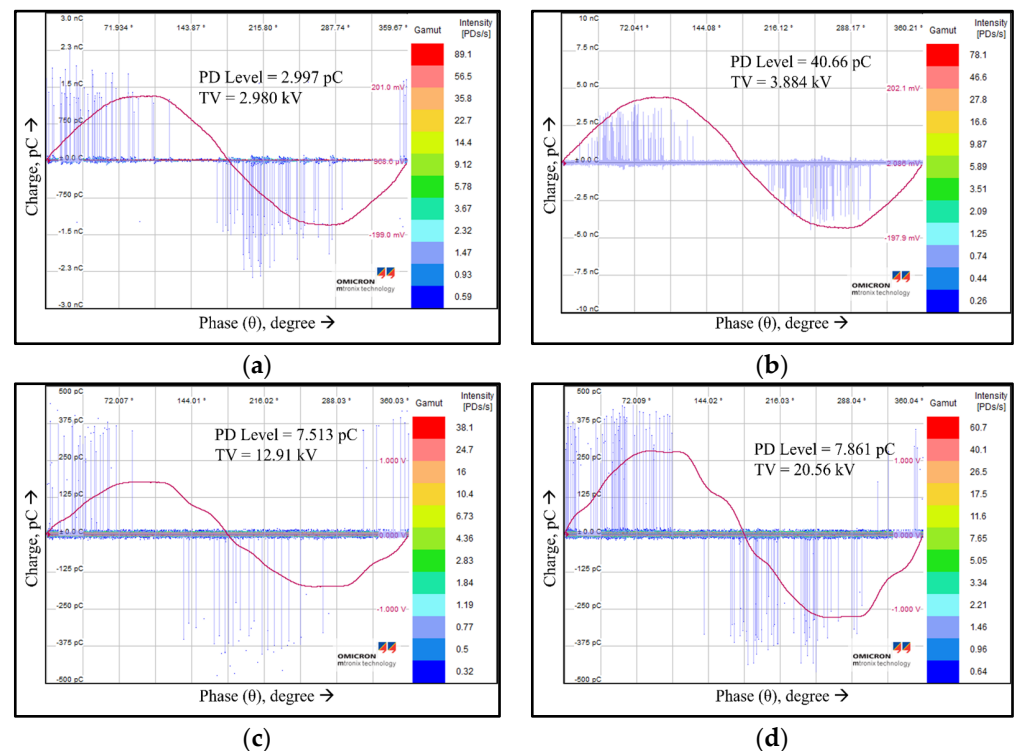


Figure 9. PRPD pattern of the encapsulated PCB samples of Group 3, conditioned in deionized water at 90 °C temperature: (a) Gap of 3 mm; (b) Gap of 5 mm; (c) Gap of 5 mm, with an intermediate slit of 4 mm × 1 mm; (d) Gap of 10 mm.

Figure 10a–d shows the PRPD pattern of surface discharges arising in the aged PCB samples of Group 3 at increased test voltage, where a nearby failure condition is reached. Intense discharge events repeat in close proximity. This pattern is similar to that of surface discharges. The PRPD pattern obtained for the aged PCB sample with 3 mm spacing (Figure 10a) reveals two overlapping PD pulse distributions with different magnitudes. This might be due to the intensive brush discharges occurring in the gap since more charges are accumulated. Similar patterns and behaviors don't exist in other samples with a higher track spacing, as shown in Figure 10b; the discharges in the sample with 5 mm gaps are more regular with a lower magnitude than in the sample with 3 mm gaps. They span the complete phase of the applied voltage. It can be noted from Figure 10c that the introduction of a simple slit between the track spacings reduces PD considerably. As shown in Table 4,

the PD level decreases although the voltage is increased from 26.08 kV to 36.35 kV. A quite similar PD level has been measured from the aged samples with 10 mm spacing, but at a test voltage of 31.32 kV, which is larger than that for the samples with a 5 mm gap without the slit and lower than for the samples with the slit. This confirms the fact that the wider space between tracks has reduced the field; however, providing a slit between the conductive tracks leads to a better field distribution.

Table 4. Measurement of discharges arising on PCB samples aged in deionized water at 90 °C.

Spacing mm	Discharge Inception		Nearing Failure		Failure Due to Discharge	
	App. Charge C	Voltage kV	App. Charge C	Voltage kV	App. Charge C	Voltage kV
3	10×10^{-12}	3.128	3.22×10^{-9}	23.15	4×10^{-9}	23.36
5	17×10^{-12}	3.579	1.86×10^{-12}	26.54	2.7×10^{-12}	26.89
5 (Slit)	12×10^{-12}	13.03	835×10^{-12}	38.14	1.6×10^{-9}	38.51
10	12×10^{-12}	19.48	777.8×10^{-9}	32.16	993×10^{-9}	33.48

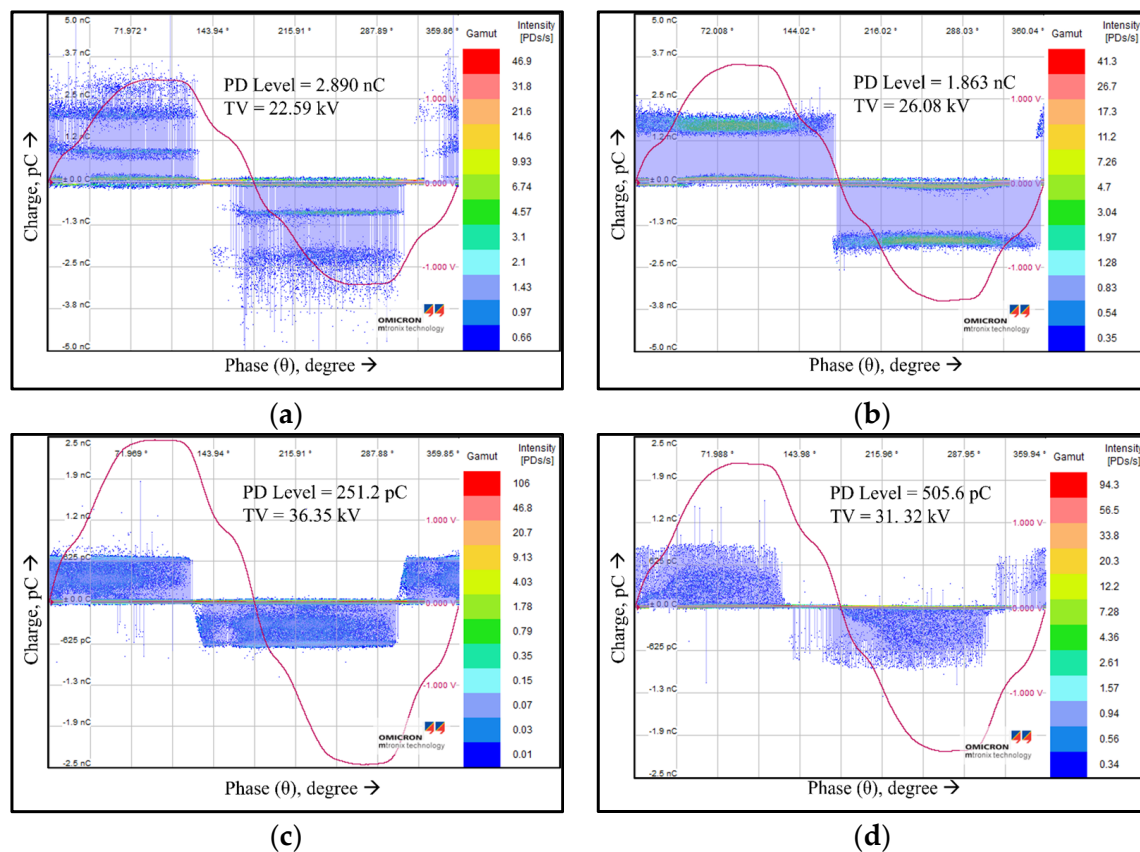


Figure 10. PRPD pattern of the electrical discharges arising between the tracks of chosen PCB samples, conditioned by immersing in deionized water at 90 °C temperature resulting in a *nearby* insulation failure: (a) Gap of 3 mm; (b) Gap of 5 mm, without any intermediate slit between the gaps; (c) Gap of 5 mm, with an intermediate slit of 4 mm × 1 mm in dimension; (d) 10 mm.

The PRPD pattern of the inception of discharges in the gel-encapsulated PCB samples (Group 4) with track spacings of 3 mm, 5 mm, 5 mm with a slit, and 10 mm aged in deionized water at room temperature is shown in Figure 11a–d, respectively. At first glance, the PRPD pattern of these aged samples (at room temperature) with 3 mm shows a certain

degree of resemblance with reference measurements. The corresponding discharge events appeared as discrete PD pulses (Figure 11a), correlated to the peak value of applied voltage. The values of apparent charge measured are 13.03 pC, initiated at 28.60 kV (Table 5), which remains within the range of reference measurements. The reason might be due to the water ingress into the encapsulation material not being as uniform as at 90 °C. As the spacing between the tracks increases to 5 mm and 10 mm, the discharges appear at 18.53 kV and 12.52 kV, and the PRPD pattern (Figure 11b–d) contains stronger PD pulses, distributed near each other at the first and third quadrants of applied voltage. The corresponding test voltages at which these PD pulses start appearing are 18.79 kV (5 mm, slit) and 12.52 kV (10 mm), respectively. The proximal distribution of pulses might indicate brush-type discharges, which usually occur on curved electrodes or micro-voids. In the present context, it might be the curved electrodes that initiate the brush-type discharges. Although the water ingress might be non-uniform, the curved face of the conductive tracks is sufficient to produce brush discharges as the applied voltage is higher. Nevertheless, irrespective of any other factors, the pulse correlation to the first and third quadrants and its dependency on the applied voltage might confirm the occurrence of surface discharges on the samples. Following this, the applied voltage is increased, and the PRPD pattern of discharges arising under such non-uniform water ingress in the encapsulating material prior to the failure or nearby failure is studied.

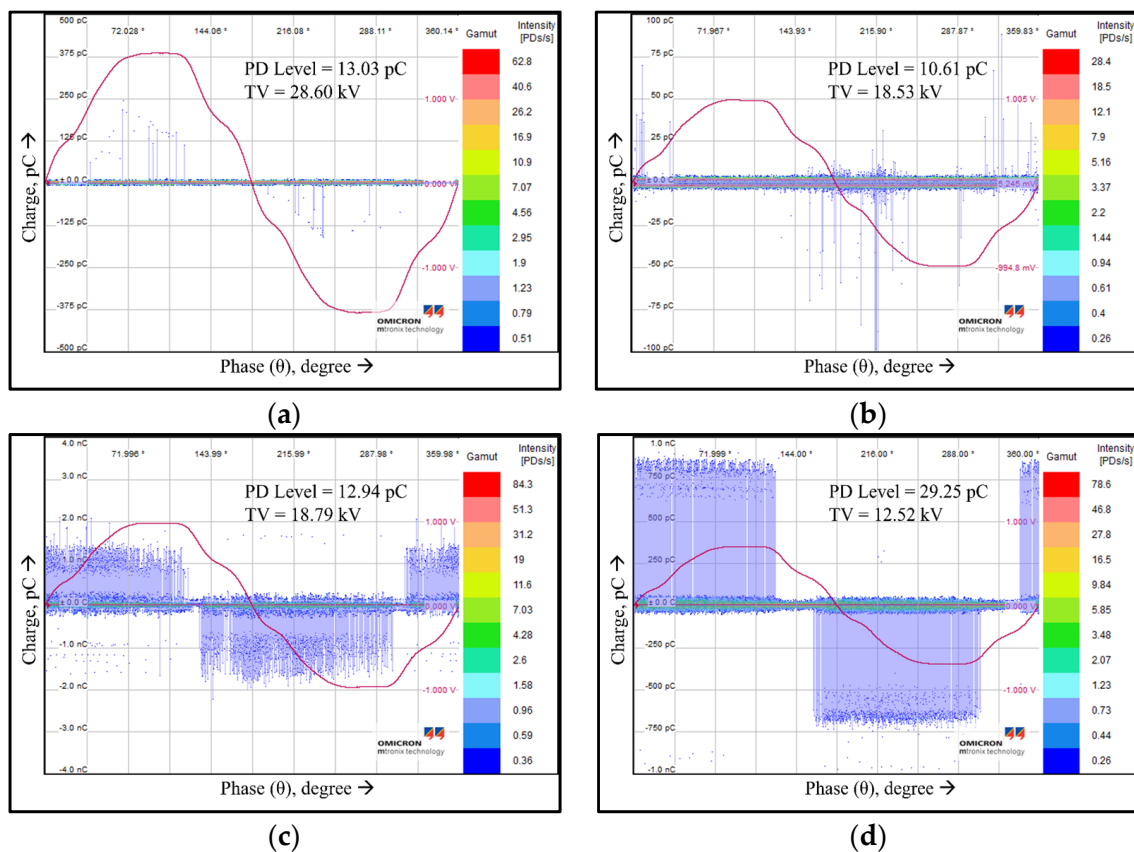


Figure 11. PRPD pattern of the inception of electrical discharges arising between the tracks of chosen PCB samples, conditioned by immersing in deionized water at room temperature: (a) Gap of 3 mm; (b) Gap of 5 mm, without any intermediate slit between the gaps; (c) Gap of 5 mm, with an intermediate slit of 4 mm × 1 mm in dimension; (d) Gap of 10 mm.

Table 5. Measurement of discharges on PCB samples aged in deionized water at room temperature.

Spacing	Discharge Inception		Nearing Failure		Failure Due to Discharge	
	App. Charge	Voltage	App. Charge	Voltage	App. Charge	Voltage
Mm	C	kV	C	kV	C	kV
3	9.2×10^{-12}	28.72	418×10^{-12}	33.17	617×10^{-12}	33.24
5	10×10^{-12}	12.26	3.3×10^{-9}	43.93	4.7×10^{-12}	46.46
5 (slit)	28×10^{-12}	19.02	1.3×10^{-9}	41.02	2.3×10^{-9}	43.36
10	28×10^{-12}	12.61	6.2×10^{-9}	59.36	9.4×10^{-9}	60.51

Figure 12a–d shows the PRPD pattern of PCB samples measured just before they reach their nearby PD failure condition. Since the samples are aged in deionized water at room temperature, the water ingress into the material may not be as uniform as its predecessor (i.e., aging at 90 °C). As expected, there are similarities with reference measurements and some notable differences observable in their respective PRPD patterns.

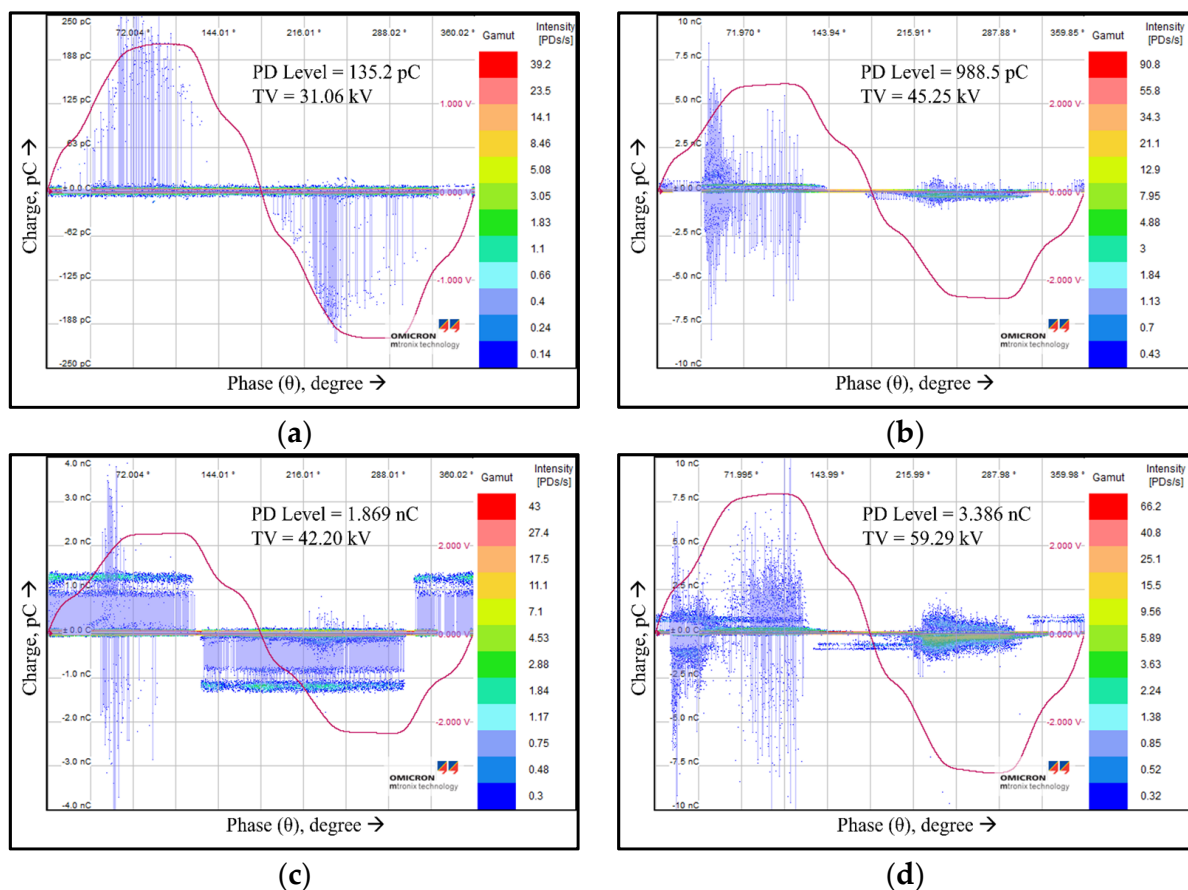


Figure 12. PRPD pattern of the electrical discharges arising on chosen PCB samples, aged in deionized water at room temperature, resulting in a *near-by* insulation failure: (a) Gap of 3 mm; (b) Gap of 5 mm, without any intermediate slit between the gaps; (c) Gap of 5 mm, with an intermediate slit of 4 mm × 1 mm in dimension; (d) Gap of 10 mm.

The PRPD pattern (Figure 12a) of discharges measured from the PCB samples aged at room temperature (Group 4) with 3 mm track spacing is correlated predominantly to the peak value of applied voltage and spans into the first and third quadrants, respectively. The relevant pulses appear stable, strong, repetitive, and span in discrete steps throughout the first and third quadrants. The PD level quantified using apparent charge appears as 135.2 pC, and the respective magnitude of voltage that initiates it is given as 31.06 kV

in Table 5. At the same time, the PCB samples with track spacings of 5 mm with slit, 5 mm without slit, and 10 mm showed different patterns. The first pattern is relevant to normal surface discharges, with PD events of stronger pulses distributed in the first and third quadrants of the applied voltage. The second pattern is of discrete, proximal pulses (sharp bipolar), distributed between the first and third quadrants of applied voltage. The discrete pulses might indicate corona activities, while the proximal counterpart might be due to the brush discharges appearing at the curved electrodes. It is also worth mentioning that the discharge patterns, particularly those of the 5 mm sample, are erratic, indicating a non-uniformity due to the water ingress into the gel material. So, the sample with 5 mm spacing between tracks and an intermediate slit (Figure 12c) emerged as a feasible option.

4.2.3. Influence of Sea Water Ingress on PD Phenomena

Figure 13a–d shows the PRPD pattern of PCB samples (Group 5), aged in seawater at room temperature. Pertinent values of the apparent charges of PD events measured from the samples aged in seawater and the magnitude of the applied voltage that initiates them are given in Table 6. An interesting observation can be made from the PRPD pattern of aged PCB samples with 3 mm track spacing (Figure 13a). The PD pulses appear bipolar with an apparent charge of magnitude 16.70 pC, initiated at 8.260 kV in discrete steps correlated to the first and third quadrants of the applied voltage. Such an observation can be made only on this PCB sample with 3 mm track spacing and aged in seawater. Usually, the surface discharges manifest as unipolar pulses in the first and third quadrants, with the same polarity as that of the applied voltage. On the contrary, the discharges in voids, micro-voids, pores, cavities, etc. appear in the same quadrant but in a polarity opposite to that of the applied voltage. Hence, in the present context (Figure 13a–d), the bipolar nature of the discharges in an aged sample with 3 mm indicates the development and progress of both streamers on the surface and the degradation of the gel material. It is understood that the sample with 3 mm spacing suffers a higher tangential electric stress component. Since the seawater has ionic salts that are not only conductive but also reduce the effective value of the material permittivity, As the water ingress progresses in the encapsulation, the ionic salts also enter and diverge from there to the surface of the PCB laminate. So, on the application of high voltage, the tangential component of the electric stress initiates discharges on the surface that is not only influenced by the moisture or water but also by the salt depositions. The discharges initiated are low-thermal plasma, but they can still react with the salts, causing material degradation. The combined effect of the stress, water, and salt depositions on the surface and the interaction of the same in the pore may procreate such bipolar discharges. Nevertheless, such discharges are missing as the track spacing is increased from 3 mm to 5 mm and 10 mm, respectively. Further investigation on gel-encapsulated samples with conductive tracks 5 mm apart revealed patterns appearing in the first and third quadrants of the applied AC voltage. This resembles the pattern formed by the surface discharges on the pertinent PCB sample. The charges start to appear as the test voltage reaches 13.60 kV. However, the PCB samples with 5 mm and 10 mm spacings are more or less similar. On observing the PD levels and test voltage (Table 5) that initiate discharges, once again it appears that the sample with 5 mm track spacing with a slit emerges as a better design choice. So, comprehensively, it might appear that the discharge behavior of the seawater in the PCB sample may be more distinct than the case mentioned in Group 4.

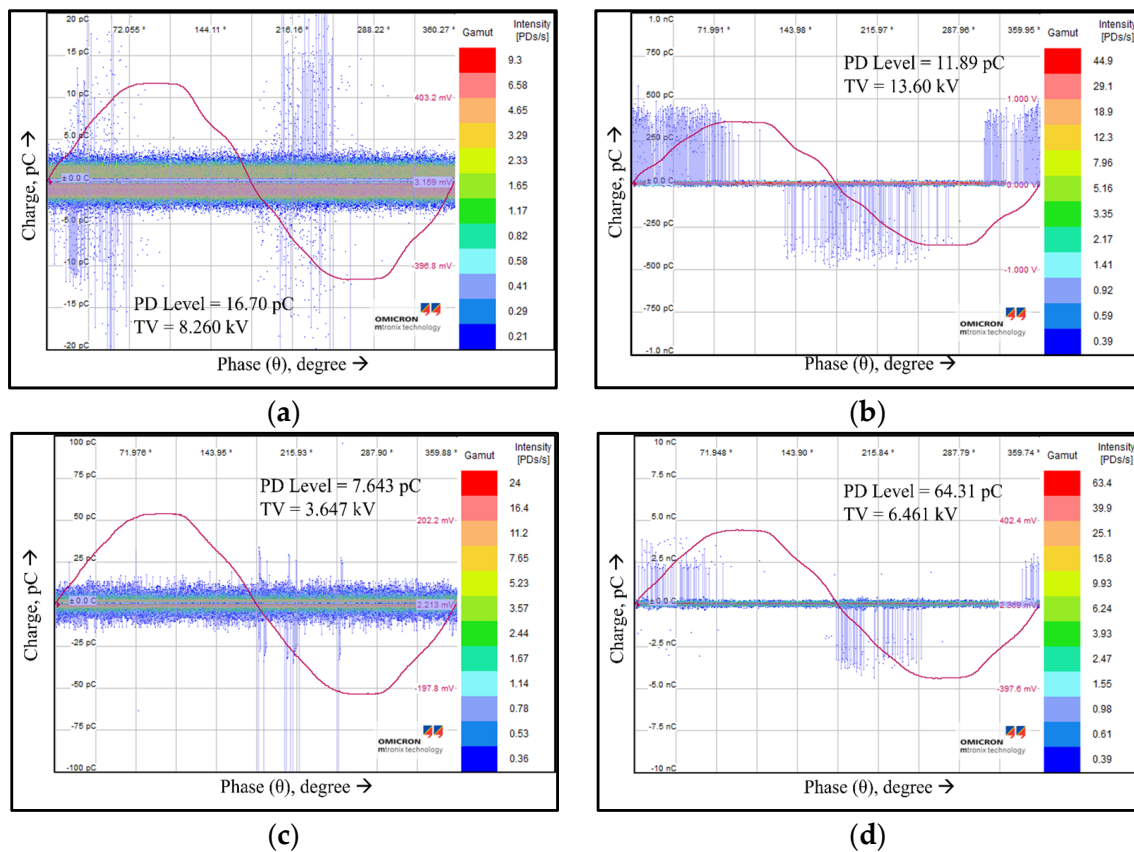


Figure 13. PRPD pattern of the inception of electrical discharges arising between the tracks of chosen PCB samples, aged by immersing in seawater at room temperature for a specific duration: (a) Gap of 3 mm; (b) Gap of 5 mm, without any intermediate slit between the gaps; (c) Gap of 5 mm, with an intermediate slit of 4 mm × 1 mm in dimension; (d) Gap of 10 mm.

Table 6. Measurement of discharges arising on PCB samples aged in seawater at room temperature.

Spacing	Discharge Inception		Nearing Failure		Failure Due to Discharge	
	App. Charge	Voltage	App. Charge	Voltage	App. Charge	Voltage
Mm	C	kV	C	kV	C	kV
3	12×10^{-12}	4.177	155×10^{-12}	35.38	251×10^{-12}	36.65
5	15×10^{-12}	8.565	2.4×10^{-9}	38.93	3×10^{-9}	39.16
5 (Slit)	10×10^{-12}	22.97	4.8×10^{-9}	47.93	5×10^{-9}	48.88
10	11×10^{-12}	6.117	4.33×10^{-9}	43.62	5.1×10^{-9}	43.72

The PRPD pattern of PCB samples aged in sea water at room temperature and nearing a PD failure condition is shown in Figure 14a–d respectively. Table 6 shows the values of the apparent charges of discharge events and their respective voltages that initiate them. At first glance, certain interesting observations can be made from Figure 14a–d, respectively. Once again, these observations are dependent on the track spacing, particularly the 3 mm case study shown in Figure 14a. It can be observed from Figure 14a that the aged sample with 3 mm track spacing manifests two different patterns overlapping each other. The first pattern is strong PD pulses that are correlated to the peak values of the applied voltage spans in the first and third quadrants in discrete steps. The second pattern is composed of bipolar discharges, both of which consist of pulses that are proximally positioned but phase-correlated to the first and third quadrants of the applied voltage. This different

pattern indicates stronger discharges on the surface, predominantly brush type, while the negative polarity indicates material degradation. Nevertheless, the inception of discharges appears as soon as the applied voltage reaches 4.177 kV. Contrary to this, the PCB samples with 5 mm (no slit), 5 mm (with slit), and 10 mm track spacing revealed a pattern similar to that of previous observations. The PRPD pattern is correlated to the first and third quadrants, while the discharges are mostly proximally positioned to each other. All in all, the PCB sample with 5 mm track spacing and an intermediate slit emerged with better characteristics. The PD level is relatively lower, while the voltage required to initiate the same is higher. For instance, in the present context, as the sample nears failure at a voltage of 30.09 kV, the apparent charge is 527 pC, while the same for 5 mm without a slit is 532 pC at 22.59 kV.

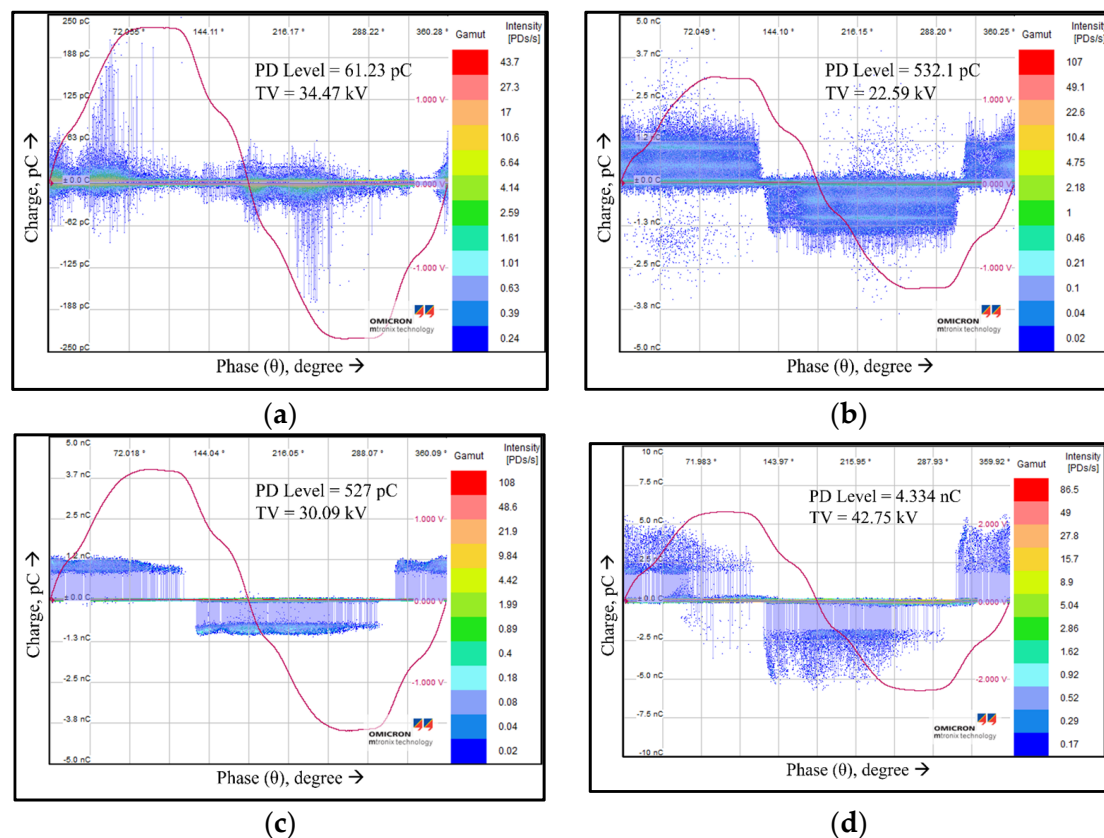


Figure 14. PRPD pattern of the electrical discharges arising between the tracks of chosen PCB samples, conditioned by immersing in sea water at room temperature, eventually resulting in a *nearby* insulation failure: (a) Gap of 3 mm; (b) Gap of 5 mm, without any slit between the gaps; (c) Gap of 5 mm, with an intermediate slit of 4 mm × 1 mm in dimension; (d) Gap of 10 mm.

Thus, it appears from these experiments that increasing the gap between the tracks naturally improves the discharge resistance level, which is an obvious reason for the reduction in electric stress conditions. However, as an optimal choice, introducing slits between the crucial locations of the PCB might still provide an opportunity to improve the PD resistance characteristics.

4.3. Trend of PD Phenomenon

The PD on PCB samples can be segregated into many stages depending on its time of occurrence (i.e., inception, elevated, near-by failure, and extinction). Subsequently, each PD stage manifests a typical trend with respect to parameters such as geometry, moisture, temperature, aging, and so on. The primary dependency factors are considered to be water ingress and spacing between the conductive tracks. The trend manifested by the

discharges at different stages, right from inception until final PF failure, is measured and their dependency is analyzed. Figure 15a shows the trend of inception of surface discharges arising on the PCB samples aged under deionized water at 90 °C. The prominent peak value of the applied test voltage that initiates such surface discharges is shown in Figure 15b. Two observations can be made from Figure 15a,b. First, the apparent charge measured during the inception of discharges seems to be the same with respect to the track spacing. This might be due to the value of the threshold set for measuring the apparent charge (i.e., $Q_{IEC} = 3 \times 3 \text{ pC}$ (noise)) during discharge inception. Obviously, the trend manifested by PD's inception with respect to track spacing appears to be a straight line. On the contrary, the magnitude of the test voltage at PD inception increases with track spacing. For instance, in the sample with a 3 mm gap, the PD inception appears at less than 5 kV, while the same is true for 5 mm and 10 mm, which are approximately close to 10 kV and 20 kV, respectively. However, the PD level at near-by failure and at insulation breakdown decreases with increasing spacing between tracks. A prominent trend appears as line dropping with respect to increasing track spacing. The corresponding test voltage, where inception and failure occur, increases with spacing, and the test voltage at which the samples suffer insulation failure shows less deviation from a straight line than that of the nearby failure records. This variability of the apparent charge values at nearby failures indicates the stochastic nature of the charge build-up on the surface.

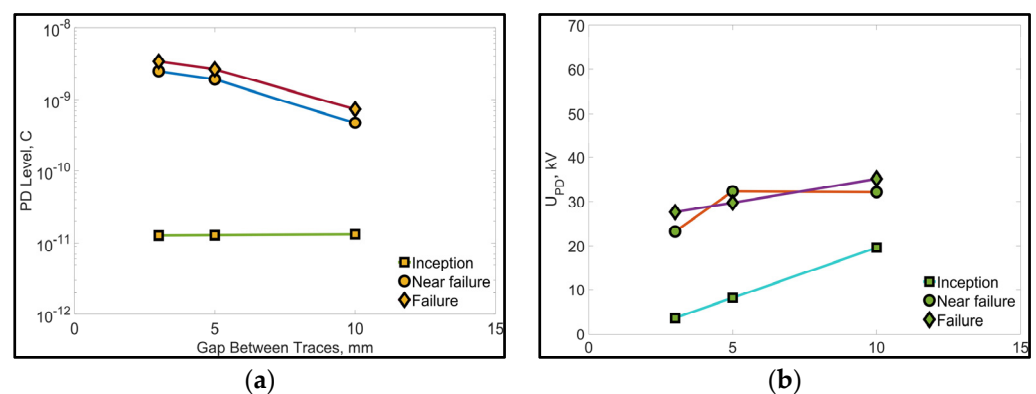


Figure 15. Trend manifested by the apparent charges of electrical discharges arising on the surface of the PCB samples aged in deionized water at 90 °C, with respect to the track spacing: (a) PD measured; (b) Corresponding test voltage.

Figure 16a,b shows the trend manifested by the surface discharges measured from the gel-encapsulated PCB samples aged in deionized water at room temperature. As opposed to the previous case, the water ingress at room temperature has modified the trend formed by the PD inception with respect to the spacing of the conductive tracks. The level of PD measured at the inception of surface discharges seems to increase with increasing spacing. For instance, the PD inception at 3 mm is 10 pC, while the same is close to 12 pC and 17 pC for the spacing of 5 mm and 10 mm, respectively. Similarly, the PD levels measured as the sample nears failure and suffers an insulation breakdown tend to increase with the increase in track spacing. Relatively, the changes in the PD level are higher as the sample nears failure. This observation is opposite to the previous case, where the samples were immersed and aged in deionized water at 90 °C. Similar differences are also observable in the PD inception voltage (Figure 16b). The voltage at the PD inception, nearing failure and insulation breakdown, seems to decrease with the increase in track spacing. At the same time, the test voltage at which the sample nears failure and eventually suffers a breakdown continues to increase with the track spacing. In addition, the trend formulated by the test voltage during a nearby and complete failure of the insulation seems to be more certain and substantial than in the previous case. Such deviations might be due to differences in water ingress into the material. For instance, aging the material in the deionized water at

90 °C might be more uniform and intensive, while doing the same at room temperature might be non-uniform and less intensive.

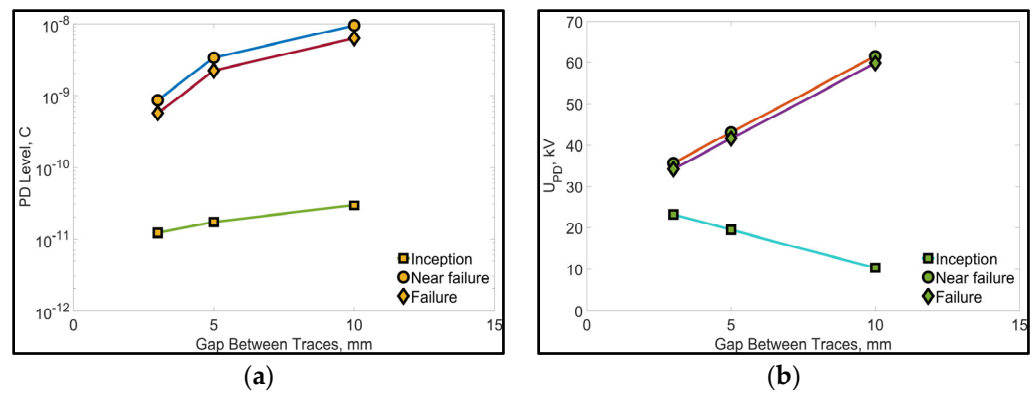


Figure 16. Trend manifested by the apparent charges of electrical discharges arising on the surface of the PCB samples aged in deionized water at 25 °C, with respect to the track spacing: (a) PD measured; (b) Corresponding test voltage.

Following this, the trend manifested by the apparent charges of electrical discharges arising on the surface of a gel-encapsulated PCB sample aged in seawater at 25 °C is measured and analyzed. Figure 17a,b show the pertinent trend manifested by the PD inception, near-by failure, and breakdown failure on chosen samples. The trend manifested by the PCB samples aged in seawater at 25 °C is more or less similar to that of the previous case (shown in Figure 17a,b). The PD inception seems to be more or less similar, but once again, this might be due to the threshold values adopted while recording the data. The trend of test voltage measured during PD inception seems to decrease with an increase in track spacing. The only difference is the numerical value. In the present case, the inception voltage at 3 mm is more than 10 kV; however, it decreases to 6 kV as the spacing increases to 10 mm. Thus, it can be collectively substantiated that the pattern of PD inception is influenced by water ingress, but remains more or less the same at room temperature. Similar observations could be made as the aged sample (in seawater) reaches a nearby failure and insulation breakdown. In any case, the trend seems to be the same, i.e., as the track spacing increases, the PD level and corresponding test voltage increase. Once again, the apparent values are entirely different. The reason for such differences in the apparent values might be due to the salts in the seawater.

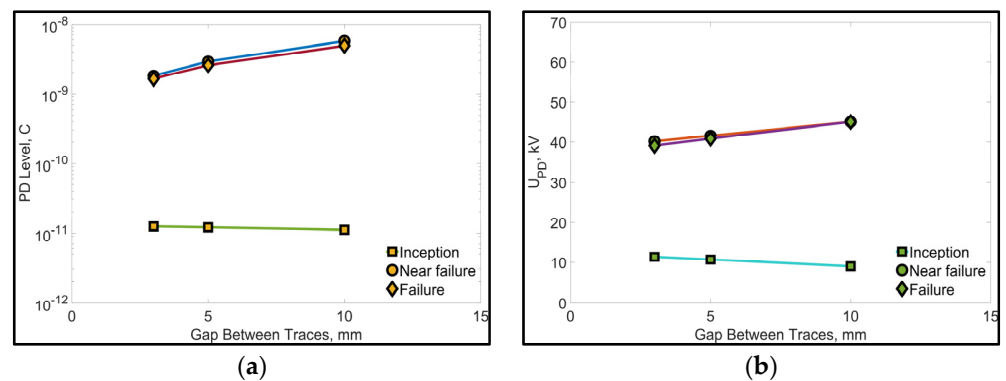


Figure 17. Trend manifested by the apparent charges of electrical discharges arising on the surface of the PCB samples aged in seawater at 25 °C, with respect to the track spacing: (a) PD measured; (b) Corresponding test voltage.

Summarizing all, it appears from these experimental results that the environmental conditions and the condition of the gel encapsulations have a significant impact on the behavior of surface discharges. The specific pattern manifested by each condition indicates the possibility of early detection of a developing fault condition and initiating a preventive measure. With all these results put together, the inferences that can be gathered from this experimental study are summarized and given below.

5. Discussion

Pertinent inferences gathered from this experimental study are discussed below:

- Simulation of a two-dimensional CAD model indicates that the electric displacement field appears predominantly at the curvature of the conductive tracks, with higher intensity at their tips. A further increase in test voltage drastically increases the intensity of the electric displacement field, not only at the curvature but also on the sides of the conductive tracks. The perpendicular displacement field increased from 192 pC (at 5 kV) to 1.15 nC (at 30 kV), respectively. It may be deduced that weaker insulation at the sides may cause a failure at these locations rather than at the semicircular ends.
- The experiments on virgin PCB samples with and without gel encapsulation (Groups 1, 2) provide the reference values so that a comparison can be made to analyze the status of the other PCB samples aged in deionized and seawater. The PD measurements on the virgin PCB sample (Group 1) show the pattern of surface discharges directly appearing on the FR4 laminate, while the same on Group 2 shows the impact of encapsulating material on the surface discharges. Subsequent experiments revealed that the PRPD pattern of discharge events occurring on the surface of the virgin samples without gel encapsulation is similar to that of the corona. Pertinent discharge events appear as individual, strong, stable pulses that are predominantly correlated to the peaks of the applied voltage and later span into the first and third quadrants in discrete steps. As the voltage increases, so do the PD magnitude and intensity in the respective patterns. On the contrary, the discharge events occurring on the gel-encapsulated virgin sample start to appear directly in the first and third quadrants. As the applied voltage is increased, the pertinent sample reaches a near-failure condition where the discharges start to appear bipolar, predominantly negative to the applied voltage. The pulses appearing at a polarity opposite to the applied voltage indicate degradation of the gel in that location. This might be since the surface resistivity of the FR4 laminate ($10^{13} \Omega\text{-cm}$) is much lower than that of the silicone gel encapsulation ($10^{11} \Omega\text{-cm}$). In addition to this, a certain degree of discharge pulses that are proximally positioned to each other appears but at a smaller intensity. This pattern is similar to that of brush discharges that usually arise due to curved electrode surfaces and micro-voids on the surface.
- Further experiments on gel-encapsulated PCB samples aged in deionized and seawater indicate a similar pattern but with a slight deviation in their correlation. For instance, the pattern formed by the PCB samples aged in deionized water at 90 °C seems to be more uniform. As soon as the applied voltage reaches a sufficient magnitude to initiate surface discharges, the pulses appear in the first and third quadrants with well-defined intensity levels. This behavior remains the same for all the samples with different gaps. The only difference is the intensity of PD measured and the magnitude of applied voltage. As the magnitude of applied voltage increases, the intensity of discharges increases, causing severe events that eventually cause a permanent failure. Pertinent patterns appear similar to those of brush discharges, and henceforth the location suffers degradation. On the contrary, similarities between deionized and seawater-aged samples at room temperature were observed, especially for PCB samples with a 3 mm track spacing. A prominent PRPD pattern indicated that the surface discharges are initiated by the field enhancements at the curved electrodes. At the same time, the QV diagram pointed out that the sample with 3 mm track spacing had several opportunities for momentary discharges. As the voltage is higher, the intensity of

such discharges is higher, eventually resulting in brush-type discharge failure. Since the brush-type discharges have more energy than their corona counterparts, there is always a likely chance that the gel encapsulation might suffer degradation. In addition, it was observed that the PCB sample with 5 mm track spacing and an additional slit between the conductive tracks showed better PD characteristics. The operating voltage can be increased, while the apparent charge responsible for PD failure is also lower. So, the material degradation can be less than for the other geometries. In addition, the sample with 10 mm spacing also emerges with better characteristics but may not be a feasible choice where high-power density is considered.

Thus, it appears from these experimental studies that there exists a regular pattern describing the discharge phenomena on the surface of gel-encapsulated PCB samples. The regularity in the pattern describes the type of defect due to water ingress into the material. This trend seems to match the simulation studies.

6. Conclusions

An experimental study that focuses on evaluating the surface discharges arising on the surface of FR-4 PCB laminate has been accomplished. Thus, it is evident from this study that the sample has acquired water in the encapsulating material, which was transported to the surface of the material within a week. The sample in deionized water at 90 °C seems to have more uniform water ingress than the other cases. The presence of deionized and seawater has a significant influence on electrical discharges occurring on the surface of silicone gel-encapsulated FR-4 PCB laminates. Pertinent discharges arising due to the water ingress in the encapsulating material manifest a noticeable pattern when correlated to the phase of the applied test voltage. Pertinent discharges can degrade the insulation locally. Making a slight modification, such as a slot between the tracks and/or at crucial positions, might help to retain the material integrity by reducing the stresses. Nevertheless, a clearer picture of understanding the same might emerge after careful studies on several samples and design improvements, which is the scope of future work.

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