

Article

Lightweight Arc Fault Detection Method Based on Adam-Optimized Neural Network and Hardware Feature Algorithm

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Abstract: Arc faults are the main cause of electrical fires according to national fire data statistics. Intensive studies of artificial intelligence-based arc fault detection methods have been carried out and achieved a high detection accuracy. However, the computational complexity of the artificial intelligence-based methods hinders their application for arc fault detection devices. This paper proposes a lightweight arc fault detection method based on the discrimination of a novel feature for lower current distortion conditions and the Adam-optimized BP neural network for higher distortion conditions. The novel feature is the pulse signal number per unit cycle, reflecting the zero-off phenomena of the arc current. Six features, containing the novel feature, are chosen as the inputs of the neural network, reducing the computational complexity. The model achieves a high detection accuracy of 99.27% under various load types recommended by the IEC 62606 standard. Finally, the proposed lightweight method is implemented on hardware based on the STM32 series microcontroller unit. The experimental results show that the average detection accuracy is 98.33%, while the average detection time is 45 ms and the average tripping time is 72–201 ms under six types of loads, which can fulfill the requirements of real-time detection for commercial arc fault detection devices.



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Keywords: arc fault detection; Adam-optimizer; neural networks; series arc fault

1. Introduction

The distribution lines in high-rise buildings are densely distributed and partially exposed, making them prone to insulation aging and poor contact when exposed to wind and rain. Aging insulation and poor contact of the circuit can easily cause faults and arcs in the circuits. The arc with a center temperature of up to 5000–15,000 °C can easily cause electrical fires by igniting surrounding flammable materials, resulting in an adverse effect on the safe and reliable operation of the distribution network [1]. According to national statistics from 2012 to 2021, there were 1.324 million residential fires in China, of which electrical fires accounted for 42.7% [2].

According to the topology of the arc fault in the circuit, it can be divided into series and parallel arc faults. When a parallel arc fault occurs, the circuit current significantly increases, and traditional circuit breakers can be triggered to cut off the circuit promptly. When a series arc fault occurs, the circuit current will decrease, making it impossible to trigger traditional circuit breakers [3]. The series arc fault has the characteristics of concealment, complexity, and instability, making it hard to be accurately detected [4,5].

The occurrence of an arc is usually accompanied by phenomena such as arc light, arc sound, and electromagnetic radiation. Therefore, temperature, photosensitive, antenna, and other sensors were often used to monitor arc faults in the early stages [6–10]. However, the effectiveness of these non-contact methods is limited by the installation location of the

sensors and is easily affected by external environmental factors. Due to the significant changes in the current waveform, such as a decrease in amplitude and waveform distortion, the time domain and the frequency domain characteristics of the current waveform were also used to detect the arc fault [11,12]. However, the interference of high-frequency harmonic from numerous nonlinear loads, such as switching power supplies, makes it hard to accurately detect arc faults by fixed feature thresholds, leading to a protection mis-operation or mal-operation.

In recent years, with the widespread application of artificial intelligence methods in various fields, lots of work has been carried out using machine learning to detect arc faults and has achieved good results in some aspects [13]. The authors in [14] compare the performances of eight machine learning approaches with five time domain parameters of the current for series dc arc fault detection under several typical loads, especially nonlinear and complex loads such as power electronic loads. The authors in [15] propose a lightweight ac arc fault detection method by integration of load classification by K-nearest neighbor (KNN) and feature selection by sequential floating forward selection. The authors in [16] provide a lightweight arc fault detection method based on the EffNet module, deployed on the embedded platform Raspberry Pi 4B for an arc fault detection device (AFDD). The authors in [17] propose a one-dimensional convolutional neural network (CNN) method driven by an improved high-frequency RLC arc model. The authors in [18] apply a CNN-based network directly to the raw data without processing, achieving a high accuracy and load classification along with an arc fault detection accuracy of 99.05% for four major load groups. The authors in [19] establish a phase space reconstruction and CNN-based method implemented by the field programmable gate array (FPGA) hardware platform.

Most of the practical applied artificial intelligence methods are implemented on the embedded platform with rather high computing power due to massive samples and training parameters. In practical application for AFDD, it is challenging to run the artificial intelligence methods on the industrial microcontroller units (MCUs) such as STM32 series MCUs with properties of relatively low cost and computing power. The authors in [20] offer a hybrid time and frequency analysis and fully connected neural network (HTFNN)-based method, which uses category recognition to address the feature overlap among different loads and working states, as well as reduce the state identification complexity. The HTFNN method is implemented on a STM32F407ZG MCU from Italian company STMicroelectronics (Plan-les-Ouates, Switzerland), and general accuracies of normal and arcing state identification in the Re, CI, and Sw categories is 99.64%, 100%, and 98.45%, respectively. However, the HTFNN method may encounter difficulties in practical applications due to the poor feasibility of the category classification under masking loads.

There are currently few studies on lightweight arc fault detection approaches for artificial intelligence models implemented on industrial MCUs under random masking load. Therefore, studying a lightweight arc fault detection method based on neural network, enhancing its accuracy and lowering its computational complexity, is of considerable importance and has extensive application potential.

This paper proposes a hybrid arc fault detection method based on a Back Propagation (BP) neural network and hardware feature algorithm. To reduce the complexity, the sample state is classified into two categories by the level of the total harmonic distortion (THD) of the current. The category with THD is managed by the BP neural network, while the other one is assessed by a fixed threshold of a novel feature named pulse signal number per unit cycle, which is converted from the high-frequency components by a feature extraction circuit. Finally, the arc fault detection is implemented on hardware based on the STM32F401RCT6 MCU for a micro circuit breaker. The main studies are listed as follows:

1. Experiments are carried out to collect data under various loads, creating a series arc fault dataset for extensive analysis and modeling. The current waveform features of the arc faults are discussed under different load types.
2. A novel feature named pulse signal number per unit cycle is extracted, reflecting the zero-off phenomena when an arc fault occurs. The current features, including pulse

signal number per unit cycle, amplitudes of third and fifth harmonic contents, THD, and root mean square (RMS) value and its change rate, are analyzed and chosen for the arc fault detection.

3. Instead of raw current data, six current features are chosen to drive the BP neural network, lowering the computational complexity. Adam optimizer is applied for the BP neural network and its performance is compared to other commonly used optimizers.
4. The proposed arc fault detection method is validated on a hardware platform for micro circuit breakers. The performance of the proposed method is evaluated along with typical methods from the recent literature.

2. Data Collection and Analysis

Five types of household loads, including pure resistive load, and six kinds of masking loads are selected for the experiments, as shown in Table 1. According to the recommendations from IEC 62606:2022 [21], resistors, vacuum cleaners, fluorescent lamps plus an additional 5A resistive load, electronic lamp dimmers, capacitor starting (air compressor type) motors, electric hand-held drills, and electronic switching power supplies are selected as representatives loads for testing.

Table 1. Types and descriptions of different loads.

Load Type	Appartus	Description
Pure resistive	Resistor	-
Masking loads	Vacuum cleaner	Rated at 5 A to 7 A for a 230 V rated voltage
	Fluorescent lamp	Two 40 W fluorescent lamps plus an additional 5 A resistive load
	Electronic lamp dimmer	600 W with a filtering coil controlling a 600 W tungsten load
	Capacitor starting motor	Peak inrush current of 65 A $\pm$ 10% for a 230 V voltage
	Electric hand-held drill	600 W
	Switching power supply	Current of at least 2.5 A, with a minimum THD of 100%, and individual minimum current hrmonics of 75% at the 3rd, 50% at the 5th, and 25% at the 7th.

Figure 1 shows the current waveforms of different loads. Figure 1a shows the current waveform of the pure resistive load. The load is under normal and fault conditions in the first and last three cycles, respectively. The flat shoulder features, generated by the arc extinguishing near the zero-crossing points due to the fault, are marked with red circles. Figure 1b shows the current waveform of the vacuum cleaner load. The waveform represents a normal condition on the left side of the dashed line, while an arc fault condition is on the other side. Figure 1c,d show the current waveforms of the vacuum cleaner load during normal, early-arc, and mid-arc periods. The amplitude of the current waveform in the early-arc period is unstable, with an overall decrease and an insignificant waveform distortion. The current waveform during the mid-arc period is shown in Figure 1d. The violently burning fault arc generates rich high-order harmonic contents, which are reflected in the burrs marked in the figure on the waveform.

The features of the arc faults are summarized below.

1. Both the waveforms of the pure resistor and the fluorescent lamp loads emerge with significant differences between the normal and the arc fault conditions. Moreover, the zero-off features occur at the zero-crossing points.
2. Due to the influence of the internal components, zero-off features exist in the waveforms of the vacuum cleaner and the capacitor starting motor loads. However, the current waveform exhibits high-order harmonic contents near the zero-crossing points under the arc fault condition.
3. A fault arc is equivalent to a series resistor in the circuit, leading to a decrease in the amplitude of the current.

Thus, the arc fault can be detected by the above time domain features of the current waveform under specific loads and circuit configurations. However, the features could be inconspicuous with masking loads in the circuit, making it difficult to detect arc faults solely by the time domain features. Therefore, it is necessary to carry out an arc fault detection method for different loads and circuit configurations.

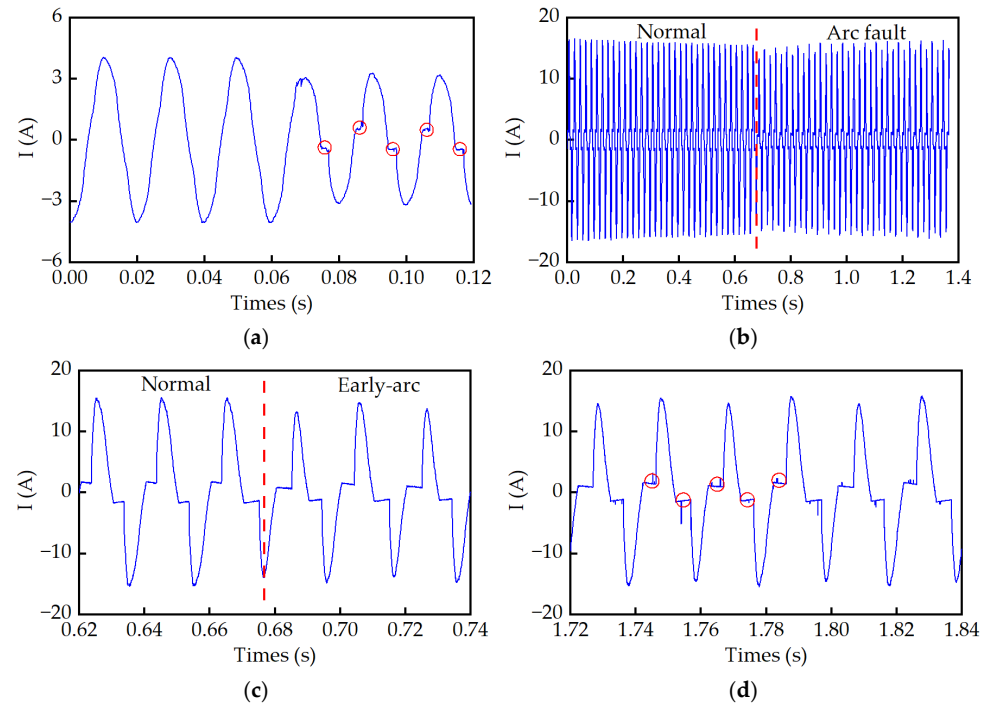


Figure 1. Current waveforms under different loads. (a) Pure resistive load. (b) Vacuum cleaner load. (c) Enlarged view of the vacuum cleaner load during normal and early-arc conditions. (d) Enlarged view of the vacuum cleaner load during mid-arc condition.

3. Discussion of Current Features in Time and Frequency Domains

3.1. Pulse Signal Number per Unit Cycle

When an arc fault occurs in the circuit with low-voltage AC apparatuses, zero-off phenomena are exhibited near the zero-crossing points. These phenomena are manifested in the waveform as flat shoulder features and in the electrical quantity as sharp increases in di/dt at the zero-crossing points. A feature extraction circuit is built to convert the flat shoulder features into pulse signals, shown in Figure 2. The current samples are filtered into low-frequency and high-frequency signals. The high-frequency signals are imported into a differentiator, enlarging the signals reflecting the flat shoulder features and resulting in spike signals. The spike signals are then converted into pulse signals by comparing the peak value to a fixed threshold. Figure 3 shows the pulse signal converted from the flat shoulder features near the zero-crossing points.

When there are components such as thyristors and inductors in the circuit, the current waveform will also exhibit flat shoulder features. The current waveforms and the pulse signals of different loads under both normal and arc fault conditions are presented in Figure 4. It can be observed that the arc faults can be detected by the pulse signals converted from the flat shoulder features for the loads of vacuum cleaner, fluorescent lamp, electronic lamp dimmer, air compressor, electric hand-held drill, and switching power supply. Since the switching moments of thyristors also present flat shoulder features, it is not possible to accurately detect the fault arc by the pulse signals for the electronic lamp dimmer load.

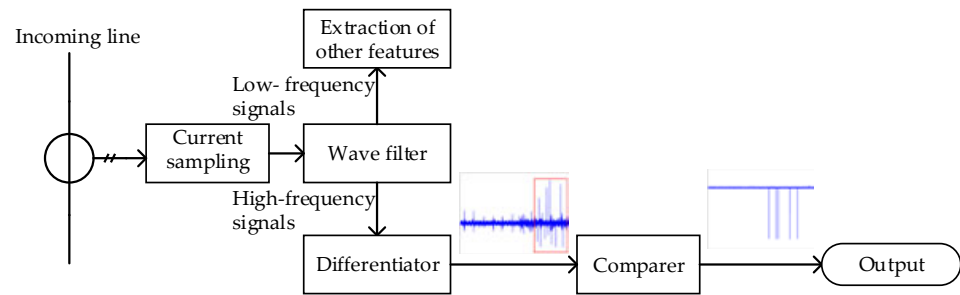


Figure 2. Diagram of the extraction circuit.

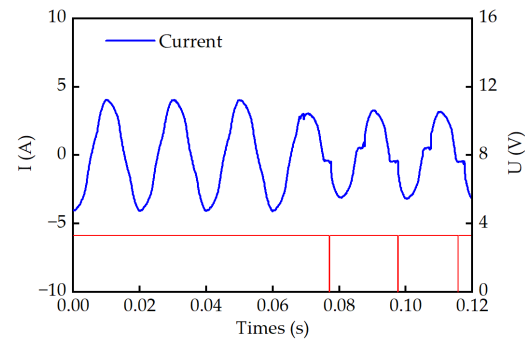


Figure 3. Pulse signal converted from the flat shoulder features.

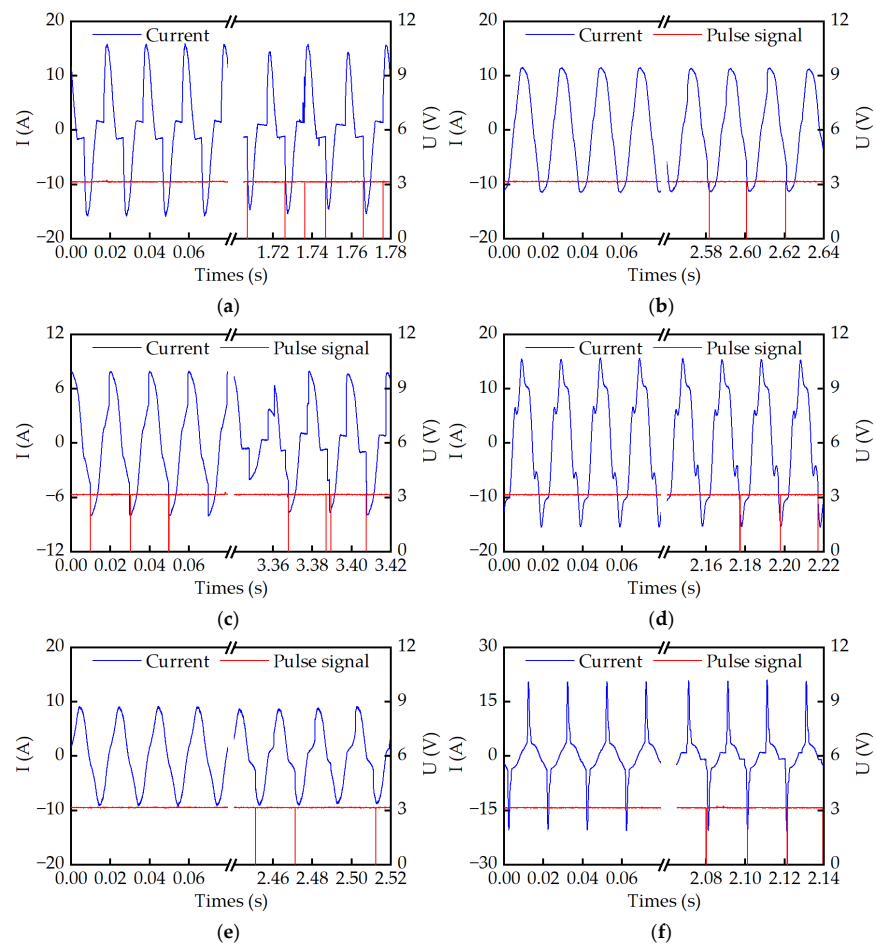


Figure 4. Waveforms of currents and pulse signal under different loads. (a) Vacuum cleaner. (b) Fluorescent lamp. (c) Electronic lamp dimmer with a conduction angle of 60° . (d) Air compressor. (e) Electric hand-held drill. (f) Switching power supply.

Although the feature acquisition circuit performs poorly on the electronic lamp dimmer load, the pulse signal number is still one of the important indicators to detect arc faults in the circuit. The pulse signal number per unit cycle is entitled as c .

$$c = \frac{\text{count}}{T} \quad (1)$$

where count is the number of pulse signals, and T is the unit cycle, which is 0.02 s in this paper.

3.2. Frequency Domain Features

The arc fault will lead to a sharp drop in the voltage waveforms and distortion in the current waveforms. A fast Fourier transform (FFT) is applied to analyze the differences in the frequency domain. Figure 5 shows the harmonic contents of different loads before and after the occurrence of arc faults. The high-order harmonic contents, especially the third and the fifth orders of the harmonic contents, present apparent increases for the arc fault condition. Thus, THD, along with amplitudes of the 3rd and the 5th harmonic contents are selected for the arc fault detection.

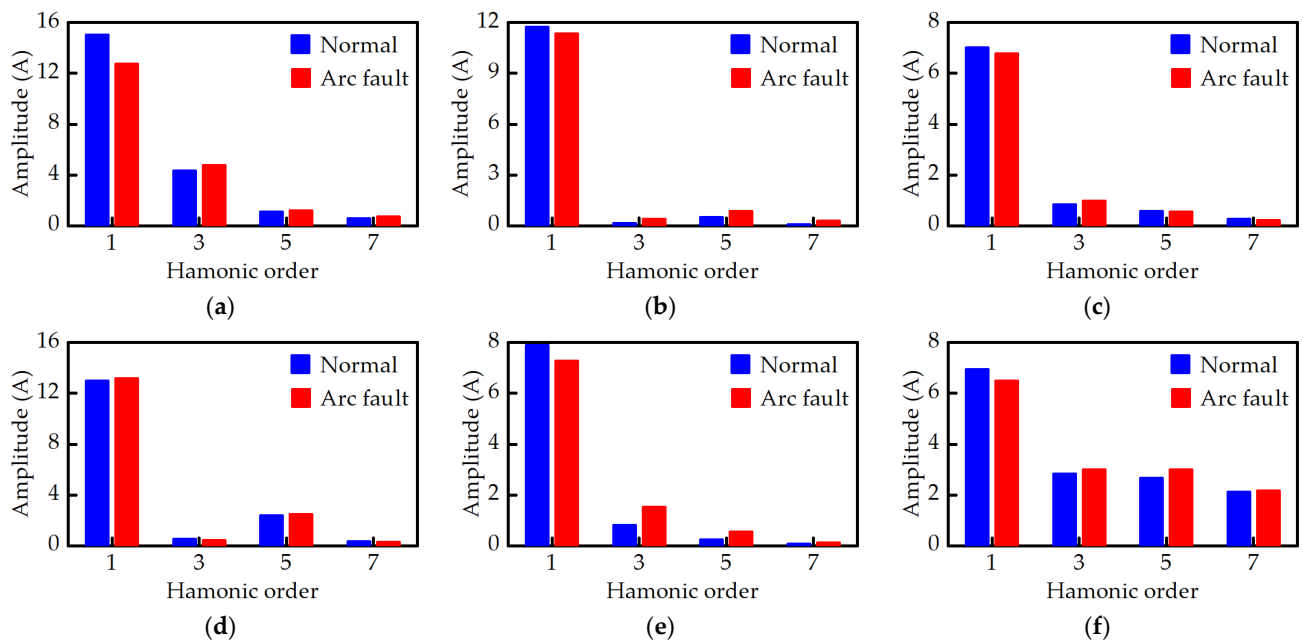


Figure 5. Frequency spectral analysis of various loads. (a) Vacuum cleaner. (b) Fluorescent lamp. (c) Electronic lamp dimmer with a conduction angle of 60° . (d) Air compressor. (e) Electric hand-held drill. (f) Switching power supply.

3.3. Time Domain Features

Since the series arc fault will lead to an increase in the total impedance of the circuit and a decrease in the current amplitude, the current amplitude is also selected as a criterion for arc fault detection. The RMS value of the current, denoted as I_{RMS} is calculated as

$$I_{\text{RMS}} = \sqrt{\frac{\sum_{i=1}^N x_i^2}{N}} \quad (2)$$

where N refers to the number of current sampling points per unit cycle, and x_i refers to the value of the first current sampling point.

Table 2 shows the RMS values of the circuit current for different loads under normal operation and arc fault conditions. It can be observed that the circuit current of various loads changes when an arc fault occurs.

Table 2. Changes in currents for different loads under normal operation and arc fault conditions.

Load	Condition		Change Rate
	Normal	Arc Fault	
Vacuum cleaner	10.01 A	9.85 A	1.65%
Fluorescent lamp	8.33 A	8.08 A	3.02%
Electronic lamp dimmer	5.06 A	4.90 A	5.56%
Air compressor	9.38 A	9.53 A	1.52%
Electric hand-held drill	5.63 A	5.32 A	5.56%
Switch power supply	6.19 A	6.10 A	1.46%

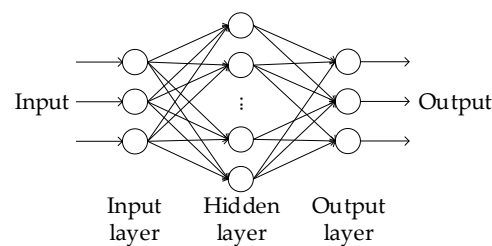
4. Arc Fault Detection Method

4.1. Adam-Optimized BP Neural Network

To achieve lightweight arc fault detection while maintaining high accuracy and reliability, a BP neural network with relatively low computational complexity is introduced for practical application on AFDD. BP neural network is a multi-layer feedforward neural network trained using an error backpropagation algorithm, which has strong nonlinear mapping ability and a flexible network structure. Figure 6 shows the structure of the BP neural network consisting of one input layer, one hidden layer, and one output layer. The output of the BP neural network is calculated as

$$y = f[f(W_1x + B_1)W_2] + B_2 \quad (3)$$

where x and y are the input and output matrix, f is the activation function, W_1 and B_1 are the weights and biases between the input layer and the hidden layer, and W_2 and B_2 are the weights and biases between the hidden layer and the output layer.

**Figure 6.** Structure of BP neural network.

Instead of raw current data, the acquired current features in both time domain and frequency domain are imported into the BP neural network to reduce the computational complexity, matching the computing power of STM32 series MCUs. The structure of the proposed BP neural network is shown in Figure 6. The neural network consists of one input layer, three fully connected layers, and one output layer. The input is a 1×6 array containing c , amplitudes of the 3rd and the 5th harmonic contents, THD, I_{RMS} , and change rate of I_{RMS} between adjacent current cycles. The output is a 1×2 array that provides two classifications in a one-hot encoding form. The specific parameters of the BP neural network are shown in Table 3.

Table 3. BP neural network parameters.

Network Layer	Output Size	Parameter Amount
Input	1×6	-
Dense	1×32	224
Dense_1	1×16	528
Dense_2	1×16	272
Output	1×2	34
Total params: 1058		

The Adam optimizer, which is an extension of Stochastic Gradient Descent (SGD) uses momentum and an adaptive learning rate to accelerate convergence speed. It estimates the first-order and second-order moments of the gradient for each parameter based on the objective function with exponential moving average. By keeping the feature scaling of each parameter's gradient unchanged, high noise and gradient dilution issues can be solved during the parameter space iteration process [22].

$$\begin{cases} \theta_i^{(k+1)} = \theta_i^{(k)} - g_i^{(k)} \\ g_i^{(k)} = \frac{\eta \hat{v}_i^{(k)}}{\sqrt{\hat{s}_i^{(k)} + \varepsilon}} \end{cases} \quad (4)$$

$$\begin{cases} \hat{v}_i^{(k)} = \frac{v_i^{(k)}}{1 - \beta_1^k} \\ \hat{s}_i^{(k)} = \frac{s_i^{(k)}}{1 - \beta_2^k} \end{cases} \quad (5)$$

where k is the number of iterations, θ_i is the i th feature parameter during the iteration process, g_i is the descent distance along the gradient direction, v_i is the exponential decay average of historical gradients, s_i is the exponential decay average of historical gradient quadratic, $\hat{v}_i$ and $\hat{s}_i$ are the deviation correction values for v_i and s_i , respectively. ε is a manual parameter, hyperparameters η , β_1 , and β_2 are defined as 0.001, 0.9, and 0.999, respectively. The training chart of the Adam-optimized BP neural network is shown in Figure 7.

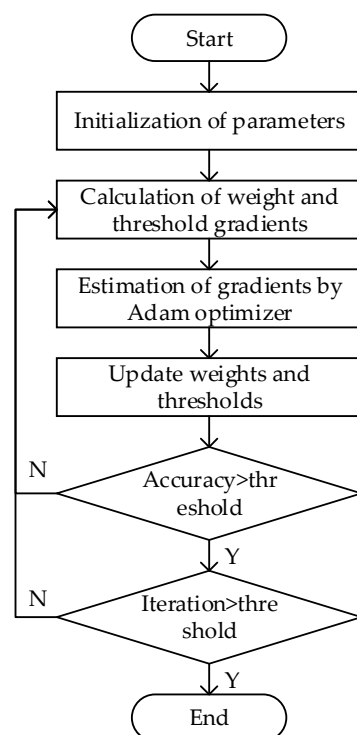


Figure 7. Flowchart of Adam optimization.

The Adam optimizer is compared to three commonly used neural network optimizers, including AdaDelta [23], SGD [24], and Root Mean Square Prop (RMSprop) [25], under the conditions of the same network structure, training samples, learning rate, and other factors. Figure 8 reflects the performances of different optimizers in arc fault detection from the accuracy and loss function values of the training and testing sets after 500 iterations.

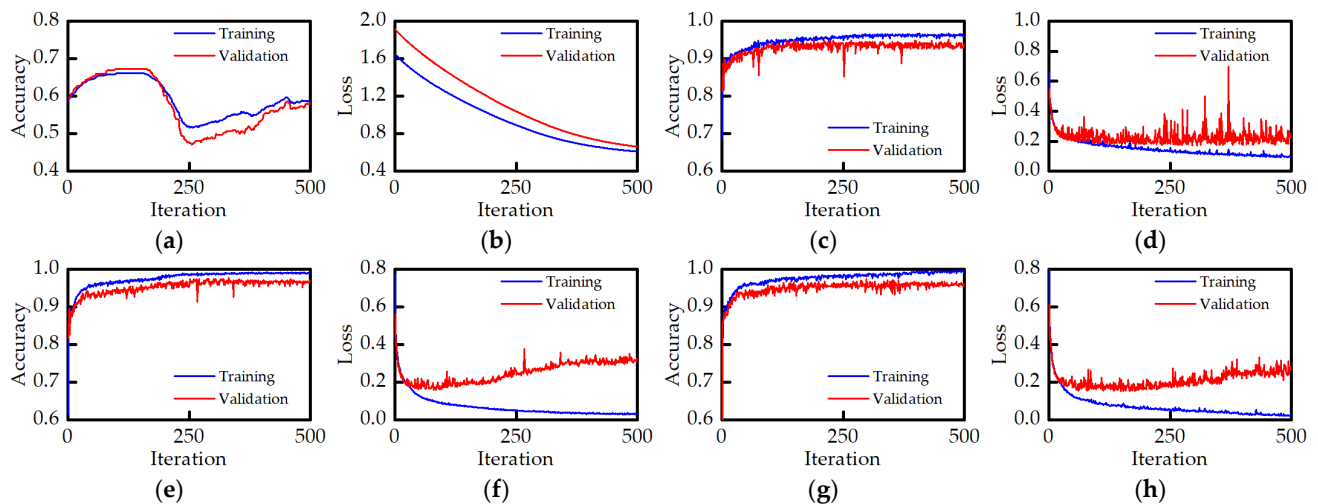


Figure 8. Performances of different optimizers. (a) Accuracy of AdaDelta. (b) Loss of AdaDelta. (c) Accuracy of SGD. (d) Loss of SGD. (e) Accuracy of RMSprop. (f) Loss of RMSprop. (g) Accuracy of Adam. (h) Loss of Adam.

The AdaDelta optimizer is not highly applicable in this model. The SGD optimizer reduces the accuracy while pursuing speed, resulting in unstable accuracy curves and loss function value curves. The RMSprop optimizer alleviates the problem of gradient descent oscillation with a steady increase in accuracy. However, the loss function value curve rises significantly as the number of iterations increases. The Adam optimizer presents a good performance in both accuracy and loss function value. Additionally, the results of the iteration numbers required to achieve a certain accuracy are shown in Table 4. The RMSprop and the Adam optimizers need much fewer iterations than the SGD optimizer to reach the same accuracy. Thus, the Adam optimizer is chosen due to the best performance among the four optimization algorithms.

Table 4. Comparison of iteration numbers with different optimizers.

Optimizer	Iteration Number with the Same Accuracy				
	95%	96%	97%	98%	99%
SGD	163	240	405	667	1943
RMSprop	25	63	97	153	309
Adam	19	32	60	110	296

4.2. Design of Hardware System

A hardware system is developed to acquire the current features, including c , harmonic contents, distortion rate, and I_{RMS} and its change rate, for arc fault detection in the circuit. An STM32F401RCT6 MCU-based system is established to analyze and discriminate whether an arc fault occurs in the circuit. The arc fault feature detection system, shown in Figure 9, includes a current acquisition module, a filtering module, a feature extraction module, and an MCU.

The currents are acquired by a current transformer and converted into current features. Then, the MCU uses serial communication and self-developed micro breakers to achieve arc fault detection and action protection, as shown in Figure 10.

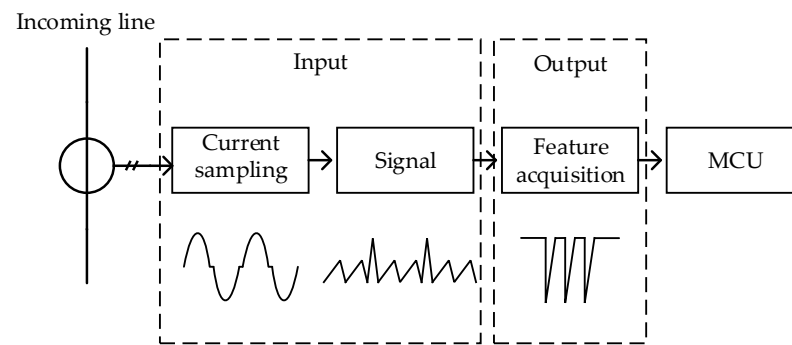


Figure 9. Hardware block diagram.

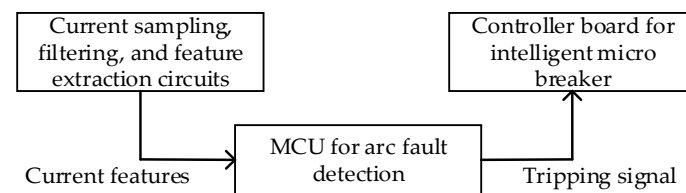


Figure 10. System block diagram.

In this paper, an arc fault detection method based on feature c assessment and the Adam-optimized BP neural network for different states of the THD is developed. The flowchart, including real-time sampling and feature extraction, state discrimination, feature c assessment, and Adam-optimized BP neural network, is shown in Figure 11 for arc fault detection. A real-time A/D acquisition of circuit current signals is built in the main program, while a real-time feature acquisition is achieved in one unit cycle. An interrupt program is triggered to count the number of pulse signals when the flat shoulder features occur. The state discrimination module determines the arc fault detection, accomplished with the fixed threshold or the Adam-optimized BP neural network.

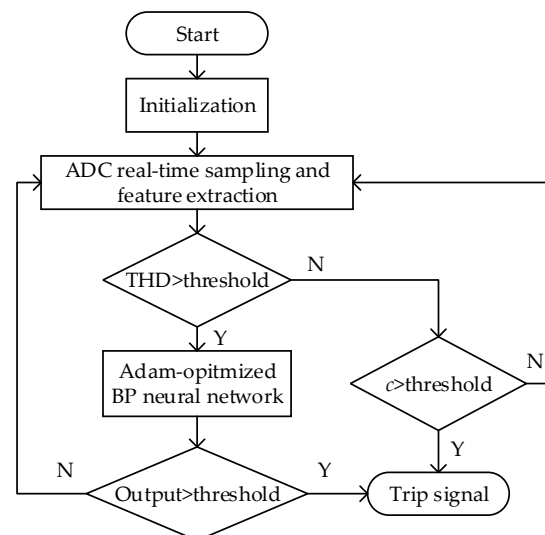


Figure 11. Flowchart of the propose arc fault detection method.

Pure resistive loads and resistive-inductive loads, including fluorescent lamp and halogen lamp loads, have less high-order harmonic contents in the circuit currents under normal operation conditions. The flat shoulder features are easily acquired when an arc fault occurs. For pure resistor and resistor-inductance loads, the algorithm module will choose the hardware feature algorithm, resulting in a fast speed and lower computing effort in arc fault detection.

Masking loads such as vacuum cleaners, composite loads such as capacitor starting motors, and switching power supplies contain many high-order harmonics in the circuit current under normal operation conditions. The distortion of current signals caused by high-frequency harmonics interferes with the detection by the hardware feature algorithm. At the same time, the absorption of high-frequency signals weakens the flat shoulder features, resulting in an inaccurate arc fault detection by the hardware feature algorithm. In these cases, the Adam-optimized BP neural network is more suitable for the arc fault detection.

5. Experimental Validation and Analysis

This section illustrates the experimental results carried out to evaluate the performance of the Adam-optimized BP neural network with 8000 tests under various load conditions. The proposed lightweight arc fault detection method based on the Adam-optimized BP neural network and the hardware feature algorithm is deployed on the STM32F401RCT6 MCU for a micro circuit breaker, and its performance is compared to several typical methods from the recent literature.

5.1. Performance of the Adam-Optimized BP Neural Network

The Adam-optimized BP neural network is trained for 296 iterations with the primary dataset. The memory size of the neural network is 3304 bytes. In the detection performance assessment, cases of true positive (TP), true negative (TN), false positive (FP), and false negative (FN) are, respectively, considered. The model is also evaluated using some performance measures such as accuracy, recall, precision, and F1-Score. These performance metrics are given in Table 5. The accuracy, recall, precision, and F1-Score of the Adam-optimized BP neural network are 99.27%, 98.73%, 99.52%, and 99.12%, indicating that the model shows good performance in the arc fault detection.

Table 5. Performance metrics of the Adam-optimized neural network.

Case	Count	Performance Metric	Rate
TP	622	Accuracy	99.27%
TN	867	Recall	98.73%
FP	3	Precision	99.52%
FN	8	F1-Score	99.12%

5.2. Experimental Verification on AFDD

A prototype of an arc fault detection module is installed in a circuit breaker controller board, shown in Figure 12. Experiments are carried out to validate the accuracy of the arc fault detection algorithm under different loads including vacuum cleaners, fluorescent lamps, electronic lamp dimmers, air compressors, electric hand-held drills, and electronic switching power supplies.

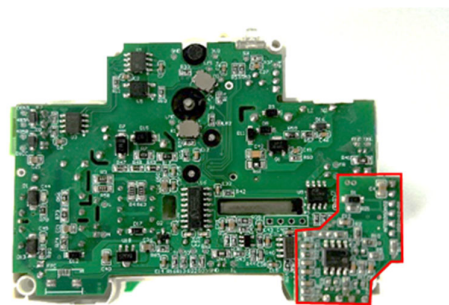


Figure 12. Circuit breaker control board installed with arc fault detection module, highlighted in red lines.

Figure 13 shows the waveforms of the circuit current and the fault arc recognition trip signal under a vacuum cleaner load. It takes 127 ms for the MCU to detect the occurrence

of the arc fault and send the trip signal, while it takes 75ms for the breaker to break the circuit for protection. The total tripping time is 202 ms. According to IEC 62606:2022, the maximum allowable detachment time at the current of 7 A is 0.25 s, indicating the effectiveness of the arc fault detection.

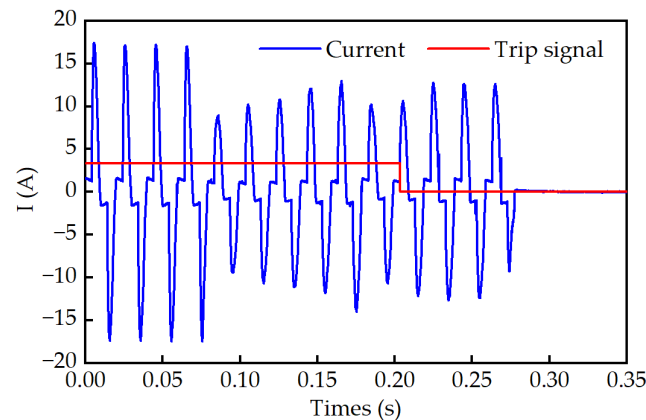


Figure 13. Waveform of the current and the trip signal under a vacuum cleaner load.

The accuracy of the arc fault detection is tested under seven loads, as shown in Table 6. An arc fault detection is considered valid when the break time is less than the maximum break time by IEC 62606:2022. Except for the electronic lamp dimmer load, the accuracy rate of the arc fault detection under other loads can reach over 98%. Due to the use of thyristors in electronic dimming lamps, the current waveform of thyristors at the switching moment also presents a flat shoulder feature, resulting in a decrease in detection accuracy. The average runtime of the arc fault detection with a 12.8 kHz sampling rate is 45 ms, indicating the feasibility of the proposed method in hardware for AFDD.

Table 6. Accuracy of identifying fault arcs under various loads.

Load	Number of Tests	Current	Accuracy	Average Tripping Time
Vacuum cleaner	50	10.6 A	100%	201 ms
Fluorescent lamp	50	8.1 A	100%	72 ms
Electronic lamp dimmer	50	5.4 A	94%	160 ms
Air compressor	50	10.5 A	98%	183 ms
Electric hand-held drill	50	5.9 A	98%	122 ms
Switching power supply	50	7.0 A	100%	87 ms

5.3. Method Comparison

In the comparison with some typical methods, aspects such as method framework, parameter amount, deployed hardware platform, detection accuracy, etc., are contrasted to evaluate the proposed arc fault detection method, as shown in Table 7. Compared to other methods, the parameter amount of the proposed method is significantly reduced using current features instead of raw current data, indicating a lower computational complexity. Although the use of six current features lost arc information to a certain extent, our method's accuracy is at the same level (above 99%) as the contrastive methods. In the aspect of AFDD application, the tripping time of our method is less in contrast with the CNN based on the EffNet module in [16]. Therefore, the method proposed in this paper reaches high detection accuracy at lower computational complexity and has been validated for the application of AFDD.

Table 7. Comparison with typical methods.

Method	Ning et al. [1]	Wang et al. [2]	Zhou et al. [3]	Ours
Method framework	Lightweight CNN based on EffNet module	CNN based on load classification	Phase space distance feature matrix + CNN	Adam-optimized BP neural network and hardware feature algorithm
Data input	Raw current data	Raw current data	50 × 50 distance matrix	Six current features
Parameter amount	Over 76,000	Over 88,000	Over 72,000	1058
Deployed hardware platform	Raspberry Pi 4B with a 1.5 GHz ARM Cortex-A72 CPU	Raspberry Pi 3B with a 1.2 GHz ARM Cortex-A53 CPU	FPGA	STM32F401RCT6 with an 84 MHz ARM Cortex-M4 CPU from Italian company STMicroelectronics
Detection accuracy	99.75%	99.47%	99.00%	99.27%
Application of AFDD	The average tripping time is 110–240 ms ¹ , while the accuracy is not introduced.	No application.	No application.	The average tripping time is 72–201 ms, while the average accuracy is 98.33%.

¹ The tripping times of different methods are compared under same load types.

6. Conclusions

This paper proposes a series AC arc fault detection based on a novel current feature and Adam-optimized BP neural network. Based on the analysis of arc features, a novel feature named pulse signal per unit cycle is extracted and chosen as the discrimination indicator for tests with lower THD and as one of the six input features of the neural network for tests with higher THD, which can help reduce the computational complexity of the neural network. The Adam optimizer is selected and applied to achieve a high accuracy (99.27%) with fewer iterations after comparing with AdaDelta, SGD, and RMSprop optimizers. Finally, a prototype based on the STM32F407ZG MCU is designed and tested on a micro circuit breaker. The experimental results show that the average accuracy in AFDD application is 98.33%. Meanwhile, the average runtime of the arc fault detection with a 12.8 kHz sampling rate is 45ms, and the average tripping time is 72–201 ms, which meets the requirements of IEC 60606:2022. The implementation assessment shows its feasibility in hardware for commercial AFDD applications. Further study will be carried out to extend the feasibility of multi-load conditions and complex working states.

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