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Failure Characterization of Discrete SiC MOSFETs under Forward Power Cycling Test

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Abstract: Silicon carbide (SiC)-based metal–oxide–semiconductor field-effect transistors (MOSFETs) hold promising application prospects in future high-capacity high-power converters due to their excellent electrothermal characteristics. However, as nascent power electronic devices, their long-term operational reliability lacks sufficient field data. The power cycling test is an important experimental method to assess packaging-related reliability. In order to obtain data closest to actual working conditions, forward power cycling is utilized to carry out SiC MOSFET degradation experiments. Due to the wide bandgap characteristics of SiC MOSFETs, the short-term drift of the threshold voltage is much more serious than that of silicon (Si)-based devices. Therefore, an offline threshold voltage measurement circuit is implemented during power cycling tests to minimize errors arising from this short-term drift. Different characterizations are performed based on power cycling tests, focused on measuring the on-state resistance, thermal impedance, and threshold voltage of the devices. The findings reveal that the primary failure mode under forward power cycling tests, with a maximum junction temperature of 130 °C, is bond-wire degradation. Conversely, the solder layer and gate oxide exhibit minimal degradation tendencies under these conditions.

Keywords: forward power cycling test; on-state resistance; discrete SiC MOSFET; threshold voltage; thermal impedance measurement

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1. Introduction

In the pursuit of global efforts toward developing clean energy sources, the proportion of renewable energy sources, including wind and photovoltaic power, in the power grid is escalating, paralleled by a remarkable surge in the installed capacity of these units [1,2]. According to the latest data released by the International Energy Agency (IEA) in June 2023, global renewable energy capacity additions are anticipated to surge to 550 GW in 2024, necessitating the integration of an increasing amount of renewable energy into the grid via converters. This extensive and high-capacity integration of renewable energy imposes stringent performance criteria on converters [3], particularly in terms of their efficiency [4], reliability [5], and active support capabilities [6].

In the novel operational setting, the switching loss of the converter assumes a pivotal role as a critical quality factor, accounting for an increasing percentage of the overall loss due to high-frequency switching operations [7]. Silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) offer a substantial edge over silicon (Si) insulated-gate bipolar transistors (IGBTs), exhibiting a remarkable 2.86-fold reduction in switching losses across the same frequency range [8]. Furthermore, SiC MOSFETs boast not only lower switching losses but also reduced conduction losses compared to Si MOSFETs [9]. Theoretically, under equivalent withstand voltage, the drift layer resistance per unit area of SiC can be significantly diminished up to 300 times lower than Si [10]. Additionally, Si-based devices have encountered their inherent physical constraints in terms of blocking voltage,

making them insufficient for the upcoming era of high-voltage DC transmission lines, which typically boast rated voltages reaching up to 800 kV [11]. In contrast, SiC devices exhibit a significantly superior blocking capability, allowing systems that employ these devices to reduce the number of components required in series submodule units [12] and affiliated auxiliary electronic components [4,13]. This, in turn, leads to a further miniaturization of the converter. Furthermore, SiC material possesses the inherent advantage of being able to operate at elevated temperatures, unlike Si [14]. By capitalizing on these advantages, SiC MOSFETs demonstrate exceptional performance in high-temperature, high-frequency, and high-voltage applications [15]. However, despite the numerous benefits of SiC MOSFETs, their long-term reliability issues, as an emerging power electronic device, still necessitate in-depth research and solutions [16].

Power electronic devices consist of materials exhibiting diverse coefficients of thermal expansion (CTE), as depicted in Figure 1. Temperature fluctuations within high-temperature, high-frequency, and high-voltage operating environments give rise to internal thermal stresses, resulting in degradation phenomena such as cracks. These cracks ultimately limit the device's lifespan [17]. In practical working conditions, device failure is a gradual process that occurs over an extended period. Consequently, in experimental research, the power cycling test (PCT) method is frequently utilized to expedite the failure process. The PCT is designed to simulate the thermo-mechanical stresses imposed on power electronic devices in their actual operating environments, enabling the investigation of component failures [18].

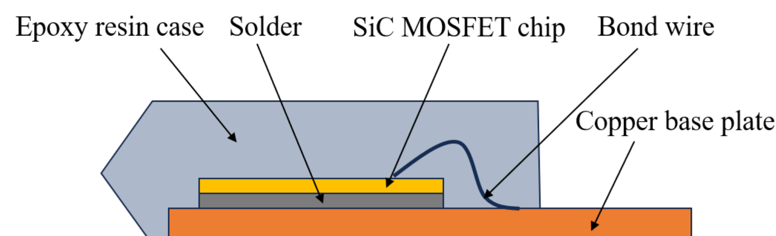

Figure 1. Cross-sectional view of TO-247 packaged SiC MOSFET.

This paper aims to conduct a thorough investigation into the performance evolution of SiC MOSFETs under specific power cycling conditions, analyzing the underlying failure mechanisms through a systematic series of experimental studies. To establish a solid foundation, this paper begins with a concise overview of failure experiments conducted under power cycling conditions. This overview includes elucidating the fundamental failure principles of the device, discussing various experimental methodologies employed in power cycling, describing calibration procedures for temperature-sensitive parameters, and explaining the measurement techniques used to assess thermal impedance. Subsequently, a detailed description of the experimental methodology is presented. To accurately measure the variation in its threshold voltage, an offline threshold voltage measurement circuit is utilized, mitigating the short-term drift value arising from the wide bandgap characteristics of SiC [19]. Furthermore, to precisely monitor the junction-to-case thermal impedance and identify the aging state of the solder layer, a thermal characterization experiment is conducted based on JESD51-14 [20]. In the final section, the experimental results are comprehensively analyzed, delving into the exploration of potential failure mechanisms. Additionally, a brief discussion is presented regarding strategic measures to enhance the reliability of SiC MOSFETs.

2. Background

2.1. Main Failure Modes and Characterization Parameters

Device failures primarily include chip-level failures and package-level failures [21], as shown in Table 1. Chip-level failures manifest as gate oxide failures and body diode failures. Gate oxide failures are generally caused by interfacial charge or breakdown effects

induced by electrical overstress and high temperatures [22,23], whereas body diode failures mainly stem from forward voltage bias stress [24].

Table 1. Main failure modes of SiC MOSFETs and their characterization parameters.

Package failures	Bond-wire lift-off Solder fatigue Metallized reconstruction	V_{dson}, R_{dson}, Bond-wire resistance Z_{th}, Solder layer resistance R_{dson}, V_{dson}
Chip failures	Gate oxide Body diode	V_{mp}, t_{mp}, R_{dson}, I_{dss}, V_{th}, I_{gss} R_{on}, V_f, I_{dss}

Currently, widely employed indicators for gate oxide failure [25] include various parameters such as the miller plateau voltage amplitude (V_{mp}) [26], miller plateau duration (t_{mp}) [26], on-state resistance (R_{dson}) [27], drain leakage current (I_{dss}) [28], threshold voltage (V_{th}) [22,29], and gate leakage current (I_{gss}) [30], among others. These indicators provide crucial insights into the health and degradation of the gate oxide layer. When it comes to characterizing body diode degradation, key parameters mainly include the on-state resistance of the body diode (R_{on}) [31], forward voltage (V_f) [32], and drain leakage current (I_{dss}) [33].

Common package-level failures for devices mainly comprise bond-wire failures and solder fatigue [34], as shown in Figure 2. This type of failure primarily stems from thermo-mechanical stresses [35], relative humidity stresses [36], and high current density stresses [37] during device operation, with thermo-mechanical stresses being dominating.

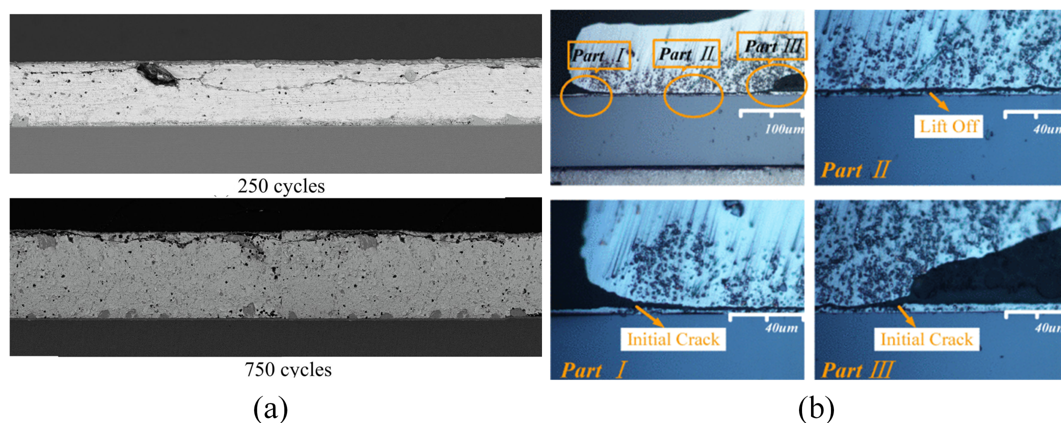

Figure 2. Package level Failure. (**a**) Crack failure in the solder layer [38]. (**b**) Bond wire crack and lift-off failure [39].

There are two main failure mechanisms of bond wires [40]. One is caused by the difference in CTEs between the bond wire and the SiC chip, leading to crack formation and eventually bond-wire lift-off [41,42]. Heel cracking is the second failure mode, which comes from the thermo-mechanical stresses generated by heat transfer within the bond wire and the displacement between the two bond pads due to the overall CTE mismatch [43]. The failure modes of bond wires are related to their aspect ratios, and studies have indicated that bond wires with different aspect ratios have different failure modes [44]. They primarily affect the conduction current path; thus, the key characterization parameters are the on-state voltage (V_{dson}) and on-state resistance (R_{dson}). In the literature [45], the on-state voltage is used as an indicator for bond-wire lift-off. Standard AQG324 [46] states that the device is considered to have reached a failure criterion when the on-state voltage increases by more than 5% of its initial value.

Solder fatigue is mainly due to differences in CTEs between the solder and the connected materials, as well as between different pads, resulting in solder delamination [47,48].

Solder fatigue primarily affects the thermal conduction path, where cracks and voids reduce the effective thermal conduction area between the chip and copper board, leading to changes in thermal impedance (Z_{th}) between them [49]. In Ref. [50], thermal impedance was used as a characterization parameter for solder fatigue under narrow temperature fluctuations, and in [51] B. Ji et al. carried out fatigue state monitoring of solder layers in IGBT modules using thermal impedance as a parameter. Standard AQG324 [46] mentions that the failure criterion for thermal impedance is a growth to 20% of the initial value.

2.2. Power Cycling Test Modes

The PCT is a rapid experimental method used to induce failure in research devices. As shown in Figure 3, it heats and cools the device with cyclic load currents (I_L), and during the cooling phase, a small sense current (I_{sense}) is applied for parametric measurements. This repeated heating and cooling creates thermo-mechanical stresses within the device, causing cumulative fatigue and accelerated aging.

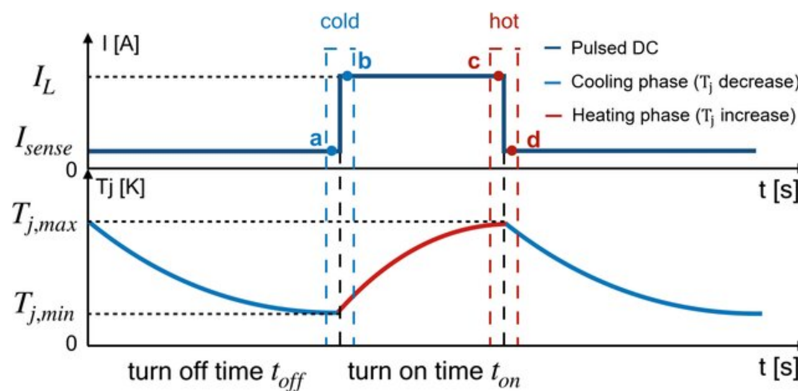

Figure 3. Power cycling test procedure [52].

The PCT can be classified into DC and AC versions, distinguished primarily by the nature of the heating current. Despite their common failure modes [53], the DC method stands out due to its simplicity in control, making it the preferred option. Regarding heat generation mechanisms, three distinct modes of power cycling exist: forward mode, reverse mode, and body diode mode. In forward mode, heat is primarily generated by the forward on-state resistance during the device's on state. Conversely, in reverse mode, heat generation arises from both the reverse on-state resistance and the body diode while the device is in its on state. Finally, the body diode mode specifically involves heat generation solely by the body diode when the device is in its off state. It is noteworthy that the latter two modes are influenced by the negative temperature coefficient of the body diode, resulting in deviations from the typical operational behavior of SiC MOSFETs in practical scenarios [54]. Consequently, the forward mode is generally preferred.

The control strategies for power cycling mainly encompass four types [55], as shown in Table 2.

Table 2. Four power cycling test strategies.

Control Strategy	Control Means	Compensation
T_{on}, T_{off} = constant	Direct control of switching time	No
ΔT_c [1] = constant	Control of switching time	Potential degradation of the thermal interface between the casing and the heatsink surface
P_v [2] = constant	Control of gate voltage	Increased positive pressure drop due to degradation
ΔT_j [3] = constant	Control of load current, switching time, cooling conditions, gate voltage	Fully compensates for all degradation effects

[1] T_c is the case temperature. [2] P_v is the power loss. [3] T_j is the junction temperature.

In practical applications, compensating for attenuation by reducing output power is generally unacceptable [56]. Consequently, the PCT without attenuation compensation is the preferred approach, and this experiment employs the active mode along with a control strategy that maintains a constant switching time.

2.3. Junction Temperature Measurement

There are two primary categories of measurement methods for the device junction temperature: invasive and non-invasive methods. Invasive methods necessitate direct or indirect contact with the chip, necessitating the opening of the package during measurement. However, this process can potentially damage the chip, thereby compromising the experiment's outcomes. Conversely, non-invasive methods eliminate the need for chip contact and indirectly measure the junction temperature through other parameters. These methods are outlined in Table 3.

Table 3. Junction temperature measurement methods.

	Measurement Method	Control Means	Response Speed	Accuracy	Ease of Implementation
Invasive Measurements	Physical contact method	Thermocouple or thermistor placed inside the device [57]	Slow	Normal	Easy
	Optical method	Infrared imaging [58] or body diode electroluminescence [43]	Normal	Not good	Normal
Non-Invasive Measurements	Thermal modeling method	Total impedance thermal network model [59]	Fast	Bad	Difficult
	TSEP methods	Thermal parameters that are linear with temperature	Fast	Good	Easy

The temperature-sensitive electrical parameter (TSEP) method is the most commonly used method to characterize junction temperature changes at this stage. The choice of parameters should meet several criteria, including a linear relationship with the junction temperature, ease of measurement, and independence from device aging. Currently, the mainstream junction TSEPs include the forward voltage drop of the body diode under low current, on-state resistance, and threshold voltage.

The on-state resistance [60], while serving as a notable indicator of device aging, exhibits a significant drift in its relationship with the junction temperature curve following device failure. Regarding the threshold voltage [61], its value experiences considerable fluctuations during measurement due to the presence of traps within the device. Consequently, accurately determining whether these fluctuations are attributed to traps or temperature changes becomes challenging, as uncontrollable factors exert a significant influence. In contrast, the body diode exhibits excellent stability and high sensitivity during the aging process of the device, with its characteristics remaining unchanged over time [62]. Therefore, the voltage drop across the body diode under low current conditions was chosen as the TSEP.

2.4. Thermal Impedance Measurement

Thermal impedance measurements, crucial for characterizing solder layer failures in package-level failures, remain a pivotal research area.

Conventional methods for measuring thermal impedance adhere to the JESD 51-1 standard, which necessitates concurrent measurements of the junction temperature, case temperature, and power dissipation. However, this standard lacks clarity regarding whether the case temperature should be represented as an average or a maximum value [63]. Furthermore, when the device is mounted on a heatsink, accurately gauging the device's

external case temperature necessitates drilling a small hole in the heatsink for thermocouple placement, potentially perturbing the temperature field.

In [64], a method for evaluating heating curves was proposed, but it still does not determine the thermal interface resistance between the package case surface and the heatsink. Building on this, Szabo et al. [65,66] proposed to compare the structure functions obtained from two transient measurements at different interface layers between the case and the heatsink to identify the thermal impedance, known as the transient dual-interface measurement (TDIM), but the structure-function composition is not very accurate. Schweitzer [67] provided an alternative assessment method for the TDIM based on the derivative of the Z_{th} curve. This eventually led to the development of JESD51-14 [20], which defines the TDIM and its measurement method.

3. SiC MOSFET Degradation Experiment

Two device types, C2M0080120D with multiple bond wires (Wolfspeed, Durham, NC, USA) and SCT30N120 with a single bond wire (STMicroelectronics, Geneva, Switzerland), were utilized for the power cycling test to compare the performance of devices with single bond-wire and multiple bond-wire configurations. Table 4 summarizes the key characteristics of the devices used. Given the significance of real-time temperature monitoring in the experiment, calibration tests were conducted on the TSEP prior to commencing the experiment. Furthermore, we optimized the control sequence to minimize noise and overvoltage generation during the PCT. Additionally, to ensure accurate threshold voltage measurements, a pre-study was conducted using an offline approach to mitigate the short-term drift of the threshold voltage. Lastly, emphasis was placed on accurate and reliable measurements of the thermal impedance. Offline measurements of the threshold voltage and thermal impedance were performed every 500 or 2000 cycles, and a detailed experimental flowchart is presented in Figure 4.

Table 4. Main characteristics of DUTs.

Name	Type	R_{thJC}	R_{dson}	V_{th}
DUT1 DUT2	C2M0080120D	0.6 K/W	140 mΩ (V_{gs} = 16 V, T_j = 125 °C, I_{ds} = 20 A)	3.25 V ($V_{gs} = V_{ds}$, I_d = 5mA, T_j = 25 °C)
DUT3	SCT30N120	0.65 K/W	90 mΩ (V_{gs} = 20 V, T_j = 150 °C, I_{ds} = 20 A)	3.5 V (V_{gs} = V_{ds}, I_d = 1 mA)

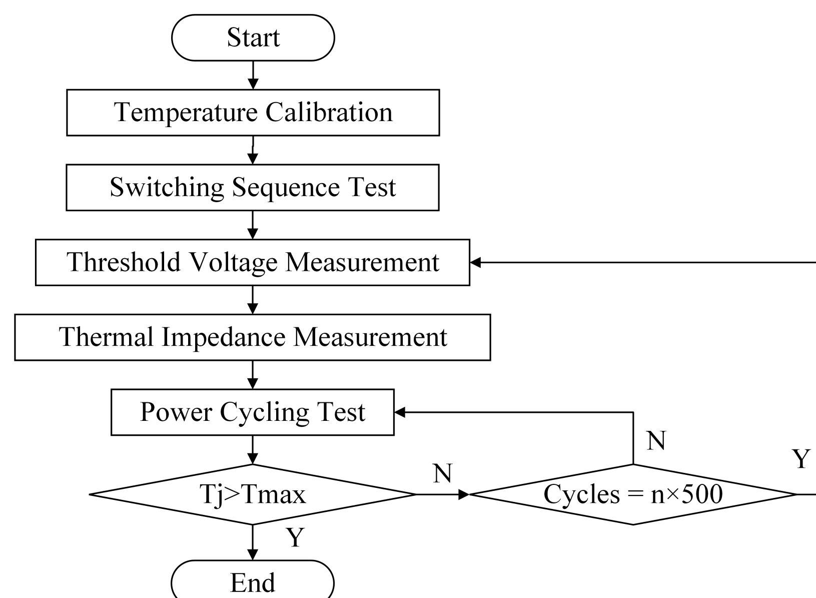

Figure 4. Flowchart of SiC MOSFET degradation experiment.

3.1. Temperature Estimation Using the TSEP

The junction temperature was measured using the body diode voltage drop as the TSEP, and the calibration circuit is shown in Figure 5. After the temperature in the oven reached a steady state, a sense current was applied to measure the voltage drop across the body diode. To minimize the self-heating effect caused by the sense current, the sense current was applied in the form of pulses. The device's drain-to-source voltage was measured as the voltage drop across the body diode at this temperature.

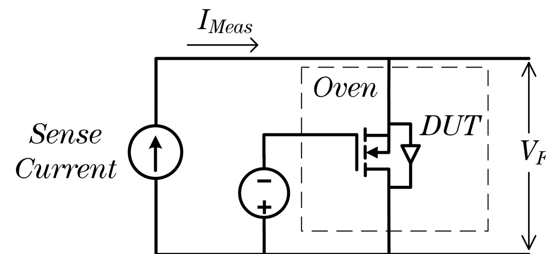

Figure 5. Circuit diagram of junction temperature calibration experiment.

Tests were conducted using small currents of 10 mA, 50 mA, 80 mA, and 100 mA. Ensuring the MOSFET remained in a fully off state during measurements was paramount, necessitating the maintenance of a gate-source voltage of −5 V, as stipulated in the device's datasheet. This voltage level ensured the complete shutdown of the MOSFET's forward conduction channel, thereby eliminating any influence from the forward conduction resistance when measuring the voltage across the drain and source terminals. The outcomes are depicted in Figure 6, demonstrating excellent linearity across all four measured currents. Given the laboratory equipment conditions, 100 mA was selected as the sense current for this experiment.

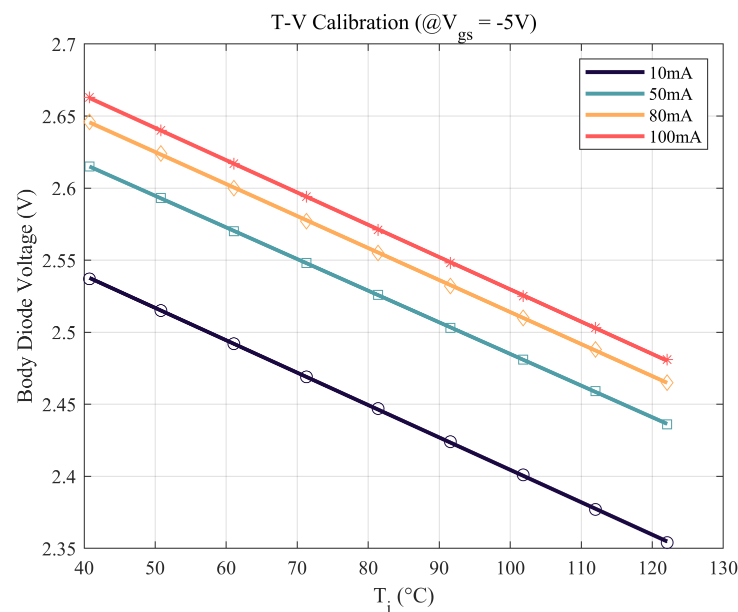

Figure 6. Calibration curves at different sense currents.

3.2. Power Cycling Test

The PCT was conducted in the forward MOSFET mode, involving the passage of a constant current to generate heat within the device. The circuitry for the PCT is depicted in Figure 7, while the test bed is schematically illustrated in Figure 8. The cycling conditions are summarized in Table 5.

Table 5. Conditions of the power cycling test.

Ton	Toff	On-State Gate Voltage	Off-State Gate Voltage	Heat Current	Sense Current
2 s	6 s	15 V	−5 V	22 A	100 mA

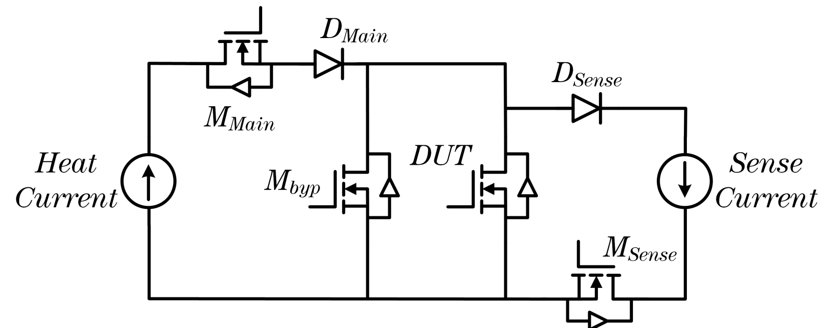

Figure 7. Circuit diagram of forward-mode power cycling test.

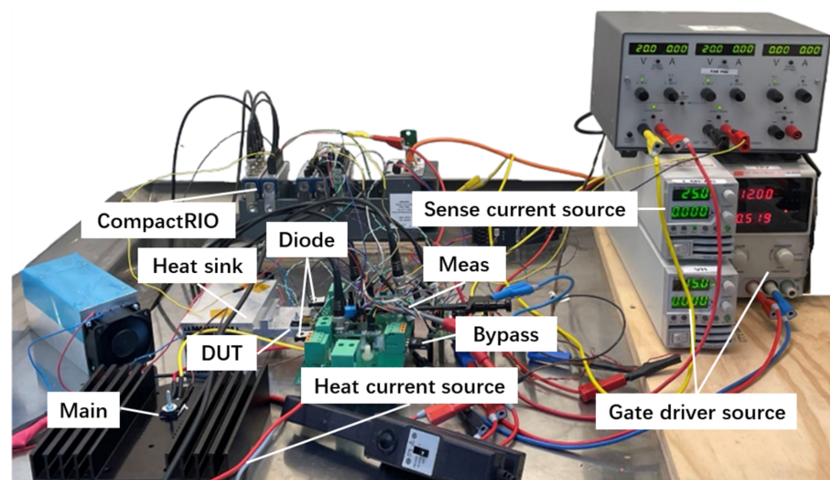

Figure 8. Illustration of the test bed.

3.3. Switching Sequence Test

Reference [54] indicated that the device may encounter voltage spikes and extended transient effects during switching state transitions. When measuring the maximum junction temperature, it was observed that the junction temperature experienced a significant drop in a brief period at the commencement of device turn-off. Consequently, the accurate and prompt capture of the voltage value at the instant of device turn-off was paramount for accurate maximum junction temperature measurement. To tackle this challenge, we conducted an investigation into the circuit switching sequence during the device's turn-off process.

The deactivation sequence during turn-off encompassed the shutdown of both the device under test (DUT) and the Main power source. Figure 9 depicts the traced and measured voltage fluctuations across various sequences. Preceding the deactivation of the Main, turning off the DUT led to a notable voltage spike exceeding 50 V, accompanied by a transient response spanning over 15 µs. Alternatively, if both were deactivated concurrently or the Main was deactivated initially, the transient duration was reduced to approximately 3 µs. However, the former sequences still induced a voltage spike exceeding 40 V. Therefore, during the experimental setup, it was determined to deactivate the Main initially, followed by the DUT after a brief delay of 1 µs.

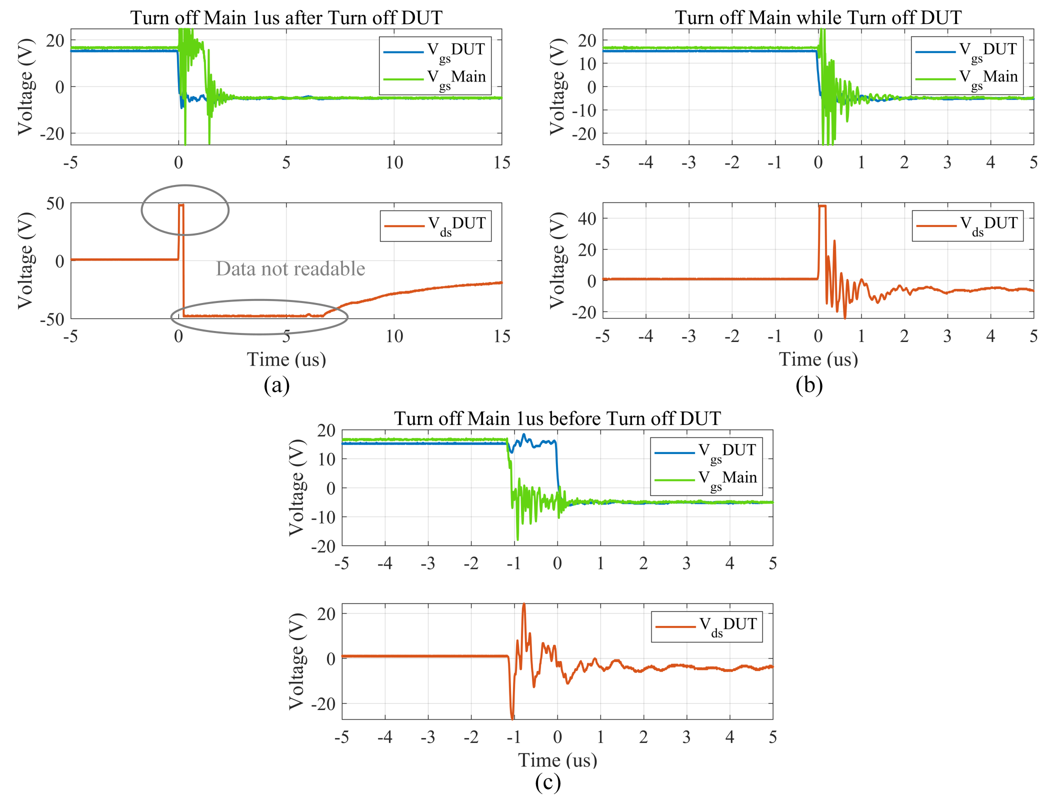

Figure 9. Experimental comparison of different switching-off sequences to assess their impact on body diode voltage measurements for calculating the maximum junction temperature. (**a**) Turn off Main first, then turn off DUT. (**b**) Turn off Main and simultaneously turn off DUT. (**c**) Turn off DUT first, then turn off Main.

3.4. Threshold Voltage Measurement

According to the datasheet for the C2M0080120D [68] shown in Table 4, the threshold voltage is defined as the gate-source voltage when the gate and drain are short-circuited with a gate-source current of 5 mA flowing.

Guided by the threshold voltage measurement conditions outlined in the datasheet, a measurement circuit was devised, as depicted in Figure 10. During experimentation, it was noticed that, despite maintaining a constant measuring current, the threshold voltage gradually rose with increasing dwell time, exhibiting a fluctuation amplitude of up to 0.1 V, as shown in Figure 11. This voltage instability arises from transient effects caused by point defects at the semiconductor–electrode interface in SiC MOSFETs [19], thus posing challenges in accurately determining the threshold voltage during measurement.

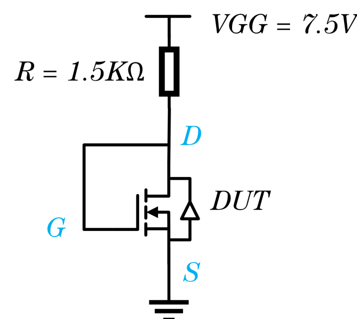

Figure 10. Threshold voltage measurement circuit 1 based on the datasheet [68]. The gate and drain were shorted before measurement with a 7.5 V voltage applied. A 1.5 kΩ resistor limits the current to 5 mA.

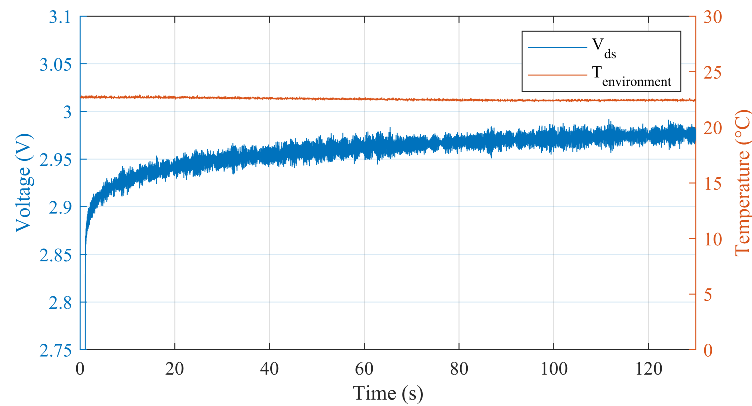

Figure 11. The results of threshold voltage measurement circuit 1. With the VGG and temperature held relatively constant, the drain-to-source voltage decreased by approximately 0.1 V over time.

Moreover, owing to their wide bandgap characteristics, SiC materials cause notable shifts in the Fermi level's position during upward voltage scans, necessitating a prolonged period to attain thermal equilibrium. Conversely, during downward voltage scans, the alterations in the Fermi level are minimal, resulting in a nearly instantaneous restoration of thermal equilibrium. This asymmetry introduces a drift in the measured threshold voltage values in both measurement techniques. Notably, the threshold voltage is more precisely determined during the downward scan voltage due to reduced drift, as reported in [19].

Accordingly, the threshold voltage measurement circuit was set based on standard JEP183A and JEP184 [69,70]. The circuit and timing diagrams are shown in Figure 12. The results are illustrated in Figure 13, where it can be observed that the device voltage decreased slightly at a constant current of around 10 mV, indicating that this approach can greatly improve the effects of the trap near the gate. However, with the second circuit, the duration was short and controllable, enabling the determination of the threshold voltage at a current of 5 mA.

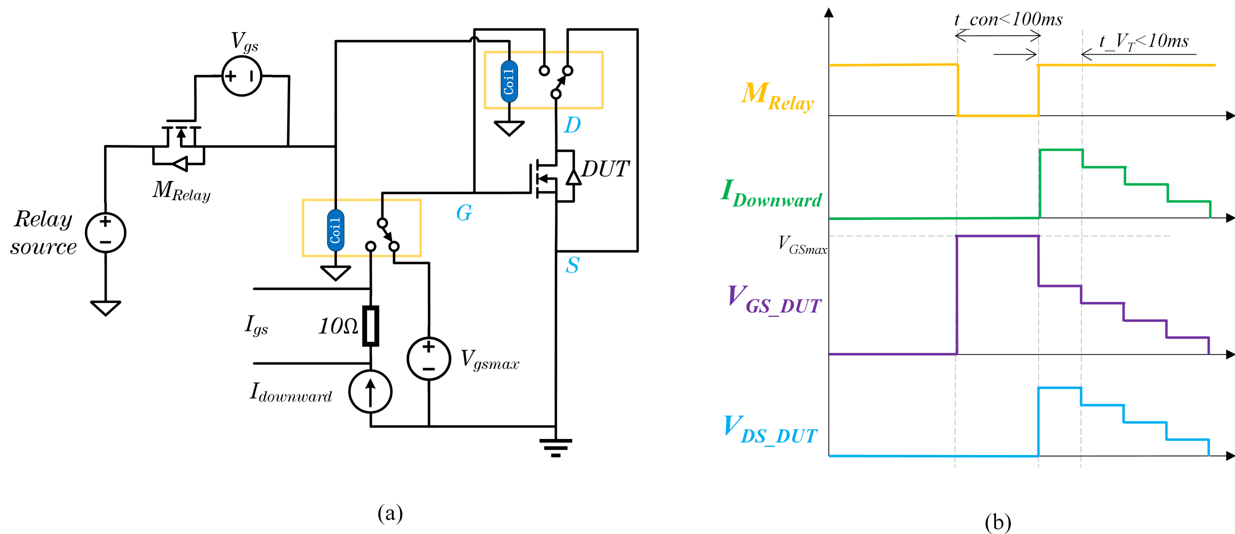

Figure 12. Threshold voltage measurement circuit 2 set according to JEP183A specifications [69]. (**a**) Circuit diagram. (**b**) Timing diagram. Prior to measurement, the drain and source are shorted, and the maximum gate voltage (25 V for this device) is applied. During measurement, the gate and source are quickly disconnected and shorted with a drain while gradually reducing the current. The threshold voltage measurement is taken when the current reaches 5 mA. M_{relay} is used to control relay switching.

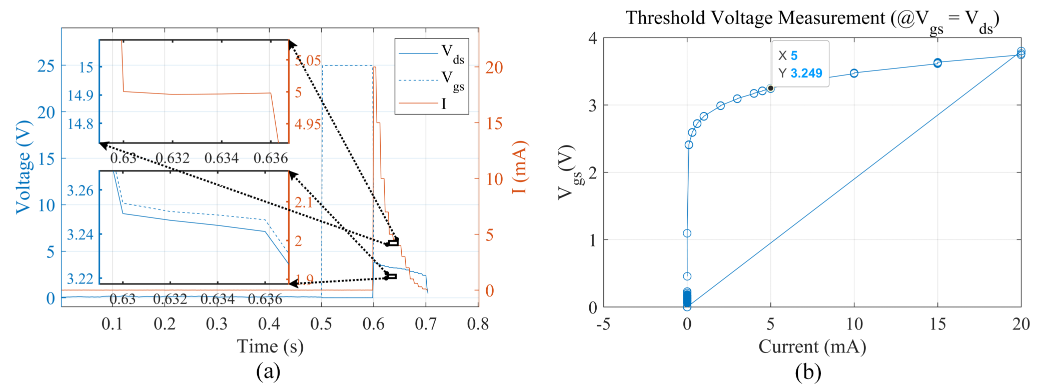

Figure 13. Timing diagram of threshold voltage measurement circuit 2. (**a**) Results of voltage and current variation with time. DUT's V_{gs} is initially set to the maximum value of 25 V, and during measurement, it quickly becomes equal to V_{ds}. The current starts decreasing gradually from 20 mA. In the zoomed-in area, it can be observed that the voltage variation remains around 0.01 V, while the circuit remains essentially unchanged. (**b**) Corresponding V_{ds} values for different currents.

In the device's datasheet [68], the threshold voltage of the device at room temperature is approximately 3.25 V. The experimental results, depicted in Figure 13, indicate a threshold voltage of 3.249 V, which aligns well with this specified value.

3.5. Thermal Impedance Measurement

When utilizing the body diode voltage drop under low current as an indicator of the junction temperature, it is feasible to measure the junction temperature solely during the cooling phase. Consequently, we measured the thermal impedance curve of the device corresponding to its cooling curve.

To mitigate the current delay resulting from the power supply mode switch, a 69 Ω resistor was integrated in series with the measurement circuit. The circuit configuration is depicted in Figure 14.

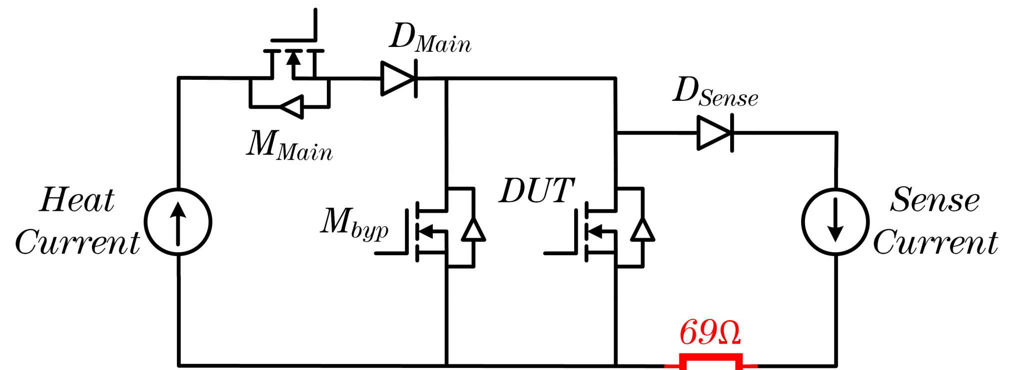

Figure 14. Thermal characterization measurement circuit. A 69 Ω resistor is substituted for M_{sense} to mitigate current and voltage fluctuations induced by power switching.

After reaching a thermal equilibrium state, data were recorded for 50 ms during the heating phase to compute the heating power. Subsequently, the cooling phase commenced, and data were recorded for 100 s throughout the cooling process. By this time, the device had cooled nearly to room temperature. Consequently, the cooling curve obtained from the measurements, following appropriate data processing, delineates the thermal impedance curve between the device junction and the surrounding environment. The results are illustrated in Figure 15 ($Z_{th}int$ denotes the result after interpolation, and $Z_{th}diff$ represents the result after differentiation).

The initial step in calculating the thermal impedance curve involves converting the cooling curve into the heating curve using Equation (1). Subsequently, the thermal impedance curve is derived by applying Equation (2).

$$T_{jheat}(t) = T_{jcool}(t) - T_{jmax} + T_{jmin}. \tag{1}$$

$$Z_{th}(t) = \frac{T_{jheat}(t) - T_{jmin}}{P_L} = \frac{T_{jheat}(t) - T_{jmin}}{U_{ds} \cdot I_{ds}}. \tag{2}$$

T_{jmax} represents the maximum junction temperature of the device in thermal equilibrium under this heating power, while T_{jmin} denotes the junction temperature of the device after 100 s of cooling, approaching room temperature. P_L stands for the power passing through the DUT during heating, U_{ds} represents the on-state voltage across the DUT during heating, and I_{ds} denotes the on-state current flowing through the DUT during heating.

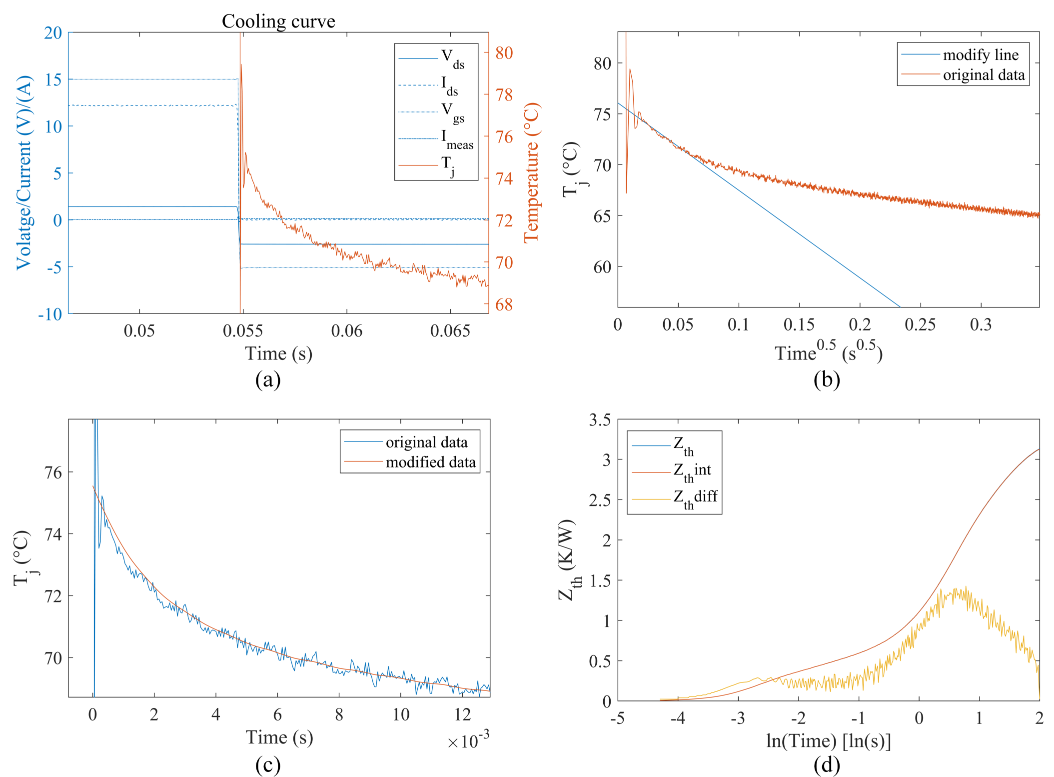

Figure 15. Thermal impedance calculation process. (**a**) There is approximately a 40 µs fluctuation in the initial switching off. (**b**) The initial temperature drops linearly with the square root of time. (**c**) The modified data follow a trend consistent with the original data. (**d**) Calculated thermal impedance according to Equations (1) and (2).

To precisely measure the thermal impedance curve between the device junction and the case, the TDIM method, as outlined in JESD51-14 [20], was utilized. In the initial measurement, a layer of thermal paste was applied between the device and the heatsink, while in the subsequent measurement, a thermal pad was inserted between them. The significant variance in thermal resistance between the thermal paste and the thermal pad caused the cooling curves to diverge at a specific point along the thermal path, indicating the location of the device case. The experimental findings, particularly the curves preceding 0.1 s, are depicted in Figure 16, offering insights into the thermal impedance curve from the device junction to the case.

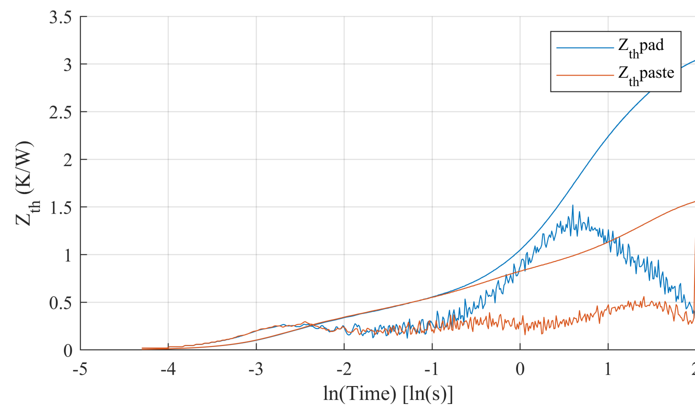

Figure 16. Measurement of junction-to-case thermal impedance using the TDIM method. The red line represents the measurement result with a layer of paste added between the device and the heatsink, while the blue line represents the measurement result with a thermal pad added.

4. Results and Discussion

The thermal impedance curve of the device during the PCT is presented in Figure 17, where the measured data for the initial 0.1 s represent the junction-to-case thermal impedance curve. The experimental results indicate that the thermal impedance did not exhibit a distinct or consistent increasing or decreasing trend, exhibiting fluctuations ranging from +4.7% to −5.6%. These fluctuations in the data can be attributed to inherent measurement errors in the instrumentation and variations in ambient temperature. Consequently, it can be deduced that there was no significant degradation of the solder layer within the device.

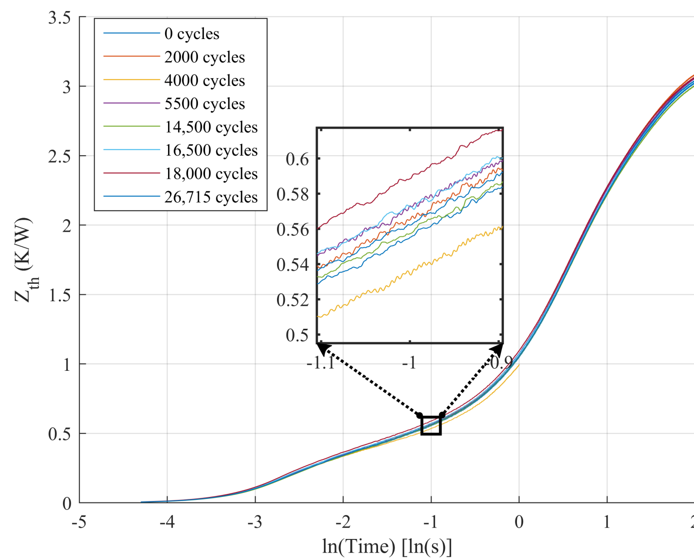

Figure 17. Fluctuations in thermal impedance curve for DUT1 over the course of a power cycling test.

As depicted in Figure 18, after completing the initial 2000 cycles, the device was removed from the test bench, resulting in a change in the contact resistance between the device and the test bench, thereby causing a variation in the maximum T_j. Subsequently, the maximum T_j stayed at around 130 °C for the initial 21,000 cycles, exhibiting a slightly increasing trend, as shown in Table 6. Figure 18 indicates that the environmental temperature also influenced the maximum T_j. At around 21,650 cycles, there was a significant rise in the maximum T_j. A distinct and abrupt increase in the maximum T_j was observed during power cycling at around 26,500 cycles. Utilizing the maximum temperature of the 3200th cycle as the baseline value, the percentage variation corresponding to the maximum T_j for different cycles is detailed in Table 6. The results of V_{dson}, a parameter characterizing

bond-wire failure, are illustrated in Figure 19, with the associated cycle numbers and percentage increases shown in Table 6. V_{dson} demonstrates a high degree of correlation with the trend of maximum T_j.

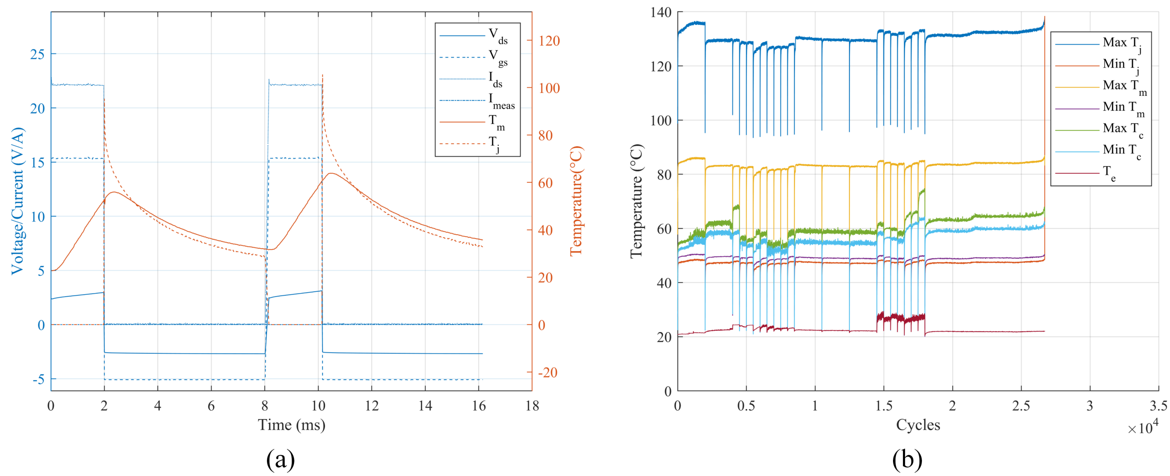

Figure 18. (**a**) Temperature, current, and current of DUT1 over time for the first two cycles. (**b**) Temperature log over the course of a power cycling test. T_j is the junction temperature, T_m is the middle pin temperature, T_c is the case temperature, and T_e is the environmental temperature.

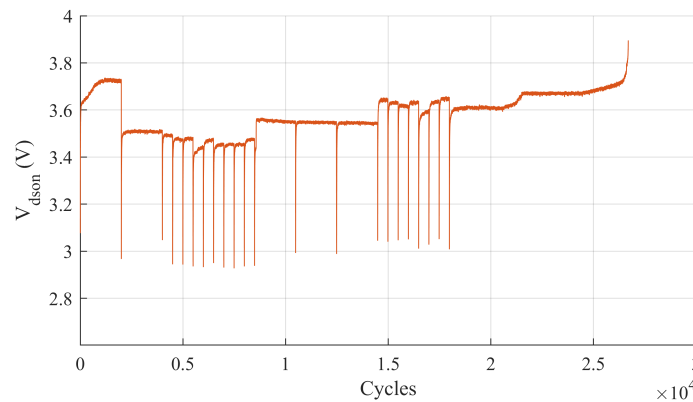

Figure 19. Log of maximum on-state voltage of DUT1 over the course of a power cycling test.

Table 6. Maximum junction temperature and on-state voltage and resistance of DUT1 over the course of a power cycling test.

Cycle Number	T_{jmax}	ΔT_{jmax}%	$V_{dsonmax}$	$\Delta V_{dsonmax}$%	R_{dson}	ΔR_{dson}%
3200	130.0	0.00	3.51	0.00	148.0	0.00
6900	127.2	−2.15	3.456	−1.54	148.3	0.20
11,530	130.1	0.08	3.549	1.11	149.6	1.08
16,260	132.2	1.69	3.633	3.50	151.8	2.57
18,630	131.3	1.00	3.610	2.85	151.8	2.57
21,650	133.0	2.31	3.677	4.76	153.9	3.99
26,690	138.4	6.46	3.896	11.00	158.8	7.30

To mitigate the influence of current fluctuations, the corresponding R_{dson} for different cycles was calculated. However, since R_{dson} exhibited a positive correlation with T_j, it was necessary to consider the impact of T_j fluctuations on R_{dson}. As the TSEP utilized was the body diode voltage drop at small currents, determining T_j during the high-current heating phase, i.e., the on-state phase of the device, was impractical. However, T_m could be reliably

measured by affixing a thermocouple at the middle pin of the device, and T_m during the PCT was notably more discernible compared to the case temperature, as depicted in Figure 18. Hence, T_m was regarded as representative of T_j during the heating phase. Given that the thermal impedance of the device remained relatively stable, the relationship between T_m and T_j theoretically remained consistent. The correlation between T_j and T_m during the cooling process was plotted for varying cycle numbers, and the outcomes are illustrated in Figure 20.

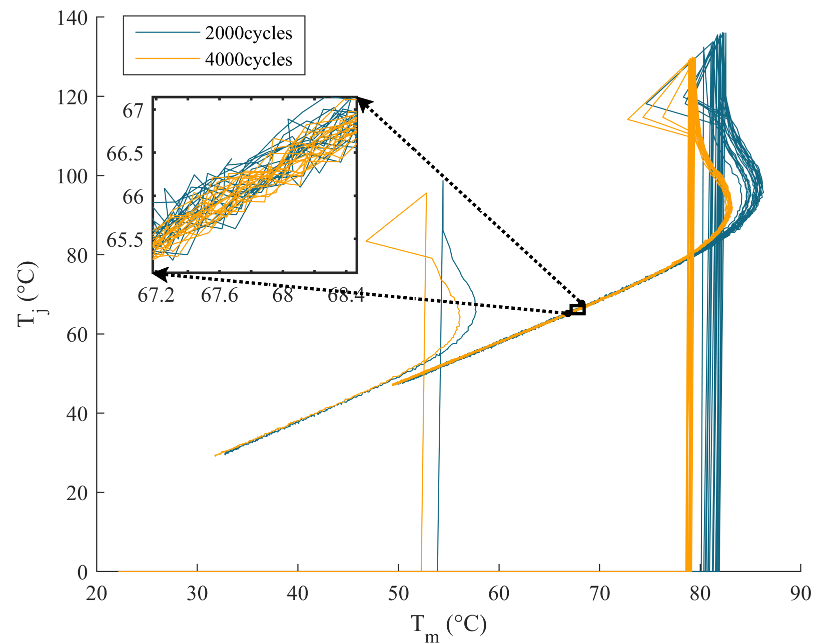

Figure 20. The relationship between the middle pin temperature and junction temperature of DUT1 during the PCT process.

The relationship between T_j and T_m exhibits non-linearity as T_j nears its peak value following cycle stabilization across various cycle counts. Nevertheless, within the temperature range of 50 °C to 75 °C, a distinct linear correlation is evident, with a maximum error margin of less than 1 °C. This correlation is expressed by Equation (3).

$$T_j = 0.933T_m + 5.85. \quad (3)$$

R_{dson} was plotted against T_m at 70 °C for each cycle, as depicted in Figure 21. The corresponding R_{dson} measurements for each cycle, along with their percentage increases, are summarized in Table 6. A more consistent increasing trend can be observed from the R_{dson} data. The 5 mΩ to 6 mΩ drop in R_{dson} produced after the 2000 cycle can be attributed to changes in contact resistance within the circuit.

Since there was no significant degradation in the solder layer of the device, the change in R_{dson} primarily stemmed from the failure of the bond wires. The C2M0080120D device with multiple bond wires shown in Figure 18b was compared to the SCT30N120 device with a single bond wire, as shown in Figure 22 (the notch in the PCT from 5000 to 9800 cycles is the maximum T_j change due to the current reduction caused by the misoperation of the current source). It was observed that the sudden T_j change phenomenon occurred only once for the device with a single bond wire, and the device could no longer operate for switching after 20 cycles following the sudden change in T_j. Therefore, it was concluded that one of the bond wires of the C2M0080120D device was lifted at 21,650 cycles, and the other bond wire exhibited visible cracking at 26,500 cycles, during which time the device could continue to operate.

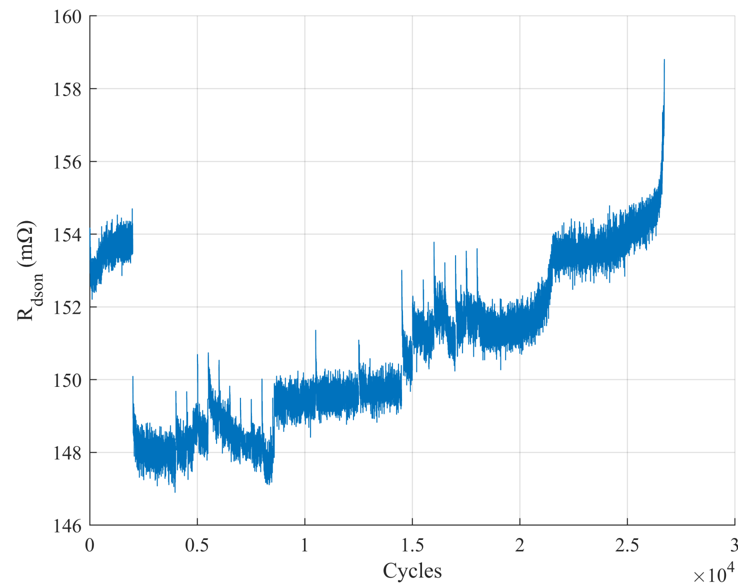

Figure 21. Log of on-state resistance of DUT1 at a middle pin temperature of 70 °C and a current of 22 A over the course of a power cycling test.

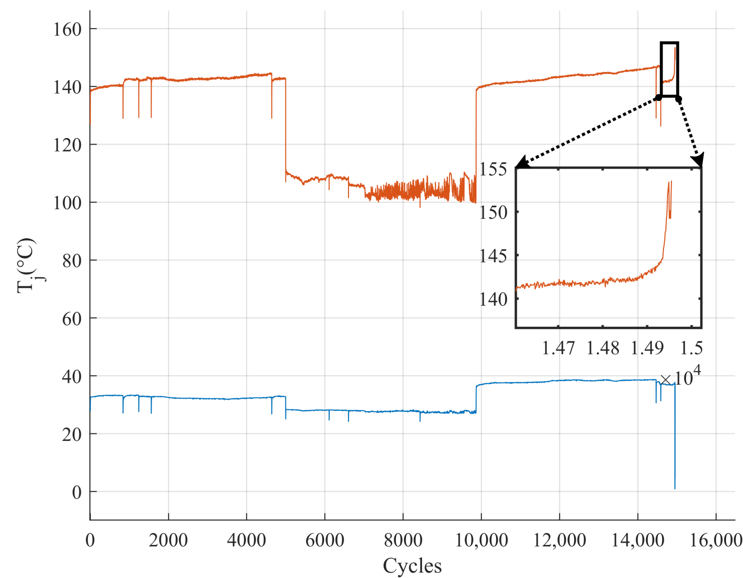

Figure 22. The variation in maximum and minimum junction temperatures of the single bond-wire device of DUT3 over the course of a power cycling test.

The subsequent operation of another device of the same type after generating a drop of more than 5% in R_{dson} is illustrated in Figure 23. Following the lifting of one bond wire, the R_{dson} of the device increased, resulting in higher power loss at the same current level. This increased power loss led to elevated currents passing through the remaining bond wires, intensifying the thermal stresses on the wires and accelerating the lifting of the other bond wire. The 5% failure criterion typically occurred between the lifting of the first bond wire and the lifting of the other bond wire. Remarkably, the device retained its operational capability during this process. In contrast to a single bond wire, which rapidly lost its functionality, multiple bond wires could still function for a certain period after reaching the failure criterion, thereby potentially enhancing the device's reliability.

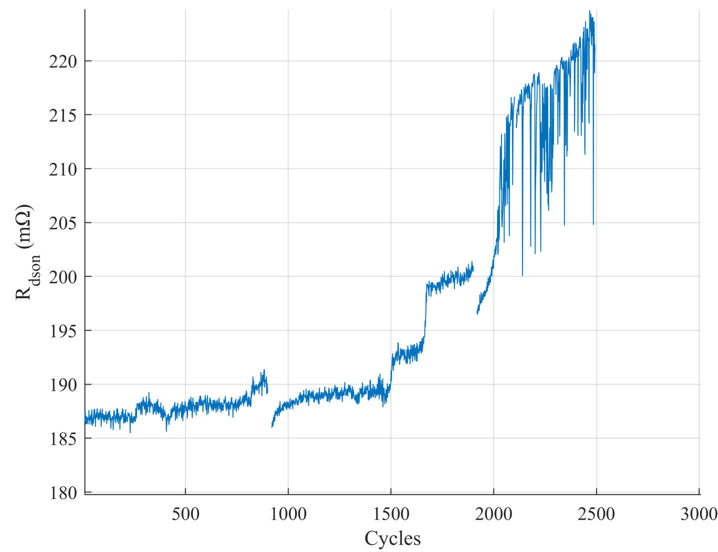

Figure 23. Subsequent changes in on-state resistance of DUT2 after it increased by more than 5% at a middle pin temperature of 70 °C and a current of 25 A.

As shown in Figures 17 and 21, the experimental results indicate that under second-level power cycling with T_j fluctuations ranging from approximately 47 °C to 130 °C, the predominant failures in devices were bond-wire failures, while there was no notable failure observed in the solder layer. The relationship between the number of cycle failures (N_F) and the maximum T_j can be expressed as follows: $N_F \propto exp(\frac{E_A}{K_B \cdot T_{Jmax}})$, where E_A represents the activation energy and k_B denotes the Boltzmann constant. Compared to bond wires, solder layer fatigue necessitates higher activation energy, approximately twice the activation energy required for bond wires [71], as illustrated in Figure 24. Under the experimental conditions, where the maximum T_j was slightly lower, the number of cycles needed for solder layer failure exceeded that required for bond wires, thus rendering bond wires more susceptible to failure.

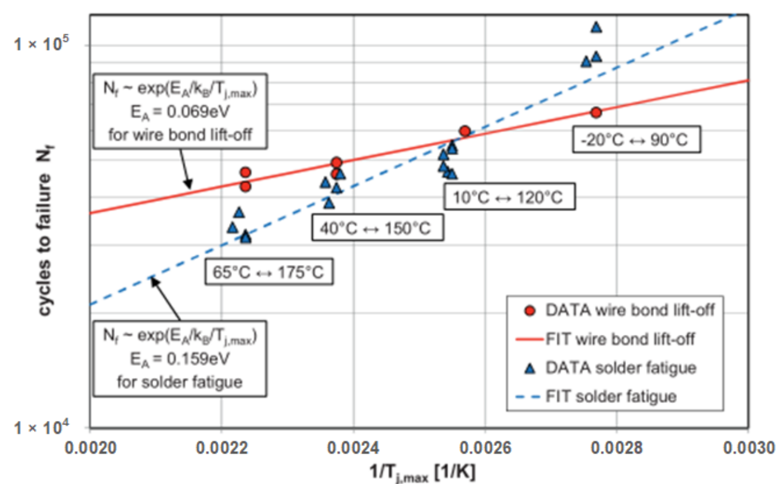

Figure 24. Impact of maximum junction temperature on solder fatigue and Al bond-wire degradation [56].

Figure 25 illustrates the fluctuation in the device's threshold voltage throughout the entire power cycling process. Notably, during the experiment, the threshold voltage exhibited minimal changes, with a fluctuation range of 0.2 V. Given the power cycling test

conditions, which involved a positively biased gate voltage of +15 V for 2 s during turn-on and a negatively biased gate voltage of −5 V for 6 s during turn-off, the products of the duration and value for both positively and negatively biased voltages were equivalent. This arrangement mitigates, to some extent, the threshold voltage drift caused by prolonged positive/negative biasing, as reported in [29]. Furthermore, the existing literature [72] indicates that the threshold voltage remains relatively stable when the gate voltage alternates between positive and negative values. This could explain the limited degradation observed in the threshold voltage. According to [19], an increase in the threshold voltage due to drift would typically lead to an increase in channel resistance. However, when comparing the fluctuations in the threshold voltage and resistance, no corresponding decrease in R_{dson} was observed despite an increase in the threshold voltage. Based on our experimental results, a clear correlation between these two parameters does not seem to exist.

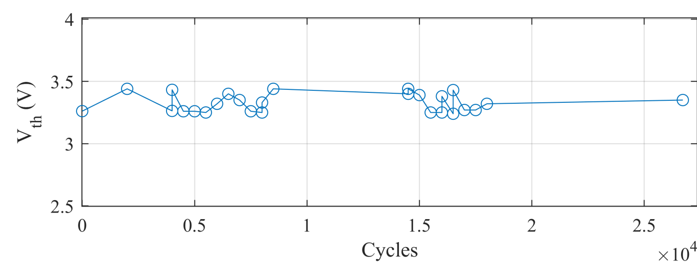

Figure 25. Fluctuation in threshold voltage of DUT1 over the course of a power cycling test.

5. Conclusions

This paper delved into a comprehensive analysis of the forward power cycling behavior of SiC MOSFETs, particularly focusing on temperature fluctuations ranging from 47 °C to 130 °C. During the experimental process, meticulous attention was paid to eliminating real-time monitoring errors that could arise from the switching sequence, while effectively minimizing errors attributed to short-term threshold voltage drift. Real-time tracking of temperature and resistance parameters was meticulously conducted throughout the experiment, with threshold voltage and thermal impedance measurements taken at specific intervals. The findings revealed a significant increase in both the temperature and on-state resistance with aging. Based on these rigorous experiments, the following conclusions are drawn:

1. Bond wires in discrete devices are more susceptible to failure compared to solder layers and chips. For this type of operating environment, it is possible to consider optimizing the bonding wire-to-chip connection to improve the reliability of the device. One possible optimization strategy is to use multiple bond wires and increase the strength of the bond wire-to-chip connection. Such an improvement is expected to significantly enhance the performance and lifetime of the device.
2. In this paper, we discussed that using an offline approach to threshold voltage measurement can largely attenuate the short-term drift of a single threshold voltage measurement. However, there was still a 0.2 V fluctuation in the threshold voltage during the PCT. At the same time, we found that there was an inconsistency between the drift of the threshold voltage and the change in the on-state resistance. In subsequent experiments, we intend to expand the number of research devices to further investigate the threshold voltage measurement and its relationship with on-state resistance in depth.

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Abbreviations

CTE	coefficients of thermal expansion
DUT	device under test
IGBT	insulated-gate bipolar transistor
MOSFET	metal–oxide–semiconductor field-effect transistor
PCT	power cycling test
TDIM	transient dual-interface measurement
TSEP	temperature-sensitive electrical parameter
Si	silicon
SiC	silicon carbide

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