

Article

Stability Control of Grid-Connected Converter Considering Phase-Locked Loop Frequency Coupling Effect

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Abstract: Given the problems that the phase-locked loop frequency coupling effect (PLL-FCE) in a weak grid reduces the quality of the output current waveform and brings challenges to maintaining a steady running of the grid-connected converter (GCC), this paper analyzes the coupling relationship between the FCE of the PLL, grid impedance and the output impedance of GCCs under a weak grid. It elucidates the role of the above coupling relationships in system stability and then proposes a stability optimization control method. Firstly, this paper delves into the frequency coupling phenomenon and its coupling mechanism in GCCs operating within weak grid conditions. Through analysis using small signal disturbance, it elucidates the significance of the PLL-FCE, particularly in medium- and low-frequency ranges, by establishing the coupling admittance model. Secondly, it presents the output impedance model for a three-phase LCL-type GCC, incorporating the characteristics of PLL frequency coupling. This model elucidates the interplay between the GCC's output impedance, the PLL-FCE and the grid impedance. It also unveils the impact of the PLL-FCE on system stability in weak grid scenarios. Building upon these insights, this paper proposes an enhanced PLL based on the Second-Order Generalized Integrator (SOGI). It provides a detailed parameter design process for implementing these improved PLL structures. Finally, the study conducts simulation and experiment verification under weak grid conditions. The findings indicate that the PLL-FCE indeed undermines the stability of GCCs in the weak grid, with this effect becoming more pronounced as the grid impedance increases. However, the implementation of the SOGI-PLL successfully mitigates the adverse impact of the PLL-FCE on the stability of the converter–weak grid interactive system, thereby enhancing the adaptability of GCCs to weak grid environments.

Keywords: frequency coupling effect; grid-connected converter; stability; grid impedance; SOGI-PLL

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1. Introduction

As renewable energy sources become more integrated into the power grid, maintaining power quality and system stability becomes increasingly challenging, especially in weak grid conditions. These challenges are expected to escalate further [1–4]. Phase-locked loops (PLLs) play a vital role in synchronizing renewable energy systems with grid voltage, making them pivotal for ensuring the stability of GCCs [5–8].

In numerous studies, the stability analysis of GCCs in weak grid conditions is often simplified to the system where a frequency disturbance results in a uniform frequency response [9]. However, this presumption is only valid for high-frequency ranges and does not accurately represent behavior in middle- and low-frequency ranges. Due to the asymmetrical control of the d and q axes within the PLL structure, the input of the PLL is solely the q -axis voltage. This asymmetry introduces frequency coupling into the control system of the GCC, as observed in several studies. Consequently, the GCC exhibits a single-input multiple-output characteristic, causing a frequency disturbance to produce different frequency responses. Neglecting the frequency coupling components of the

PLL, even when they are small, can result in inaccurate stability analysis outcomes for GCCs. Research indicates a positive correlation between the coupling component and the bandwidth of the PLL. Consequently, enhancing the bandwidth of the PLL can degrade system stability [10,11].

To solve the above problems, many scholars have proposed various solutions in recent years. In [12], the general form of the inner and outer loop admittance remodeling factors is constructed, and the admittance remodeling factor is properly selected. By reducing the admittance value of the converter, the quality of the grid-connected current is improved, and the purpose of eliminating the frequency coupling characteristics of the converter and suppressing the background harmonics of the power grid is achieved. Reference [13] introduces a single-input single-output (SISO) transfer function-based model to depict the interaction among control loops, facilitating analysis of the correlation between the proportional gain of the current controller and the instability induced by the PLL. Building upon this foundation, a collaborative design method for the PLL and current controller is presented. In [14], the frequency coupling caused by the asymmetry of the control parameters of the PLL control structure and the power outer loop is eliminated by adding a decoupling factor to the current inner loop and the power outer loop of the converter, so that the anti-angle element in the sequence admittance matrix of the converter is 0. Thus, the GCC system is simplified to a SISO system. Reference [15] proposes a method based on q -axis voltage feedforward to weaken the adverse effects of the PLL on system stability. Yet, this approach necessitates supplementary feedforward in the current loop, consequently augmenting the intricacy of the control algorithm. Reference [16] proposed an enhanced control scheme involving series lead phase correction to mitigate the effects of the PLL frequency coupling. In accordance with this method, modifications are required for the frequency coupling impedance form of the wind turbine. Reference [17] compensates the phase of the output impedance of the GCC by adding a phase correction link. However, this method requires an accurate oscillation frequency and exhibits poor robustness. In [18], a differential feedforward mechanism is introduced, incorporating the output current differential into the input voltage of the PLL. This approach effectively severs the coupling between the grid impedance and the PLL, especially in scenarios of weak grid conditions. Moreover, it maintains system stability even amidst fluctuating system parameters. However, it is worth noting that the differential component within the feedforward path may amplify high-frequency noise present in the current. This, in turn, can adversely impact the phase tracking accuracy of the PLL concerning the grid, particularly in severe instances. Reference [19] adds voltage feedforward to the d -axis control loop to offset the d -axis of the current controller. The research results show that the introduced d -axis voltage can suppress the asymmetry of the system. In [20], a constant low-coupling PLL structure is designed. The designed PLL does not affect the impedance of the GCC and can realize the decoupling between the PLL and the GCC control. In [21], a symmetric PLL control method is proposed to eliminate the FCE caused by the PLL by introducing the real phase angle and the imaginary phase angle. In addition, for the stability analysis and guarantee research of linear and nonlinear systems, some scholars have proposed some linear control methods. In [22], a novel adaptive interleaved reinforcement learning algorithm is developed so that the uniformly ultimately bounded stability of discrete-time affine nonlinear systems can be guaranteed. In [23], a robust asynchronous fuzzy predictive fault-tolerant tracking control method is proposed to ensure stable system operation. A fault-tolerant tracking control method with robustness is proposed for industrial production systems with uncertainty, set-point changes, external bounded disturbances and partial actuator failures. Reference [24] put forward a robust predictive fault-tolerant switching control method to predict robustness of a discrete linear system. And the above methods can provide some new ideas for enhancing stability of GCCs.

The aforementioned literature investigates the impact of PLL frequency coupling on the output characteristics of GCCs in weak grid scenarios, along with proposing optimal

control schemes. However, there remains a lack of clarity regarding the influence of the grid impedance on the output admittance/impedance of GCCs under PLL frequency coupling in weak grids. Furthermore, existing methods for enhancing the stable operating ability of the system primarily revolve around implementing phase/voltage compensation in control loops and parameter design based on stability region. It is therefore imperative to delve deeper into the relationship between the grid impedance and the output impedance of GCCs under PLL-FCEs, aiming to mitigate these effects and enhance system stability. This paper studies the influence of the PLL-FCE on the stability of GCCs and robust control methods in weak grids. The main contributions are as follows: (1) The coupling admittance model is developed to reveal how the PLL-FCE influences the output impedance and system stability across different frequency ranges; (2) The output impedance model for GCCs with PLL frequency coupling characteristics is established, providing a theoretical foundation for understanding low-frequency oscillation phenomena of GCCs in weak grids; (3) An analysis of the relationship between the PLL-FCE, grid impedance and output impedance of grid-connected inverters is conducted to offer design insights and a theoretical basis for enhancing inverter stability. The rest of the paper is organized as follows: In Section 2, the frequency coupling traits of the PLL are delved into via small signal voltage disturbance. In Section 3, the output impedance of the GCC under the frequency coupling characteristics is constructed. Additionally, how the FCE of the PLL impacts the stability of the GCC is scrutinized, particularly under weak grid conditions. In Section 4, a scheme for suppressing the FCE of the PLL and optimizing system stability is presented. In Section 5, a theoretical analysis and the efficacy of the optimization scheme are validated through simulation and experimentation. In Section 6, some conclusions are drawn.

2. Frequency Coupling Mechanism of PLL

The voltage disturbance signal Δu_p of ω_p is injected at PCC, and it is expressed as after the Clark and Park transformation:

$$\begin{cases} \begin{bmatrix} \Delta u_{p\alpha} \\ \Delta u_{p\beta} \end{bmatrix} = \Delta u_p \begin{bmatrix} \cos(\omega_p t + \varphi_p) \\ \sin(\omega_p t + \varphi_p) \end{bmatrix} \\ \Delta u_{pdq} = \Delta u_p e^{j(\omega_p - \omega_0)t} - jU_1 \Delta \theta \end{cases} \quad (1)$$

where ω_p , φ_p , Δu_p represent the frequency, initial phase and amplitude of the disturbance voltage Δu_p ; $\Delta u_{p\alpha, \beta}$, $\Delta u_{pd, q}$ are the expressions of Δu_p in the static and rotating coordinate systems; $\Delta \theta$ is the disturbance phase; and U_1 denotes the amplitude of the fundamental voltage at PCC.

The Synchronous Reference Frame PLL (SRF-PLL) realizes phase tracking by regulating the q -axis voltage at PCC, and it can be expressed as

$$\Delta u_{pq} = - \underbrace{0.5j(\Delta u_{pd} + j\Delta u_{pq})}_{\omega_p - \omega_0} + \underbrace{0.5j(\Delta u_{pd} - j\Delta u_{pq})}_{-(\omega_p - \omega_0)} \quad (2)$$

Thus, $\Delta \theta$ can be equivalent to the complex phase angles of positive and negative sequences [25]:

$$\Delta \theta = - \underbrace{0.5jT_{PLL}(\omega_p - \omega_0)\Delta u_p e^{j(\omega_p - \omega_0)t}}_{\Delta \theta_+} + \underbrace{0.5jT_{PLL}(\omega_0 - \omega_p)\Delta u_p e^{-j(\omega_p - \omega_0)t}}_{\Delta \theta_-} \quad (3)$$

For the expression of T_{PLL} , we can refer to [21].

Therefore, $\Delta u_{pd, q}$ in (1) is given as

$$\Delta u_{pdq} = \Delta u_{pdq, \omega_p - \omega_0}(t) + \Delta u_{pdq, \omega_0 - \omega_p}(t) \quad (4)$$

Then, (1), (3) and (4) can be obtained simultaneously:

$$\begin{cases} \Delta u_{pdq, \omega_p - \omega_0}(t) = [1 - 0.5U_1 T_{PLL}(\omega_p - \omega_0)] \Delta u_{p, \omega_p} e^{j(\omega_p - \omega_0)t} \\ \Delta u_{pdq, \omega_0 - \omega_p}(t) = 0.5U_1 T_{PLL}(\omega_p - \omega_0) \Delta u_{p, \omega_p}^* e^{j(\omega_0 - \omega_p)t} \end{cases} \quad (5)$$

According to (4) and (5), a small signal disturbance of frequency ω_p at PCC results in two frequency responses in the dq coordinate due to the asymmetry control of the PLL. These responses are namely $\omega_p - \omega_0$ and $\omega_0 - \omega_p$, leading to a coupling current of the $\omega_p - \omega_0$ frequency disturbance current and $\omega_0 - \omega_p$ frequency current in the grid-connected current. Upon applying the inverse Park transformation, these frequencies become ω_p and $2\omega_0 - \omega_p$. The above phenomenon is called the PLL-FCE, that is, owing to the asymmetry control of the PLL in weak grids, a single-frequency disturbance voltage will stimulate a multi-frequency current response. The frequency relationship of the voltage disturbance and the current response is shown in Figure 1.

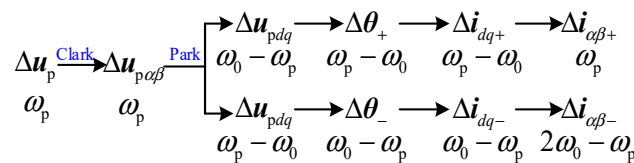


Figure 1. Frequency relationship of Δu_p and $\Delta i_{\alpha\beta}$.

3. Impact of PLL-FCE on the Output Impedance and Operating Characteristics of GCCs

3.1. Coupling Admittance Modeling

This paper introduces coupling admittance as a quantitative measure to assess the impact of PLL frequency coupling on the output impedance and operating characteristics of GCCs. Through the construction of a coupling admittance model, the paper analyzes how the PLL-FCE influences the output impedance and system stability.

In the context of an LCL filter, the primary function of a filter capacitor is to absorb the high-frequency component of the grid-connected current. However, it is noteworthy that the PLL-FCE predominantly influences the operating characteristics within the bandwidth of the PLL. Therefore, the LCL filter could be considered as an L-type filter during the coupling admittance modeling, and Figure 2 depicts the control system.

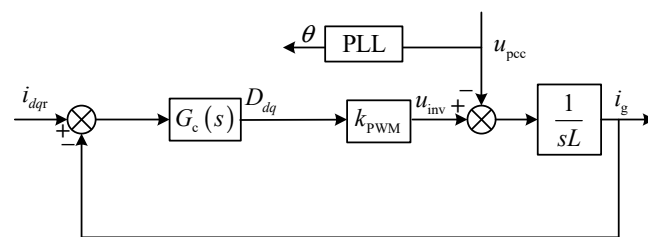


Figure 2. Control diagram of the LCL-type GCC.

In the above figure, i_{dqr} , i_g , D_{dq} , k_{PWM} , u_{inv} and $G_c(s)$ represent the current reference value, grid-connected current sampling value, duty cycle, PWM modulation coefficient, converter output voltage and current controller, respectively; L represents the sum of filter inductors L_1 and L_2 .

The small signal expression of the disturbance loop under the coupling current in stationary coordinates is

$$\mathbf{d}_{p, 2\omega_0 - \omega_p} k_{PWM} = (j2\omega_0 - s)L \cdot \mathbf{i}_{p, 2\omega_0 - \omega_p} \quad (6)$$

where $\mathbf{i}_{p, 2\omega_0 - \omega_p}$, $\mathbf{d}_{p, 2\omega_0 - \omega_p}$ denote the coupling current phasor and duty cycle phasor with $2\omega_0 - \omega_p$, respectively.

The small signal representation of the coupling loop under the coupling current in the rotating coordinate is as follows:

$$\mathbf{d}_{p,\omega_0-\omega_p} = -\mathbf{i}_{pdq,\omega_0-\omega_p} G_c(j\omega_0 - s) \quad (7)$$

The expressions of $\mathbf{i}_{pdq,\omega_0-\omega_p}$, $\mathbf{d}_{p,2\omega_0-\omega_p}$ are [26]

$$\begin{cases} \mathbf{i}_{pdq,\omega_0-\omega_p} = \mathbf{i}_{p,2\omega_0-\omega_p} + 0.5\mathbf{i}_{dq} T_{PLL}(j\omega_0 - s) \mathbf{u}_{p,\omega_p}^* \\ \mathbf{d}_{pdq,\omega_0-\omega_p} = \mathbf{d}_{p,2\omega_0-\omega_p} + 0.5\mathbf{d}_{dq} T_{PLL}(j\omega_0 - s) \mathbf{u}_{p,\omega_p}^* \end{cases} \quad (8)$$

where “*” denotes the conjugate component.

Combining the above, (6)–(8), we can obtain

$$\mathbf{d}_{p,2\omega_0-\omega_p}(s) = -G_c(j\omega_0 - s) \mathbf{i}_{p,\omega_p} - 0.5T_{PLL}(j\omega_0 - s) [\mathbf{i}_{dqr} G_c(j\omega_0 - s) + \mathbf{d}_{dq}] \mathbf{u}_{p,\omega_p}^* \quad (9)$$

Substituting (9) into (6) yields

$$Y_c(s) = -\frac{\mathbf{i}_{p,2\omega_0-\omega_p}}{\mathbf{u}_{p,\omega_p}^*} = \frac{0.5k_{PWM} T_{PLL}(j\omega_0 - s) [\mathbf{i}_{dqr} G_c(j\omega_0 - s) + \mathbf{d}_{dq}]}{(j2\omega_0 - s)L + k_{PWM} G_c(j\omega_0 - s)} \quad (10)$$

The coupling admittance amplitude $|Y_c(s)|$ reflects the coupling strength under PLL frequency coupling characteristics. It can also be seen from the numerator term of (10) that $Y_c(s)$ is positively correlated with $T_{PLL}(j\omega_0 - s)$, and it exerts a key influence on $Y_c(s)$. Since the PLL only impacts the operational characteristics of the converter during its bandwidth [17], we can deduce that the coupling admittance predominantly shapes the output impedance characteristics of the GCC within the medium- and low-frequency spectrum.

Similarly, we can derive the output admittance model of the GCC without accounting for the PLL-FCE:

$$Y_s(s) = -\frac{\mathbf{i}_{p,\omega_p}}{\mathbf{u}_{p,\omega_p}} = \frac{1 - 0.5k_{PWM} T_{PLL}(s - j\omega_0) [\mathbf{i}_{dqr} G_c(s - j\omega_0) + \mathbf{d}_{dq}]}{sL + k_{PWM} G_c(s - j\omega_0)} \quad (11)$$

The Bode diagram of $Y_c(s)$ and $Y_s(s)$ can be obtained from (10) and (11), and it is depicted in Figure 3. It is found that when the disturbance voltage frequency is $0 < f_p < 100$ Hz, the amplitude of $Y_c(s)$ is greater than that of $Y_s(s)$, indicating that the PLL-FCE plays a leading role. While $f_p > 100$ Hz, although the amplitude of $Y_s(s)$ is higher than that of $Y_c(s)$, the impact of $Y_c(s)$ is still not negligible in the range of 1000 Hz.

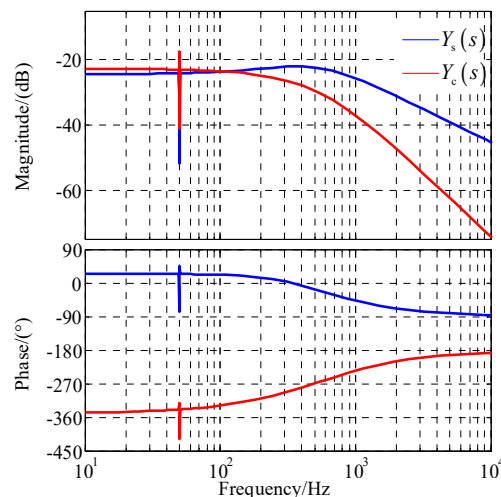


Figure 3. Bode diagrams of $Y_c(s)$ and $Y_s(s)$.

3.2. Output Impedance Modeling for GCCs under the PLL Frequency Coupling Characteristics

It has been deduced that the PLL-FCE introduces both disturbance and coupling loops in the converter–grid system. This coupling loop notably impacts the output characteristics, particularly in the low-frequency range. Consequently, an output impedance model that incorporates the coupling loop is formulated to elucidate how the PLL-FCE influences the stability of the GCC grid system.

The grid-side current i_s considering the PLL frequency coupling characteristics under small signal disturbance can be expressed as

$$i_s = i_{s,\omega_p} + i_{s,2\omega_0-\omega_p} \quad (12)$$

Considering the non-negligibility of grid impedance in weak grids, it is crucial to acknowledge that the PCC voltage comprises both the disturbance voltage component and the coupling voltage component:

$$u_{pcc} = u_{pcc,\omega_p} + u_{pcc,2\omega_0-\omega_p} \quad (13)$$

The relations among the disturbance voltage, current and the coupling voltage are derived in (14):

$$\begin{cases} u_{pcc,\omega_p} = u_{s,\omega_p} - i_{s,\omega_p} Z_{wg}(\omega_p) \\ u_{pcc,2\omega_0-\omega_p} = -i_{s,2\omega_0-\omega_p} Z_{wg}(2\omega_0 - \omega_p) \end{cases} \quad (14)$$

where Z_{wg} denotes the grid impedance in the weak grid.

By combining (12)–(14), the relationship among the disturbance voltage, the disturbance current and the coupling current is deduced in (15):

$$\begin{cases} i_{s,\omega_p} = Y_s(s) u_{pcc,\omega_p} + Y_c(j2\omega_0 - s) u_{pcc,2\omega_0-\omega_p}^* \\ i_{s,2\omega_0-\omega_p} = Y_s(j2\omega_0 - s) u_{pcc,2\omega_0-\omega_p} + Y_c(s) u_{pcc,\omega_p}^* \end{cases} \quad (15)$$

where u_{pcc,ω_p}^* , $u_{pcc,2\omega_0-\omega_p}^*$ represent the conjugate of the disturbance voltage and the coupling voltage, respectively.

The equivalent impedance model of the three-phase GCC considering the PLL-FCE can be obtained from (12)–(15):

$$Z_{FCE}(s) = \frac{1 + Z_{wg}^*(j2\omega_0 - s) Y_s^*(j2\omega_0 - s)}{Y_s(s) + Y_s(s) Z_{wg}^*(j2\omega_0 - s) Y_s^*(j2\omega_0 - s) - Y_c(j2\omega_0 - s) Y_c^*(s) Z_{wg}^*(j2\omega_0 - s)} \quad (16)$$

Comparing (11) and (16), it can be seen that $Z_{FCE}(s)$ and $Z_s(s)$ (corresponding to $1/Y_s(s)$) are equal and only related to the transfer function of the PLL, while the PLL-FCE is disregarded. The equivalent output impedance $Z_{FCE}(s)$ in the absence of taking into account the PLL-FCE is not only related to $Y_s(s)$ and $Y_c(s)$ but is also affected by grid impedance. The above phenomenon can be explained as follows.

The PLL-FCE results in the GCC having both a disturbance loop and a coupling loop when subjected to disturbance voltage. This, in turn, causes the grid-side current to be generated by two components: the effect of the disturbance voltage and the effect of the coupling voltage formed by the coupling current and the grid impedance Z_{wg} . Therefore, when modeling the impedance of the GCC, the grid impedance will be introduced.

3.3. Stability Analysis of GCCs under PLL Frequency Coupling Characteristics

According to (16), the Bode diagram of $Z_{FCE}(s)$ under various grid impedances is generated, depicted in Figure 4. It is found in Figure 4 that the presence of the PLL-FCE alters the amplitude of the GCC's output impedance, diminishes its phase in the medium- and low-frequency range and heightens the likelihood of instability. Furthermore, as the grid impedance Z_{wg} escalates, this effect exacerbates, intensifying the aforementioned phenomenon.

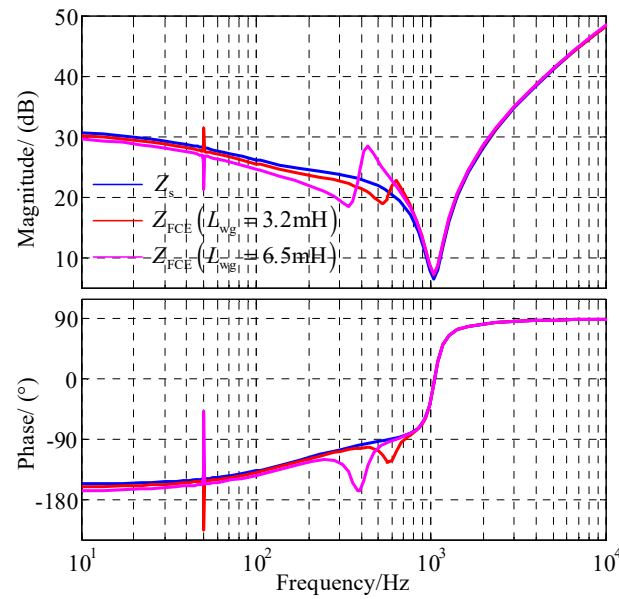


Figure 4. Bode diagrams of $Z_s(s)$, $Z_{FCE}(s)$ with different grid impedances.

To explore how the PLL-FCE influences the stability assessment, an analysis is conducted to compare the system's stability before and after accounting for this effect. The open-loop transfer functions of the system in both cases are $T_{op0}(s)$ and $T_{op}(s)$:

$$\begin{cases} T_{op0}(s) = Y_s(s)Z_{wg}(s) \\ T_{op}(s) = Y_{FCE}(s)Z_{wg}(s) \end{cases} \quad (17)$$

L_{wg} is taken as 3.2 mH and 6.5 mH, with corresponding SCR values of 9.5 and 4.5, respectively.

Figure 5 presents the Nyquist curves of $T_{op0}(s)$ and $T_{op}(s)$ when $L_{wg} = 3.2$ mH and 6.5 mH, respectively. It is evident that when not considering the PLL-FCE, the Nyquist curves of $T_{op0}(s)$ do not encircle $(-1, j0)$ for both $L_{wg} = 3.2$ mH and 6.5 mH, indicating stable operation of the GCC. However, upon considering the PLL-FCE, the Nyquist curve of $T_{op}(s)$ is not surrounded $(-1, j0)$ when $L_{wg} = 3.2$ mH. Yet, as L_{wg} progressively increases, in Figure 5b, it is observable that with $L_{wg} = 6.5$ mH, the Nyquist curve of $T_{op}(s)$ does enclose $(-1, j0)$, signaling instability in the GCC system.

To address the limitation of the Nyquist curves in directly conveying frequency and phase information regarding the unstable point of the GCC, Figure 6 illustrates the Bode diagrams of $Z_{wg}(s)$ and $Z_{FCE}(s)$ when $L_{wg} = 6.5$ mH. As depicted in Figure 6, taking into account the PLL-FCE, when $L_{wg} = 6.5$ mH, the phase angle margin δ_{PM} of the GCC at the intersection frequency f_{11} (552 Hz) is -1.2° . This indicates that harmonic oscillation will occur at f_{11} and its coupling frequency (452 Hz) in this case.

The analysis highlights the substantial impact of the PLL-FCE on the medium- and low-frequency characteristics of the GCC's equivalent output impedance. This effect results in the equivalent output impedance being affected by both $Y_c(s)$ and the grid impedance L_{wg} . Notably, an increase in L_{wg} intensifies its effect on the low-frequency characteristics of $Z_{FCE}(s)$. Neglecting to account for the PLL-FCE during stability analysis can lead to discrepancies in results for GCCs, thereby affecting parameter selection and operational stability. Consequently, mitigating the PLL-FCE becomes imperative to minimize its detrimental impact on the stability of the converter-grid system.

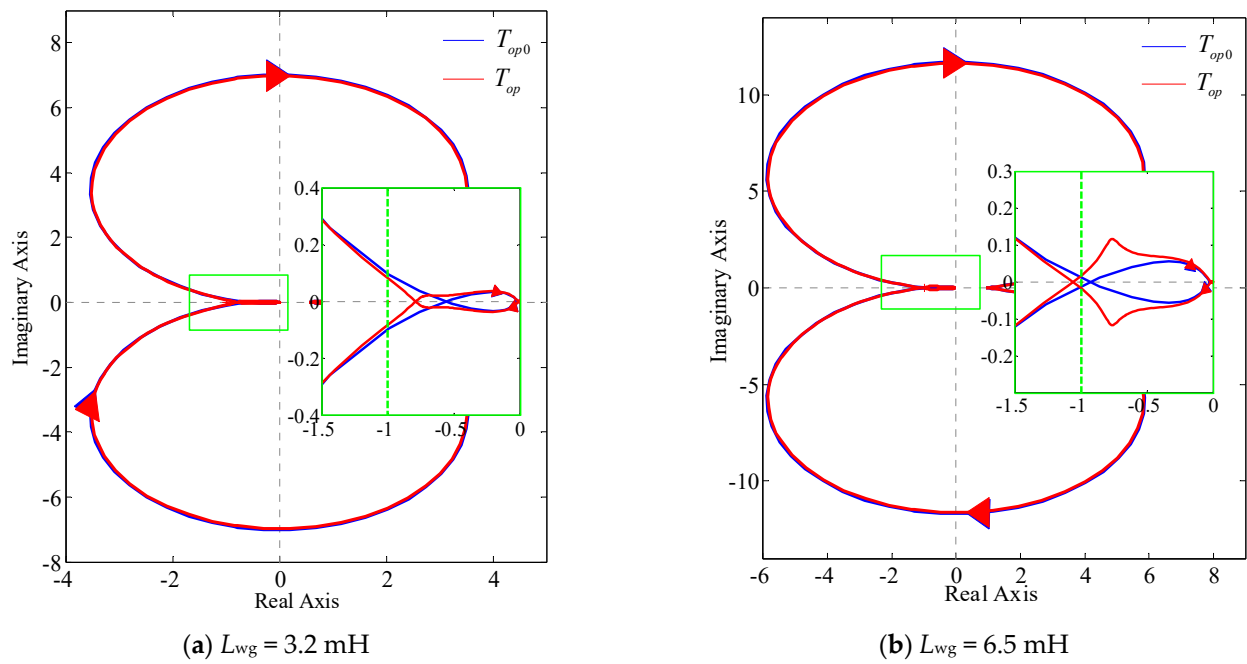


Figure 5. Nyquist curves of $T_{op0}(s)$ and $T_{op}(s)$.

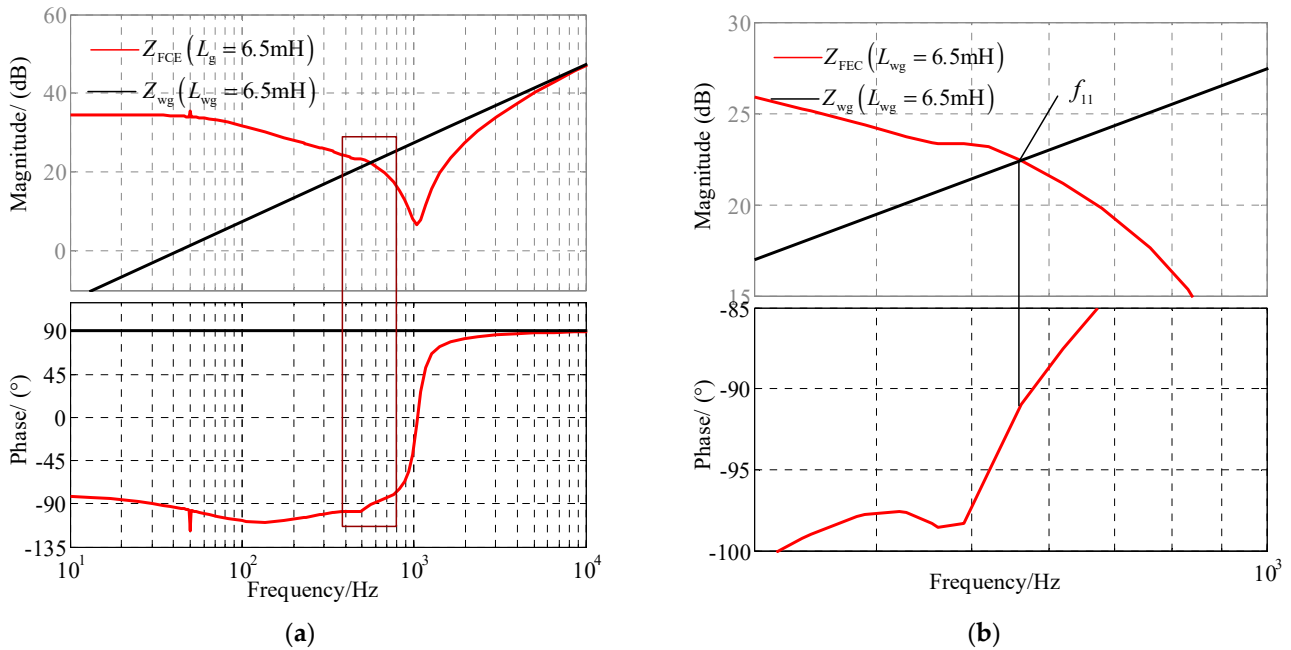


Figure 6. Bode diagrams of $Z_{wg}(s)$ and $Z_{FCE}(s)$ with $L_{wg} = 6.5 \text{ mH}$. (a) Bode diagrams of $Z_{wg}(s)$ and $Z_{FCE}(s)$ when $L_{wg} = 6.5 \text{ mH}$. (b) A zoomed-in portion of the Bode diagrams illustrating $Z_{wg}(s)$ and $Z_{FCE}(s)$ when $L_{wg} = 6.5 \text{ mH}$.

4. Strategy to Suppress the PLL-FCE

4.1. Second-Order Generalized Integral-Based PLL

Reference [27] has pointed out that embedding the second-order low-pass filter in the PLL can restrain the adverse impact of the PLL on the stable operation of the system. However, this method requires adding phase compensation.

The Orthogonal Signal Generator (OSG) in the Second-Order Generalized Integrator Phase-Locked Loop (SOGI-PLL) also has the harmonic attenuation function. Therefore, this section proposes to use the SOGI-PLL to inhibit the PLL coupling strength, thus improving the stability of the GCC grid system. Figure 7 depicts the structure of the SOGI-PLL.

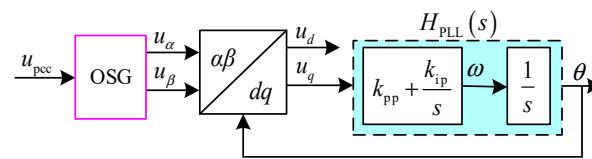


Figure 7. The structure of the SOGI-PLL.

In this above figure, the Orthogonal Signal Generator uses a Second-Order Generalized Integrator.

The structure of the OSG is illustrated in Figure 8. Here, k represents the bandwidth coefficient, and ω_1 denotes the resonant frequency of SOGI.

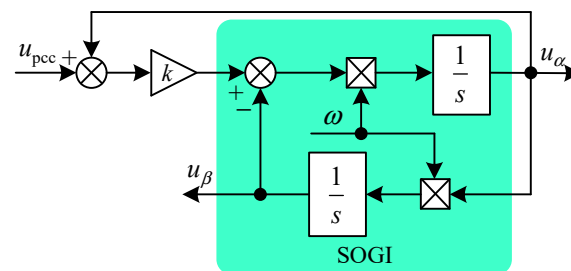


Figure 8. The schematic diagram of SOGI.

From Figure 8, we can derive the relationship between u_α and u_{pcc} :

$$u_\alpha = \frac{k\omega_1 s}{s^2 + k\omega_1 s + \omega_1^2} u_{pcc} = D(s)u_{pcc} \quad (18)$$

Therefore, the transfer function of SOGI-PLL is

$$T_{PLL_SOGI}(s) = \frac{H_{PLL}(s)}{1 + U_1 H_{PLL}(s)} \cdot \frac{k\omega_1 s}{s^2 + k\omega_1 s + \omega_1^2} \quad (19)$$

The parameters of the SOGI-PLL are designed as follows:

(1) Choose ω_1 .

The Bode diagram of $D(s)$ can be derived from Equation (18), and it is depicted in Figure 9. It is observed that $D(s)$ does not possess attenuation capability at ω_1 , but it exhibits good attenuation at frequencies other than ω_1 and does not exhibit phase deviation at ω_1 .

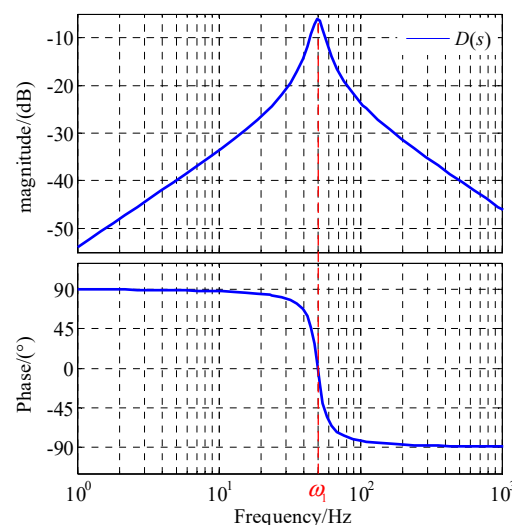


Figure 9. Bode diagram of $D(s)$.

Therefore, $\omega_1 = 100\pi$ is selected in this section. At this time, it can ensure that the signal at the fundamental frequency is not attenuated while avoiding the problem of phase lag/lead at the fundamental frequency caused by adding the OSG.

(2) Choose k .

The expression of $Z_{\text{SOGI}}(s)$ with SOGI-PLL in the mid- and low-frequency range can be approximately denoted as

$$Z_{\text{SOGI}}(s) \approx -\frac{1}{I_{\text{ref}} T_{\text{PLL_SOGI}}(s - j\omega_0)} \quad (20)$$

Then, the phase of $Z_{\text{SOGI}}(s)$ at 200 Hz is

$$\arg(Z_{\text{SOGI}}(j2\pi \cdot 200)) = 90^\circ + \arg(T_{\text{PLL}}(j2\pi \cdot 200)) - \arctan\left[\frac{400\pi k\omega_1}{\omega_1^2 + (j2\pi \cdot 200)^2}\right] \quad (21)$$

The phase margin δ_{PM} of $Z_{\text{SOGI}}(s)$ at 200 Hz can be expressed as

$$\delta_{\text{PM}} = 90^\circ + \arg(Z_{\text{SOGI}}(j2\pi \cdot 200)) \quad (22)$$

Consider a certain margin: take $\delta_{\text{PM}} = 20^\circ$. By solving (22), it is obtained that $k > 0$. As the parameter k decreases, the gain attenuation effect becomes more pronounced. However, excessively small values of k can lead to a reduction in the system's response speed. Taking these factors into account, k is chosen as 1.414.

4.2. Performance of SOGI-PLL

To assess the efficiency of the SOGI-PLL, the Nyquist curves of the open-loop transfer function of the system under various impedances are analyzed, and Figure 10 shows the Nyquist curves of $T_{\text{op}}(s)$ and $T_{\text{op1}}(s)$ when $L_{\text{wg}} = 6.5$ mH. Here, the expression of $T_{\text{op1}}(s)$ is

$$T_{\text{op1}}(s) = Y_{\text{SOGI}}(s)Z_{\text{g}}(s) \quad (23)$$

where Y_{SOGI} represents the output admittance while employing the SOGI-PLL.

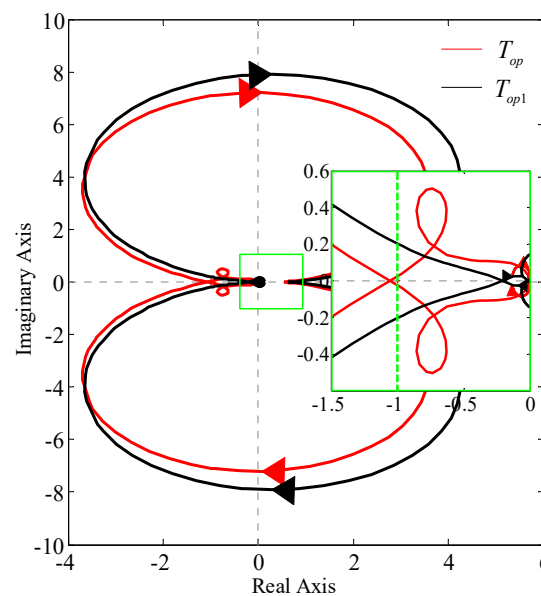


Figure 10. Nyquist curves of $T_{\text{op}}(s)$ and $T_{\text{op1}}(s)$ when $L_{\text{wg}} = 6.5$ mH.

Figure 10 indicates that when $L_{\text{wg}} = 6.5$ mH, the Nyquist curves of $T_{\text{op1}}(s)$ with SOGI-PLL do not encircle the point $(-1, j0)$. This observation suggests that the utilization of the SOGI-PLL can ameliorate the instability problem of GCCs arising from FCEs in conditions

of weak grids. This is due to the fact that the OSG in the SOGI-PLL constructs the voltage u_α and u_β in the $\alpha\beta$ coordinate system based on the PCC voltage input u_{pcc} . This has an impact on the PLL transfer function $T_{PLL}(s)$, leading to changes in the magnitude of the FCE, which subsequently alters the output impedance characteristics and stability of grid-connected inverters operating in weak grids.

5. Simulation and Experimentation Verification

To verify the accuracy of the theoretical analysis and the efficacy of the SOGI-PLL, simulation and experiment setups of the GCC were established, with detailed parameters outlined in Table 1.

Table 1. Parameters of three-phase GCC.

Parameter	Notation	Value/Unit
Capacity	S	4.0 kVA
DC source	V_{dc}	400 V
Inductance	L_{wg}	3.2/6.5 mH
PCC voltage	u_{pcc}	110 V

5.1. Simulation Results

Figure 11 depicts the simulation results for the voltage u_{pcc} and the output current i_g under a 20 Hz voltage disturbance at the PCC, with $L_{wg} = 3.2$ mH (where the GCC can maintain stable operation). It is notable to find that the grid current i_g demonstrates low-frequency oscillations.

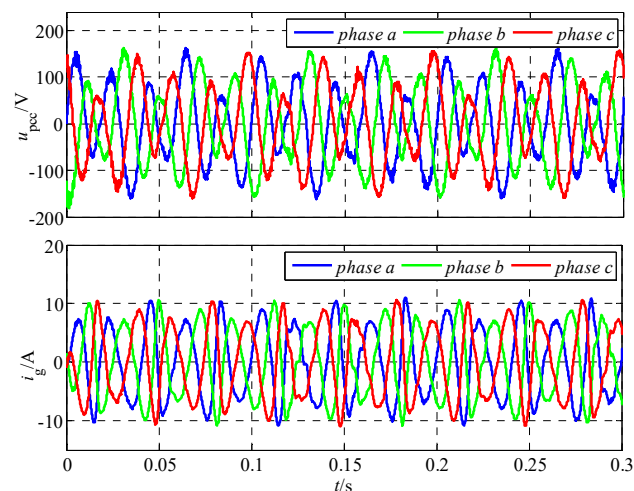


Figure 11. Simulation results for u_{pcc} and i_g under 20 Hz voltage perturbation with SRF-PLL ($L_{wg} = 3.2$ mH).

A Fourier spectrum analysis of the output current was conducted, and the outcomes of the harmonic spectrum analysis are presented in Figure 12. It is evident that the grid-side current spectrum content at 20 Hz and 80 Hz is high, indicating that a 20 Hz disturbance at PCC voltage results in a disturbance current at 20 Hz and a coupling current at 80 Hz. This finding underscores the significance of the PLL-FCE, which cannot be overlooked.

To elucidate the impact of PLL-FCEs on the stable operation of GCCs in weak grids, simulations were performed with two different grid impedances: $L_{wg} = 3.2$ mH and $L_{wg} = 6.5$ mH. Figure 13 illustrates the simulation results for u_{pcc} and i_g when $L_{wg} = 3.2$ mH and there is no voltage disturbance. It is found that the GCC demonstrates stable operation at $L_{wg} = 3.2$ mH, in line with the analytical conclusion depicted in Figure 5a. This coherence validates the accuracy of the theoretical analysis.

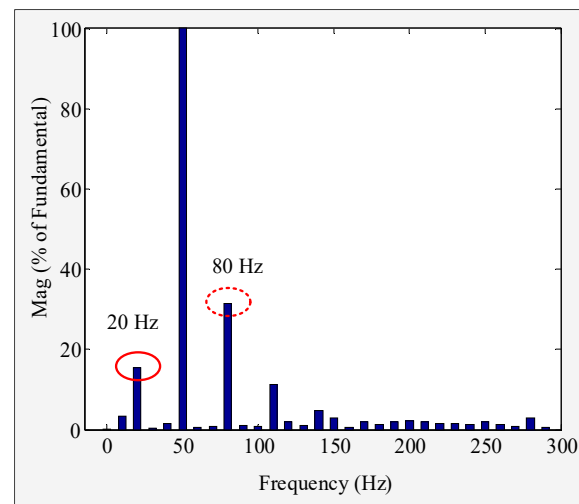


Figure 12. Frequency spectrum of i_g under 20 Hz voltage perturbation with SRF-PLL ($L_{wg} = 3.2$ mH).

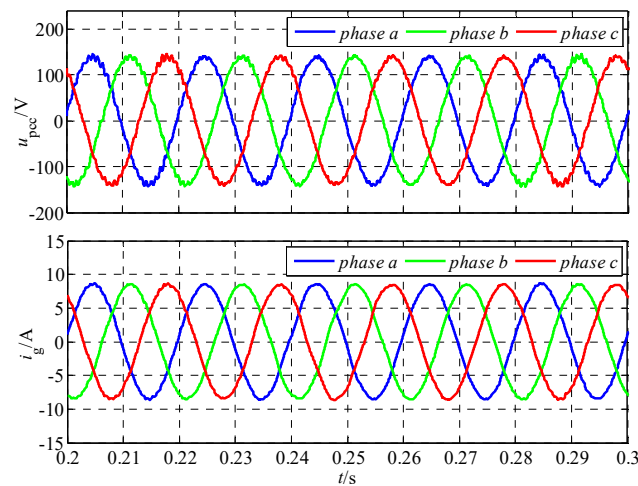


Figure 13. Simulation results for u_{pcc} and i_g employing SRF-PLL ($L_{wg} = 3.2$ mH).

By increasing the grid impedance to $L_{wg} = 6.5$ mH, the simulation results for u_{pcc} and i_g when $L_{wg} = 6.5$ mH using the traditional PLL are illustrated in Figure 14. It is evident from the results that at $L_{wg} = 6.5$ mH, the grid current displays significant low-frequency oscillations, indicating an unstable operating state of the GCC under this circumstance.

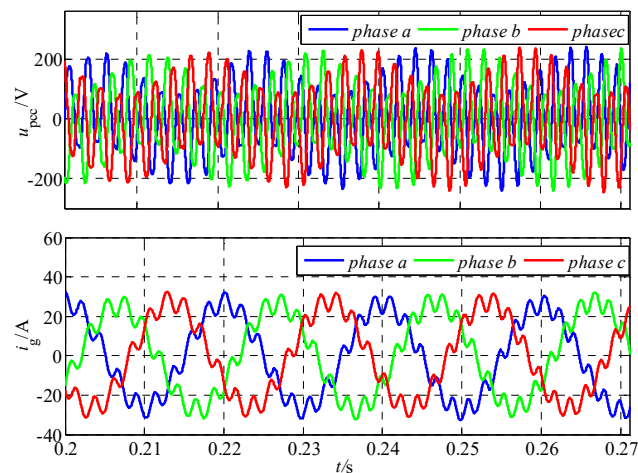


Figure 14. Simulation results for u_{pcc} and i_g using SRF-PLL ($L_{wg} = 6.5$ mH).

Figure 15 shows the FFT diagram of i_g when $L_{wg} = 6.5$ mH. It is notable from Figure 15 that the resonant points for the grid current primarily concentrate at 445 Hz and 545 Hz. Furthermore, 545 Hz closely aligns with the intersection frequency f_{11} in the Bode diagram depicted in Figure 9, while 445 Hz represents the coupled unstable frequency point of f_{11} . This indicates that under higher grid impedance, the PLL-FCE will diminish the stable operation ability of GCCs in weak grid circumstances, leading to simultaneous oscillations at both the resonant frequency and its coupled frequency. As a result, severe low-frequency oscillations are exhibited in the output current, and this phenomenon aligns with the theoretical investigation.

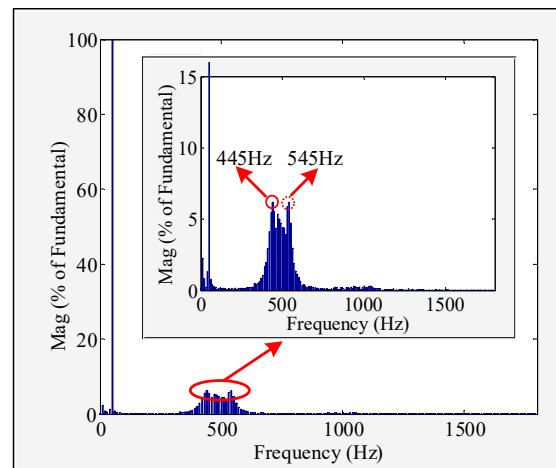


Figure 15. Harmonic spectrum of i_g employing SRF-PLL when $L_{wg} = 6.5$ mH.

To tackle this issue, a SOGI-PLL is designed in this paper. Figure 16 illustrates the transient simulation results for u_{pcc} and i_g employing the SOGI-PLL at $t = 0.3$ s with a grid impedance of $L_{wg} = 6.5$ mH. The stable operation of the GCC is evident, indicating that the SOGI-PLL can effectively mitigate the PLL-FCE, thereby enhancing the stability of three-phase GCCs under weak grid circumstance. This is because with the action of the OSG in the SOGI-PLL, the transfer function T_{PLL} , which characterizes the frequency coupling effect of the PLL, has a certain attenuation ability on harmonic voltage. The phase angle margin corresponding to the transition frequency of the impedance amplitude frequency curve gradually increases, and the stability of the grid-connected system gradually improves.

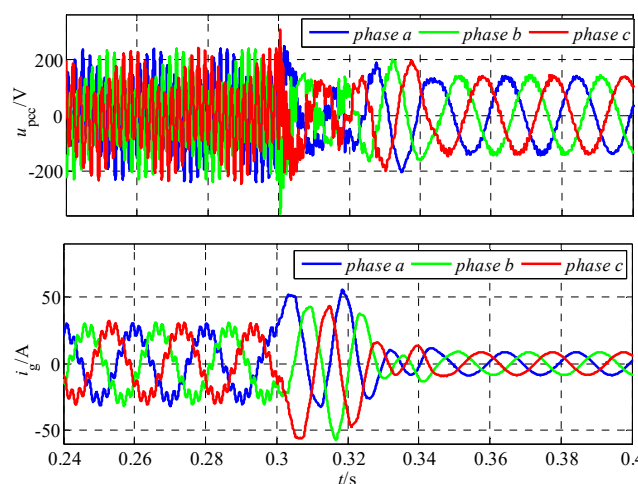


Figure 16. Transient results for u_{pcc} and i_g using the proposed SOGI-PLL ($L_{wg} = 6.5$ mH).

5.2. Experiment Results

To further confirm the negative impact of the PLL-FCE on the stability of the GCC–grid interactive system and the effectiveness of the designed PLL, a GCC hardware platform was constructed, as shown in Figure 17.

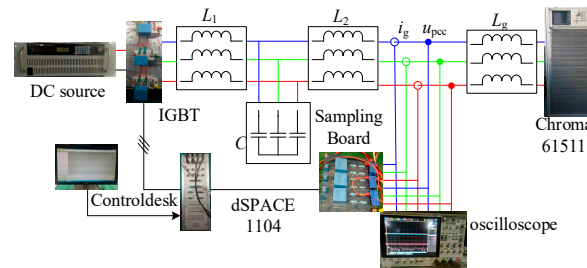


Figure 17. Experiment platform.

Figure 18 displays the experiment results for a -phase voltage at PCC u_{pcc_a} and the output current i_g when $L_{wg} = 3.2$ mH with a 20 Hz harmonic disturbance voltage, along with the Fourier spectrum of i_g . It can be observed that when a 20 Hz harmonic disturbance voltage is present in the grid voltage, the asymmetrical control of the PLL induces the FCE, resulting in low-frequency oscillations and distortion in i_g . During this scenario, the output current i_g encompasses both the 20 Hz disturbance current and the 80 Hz coupled current, with the latter being more pronounced than the former. This implies that under the conditions of a weak grid, the PLL-FCE introduces response currents at frequencies of ω_p and $2\omega_0 - \omega_p$ in the output current when a disturbance voltage with a frequency of ω_p is present. This experiment finding corroborates the simulation outcomes depicted in Figures 11 and 12, thereby reinforcing the accuracy of the theoretical investigation.

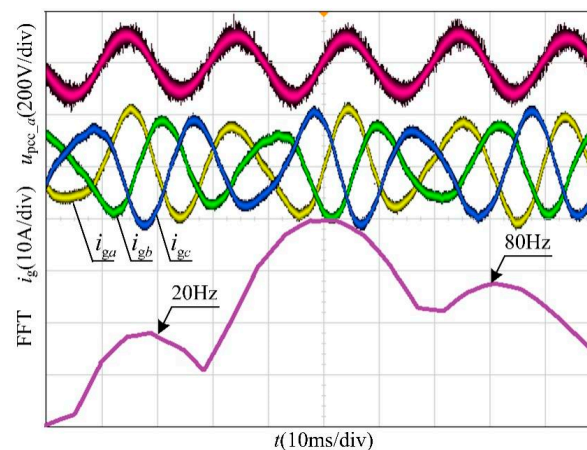


Figure 18. Experiment results for u_{pcc_a} , i_g and FFT of i_g under 20 Hz voltage perturbation with SRF–PLL when $L_{wg} = 3.2$ mH.

Figure 19 depicts the experiment results for the a -phase voltage at PCC u_{pcc_a} and i_g without voltage harmonic disturbances when utilizing the traditional PLL with a grid impedance of $L_{wg} = 3.2$ mH. It is evident from the observation that the GCC operates steadily in this condition, affirming that the traditional PLL could uphold the stability of GCCs when the grid impedance is relatively low.

With the grid impedance increased to $L_{wg} = 6.5$ mH, Figure 20 displays the experiment results for u_{pcc_a} and i_g when utilizing the traditional PLL. It is evident that the GCC with the traditional PLL experiences significant oscillations under these conditions.

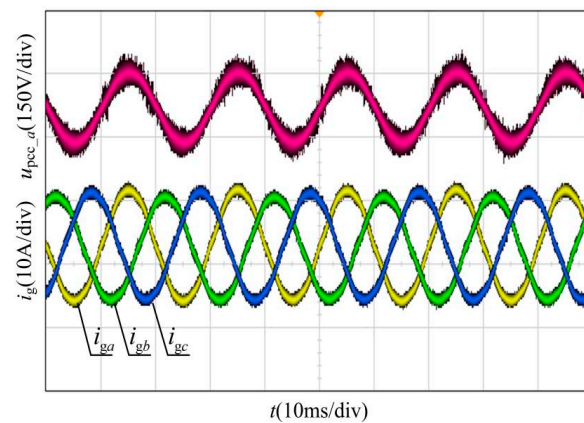


Figure 19. Experiment results for u_{pcc_a} and i_g utilizing SRF-PLL when $L_{wg} = 3.2$ mH.

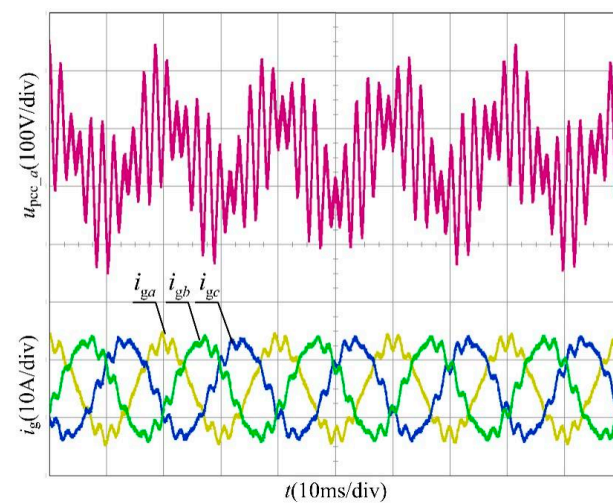


Figure 20. Experiment results for u_{pcc_a} and i_g utilizing SRF-PLL ($L_{wg} = 6.5$ mH).

A Fourier spectrum analysis of the output current was conducted, depicted in Figure 21. It is evident that the unstable frequency of i_g mainly concentrates at 445 Hz and 545 Hz, which aligns with the findings in Figures 6 and 15. This further affirms the accuracy of the theoretical investigation.

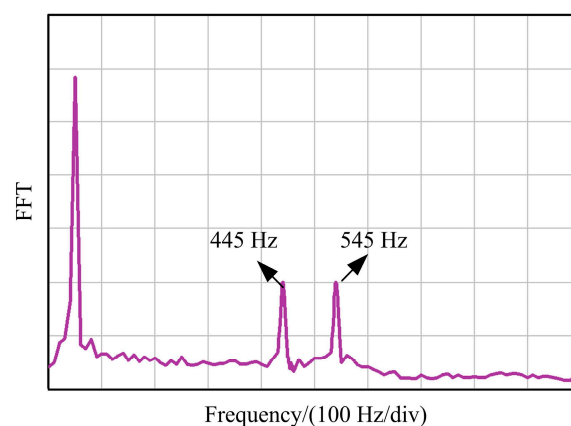


Figure 21. FFT of i_g utilizing SRF-PLL ($L_{wg} = 6.5$ mH).

This paper introduces the SOGI-PLL as a solution to mitigate the PLL-FCE, thereby enhancing the operation stability of GCCs under weak grid conditions. In Figure 22, the steady-state experiment results for u_{pcc_a} and i_g are depicted when employing the SOGI-

PLL with $L_{wg} = 6.5$ mH. It was found that the oscillations in the output current have been significantly mitigated when applying the SOGI-PLL, indicating its effectiveness in suppressing the PLL-FCE and ensuring the system operates stably.

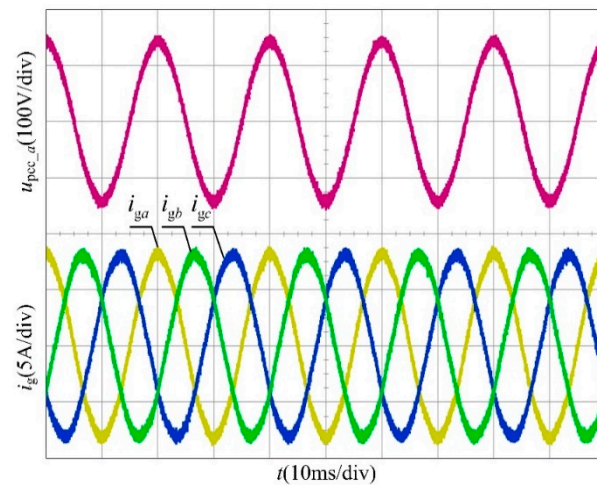


Figure 22. Experiment results for u_{pcc_a} and i_g applying SOGI-PLL with $L_{wg} = 6.5$ mH.

The above phenomenon in Figure 22 can be explained as follows: With the enhancement of the voltage harmonic filtering ability during OSG signal extraction, the stability of the grid-connected system under a weak current network is gradually improved, that is, the adverse effect of frequency coupling on the grid-connected system can be weakened by enhancing the filtering ability of the PLL pre-filter.

The analysis of the simulation and experiment results shows that the asymmetrical control of the PLL introduces FCEs, and it negatively impacts the quality of the output current waveform under voltage harmonic disturbances. As grid impedance increases, the FCE intensifies, causing issues with its interaction with both the grid and the output impedance of the GCC. This can endanger the stable operation of the converter under weak grid circumstances. The SOGI-PLL designed in this paper efficiently inhibits the FCE and reduces its impact on the output impedance of the GCC, thereby improving oscillations in the output current and ensuring stable running of GCCs even in the presence of high grid impedance.

6. Conclusions

The PLL-FCE induces significant distortion in the grid-connected current during PCC harmonic disturbances via coupling admittance. As the grid impedance rises, the ability of the GCC to run steadily diminishes, leading to low-frequency oscillations. This paper investigates the impact of the FCE on GCC stability by developing an output impedance model that incorporates PLL frequency coupling characteristics. Additionally, it presents an optimized control scheme to address these stability concerns. The following conclusions are drawn:

- (1) The analysis of the coupling admittance modeling reveals that the PLL-FCE significantly impacts the output impedance characteristics of the GCC, particularly in the range of medium and low frequency.
- (2) The impedance of the GCC is influenced not only by the coupling admittance but also by the grid impedance, particularly through the PLL-FCE. As the grid impedance increases, the coupling effect becomes more pronounced. The interplay between these factors shapes a negative impact on the overall performance and stability of the converter system and increases the risk of its instability.
- (3) The SOGI-PLL introduced in this paper serves to mitigate coupling admittance, thereby effectively suppressing the PLL-FCE. As the grid impedance escalates, this approach can ameliorate system instability stemming from PLL-FCEs.

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