

Article

Controller Hardware in the Loop Platform for Evaluating Current-Sharing and Hot-Swap in Microgrids

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Abstract: Microgrids have increased in popularity thanks to both the integration of renewable energy resources and their energy distribution capability for remote locations. Moreover, the microgrids, mainly using multiple generators connected in parallel, acquire additional advantages by using both Hot-Swap and Current-Sharing techniques. This paper presents the development of a Hardware in the Loop platform to test Current-Sharing algorithms. It is reinforced that the use of a real-time simulation based on Hardware in the Loop is a viable and cost-effective alternative in the validation of controllers. The platform was developed in a graphical programming environment (LabVIEW 2015) and implemented with NI MyRIO 1900 (National Instruments Corp., Austin, TX, USA) development boards for easier reproducibility. The entire code project is openly available and provided in this paper. A system of photovoltaic energy generators was used to evaluate the performance of the HIL platform. As a result, the platform was able to reproduce a similar behavior to the photovoltaic generator, presenting average mean errors of 0.4 V and 0.2 A in its voltage and current, respectively. Additionally, the platform showed its capability to test Current-Sharing algorithms in the occurrence of Hot-Swap events. This work contributes with a validation tool for energy management systems applied to microgrids.

Keywords: current-sharing; energy management system; Hardware in the Loop; hot-swap; microgrid; photovoltaics



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1. Introduction

In recent years, DC microgrids have increased in popularity as a plausible alternative to both generate and distribute energy in comparison to conventional energy systems. Among the multiple advantages of a DC microgrid (DC- μ G), one that stands out is its energy generation using renewable energy resources (RES). This opens the possibility of reducing the dependency on electrical centrals using fossil fuels, thus diminishing the negative impact on the environment. Between the employed RES in a DC- μ G, the use of photovoltaic panels (PV) as generators is very common due to both their financial and technical benefits [1,2]. A microgrid (μ G) is structured with five key elements interconnected in a common power bus: distributed generators, energy storage devices, an interconnection system with the AC main grid, loads, and a control unit [3]. The power electronic converters (PECs) play a key role inside a DC- μ G. The PECs add control and flexibility to the grid since they act as the main interface between the interconnected elements inside the DC- μ G and the distribution bus for the connected loads. Moreover, the DC microgrids (DC- μ Gs) can deliver successfully a power demand in a controlled and stable manner; therefore, they can be considered as an alternative power generation system for remote locations, data centers, and buildings [4].

The operation of a DC- μ G requires a hierarchical control based on two main control levels or layers, i.e., a local control (primary layer) and a global or supervisory control (secondary layer) [5,6]. On the one hand, the local control has the main purpose of regulating the distribution bus voltage; this level of control can be enhanced by including strategies such as Hot-Swap (HS) and Current-Sharing (CS) [7]. On the other hand, the supervisory control could integrate a set of secondary controls to minimize oscillations in the voltage bus, or a set of tertiary controls to handle a connection/disconnection to the AC main grid. Additionally, the supervisory control level can include an Energy Management System (EMS), which is expected to achieve ecological, economical, and calendrical goals [8,9]. As stated by the IEC 61970 norm, an EMS is defined as “a computer system comprising a software platform providing essential support services and a set of applications providing the functionality needed for the effective operation of electrical generation and transmission facilities to assure adequate security of energy supply at minimum cost” [10]. Assuredly, the EMS is responsible for guaranteeing a continuous energy supply in the DC- μ G. This becomes possible after managing the available energy in the grid among the generation resources, the storage devices, and the AC main grid. To assure an optimal operation of the DC- μ G, the EMS must maximize the usage of RES by exploiting their highest efficiency and reducing the energy losses. Following this optimal operation, the EMS can take account of the emitted greenhouse gases by the grid, too [11]. Based on these approaches for the supervisory level, the DC- μ G could have multiple state variants during its operation [12]. Consequently, an EMS must determine the optimal power produced by each generation source while it maintains the stability of the DC- μ G [13].

A DC- μ G can operate in two different modes: connected mode and islanded mode. In the first case, the DC- μ G interchanges energy with the AC main grid through a common coupling point. As this interchange is bidirectional, it is possible to maintain a DC bus regulated in cases such as an energy deficit or an energy surplus. In the islanded mode, the DC- μ G must maintain an energy balance between its components by the time that the AC main grid is not accessible. Here, the DC- μ G management defines as main goals to preserve a regulated setpoint in the DC voltage bus and to couple the energy demand based on the available energetic resources [14]. The islanded DC- μ Gs, whose RES include PV and wind turbines, present as the best alternative to satisfy the energy demand in remote locations. However, the unpredictability and variable nature of the RES reflects uncertainty during their operation; therefore, an adequate EMS becomes strictly necessary [15]. Above all, the design of EMS for DC- μ Gs operating in islanded mode (e.g., the development of electric vehicles and energy supply systems for remote locations) has found new challenges in the creation of new environment-friendly technologies. Consequently, the design of EMS for DC- μ Gs focuses on a wider addition of RES in the electrical systems in a safe, stable, reliable, robust, and coordinated manner [16].

Due to the number of elements composing a DC- μ G, as well as its operational configurations, an EMS must be validated before its implementation on the field. The real-time simulation based on Hardware in the Loop (HIL) appears as an affordable, viable, and commonly used technique to both designing and testing DC- μ Gs. This technique allows the developer to evaluate a wide variety of conditions during the operation of energy systems, the debugging and optimizing of controllers, and the viability analysis of electrical components connected to the system [17–20]. Thanks to its advantages, the HIL has been recently employed to validate control techniques in the elements forming a μ G, as presented by the following authors. First, in [21] is presented the validation of a controller for a μ G. Here, the μ G is formed by a diesel generator, a PV system, a battery-based storage system, and electric loads. The diesel generator is emulated and connected to the μ G with the Power HIL technique; the emulation employs a digital real-time simulator NovaCor from RTDS Technologies. Based on the close correlation between the Power HIL and its real counterpart, the authors conclude that the Power HIL provides flexibility in validation tests for controllers. In [22], a Current-Sharing Controller (CS-C) is proposed to limit the currents in a low-voltage DC- μ G that contains a set of PV generators connected in parallel. The

controller was validated with a real-time emulator Typhoon HIL 602, which reproduces the behavior of PV arrays, a battery-based storage system, Buck PECs, and the AC main grid. This work concludes that HIL simulations are useful to validate the effectiveness of CS strategies. Similarly, in [23] was employed the real-time emulator Typhoon HIL to simulate an AC- μ G with a 5 μ s latency. Here, the authors describe a validation of both centralized and decentralized frequency control schemes for an islanded mode operation. Finally, in [24] is described the conversion control of a wind turbine system and its validation with HIL. The wind turbine system is emulated with two Back-To-Back triphasic PECs, where one PEC emulates the grid side, while the other emulates the machine side.

Besides all the inherent advantages in the use of HIL, several commercial platforms are expensive and out of reach for some researchers. To tackle this problem, several proposals have been developed as low-cost alternatives. As an example, in [25] is presented the use of FPGAs to develop HIL simulations, where the analysis of the HIL development included both the numerical data types and the description method. In this work, it is concluded that the development of HIL simulations using a graphical language such as LabVIEW reduces the effort and time for its implementation. With an educative purpose, the authors in [26] present the development of a HIL platform using a dual-core digital signal processor TMS320F28379D (Texas Instruments Incorporated, Dallas, TX, USA) and an Atmega328P microcontroller (Microchip Technology Inc., Chandler, AZ, USA). To demonstrate the helpfulness of this platform, the authors emulate a Buck PEC and a two-container system. Finally, in [27] is described the implementation of a HIL using two DUE Arduino to simulate the control of dynamic systems. One of the Arduinos emulates a dynamic system while the other works as a DAQ and as a controller at the same time. This platform supports the emulation of dynamic systems such as an RLC circuit, a twin rotor MIMO system, and a microgrid.

Usually, a DC- μ G must count with a mechanism to monitor the energy demand on the grid while it has more than one generation system. This guarantees a proportional distribution of the energy demand. In fact, this mechanism can be included as part of the EMS and can be designed to cover the energy demand under diverse circumstances. This accomplishment becomes possible as the EMS considers the energy production capabilities by each generation system in the grid. On the one hand, the monitoring mechanism can intercommunicate globally all the generation systems. Consequently, the EMS also performs global actions to accomplish with the energy demand in the grid. On the other hand, the monitoring mechanism can be coupled to each generation system to be locally controlled. In this last approach, the generation systems do not depend on a direct communication with the EMS to establish an optimal power output [28]. Generally, a PV is directly connected to a power converter, whose joint action can produce a series of perturbances after being connected/disconnected to the DC bus in the grid. Therefore, it is recommended to implement an HS technique as part of the energy management in a DC- μ G that has at least two photovoltaic generators parallelly interconnected [29]. Additionally, the HS improves the DC- μ G operation by adding a redundancy in the PEC, which increments the reliability, adds up fault tolerance, increases the system's flexibility and robustness, and reduces the updating and maintaining times of the grid. Another common strategy for PECs connected in parallel is the CS. This strategy is focused on keeping all the converters contributing with an equitable fraction from the demanded current by the load, while the voltage in the DC bus is always maintained regulated [30]. To maintain equitable output currents from the PECs, the CS-C requires a communication channel between the PECs to monitor their available current [31]. Consequently, the equitable current demand from the PECs avoids a working overload, which results in a longer lifespan of their components, and the system maintains a stability thanks to a well-regulated DC bus. In the literature can be found some works where HS and CS strategies are employed. As an example, in [32] is presented a CS technique based on the injection of an AC signal to the DC bus and a controller. Here, the supplied energy from multiple PECs is regulated based on the induced reactive power by an AC signal. This system was evaluated in the face of HS connections.

Similarly, in [33] is proposed a secondary layer that operates based on a consensus scheme, which is applied for a Current-Sharing management for distributed generators connected in parallel; the scheme was validated in the face of HS connections also. In [34] is presented an adaptive droop control approach for CS and voltage regulation in DC- μ G applications. A virtual resistor is used to modify the reference voltage on each parallel converter; thus, the shared current error is reduced. The adaptive control approach was tested using a real-time simulator OPAL-RT OP4510, achieving a significative error reduction for different loading conditions. Similarly, in [35] is proposed a consensus algorithm based on a model predictive control for both CS and voltage regulation of a DC- μ G. The functionality of the controller was demonstrated with a DC- μ G that contained four distributed generators interconnected; the DC- μ G allowed for the configuration of the input constraints for each generator. Finally, a multi-bus DC- μ G with a novel control scheme is proposed in [36]. The novel scheme considers simultaneously both voltage regulation and CS for the grid. To evaluate the effectiveness of the novel scheme, the authors considered a grid with six distributed generators with six interconnected buses through transmission lines.

The aim of this work is to describe the development of a HIL platform to implement and validate CS algorithms. Particularly, the platform emulates three photovoltaic energy generator modules (PEGM) connected in parallel to a DC bus. Each PEGM was built with a 250 W PV, a DC/DC boost PEC with a PI controller for voltage control, a CS-C, and a switching device to produce an HS effect. In addition to having the PEGM, the DC- μ G includes an energy storage system and the interconnectivity with the AC main grid. The management of a DC- μ G requires that each of its elements has the capability to commute between different operating modes. For example, a photovoltaic generation system can switch from a Maximum Power Point Tracking (MPPT) mode to a voltage regulation mode in the DC bus, or vice versa. In this work, the proposed CS-C is analyzed assuming that the PEGM regulate the DC bus in the DC- μ G. Following this, the inclusion of both CS and HS techniques presents several advantages. Generally, it avoids either the overcharge or inactivity of any PV. Furthermore, it allows the modules to connect/disconnect to the DC bus without causing any disturbance. Finally, it keeps a regulated voltage in the face of load changes. The main objective of this research is to provide a platform which could be useful to validate a CS-C in the face of an HS and before being implemented in an EMS. Nevertheless, other operating modes of the PEGM, such as the MPPT, are still outside of the scope for this work.

To validate the HIL platform, an experiment was conducted under the following conditions: a variable working load and an HS connection/disconnection of the PEGM. As a result, the platform emulated the output voltage and the inductor current of the PEGM with mean absolute errors of 0.4 V and 0.2 A, respectively. No doubt, it was possible to conclude the usefulness of the platform to validate the CS-C.

Admittedly, a CS-C not only contributes with a satisfactory coupling of RES, but also enhances their performance. This enhanced performance is a consequence of a reliable, flexible, and robust CS controller. An additional effect of this enhancement can be seen with the reduction of perturbances in the DC bus. With a technological tool such as a HIL platform, the researcher will be able to identify and to correct failures of a CS algorithm, even before implementing it on the field. It is important to mention that this platform contributes to the development and evaluation of EMS for DC- μ G during an islanded mode, i.e., the voltage in the bus exclusively depends on the RES (e.g., a main AC grid shortage, or the absence of the main AC grid in remote locations). The islanded mode becomes a critical state for a DC- μ G as it must be reliable and offer resilience to the grid.

The HIL platform was built using the graphical programming language of LabVIEW and NI MyRIO 1900 (National Instruments Corp., Austin, TX, USA) boards. The selection of the programming language was made by considering two key ideas: first, the easiness to be reproduced, even by not-experienced researchers in embedded systems; second, to offer a more economical alternative in comparison to dedicated HIL platforms. The complete set of codes developed for this project is available for the reader to use.

The present work is ordered as follows: Section 2 presents the complete description of the system implemented under the HIL platform. Next, Section 3 shows the proposed methodology to implement the HIL platform. This is followed by the results of the experimental stage, which are presented in Section 4. Finally, Section 5 contains the conclusions and future work.

2. System Description

The complete HIL platform, with both the CS-C and the HS, contains three PEGM connected in parallel. The proposed system in this paper provides a DC- μ G with a power of 0.75 kW through a 190 V DC bus by using photovoltaic generation. The PV are placed in parallel in the DC- μ G; a resistive load is also connected to the grid. This configuration of the DC- μ G was used to evaluate both the CS and HS techniques, as well as the performance of the grid during an islanded mode operation. As a future work, it is proposed the addition of more elements such as a battery energy storage system, a wind turbine, and the interconnection with the main AC grid. The forthcoming actions related to the future work proposal is explained with detail in Section 5.

The proposed topology has a measuring line called Current-Sharing bus (CSB), where a voltage set point (v_s) was established. This set point is employed by an algorithm to manage the current distribution for the connected loads. All the elements of the system can be seen in Figure 1. To evaluate the CS-C under different conditions during an energy demand, a variable resistive load was connected to the DC grid. With this type of load, a starting point was established in the analysis of a DC- μ G using HIL; future analyses are expected to consider both inductive and capacitive loads. Additionally, the e_p switching devices of each PEGM allows a connection/disconnection to the DC grid to produce the desired HS effect.

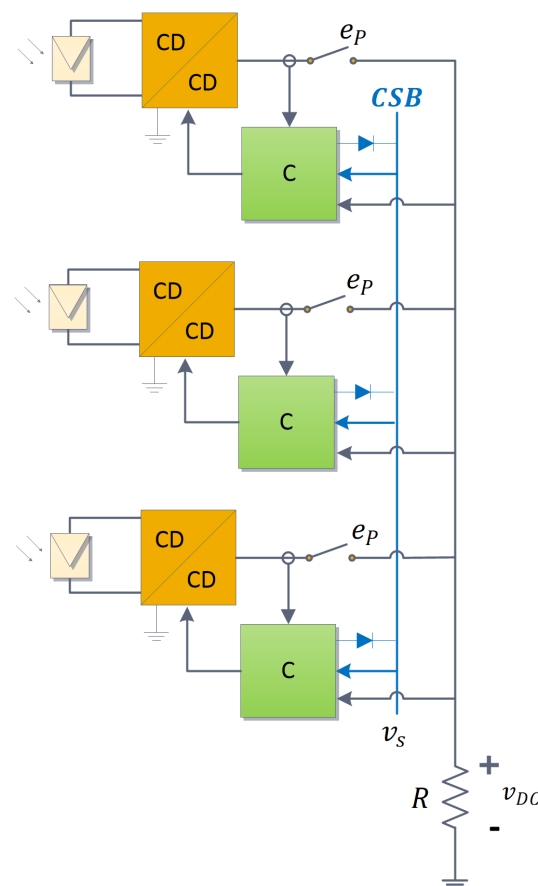


Figure 1. Developed system for CS-C validation.

As can be seen in Figure 1, each PEGM is composed by a PP, a boost DC/DC PEC, and a controller (represented by the green block C). This controller regulates the output voltage from the PEC and already includes a CS-C. The structure of the PEGM and its elements is showed in detail in Figure 2, whose description is made in the following paragraphs.

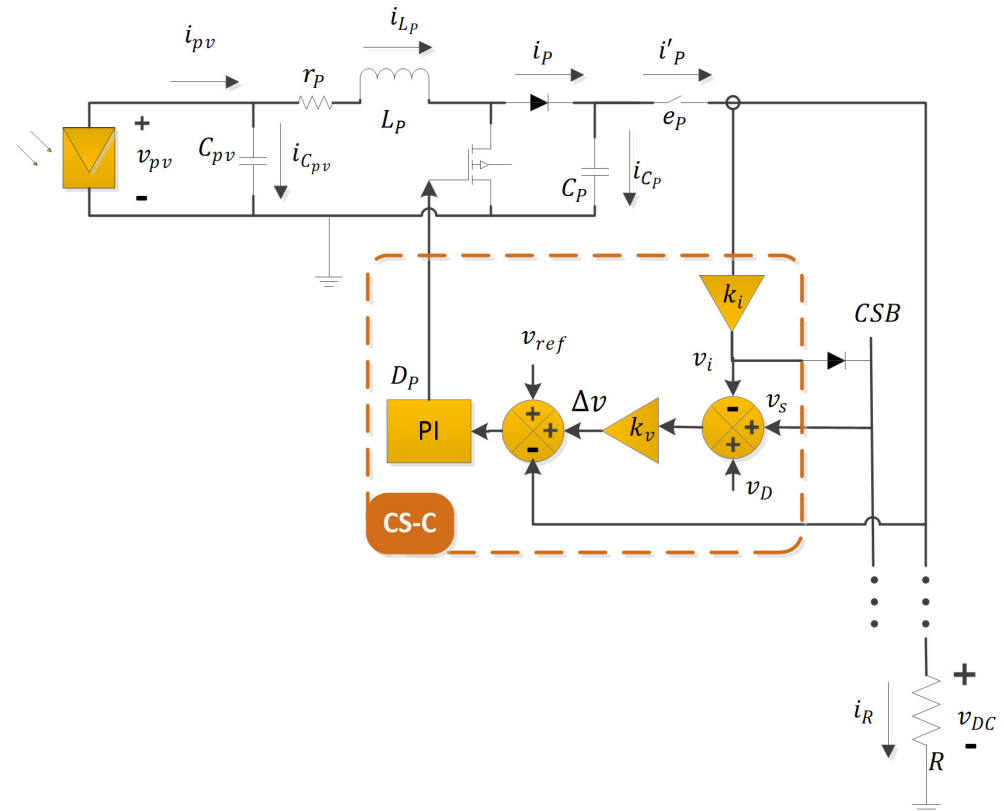


Figure 2. Photovoltaic Energy Generation Module (PEGM).

The PEGM was modeled based on a 250 W VIRTUS II PV (RENESOLA, Stamford, CT, USA). The main characteristics of this PV include a maximum power output (P_{max}) of 250 W, a maximum power voltage (V_{max}) of 30.1 V, a maximum power current (I_{max}) of 8.31 A, an open-circuit voltage (V_{OC}) of 37.4 V, and a short-circuit current (I_{SC}) of 8.83 A.

The boost PEC was designed as not isolated and to obtain the highest gain and efficiency from each PV [37]. Accordingly, the design parameters of the boost converter were defined as follows: an input voltage (V_{in}) of 30 V, an output voltage (V_{out}) of 190 V, a switching frequency (f_{sw}) of 130 kHz, and a power output (P_o) of 250 W. If the PEC receives an input voltage of 30 V to achieve a 190 V output, then it must operate with a gain of 6.33, maintaining a stability under a wide duty cycle condition [38]. Since the DC bus is considered as a large value capacitor with an inherent slow dynamic, the DC bus regulation is viable for this gain. Additionally, the converter was designed to work in a continuous conduction mode, therefore, the converter has a slow response.

The set of PEGM work collaboratively to achieve a voltage regulation in the DC bus. However, each PEGM locally regulates its outputs using a control for voltage regulation and a strategy to obtain a balanced output current. On the one hand, the voltage regulation from the boost converter is made with a PI controller set in a voltage control mode. In similar applications, it is common that the power electronic converters apply an inner loop for a current mode control. Particularly, this type of controller executes the control actions in the PEC on each commutation cycle of the power switching devices. However, the hardware employed for this HIL platform does not tolerate the development of high-switching-frequency models [39]. Then, it is not viable to implement an inner loop with the required latency. Conversely, it is possible to evaluate the proposed CS-C in this work

because it has an effect on the outer loop reference in voltage mode to achieve a balanced current distribution, and the voltage dynamics in the DC bus are relatively slower than the current dynamics on each PEC. The present analysis of the CS-C can be extended to similar controllers that have an effect over the outer loop voltage without considering the inner current mode control.

On the other hand, the CS-C monitors the injected current (i'_p) to the power bus, which through the gain k_i is converted to a voltage reference (v_i); v_i is transferred through a diode to CSB. As the diodes on each converter are connected to a common bus, the CSB voltage is defined as the maximum voltage v_i minus the voltage drop offset in the diode (v_D), i.e., $v_s = v_i|_{max} - v_D$. This v_s value acts as feedback for the CS-C to be compared versus the present voltage v_i on each module. Next, a voltage increment (Δv) is computed after multiplying the k_v gain by the voltage difference between the maximum voltage v_i and the output voltage v_i of each module. The value of Δv is then added to the PEC reference voltage (v_{ref}). In this way, if a module is supplying less energy than any other module, a positive disturbance ($\Delta v > 0$) is induced to the PEC ($\Delta v > 0$) and has the effect of demanding more energy from this module. On the contrary, when the module is supplying the grid with more energy than any other module, a negative disturbance ($\Delta v < 0$) is induced to the PEC, which is interpreted into a decreasing of the supplied energy by the module. As a result, a balanced energy demand from all the connected modules to the CSB and the power bus is achieved [40]. The CS algorithm is executed continuously on each CS-C. To ease the comprehension of the algorithm, its sequence is shown in the flow chart in Figure 3. Finally, the HS connection is produced by opening and closing the e_p switch.

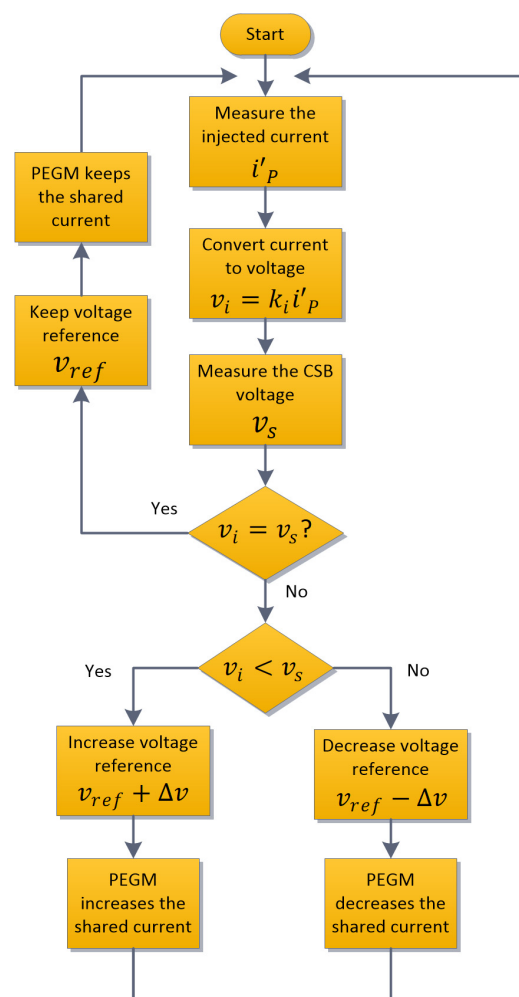


Figure 3. Current-Sharing algorithm flow diagram.

3. HIL Platform Description

Described here is the implemented methodology to both model and embed the elements that integrate the HIL platform described in the previous section.

3.1. System Modeling

A PV model was embedded using a 1024-value look-up table (LUT). These values were obtained from a Keysight E4360A (Keysight Technologies, Inc., Santa Rosa, CA, USA) emulator model; a similar approach is described in [41]. This emulator is widely used in research to substitute real PV [42–45]. The input parameters for this model are the open circuit voltage, the short circuit current, the maximum power point voltage, and the maximum power point current [46]; these values were defined based on the characteristics described in Section 2 for the 250 W VIRTUS II panel.

Similarly, to embed the DC/DC boost PEC, an average model was defined based on the circuit showed in Figure 2 [47] and deriving the discrete Equations (1)–(3). For these equations, T represents the integration period, $v_{pv}(k)$ is the voltage in the input capacitor (C_{pv}), $i_{L_P}(k)$ is the current in the L_P inductor, v_B is the voltage in the output capacitor (C_P), and $i_P(k-1)$ is the current passing through the diode. The HIL platform was implemented in a System on Chip (SoC) that includes a real-time processor (RTP) and an FPGA with a 40 MHz clock system. Particularly, these characteristics allow the device to be considered as a plausible option for developing high-latency applications with low cost; however, it is not viable to develop high-switching-frequency (>20 kHz) models due to the lack of an acceptable resolution [39]. Admittedly, this fact could be a disadvantage in comparison to dedicated HIL platforms. Nevertheless, the low cost of the hardware increases its reproducibility. For this reason, this work makes use of the average model of a converter instead of its commuted model.

$$v_{pv}(k) = v_{pv}(k-1) + \frac{T}{C_{pv}}i_{pv}(k-1) - \frac{T}{C_{pv}}i_{L_P}(k-1) \quad (1)$$

$$i_{L_P}(k) = \left(1 - \frac{r_P T}{L_P}\right)i_{L_P}(k-1) - \frac{(1-L_P)T}{L_P}v_{DC}(k-1) + \frac{T}{L_P}v_{pv}(k-1) \quad (2)$$

$$i_P(k-1) = (1-D_P)i_{L_P}(k-1) \quad (3)$$

Equation (1)–(3) describe the voltage dynamics $v_{pv}(k)$ in the input capacitor, the current $i_{L_P}(k)$ through the inductor, and the current $i_{L_P}(k)$ passing through the diode, respectively. As all the PECs are interconnected in parallel when their switches are closed, Equation (4) describes the voltage $v_{DC}(k)$ for the output capacitor, where $e_i C_i$ is the product of both the output capacitance (C_P) of each PEC and the switching state e_i of the PEC ($e_i = 0$ when the switch is open, $e_i = 1$ otherwise).

$$v_{DC}(k) = \frac{T}{\sum e_i C_i} \sum e_i i_i(k-1) + \left(1 - \frac{T}{R \sum e_i C_i}\right)v_{DC}(k-1) \quad (4)$$

The PI controller regulating the output voltage in the PEC was embedded based on its discrete model. The model is represented by Equation (5), where P is the proportional gain, I refers to the integral gain, $u(k)$ is the control signal, and $e(k)$ is the error signal computed after Equation (6).

$$u(k) = u(k-1) + Pe(k) + (TI - P)e(k-1) \quad (5)$$

$$e(k) = (v_{ref} - v_{DC}) + \Delta v \quad (6)$$

Finally, the CSB voltage was emulated using Equation (7), where v_s is the shared voltage in the bus, k_i is the gain for shared current algorithm, $\max(i_1, i_2, \dots, i_n)$ returns the

current with the highest value, and v_D represents the voltage drop offset in the diode that connects the amplified shared current and the shared bus.

$$v_s = k_i \max(i_1, i_2, \dots, i_n) - v_D \quad (7)$$

The values of the used constants from Equation (1)–(7) are shown in Table 1.

Table 1. Values of the constants included in Equations (1)–(7).

Constant	Value	Units
C_{pv}	330	μF
r_p	0.4	Ω
L_p	110	μH
T	28	μs
C_p	47	μF
P	0.004	--
I	1	--
k_i	6	V/A
k_v	2	--

3.2. Platform Implementation

To execute the evaluation of the proposed system in this work, it was necessary to embed the HIL platform, the set of PEGM, and the voltage dynamics entities of both the power and shared buses. For this purpose, it was required to use two development boards (DB) NI MyRIO 1900 (National Instruments Corp., Austin, TX, USA) These DB have a Xilinx Zynq-7010 SoC (Advanced Micro Devices, Inc., Santa Clara, CA, USA) that includes an RTP and an FPGA with a 40 MHz clock system. Particularly, this FPGA has 28 k logic cells, a 2.1 Mb RAM block, and 80 DSP slices. Under these conditions, each DB is restricted on the number of elements that can be emulated. Thus, the proposed HIL system was emulated with two DB (DB1 and DB2 in Figure 4). The communication between the RTP and the FPGA is through the ARM Advanced Microcontroller Bus Architecture (AMBA) standard. Additionally, the NI MyRIO 1900 (National Instruments Corp., Austin, TX, USA) board has 40 digital input/output (I/O) ports, 8 analog inputs, and 4 analog outputs. The analog inputs use an analog-to-digital converter (ADC) to quantify analog signals. On the contrary, a digital-to-analog converter (DAC) is used to decode digital signals for the analog outputs. Both the ADC and DAC have a 12-bit resolution. The Table 2 contains the main characteristics of the implemented DB for this work.

The connection of the embedded elements in the development boards DB1 and DB2 is shown in Figure 4, as well as the interconnection between the boards. As shown in Figure 4, the PV symbol represents the implemented LUT for a PV, which is connected to a DC/DC block. As it was previously mentioned, the response of the DC/DC block is based on Equations (1)–(3). Similarly, the C block works based on Equation (5) and the CS algorithm described in Section 2. Finally, the v_B and v_s blocks behave as described by Equation (4) and Equation (7), respectively. Additionally, a third development board (identified as DB3 in Figure 4) was required in order to perform signal acquisition during the evaluation tests. The signal acquisition was set to work with a 0.15 ms sampling rate and to maintain a sampling stage of 300 ms. During this stage, the acquired signals were recorded into FIFO registers. At the end of the sampling stage, the recorded data were transmitted to a PC through the RTP to be displayed and analyzed.

In the FPGA from the DB1 was embedded a PEGM (which contains a PP, a PEC with a controller, and the CS-C) and both blocks v_s and v_B . Conversely, the FPGA from the DB2 allocated the remaining PGEM, i.e., two additional PGEM. It is important to mention that the signals i_1 , i_2 , and i_3 correspond to the currents on each PEGM and are present as i_p in Equation (3). The values of the i_p currents, as well as the v_B and v_s voltages are shared between the boards by using the analog ports. In the case of the switching elements e_i , these are enabled/disabled with a set of digital signals, which are generated in the RTP

of DB1. The signal for the inner PEGM of DB1 is sent from the RTP to the FPGA directly, using the AMBA protocol. Correspondingly, the signals for the PEGM 2 and 3 are sent using the wired digital I/O pins between DB1 and DB2. The wiring of the development boards DB1 and DB2 as well as the implemented HIL platform can be seen in Figure 5.

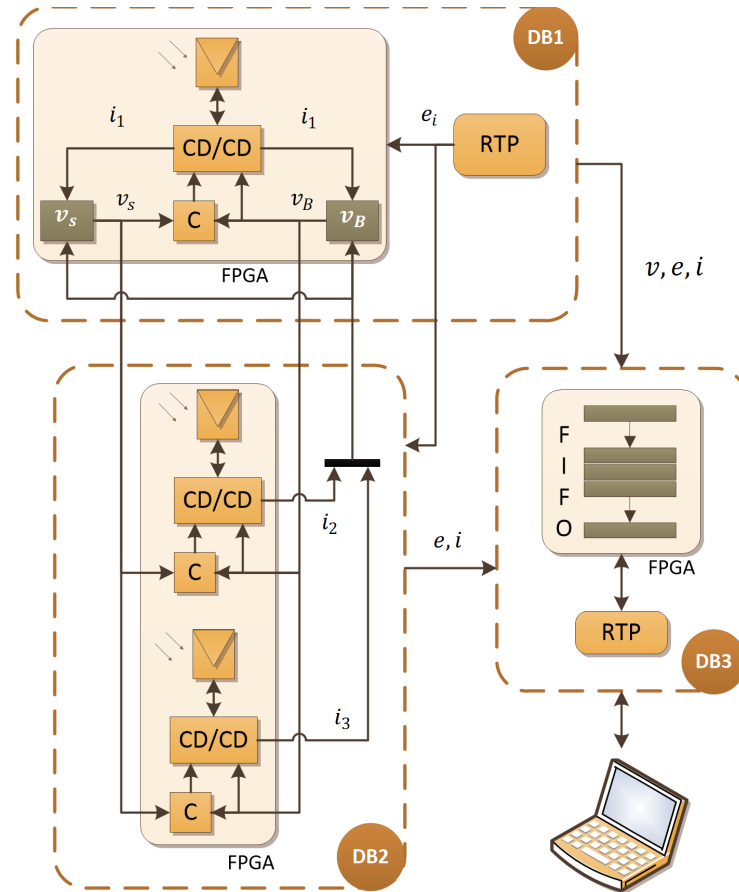


Figure 4. Implemented HIL system.

Table 2. Important parameters of the NI MyRIO DB.

Category	Parameter	Value
Processor	Type	Xilinx Z-7010 (SoC)
	Speed	667 MHz
	Cores	2
FPGA	Type	Xilinx Z-7010 (SoC)
	Clock frequency	40 MHz
	Logic cells	28 k
	DSP slices	80
	Block RAM	2.1 Mb
Analog Inputs	Sample rate	500 kS/s
	Resolution	12 bits
	Configuration	8 single-ended + 2 differentials
Analog Outputs	Update rate	345 kS/s
	Resolution	12 bits
Digital I/O	Configuration	Two 16 DIO lines ports + 8 DIO lines port
	Logic Level	5 V compatible LVTTTL input; 3.3 V LVTTTL output

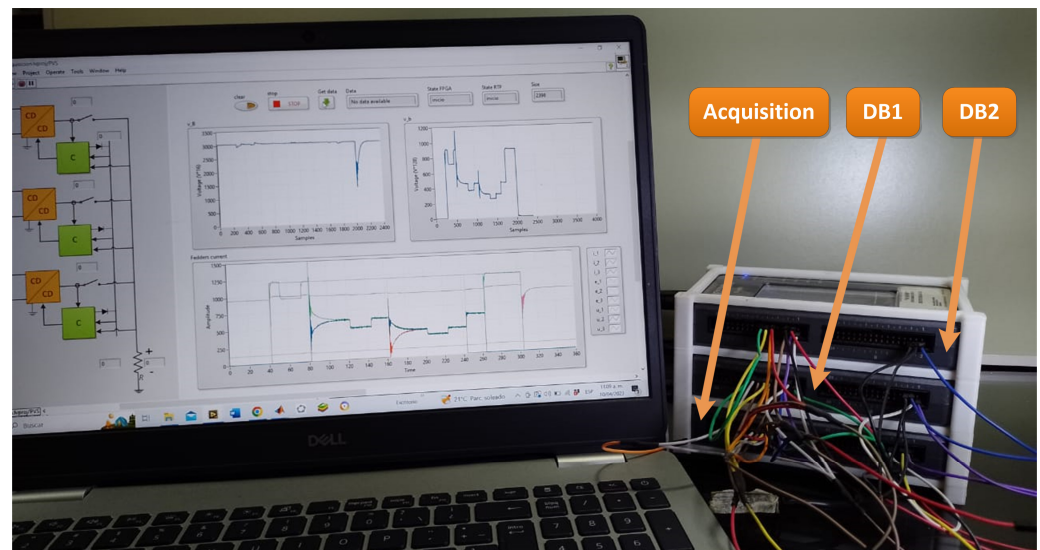


Figure 5. Implemented HIL platform.

To ease the reproduction of the HIL platform presented in this work, it was created with the development environment LabVIEW and high-performance blocks. Figure 6 shows the block diagrams developed to reproduce the PV and PEC models. These diagrams are an example of the algorithm developed for the HIL platform. The complete project and codes for the three DB are openly available in [48].

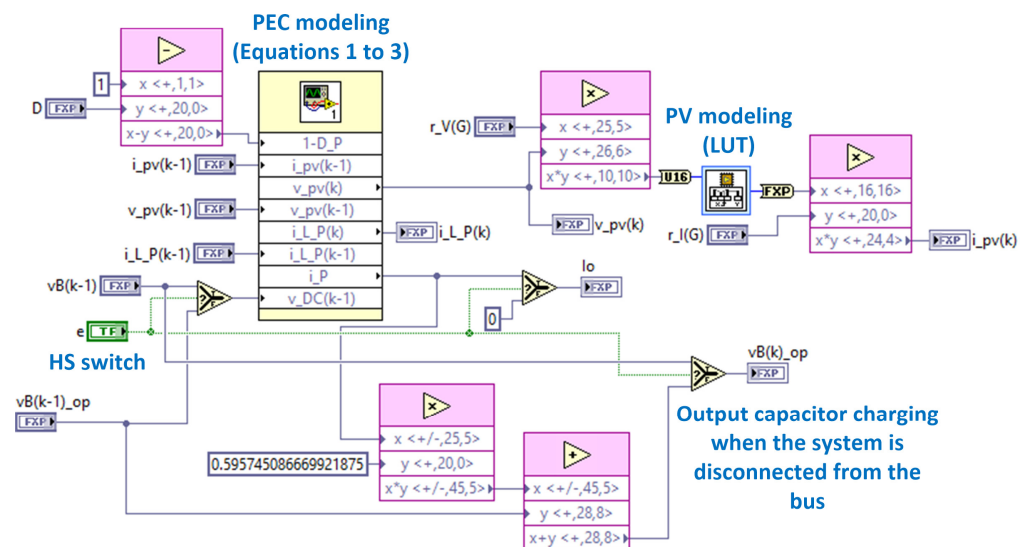


Figure 6. PV and PEC blocks developed in LabVIEW programming.

4. Results

The first step in the validation process for the HIL platform consisted in testing a PEGM individually. This test only took account of the PV, its PEC, and its PI controller without the Current-Sharing algorithm. Using MATLAB and Simulink (R2014a), a software simulation was developed for the continuous model of the PEGM, which was used to compare the accuracy of the HIL platform. Following this, the PEGM was turned on without any load and kept in this condition for 40 ms until the system achieved its stability. Next, a load was connected to demand 10% of the maximum power (25 W) from the PV for another 20 ms. Then, the load was changed to demand from the PV all its maximum power (250 W). For this test, the bus voltage and the inductor current were measured with a 0.15-ms sampling rate. A comparison of the bus voltage response between the PEGM emulation and the

PEGM simulation can be seen in Figure 7. Similarly, Figure 8 shows a comparison for the inductor current response. For both Figures 7 and 8, the letter a shows the response of the voltage bus (see Figure 7a) and the inductor current (see Figure 8a) during the whole test. The turn-on response for the bus voltage and the inductor current can be seen in the graphs labeled with the letter b in both Figures 7 and 8. Additionally, the response of the system under a 10% demand of the maximum power corresponds to letter c, where Figure 7c shows the bus voltage response and Figure 8c shows the inductor current response. Lastly, the demand of the maximum power from the PV (labeled as letter d) reflects the voltage bus response in Figure 7d, meanwhile Figure 8d shows the corresponding response for the inductor current. During the test, there were observed mean absolute errors of 0.4 V for the bus voltage and 0.2 A for the inductor current, whereas the maximum absolute error for these variables were 25.3 V and 19.3 A, respectively. Admittedly, these maximum absolute errors are present as oscillations at the beginning of the experiment while the system starts from its initial conditions. These oscillations can be an effect of the inner initialization algorithm in the simulation software. Since these variations in the results are large only during the beginning of the experiment, it is possible to consider them acceptable in the evaluation of the HIL platform performance.

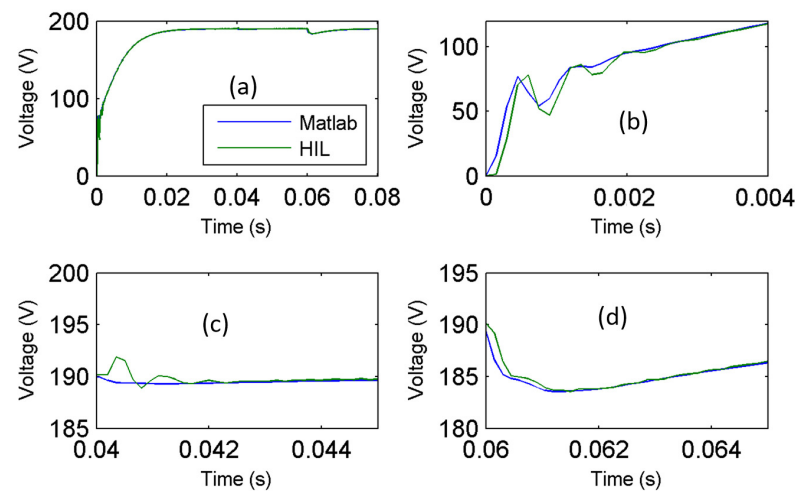


Figure 7. Response of the bus voltage for the individual PEGM test. (a) whole test response. (b) turn-on response. (c) 10% demand response. (d) maximum power demand response.

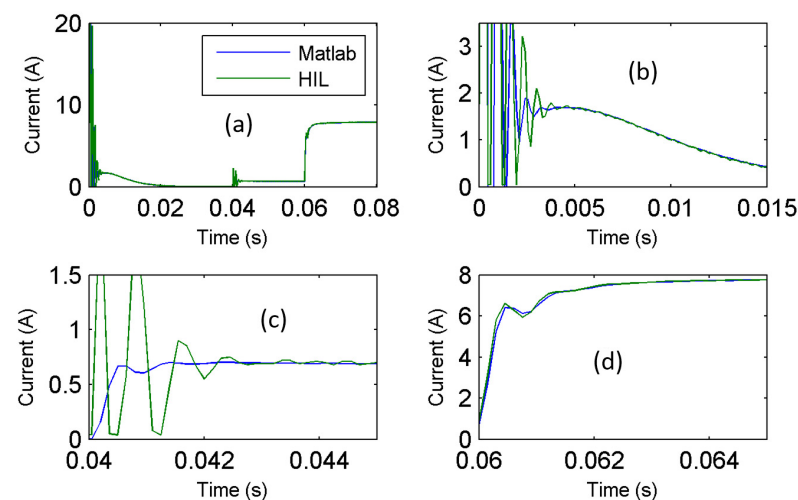


Figure 8. Response of the inductor current for the individual PEGM test. (a) whole test response. (b) turn-on response. (c) 10% demand response. (d) maximum power demand response.

Once the HIL platform demonstrated its capability to emulate a single PEGM, the next step was very clear: evaluate the functionality of the platform with the addition of a CS-C. For this test, first a PEGM was turned on (PEGM 1 connection stage); eventually, at $t = 40$ ms, a load was connected to demand the maximum power from the PV (Load connection stage), i.e., 250 W. Next, PEGM 2 was connected at $t = 80$ ms (PEGM 2 connection stage); PEGM 3 was connected (PEGM connection stage) after 80 ms, or $t = 160$ ms. During this test, the variation on the load considered three stages where the PV was required to work with 70% of the maximum power during 20 ms. The load was varied for the instants $t = 50$ ms (First load variation stage), $t = 120$ ms (Second load variation stage), and $t = 200$ ms (Third load variation stage). Each stage of the described test and the responses of both voltage and current are shown in Figures 9 and 10. On the one hand, Figure 9 shows the values of the three i_p currents present in the PEGM, the enabling of the e_p switches, and the bus voltage response scaled by a 0.007 factor. On the other hand, Figure 10 shows a detailed response of the bus voltage enclosed by two lines representing the steady state increased by +2% (green line) and decreased by −2% (blue line).

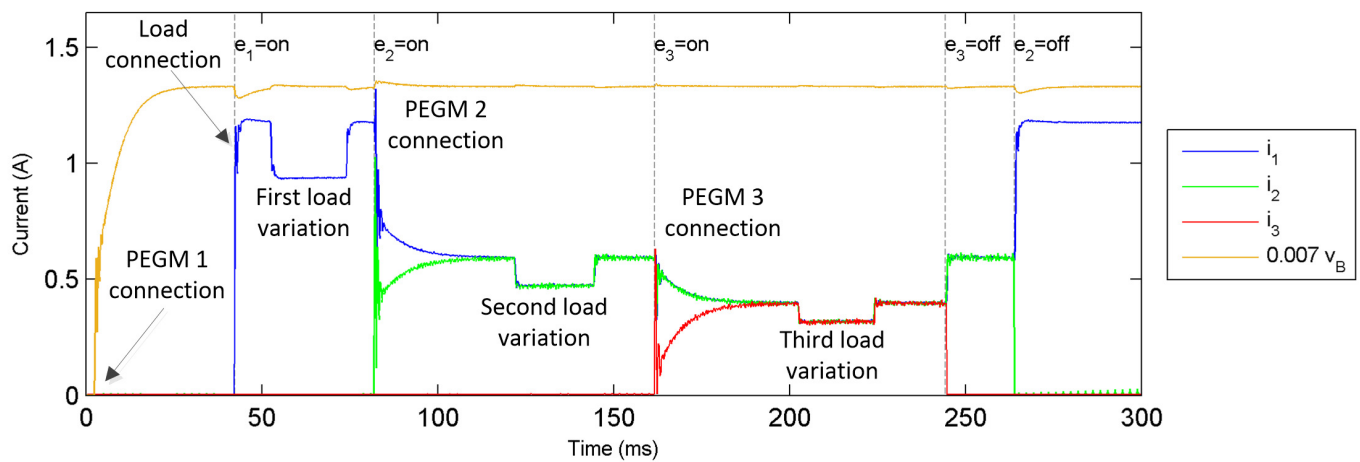


Figure 9. Response of the system during the test of Current-Sharing (CS) and Hot-Swap (HS).

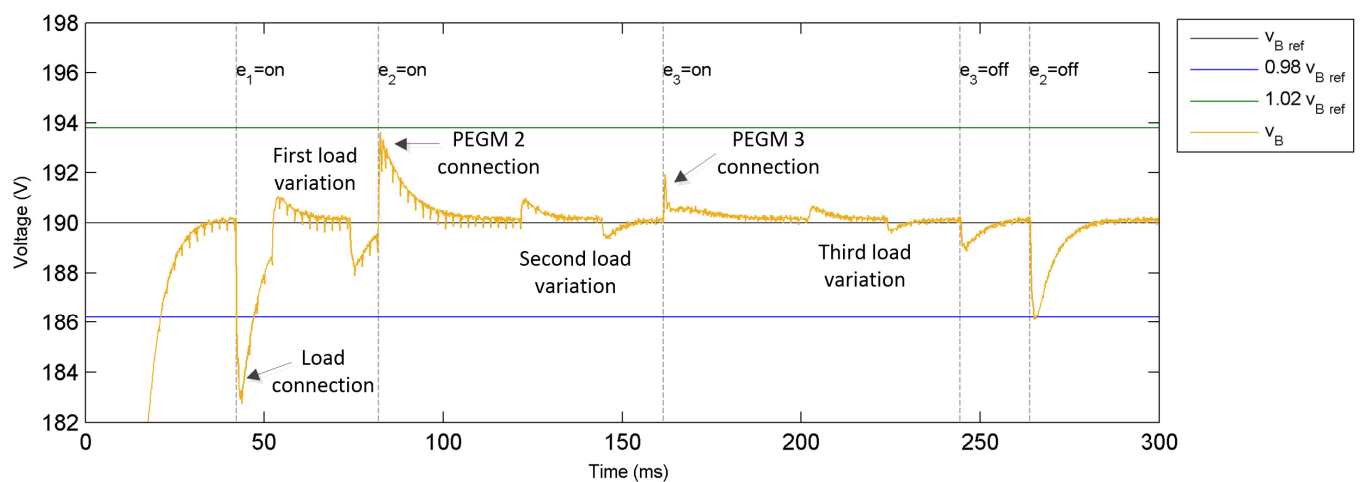


Figure 10. Detailed response of the bus voltage during the test of Current-Sharing (CS) and Hot-Swap (HS).

5. Conclusions

After comparing the response of the HIL platform versus the simulation of the continuous model, it was possible to demonstrate the accuracy of the HIL platform to reproduce the behavior of the selected PEGM for this work, where the mean absolute errors during the evaluation were 0.4 V for the bus voltage and 0.2 A for the inductor current. This accuracy

allows the asseveration that the developed HIL platform is reliable for the validation of a Current-Sharing algorithm. Therefore, it could be utilized as a tool in the validation of CS-Cs. In the long run, this type of controllers have a direct effect in the enhancement of the attributes of a DC- μ G, including its reliability, flexibility, robustness, and the reduction of disturbances.

Even though the objective of this work was to propose a HIL platform to validate any type of CS-C but not a specific CS-C, it was possible to conclude that the implemented controller was effective. This effectiveness was shown with an even distribution of the demanded current and a stable DC bus voltage. Considering a stability band criteria of 2%, it was appreciated with the aid of Figure 10 that the bus voltage maintained its stability under different conditions, e.g., during HS connections and load variations. After a load connection, a single variation above the 2% tolerance band was observed. Consequently, the DC bus suffered a 7.2 V decay, which represents a 3.8% decrease from its nominal value. In the case of low-voltage systems, the IEEE Std 1547-2018 [49] allows a distributed generator to induce a rapid voltage change when it is below 5% from the nominal value. Unquestionably, as the HIL platform had a 3.8% decrease from the nominal value, it accomplishes the standard and, consequently, it maintains the energy quality during the test. The evaluated CS-C in this work corresponds to a conventional droop control. Particularly, a disadvantage of this type of systems is that as the number of connected PEGM increases, the settling time of the system also increases. This is due to the decrease in the perturbation voltage Δv as the injected current by the PEGM decreases. The state of the art not only introduces some control schemes to solve this problem [32–36], but also offers the addition of functionalities for the CS-C such as the error reduction in the shared current [34], the input constraints setting in the available generation systems [35], and the energy interchange between multiple buses [36]. In a similar way, a low performance in the HIL system was observed due to the use of a single voltage loop for the PI controller in the PEC. However, thanks to the independency of each embedded module in the HIL platform (see Figures 4 and 6), it is possible to modify the implemented controllers separately without affecting any other system (e.g., the PV modules or the PEC). As a future work, it is proposed to employ the developed HIL platform here to evaluate and possibly improve different Current-Sharing algorithms.

The CS-C acts over the voltage reference defined for the local control in the PEC (v_{ref}) by either increasing or decreasing its value. These actions have the purpose of inducing changes in the power that is transferred to the DC bus. To extend the application of the HIL platform to different types of PV modules, or even PECs, it is only necessary to update the characteristics of the modules, or to tune the gains (i.e., k_i , k_v , P , and I) for the local controller. To update the characteristics of a PV module, it will be necessary to take from its datasheet the corresponding values to the open circuit voltage, the short circuit current, the maximum power point voltage, and the maximum power point current. Next, these values are introduced in a panel emulator, such as the Keysight E4360A (Keysight Technologies, Inc., Santa Rosa, CA, USA), to compute the V-I curve of the desired panel. With this V-I curve, a LUT is built and stored into the memory of a DB to emulate the PV module behavior. In essence, after the application of the updates in both the PV module and the CS-C gains, any user can obtain a new HIL system for its evaluation. No doubt, this represents an advantage of the proposed platform.

The HIL platform introduced here stands out in comparison to similar proposals as it offers excellent performance at a low cost. Additionally, as it uses a graphical programming language, the user can find an easiness in its reproducibility, development, and modification. To be sure, the performance of the developed HIL platform showed a respectable latency versus other low-cost alternatives such as Arduino. For example, presented in [27] is the use of an Arduino DUE to embed a dynamic system. However, this proposal has a lower latency because the board executes a software simulation at the end. On the contrary, by embedding a system in an FPGA, such as the NI MyRIO, the system is emulated in hardware, which results in a better latency. Similarly, presented in [26] is a system working with a software simulation

but running in a joint system of a DSP board with an Arduino. Although this system achieves high latency values during the software simulation by using parallel processing, the use of this type of processing requires an advanced C language developer to make use of threads, which can be found in mechanisms such as inter-processor communication. Finally, after comparing the emulation of power electronic converters in a NI MyRIO with LabVIEW versus other alternatives [25], the authors conclude that the duo does not present an adequate efficiency in terms of space and timing. However, it stands out as a powerful alternative in the aspects of design effort and design time.

In essence, the presented platform is useful to evaluate a CS algorithm in the face of HS for a set of PEGM connected in parallel. Then, it is viable to correct a controller designed to regulate a DC bus through renewable energy generators. This correction is necessary in the EMS operation for its application in a DC- μ G, as there is a great possibility that the grid depends completely on the RES to operate. However, this operation mode represents only one of the modes existing for a PEGM, so there are some future studies recommended to complement the findings of this work:

- First is to integrate the HIL platform in a DC- μ G that includes more elements of a distinct nature, e.g., a battery energy storage system, a wind turbine, a main grid interconnection, etc. An aspect contributing to this goal includes the validation of the HIL platform not only with a variable load, but also with a single equation describing both the DC bus dynamics and all the connected elements to it.
- Next is to validate the HIL platform in the face of variations of some other parameters such as the power supplied by the PV, shading of one or various panels, the sudden disconnection of loads from the grid, and the connection of R-L, R-C, and R-L-C loads. In a similar way to the previous goal, a single equation describing the DC bus dynamics and one that is independent from the PEC models will avoid an adjustment in the PEGM after modifying the characteristics and behavior of the connected loads to the bus.
- Lastly, with the inclusion of additional functions for the PEGM local controllers, e.g., an MPPT, it will be possible to evaluate more operative modes of a DC- μ G. As the weather variables have a slower time response, the MPPT demand a lower latency during an emulation than other elements such as the PECs contained in the PEGM. Therefore, this particularity allows the use of the RTP in the SoC to implement MPPT controllers without affecting the performance of other embedded systems.

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