

Article

Dead-Time Free Modulation Scheme for IM Drive System Fed by Voltage Source Inverter

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Abstract: During the modulation process of the VSI motor drive system, the nonlinear errors caused by the dead-time and conduction voltage drop will increase the phase current harmonic distortion and the torque ripple. To solve this problem, a novel dead-time free modulation scheme is proposed in this paper. In the non-zero crossing region of the phase current, the switching tube, whose body diode can provide a continuation path, is set as off-state, the driving signal is only implemented on another switching tube with the same bridge arm, and the errors caused by the conduction voltage drop and switching delay are compensated to the pulse duration. At the same time, to suppress the zero current clamp effect that exists near the zero crossing point of the phase current, another modulation scheme for the phase current crossing zero in advance is proposed, which avoids the complicated determination and calculation of the current polarity near the zero crossing point of the current. Both of the above modulation schemes eliminate the dead-time, and the switching principle is presented. In addition, to suppress the impact of the current ripple and high-frequency noise on the accuracy of the phase current detection, a second-order resonance digital filter without phase shift is introduced. Finally, compared to two deadtime compensation methods, the effectiveness and superiority of the proposed dead-time free modulation scheme are verified by the experimental results.

Keywords: voltage source inverter; deadtime; modulation; induction motor



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1. Introduction

Developing electric vehicles can slow down the pace of global climate change [1], reduce pollution, and effectively save energy [2]. Among numerous inverter topologies, the voltage source inverter (VSI) has fewer power devices, a simple structure, and mature and easy control technology, so it is the most commonly used drive topology in electric vehicles [3]. To prevent short-circuits occurring in the VSI bridge arm, the turn-on process of all switching tubes requires a delay, so the dead-time is formed, and both switching tubes of the upper and lower bridge arms are in the off-state [4]. The dead-time and conduction voltage drop lead to a nonlinear error in the VSI output voltage; especially for electric vehicle drive systems, the stator current harmonic distortion and torque ripple caused by the nonlinear voltage error cannot be ignored [5], because the electric vehicles will experience noticeable bumps and whistles [6]. For sensorless systems, the output voltage nonlinear error will reduce the accuracy of the flux and speed observers [7].

To solve the above problem, multiple nonlinear voltage compensation or suppression strategies have been proposed. Pulse time compensation is the most traditional and commonly used method for suppressing the nonlinear error, which converts the voltage error caused by the dead-time and conduction voltage drop based on the stator current polarity into a PWM pulse width within one switching period and compensates for it [8]. Reference [9] considers the influence of the snubber and parasitic capacitance in the pulse compensation, further improving the compensation accuracy. In [10], the average nonlinear

error of the three-phase voltage for each switching cycle is converted to the stationary coordinate system, then the voltage error is compensated in the voltage reference. Reference [11] considers the nonlinear voltage error of the inverter as the disturbance and decomposes it into voltage errors caused by dead-time under the snubber capacitance and voltage errors caused by the conduction voltage drop. Meanwhile, the corresponding feedforward compensation calculation methods are proposed for two types of voltage errors. An improved trapezoidal voltage compensation method is proposed in [12]; except for the trapezoidal angle, the amplitude of the trapezoidal voltage is also controlled, which can significantly improve the compensation performance. However, the above methods all belong to the offline compensation and can only correct the fundamental amplitude, but the harmonic suppression effect is not obvious. Reference [13] analyzes the harmonics caused by the dead-time and conduction voltage drop, it mainly contains fifth and seventh components, so the fifth and seventh harmonics of the phase current are mapped into the DC component, and then four PI controllers are adopted to obtain the compensation in the d - q coordinate system, but the compensation algorithm is too complex, and multiple PI parameters are needed to be tuned. After the Park transformation, the harmonics are mapped to sixth order in the d - q coordinate system, and then a parallel connection control structure between the proportional resonance (PR) controller and the current PI controller is proposed in [14]. Although the PR controller can suppress the fifth and seventh harmonics in the phase current, the dynamic response of the vector control system is affected. References [15,16] regard the voltage error caused by the dead-time as a voltage disturbance and use a disturbance observer to compensate for the dead-time. A compensation strategy based on an extended state observer (ESO) is proposed in [15]. To solve the frequency adaptation issue, a discrete multifrequency disturbance observer is proposed in [16]. A dead-time control scheme for bidirectional inductive power transfer converters is proposed in [17]. To minimize the loss and guarantee the zero-voltage switching of MOSFETs, the turn-on delay, turn-off delay, and the discharge time offline are measured and stored in the microcontroller. Then, using a lookup table, the optimal minimum deadtime is obtained based on the turn-off current and DC voltage levels, and the dynamic optimal minimum deadtime control scheme can be realized. However, this method is only suitable for applications of zero-voltage switching, and offline measurement of MOSFET switching characteristics can also be cumbersome.

The above method cannot completely eliminate the influence of the dead-time, especially at high speeds, because the frequency of the voltage disturbance caused by the dead-time is very high and difficult to observe. In this paper, a novel dead-time-free modulation scheme is proposed; according to the analysis of the phase current flow path under different polarities, the switching tube, whose body diode can provide a continuation path, can be set as off-state, so the driving signal is only implemented on another switching tube with the same bridge arm. Since there is only one switching tube in the action state in one leg, the dead-time is not needed. However, due to the zero current clamp effect, the proposed modulation scheme cannot be applied near the zero crossing point of phase current [18], and the switching state remains the maximum voltage output that can make the current cross zero point in advance. Meanwhile, since the proposed dead-time free modulation requires extremely high accuracy in phase current detection, a high-precision digital filter is designed to eliminate the influence of the high-frequency ripple and sampling noise. This paper is organized as follows:

The nonlinear voltage error caused by the dead-time and conduction voltage drop, and the zero current clamp effect near the zero crossing point of the phase current are analyzed in Section 2. The dead-time free modulation strategy in the non-zero crossing region is proposed in Section 3, and the modulation scheme for the phase current crossing zero in advance is proposed in Section 4. On this basis, the principle for switching the two proposed modulation schemes is presented in Section 5. To improve the accuracy of the phase current detection, a second-order bandpass digital filter without phase shift is presented in Section 6. Finally, the performance of the proposed dead-time free modulation

strategy for VSI is verified by the experimental results in Section 7 and compared with other dead-time compensation methods.

2. Nonlinear Voltage Error Analysis of VSI

This paper takes the induction motor (IM) drive system fed by VSI as the research object; the topology is shown in Figure 1. Next, taking a phase-A bridge arm as an example, the nonlinear voltage error caused by the dead-time and conduction voltage drop and the zero current clamp effect near the zero crossing point of phase current are analyzed, respectively.

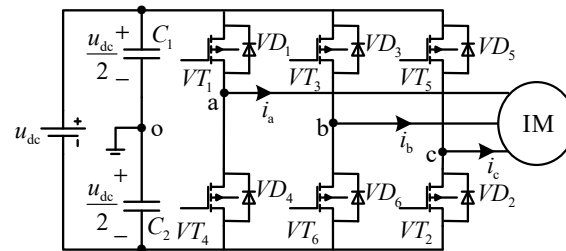


Figure 1. Topology of the induction motor drive system fed by VSI.

2.1. Nonlinear Voltage Error Caused by the Dead-Time and Conduction Voltage Drop

The schematic diagram of phase-A in VSI is shown in Figure 2. When the phase current $i_a > 0$, if the upper phase leg switching tube VT_P is turned on, the current flows through VT_P ; otherwise, when the upper phase leg switching tube is turned off and the lower phase leg switching tube is turned on, the current will not flow through VT_N , but will continue to flow through the diode VD_N . It means that when the phase current $i_a > 0$, no matter whether the VT_N is turned on or off, it will not work. Similarly, when the phase current $i_a < 0$, VT_P is in an invalid state.

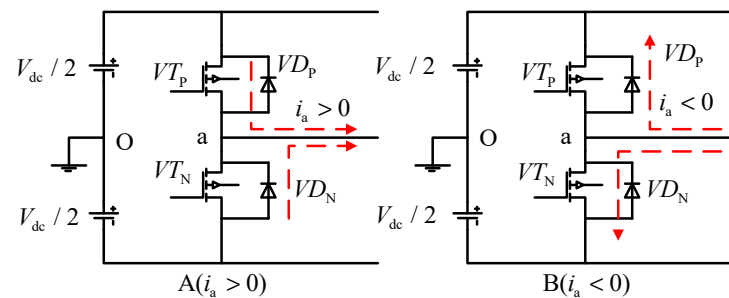


Figure 2. Single phase leg configuration of VSI.

Since the switching tube has an inherent turn-off delay, to prevent the upper phase leg and the lower phase leg from being turned on at the same time and causing a short circuit, the switching tube needs to be turned on with a delay, that is, a dead-time is inserted. During the dead-time, the upper and lower phase legs are not turned on, and the current is only continued through the parallel diode VD_P and VD_N . In addition, the tube conduction voltage drop and switching delay also increase the voltage error of the inverter.

The dead-time effect of a single phase leg in VSI is shown in Figure 3, where $PWMH^*$ and $PWML^*$ are ideal complementary drive signals; $PWMH$ and $PWML$ are the actual drive signals applied to the switching tubes after adding the dead-time; S_P and S_N are the actual switch waveforms considering the turn-on and turn-off delays; t_d is the dead-time; t_{on} is the turn-on delay time; t_{off} is the turn-off delay time; V_d is the diode conduction voltage drop; V_s is the switch tube conduction voltage drop.

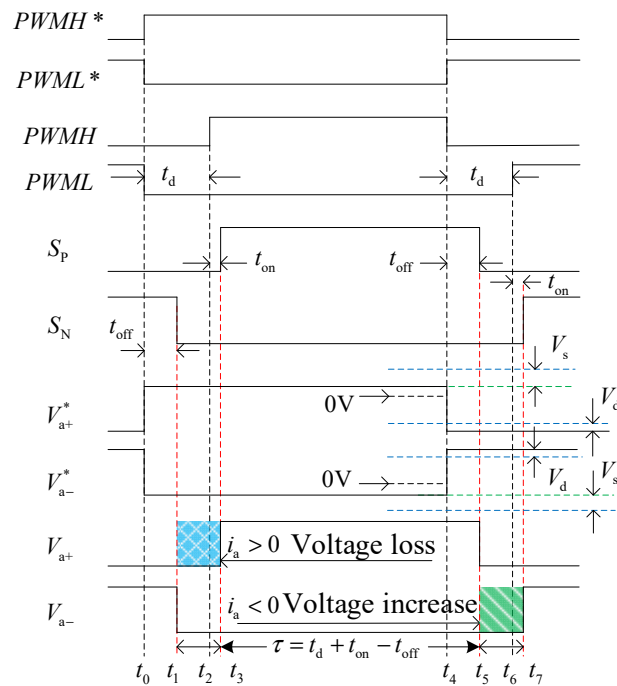


Figure 3. Dead-time effects on the output voltage.

As shown in Figure 3, the sources of nonlinear voltage error are divided into three aspects: the addition of dead-time, the switching delay of the switching tube, and the conduction voltage drop. The voltage error analysis of the specific switching process is as follows:

- (1) When the phase-A current satisfies $i_a > 0$.

Taking into account the dead time and the switching delay of the switch tube, the actual VT_P on-time in one period is $t_5 - t_3 = DT_s + t_{off} - t_d - t_{on}$, and the VT_P on-time is reduced by $\tau = DT_s - (t_5 - t_3) = t_d + t_{on} - t_{off}$, where D is the duty cycle, and T_s is the PWM period. Considering the conduction voltage drop of the power electronic device, when VT_P is turned on, the output voltage v_{ao} is $V_{dc}/2 - V_s$; when VT_P is turned off, the current flows through VD_N , and the output voltage $v_{ao} = -V_{dc}/2 - V_d$.

- (2) When the phase-A current satisfies $i_a < 0$.

Assuming that the upper phase leg conduction time is DT_s in the ideal case, the lower phase leg turn-off time is also DT_s . The actual VT_N off-time in one period is $t_7 - t_1 = DT_s + t_d + t_{on} - t_{off}$, and the on-time is $(1 - D)T_s - \tau$; the on-time is reduced by $\tau = t_d + t_{on} - t_{off}$. Considering the tube voltage drop, when VT_N is turned on, the output voltage v_{ao} is $-V_{dc}/2 + V_s$; when VT_N is turned off, the current flows through VD_P , and the output voltage $v_{ao} = V_{dc}/2 + V_d$.

It can be concluded that the reduction in VT_N on-time and the conduction voltage drop of the device both cause an increase in voltage, so the on-time needs to be compensated.

According to the voltage–time area equivalence principle, V_{error} , the average voltage error (the difference between the ideal output voltage and the actual output voltage) caused by the above factors in one PWM period can be expressed as follows:

$$\begin{cases} V_{error} = -\frac{\tau V_{dc} + (DT_s - \tau)V_s + [(1-D)T_s + \tau]V_d}{T_s} (i_a > 0) \\ V_{error} = \frac{\tau V_{dc} + (DT_s + \tau)V_d + [(1-D)T_s - \tau]V_s}{T_s} (i_a < 0) \end{cases} \quad (1)$$

According to Equation (1), the three factors of the inverter nonlinear voltage error are the addition of dead time, the conduction voltage drop, and the switching delay of the switching tube. The dead-time is the main source of voltage error.

2.2. Zero Current Clamping Effect When the Phase Current Crosses Zero

The zero current clamping phenomenon is mainly caused by the dead-time. The phase current crosses the zero point during the dead-time; both the upper and lower phase legs are turned off at this time. Due to the interaction between the back electromotive force and the DC bus voltage, the diode that should continue to flow after zero crossing cannot be turned on. As a result, the current is clamped at the zero and cannot smoothly cross zero during the entire dead-time until the next switching signal arrives. If the driving voltage provided by the controller is insufficient, the current may remain near zero for multiple PWM periods, and a current “stage” will appear. Shown in Figure 4a,b are the upper and lower phase leg driving signals, (c) is the actual voltage v_{ao} between point a and point o, the dotted line in (d) is the ideal current i_a^{ideal} after crossing the zero point, and the solid line is the actual current i_a^{real} .

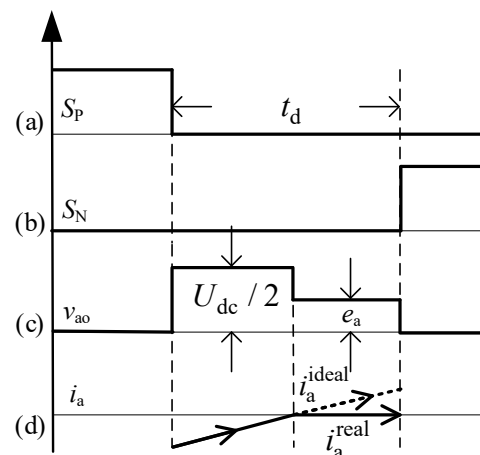


Figure 4. Diagram of the zero current clamping effect. (a) Driving signal of upper leg. (b) Driving signal of lower leg. (c) voltage v_{ao} between point a and point o. (d) Ideal current and real current.

3. Dead-Time Elimination Strategy near Non-Zero Crossing Points

Regardless of whether the phase current i_a is positive or not, there will always be a switching tube in an invalid state of one phase leg. Therefore, in the PWM period where the phase current does not cross zero, only one switching tube is activated in one phase leg. The principles are as follows:

$$\begin{cases} S_P = PWMH & S_N = 0 \quad (i_a > 0) \\ S_N = PWML & S_P = 0 \quad (i_a < 0) \end{cases} \quad (2)$$

When the phase current satisfies $i_a > 0$, VT_N is turned off; when the phase current satisfies $i_a < 0$, VT_P is turned off. Since there is a switching tube that is turned off in each PWM period, there is no need to consider the short circuit of the phase leg, and there is no need to add the dead-time. Figure 5 is the schematic diagram of ideal dead-time elimination without considering the zero crossing point.

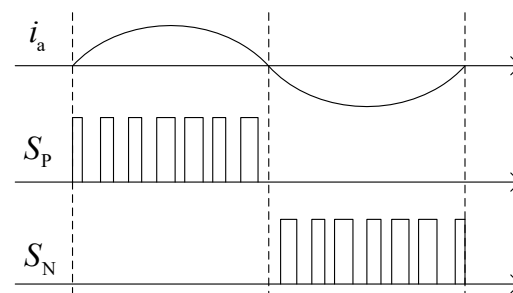


Figure 5. Modulation diagram of dead-time elimination.

At this time, only the nonlinear voltage error caused by the conduction voltage drop and the switching delay on the inverter need to be considered, it can be compensated by adjusting the pulse duration, the compensation time is derived by (1):

$$\begin{cases} t_{\text{com}+} = \frac{\lambda V_{\text{dc}} + (DT_s - \lambda)V_s + [(1-D)T_s + \lambda]V_d}{(V_{\text{dc}} + V_d - V_s)} \\ t_{\text{com}-} = \frac{\lambda V_{\text{dc}} + (DT_s + \lambda)V_d + [(1-D)T_s - \lambda]V_s}{(V_{\text{dc}} + V_d - V_s)} \end{cases} \quad (3)$$

where $\lambda = t_{\text{on}} - t_{\text{off}}$, $t_{\text{com}+}$ is the increased on-time of the upper phase leg when $i_a > 0$, and $t_{\text{com}-}$ is the increased on-time of the lower phase leg when $i_a < 0$. According to the polarity of the current, the on-time of the phase-A is determined as follows:

$$\begin{cases} t_{\text{ahon}}^* = t_{\text{ahon}} + t_{\text{com}+} \quad (i_a > 0) \\ t_{\text{alonn}}^* = t_{\text{alonn}} + t_{\text{com}-} \quad (i_a < 0) \end{cases} \quad (4)$$

where t_{ahon} represents the turn-on time of the upper phase leg before compensation; t_{ahon}^* represents the turn-on time after compensation. At the same time, the lower phase leg remains off-state; t_{alonn} represents the turn-on time of the lower phase leg before compensation; t_{alonn}^* represents the turn-on time after compensation. At the same time, the upper phase leg remains off-state.

4. Modulation for the Phase Current Crossing Zero in Advance

According to the analysis in Section 2.2, the zero current clamping effect occurs when the phase current crosses zero, and it is difficult to be suppressed through voltage compensation. Therefore, a novel modulation scheme for the phase current crossing zero in advance is proposed in this paper; the diagram is shown in Figure 6. When i_a crosses zero from positive to negative, to accelerate the zero crossing process of i_a , the upper switching signal S_P remains off-state, and the lower switching signal S_N remains on-state. When i_a crosses zero from negative to positive, the upper switching signal S_P remains on-state, and the lower switching signal S_N remains off-state. Due to generating the maximum voltage, whose polarity is the same as the changing direction of i_a , the zero current clamping effect only occurs during a very short time, and it has little impact on the phase current. In addition, the dead-time is also eliminated when i_a crosses zero, because no action occurs in the switching signals.

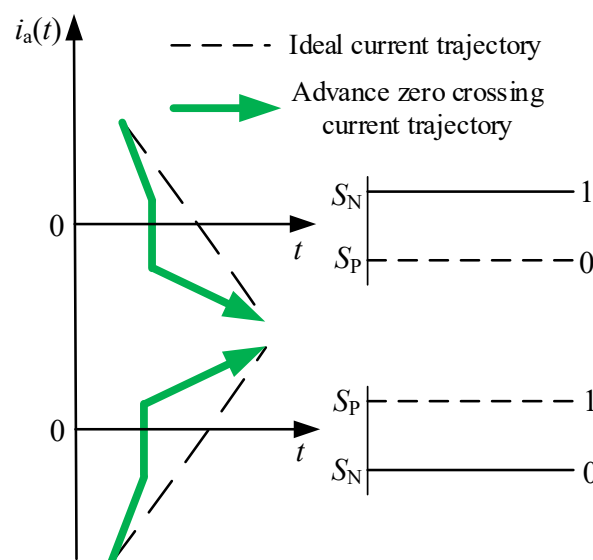


Figure 6. Diagram of the phase current crossing zero in advance.

5. Selection Principle of the Two Proposed Modulation Schemes

The proposed modulation strategy for the phase current crossing zero in advance is only suitable for near the zero crossing point; in the non-zero crossing region of phase current, the proposed single-leg action modulation scheme should be applied as much as possible. Otherwise, it will cause serious harmonic distortion in the phase current. Therefore, to adopt the optimal modulation scheme for all operating points, it is necessary to determine the principle of switching the proposed two modulation schemes.

In this paper, the phase current and motor speed are sampled in real time. The three-phase stator current is subjected to Clarke transformation and rotor flux orientation-based Park transformation to obtain the stator d - q axis current i_{sd} and i_{sq} in the two-phase rotating coordinate system. Then, the real-time electrical angular frequency ω_n and the phase current amplitude I_m are calculated. The calculation expression is as follows:

$$\omega_n = \omega_f + p\omega_r = \frac{i_{sd}}{T_r i_{sq}} + p\omega_r \quad (5)$$

$$I_m = \sqrt{i_{sd}^2 + i_{sq}^2} \quad (6)$$

where ω_f is the motor slip frequency, T_r is the rotor time constant, ω_r is the actual rotor speed, and p represents the number of IM pole pairs.

During the experiment, the A/D sampling is triggered by the PWM signal. After the A/D conversion is completed, the interrupt service program is entered to update the modulation strategy and comparison value register of the next period. Therefore, there is a time interval of less than T_s between the A/D sampling time and the start time of the next PWM period. The zero crossing moment may be located at any position in this PWM period. The maximum time interval between the A/D sampling moment of the PWM period modulation strategy (i.e., the A/D sampling moment in the previous PWM period) and the zero crossing moment in this PWM period is determined to be $2T_s$, and the absolute value of the phase current at this time is $|I_m \sin 2\omega_n T_s|$. Therefore, $I_m \sin 2\omega_n T_s$ and $-I_m \sin 2\omega_n T_s$ are used as two threshold values and compared with the real-time sampling value of the phase current, determining the modulation scheme to be applied for the next PWM period. The diagram for the switching principle of the two modulation schemes is shown in Figure 7a; four operating points (A, B, C, and D) are defined for comparison with i_a and shown as follows:

$$\left\{ \begin{array}{l} \text{Point A : } i_a = I_{th} \text{ and } i_a \text{ is increasing} \\ \text{Point B : } i_a = I_{th} \text{ and } i_a \text{ is decreasing} \\ \text{Point C : } i_a = -I_{th} \text{ and } i_a \text{ is decreasing} \\ \text{Point D : } i_a = -I_{th} \text{ and } i_a \text{ is increasing} \end{array} \right. \quad (7)$$

where I_{th} is equal to $I_m \sin 2\omega_n T_s$. When the IM operates at point A, the proposed single-leg action modulation is applied, and the switching action only occurs in S_P ; S_N remains off-state. Until the IM operating at point B, the proposed modulation strategy for the phase current crossing zero in advance is applied, S_P and S_N remain on-state and off-state, respectively. Due to the continuous output of the maximum negative polarity voltage, i_a can quickly cross zero point. When the IM operates at point C, the proposed single-leg action modulation is applied again, and the switching action only occurs in S_N ; S_P remains off-state. Until the IM operating at point D, the proposed modulation strategy for the phase current crossing zero in advance is applied again; S_P and S_N remain off-state and on-state, respectively. Due to the continuous output of the maximum positive polarity voltage, i_a can quickly cross the zero point. The state transition diagram of the above process is shown in Figure 7b.

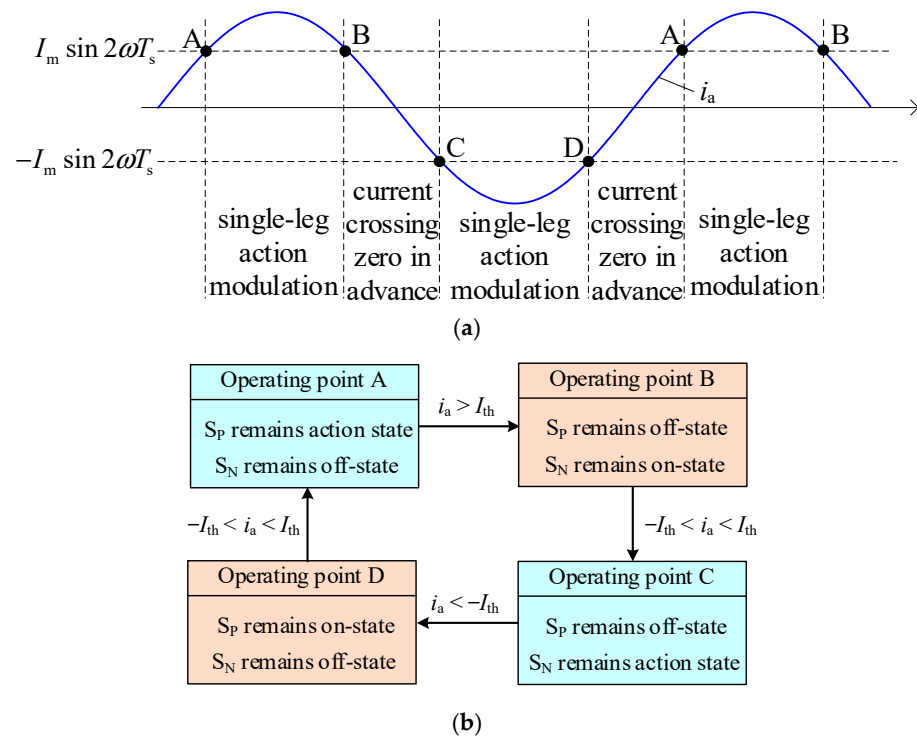


Figure 7. Diagram of modulation switching within a fundamental period. (a) Description of current changes. (b) State transition diagram.

6. Discrete Filtering Processing of the Sampling Current

The switching algorithm proposed in Section 5 has extremely high requirements for current sampling accuracy. However, affected by the current ripple and sampling burrs, There may be errors between the current sampling value and the actual value, which leads to incorrect modulation strategy being adopted. A second-order resonance filter $F(s)$ without phase shift is adopted to obtain the fundamentals of phase current. The transfer function $F(s)$ in s -domain is expressed as follows:

$$F(s) = \frac{i_{fa}(s)}{i(s)} = \frac{2\zeta\omega_n s}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \quad (8)$$

where ζ is the damping ratio; ω_n is the resonance frequency of the filter. ω_n should be equal to the electrical angular frequency of the IM. When ζ is larger, the response speed is faster, but the high-frequency component attenuation is smaller, so the value of ζ should be chosen reasonably. After multiple simulations and comparisons, ζ is set as 0.05 in this paper. The Bode plot of $F(s)$ under $\omega_n = 100\pi$ rad/s is shown in Figure 8. The amplitude and phase of $F(s)$ are 0 dB and 0 deg at 100π rad/s, and it has an attenuation effect on all other harmonic components.

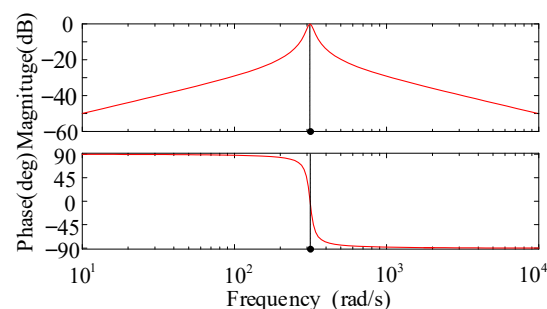


Figure 8. Bode plot of filter transfer function.

Since DSP is only used to implement the discrete algorithm, discretization of Equation (8) is required. Firstly, the state equation of (8) is derived as follows:

$$\frac{d^2 i_{fa}(t)}{dt^2} + 2\zeta\omega_n \frac{di_{fa}(t)}{dt} + \omega_n^2 i_{fa}(t) = 2\zeta\omega_n \frac{di_a(t)}{dt} \quad (9)$$

The discretization using the forward difference method yields the differential expression of the digital filter as follows:

$$i_{fa}[(n+2)T_s] = 2(1 - \zeta\omega_n T_s)i_{fa}[(n+1)T_s] - (1 - 2\zeta\omega_n T_s + \omega_n^2 T_s^2)i_{fa}(nT_s) + 2\zeta\omega_n T_s i_a[(n+1)T_s] - 2\zeta\omega_n i_a(nT_s) \quad (10)$$

After digital filter processing, i_{fa} is compared with I_{th} to determine the modulation scheme. Since the electrical angular frequency of the IM is not a fixed value, ω_n is updated in real-time at each PWM period. The waveforms of the phase current before and after the digital filter are shown in Figure 9. i_a is the sampling current, with the current ripple and sampling burrs. When the second-order bandpass digital filter is adopted, after one period, the filter current i_{fa} can follow the fundamental component of i_a without phase shift. Therefore, in the steady state, the designed digital filter can obtain the fundamental component of the phase current.

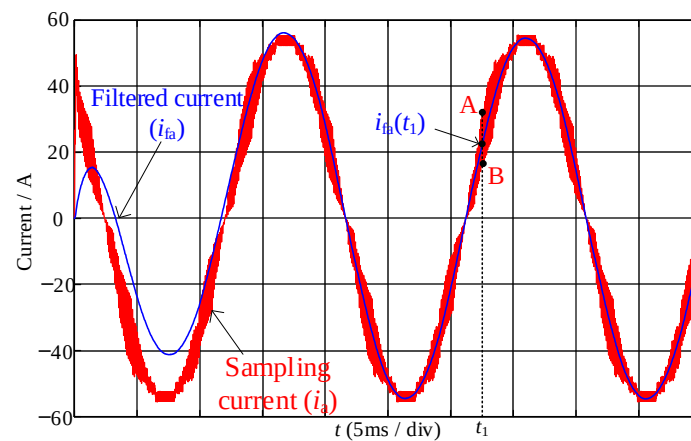


Figure 9. The waveforms of the phase current before and after digital filter.

Next, the necessity of extracting the fundamental will be explained, combined in Figure 9. At t_1 moment, affected by the current ripple and sampling burrs, the sample value of the phase current may be $i_a(A)$ or $i_a(B)$, and there is significant error between them. However, incorrect sampling values may result in inappropriate modulation algorithms being used in the next switching period, so this paper adopts the fundamental component obtained by the proposed digital filter as the basis for selecting the modulation. The flow chart of the modulation selection based on the digital filter is shown in Figure 10.

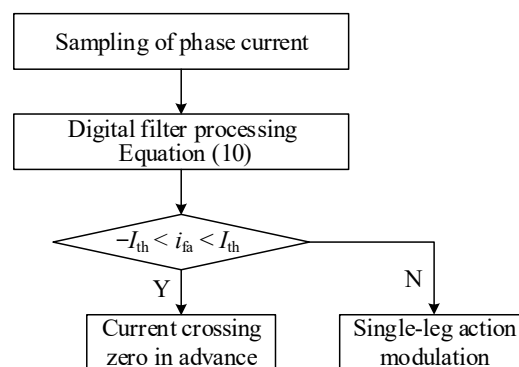


Figure 10. The flow chart of the modulation selection based on the digital filter.

7. Experimental Results and Analysis

The experimental platform as shown in Figure 11 was established to verify the proposed modulation scheme; the models with their parameters or part numbers are listed in Table 1. The DC voltage was supplied by the power supply (PR300-4, MATSUSADA, Shiga, Japan). The three-phase current was detected by the current sensors (MLX91205, MELEXIS, Ieper, Belgium), the speed was detected by the encoder, and the inverter bridge consisted of six IGBT modules (IPB042N10N, Infineon Technologies, Neubiberg, Germany, turn-on time is 1.4 μ s, turn-off time is 2.5 μ s). The control and modulation algorithm was implemented by the digital signal controller (TMS320F28035, TEXAS Instruments, Dallas, TX, USA); the switching frequency was 10 kHz.

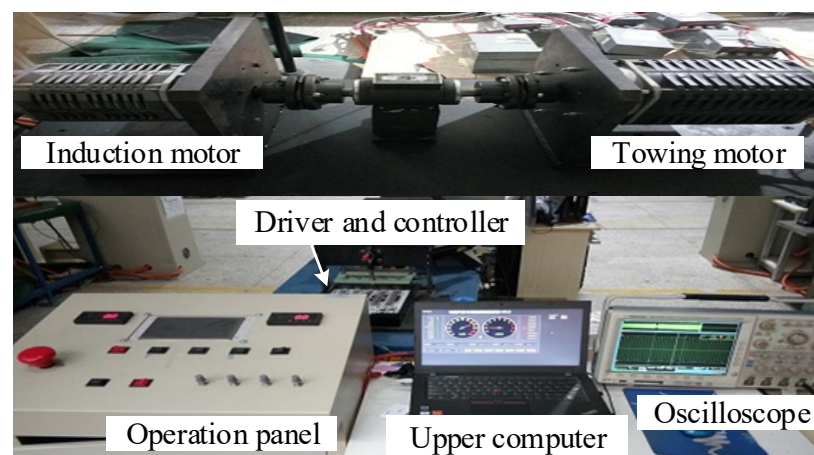


Figure 11. Experimental platform.

Table 1. Modules and parameters of the experimental platform.

Category	Part Number	Parameters
DC power supply	PR300-4	72 V
Switching tubes (IGBT)	IPB042N10N	100 V/100 A
Current sensors	MLX91205	/
Digital signal controller	TMS320F28035	/
Encoder	OIH	2500 C/T

A closed-loop control model of flux and speed was designed in a two-phase rotating coordinate system (d - q axis), the diagram that contains the field-oriented control detail, is shown in Figure 12. It is a two closed-loop control system. Two PI controllers control the speed (ω_r) and the rotor flux (ψ_r) to eliminate the steady-state errors, and the references of the phase current (i_{sd}^* and i_{sq}^*) in d - q axis are obtained. Then, the current inner loop adopts two PI controllers to obtain the references of the voltage (u_d and u_q) in the d - q axis. After the Clarke transformation, the references of the voltage (u_α and u_β) in the two-phase station coordinate system are obtained and are used as the inputs for the dead-time free modulation strategy proposed in this paper. The amplitude of the rotor flux (ψ_r) is calculated by the current model, which is expressed as follows:

$$\psi_r = \frac{L_m}{1 + T_{rs}} i_{sd} \quad (11)$$

where L_m represents the magnetic inductance of IM. The angle (θ_r) of the rotor flux is obtained by integrating the electrical angular frequency. The parameters of the IM are listed in Table 2.

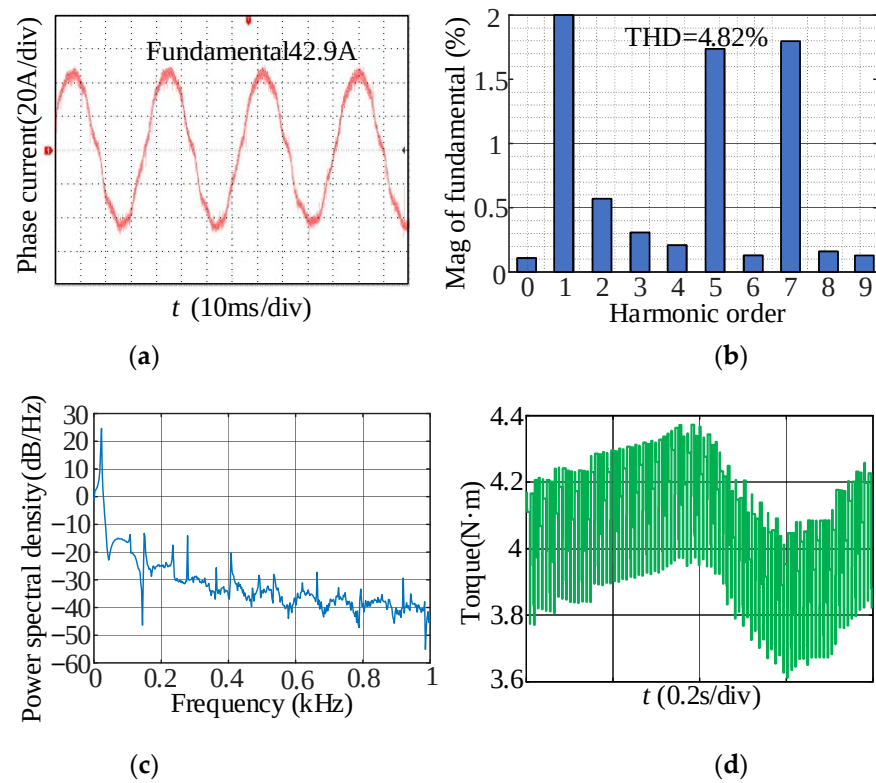


Figure 13. Experimental waveforms under compensation of the pulse duration when IM operates at 500 r/min and 4 N·m. (a) Phase current. (b) Harmonic analysis results. (c) Power spectral density. (d) Torque.

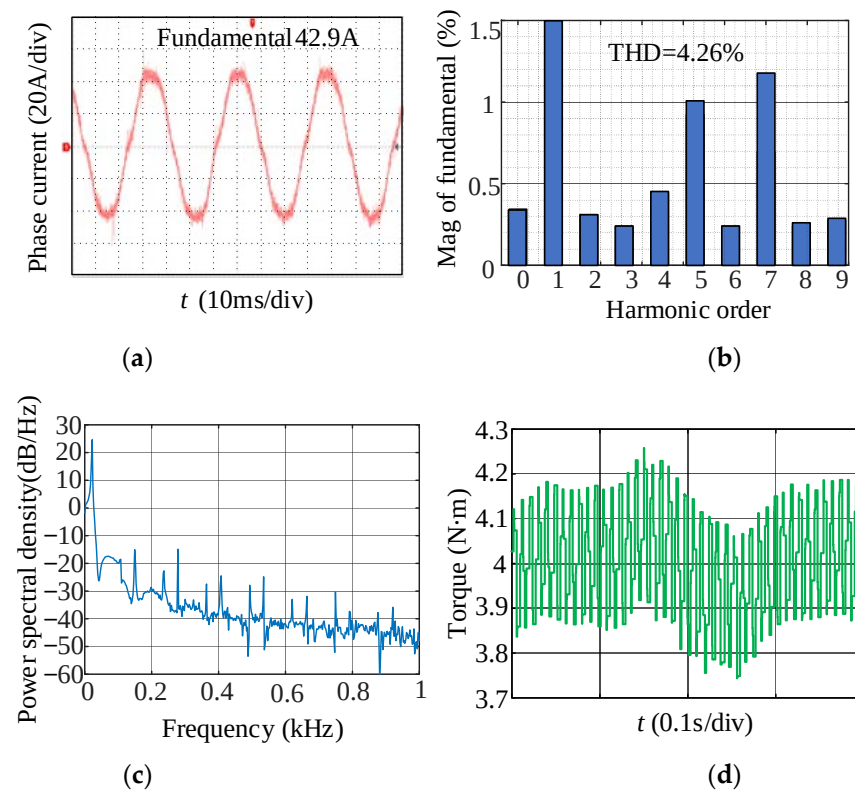


Figure 14. Experimental waveforms under inverter nonlinearity feedforward compensation when IM operates at 500 r/min and 4 N·m. (a) Phase current. (b) Harmonic analysis results. (c) Power spectral density. (d) Torque.

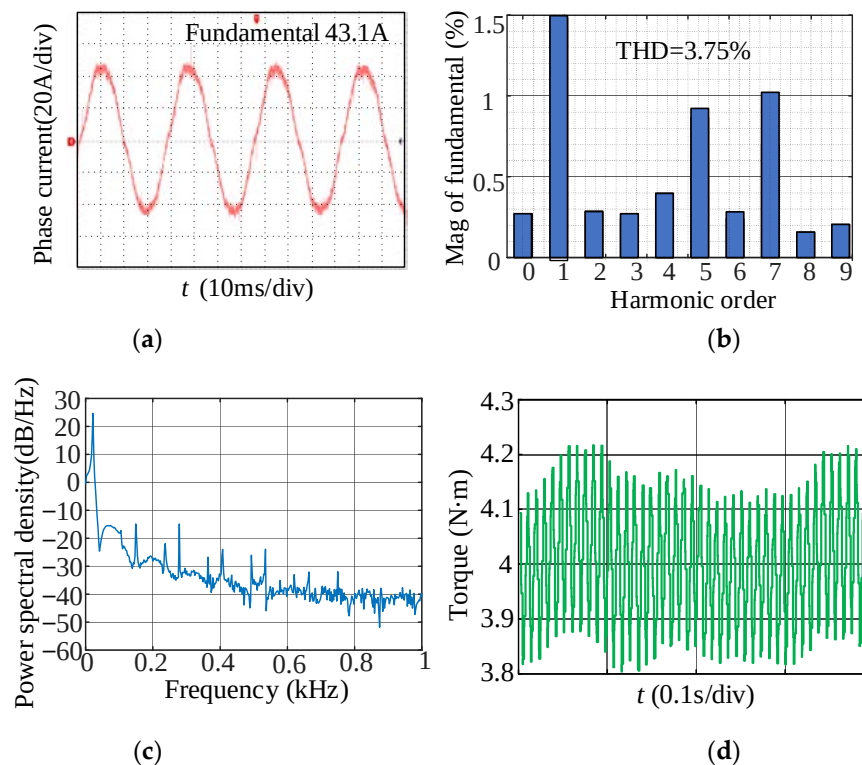


Figure 15. Experimental waveforms under proposed dead-time free modulation when IM operates at 500 r/min and 4 N·m. (a) Phase current. (b) Harmonic analysis results. (c) Power spectral density. (d) Torque.

Then, the operating condition is changed, the IM operates at 3000 r/min without load. The experimental results under the pulse duration compensation adopted in [8], the inverter nonlinearity feedforward compensation proposed in [11], and the proposed dead-time free modulation are shown in Figure 16, Figure 17, and Figure 18, respectively. Under the pulse duration compensation, the THD of the phase current is 6.01%, the torque ripple is ± 0.4 N·m, the proportion of the fifth harmonic is 2.04%, and the proportion of the seventh harmonic is 1.8%. Under the nonlinear voltage feedforward compensation method of the inverter, the THD of the phase current is 5.65%, the torque ripple is ± 0.35 N·m, the proportion of the fifth harmonic is 1.88%, and the proportion of the seventh harmonic is 1.48%. Under the proposed dead-time free modulation, the THD of the phase current is 4.38%, the torque ripple is ± 0.25 N·m, the proportion of the fifth harmonic is 1.55%, and the proportion of the seventh harmonic is 1.09%.

Finally, the operating condition is changed, the IM operates at the rated condition (1500 r/min and 4 N·m). The experimental results under the pulse duration compensation adopted in [8], inverter nonlinearity feedforward compensation proposed in [11], and the proposed dead-time free modulation are shown in Figure 19, Figure 20, and Figure 21, respectively. Under the pulse duration compensation, the THD of the phase current is 4.2%, the torque ripple is ± 0.3 N·m, the proportion of the fifth harmonic is 1.58%, and the proportion of the seventh harmonic is 1.03%. Under the nonlinear voltage feedforward compensation method of the inverter, the THD of the phase current is 3.95%, the torque ripple is ± 0.2 N·m, the proportion of the fifth harmonic is 1.13%, and the proportion of the seventh harmonic is 0.91%. Under the proposed dead-time free modulation, the THD of the phase current is 3.66%, the torque ripple is ± 0.15 N·m, the proportion of the fifth harmonic is 0.89%, and the proportion of the seventh harmonic is 0.54%.

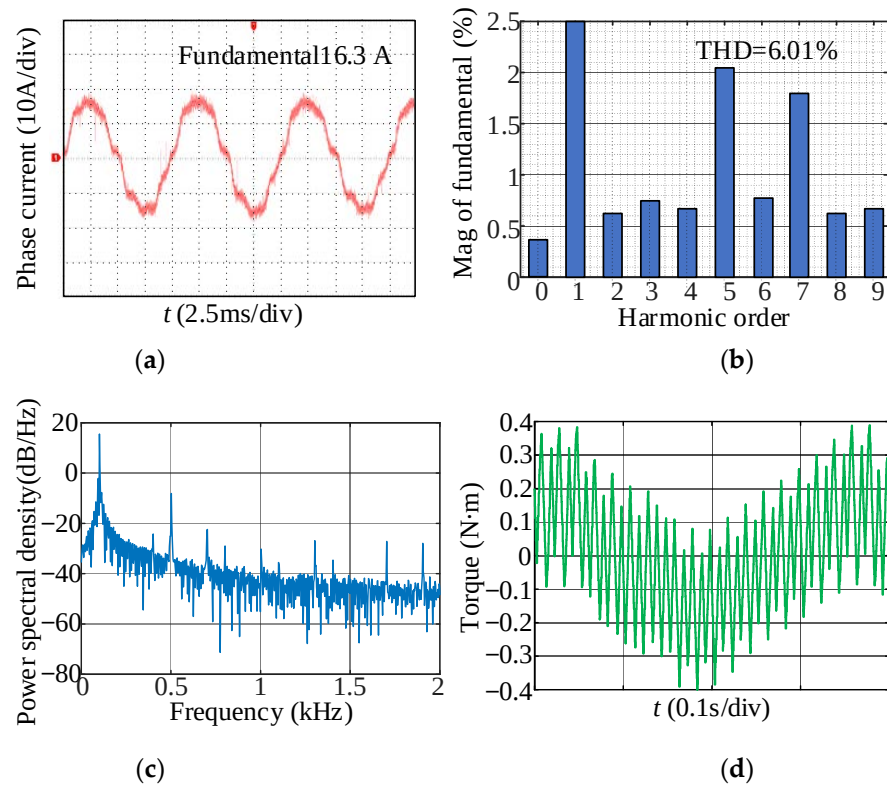


Figure 16. Experimental waveforms under compensation of the pulse duration when IM operates at 3000 r/min and 0 N·m. (a) Phase current. (b) Harmonic analysis results. (c) Power spectral density. (d) Torque.

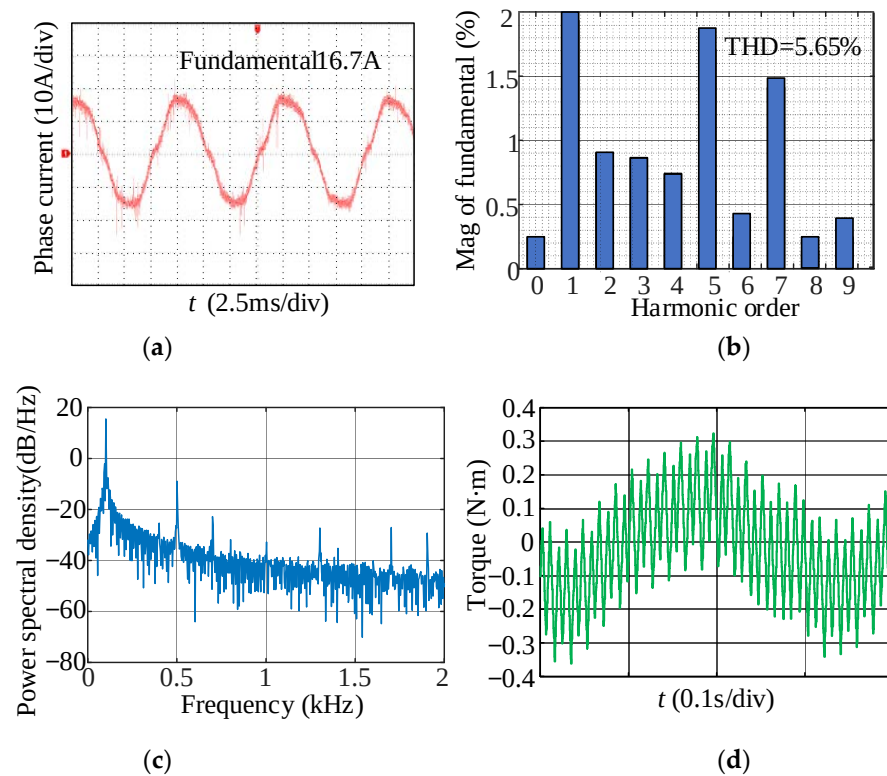


Figure 17. Experimental waveforms under inverter nonlinearity feedforward compensation when IM operates at 3000 r/min and 0 N·m. (a) Phase current. (b) Harmonic analysis results. (c) Power spectral density. (d) Torque.

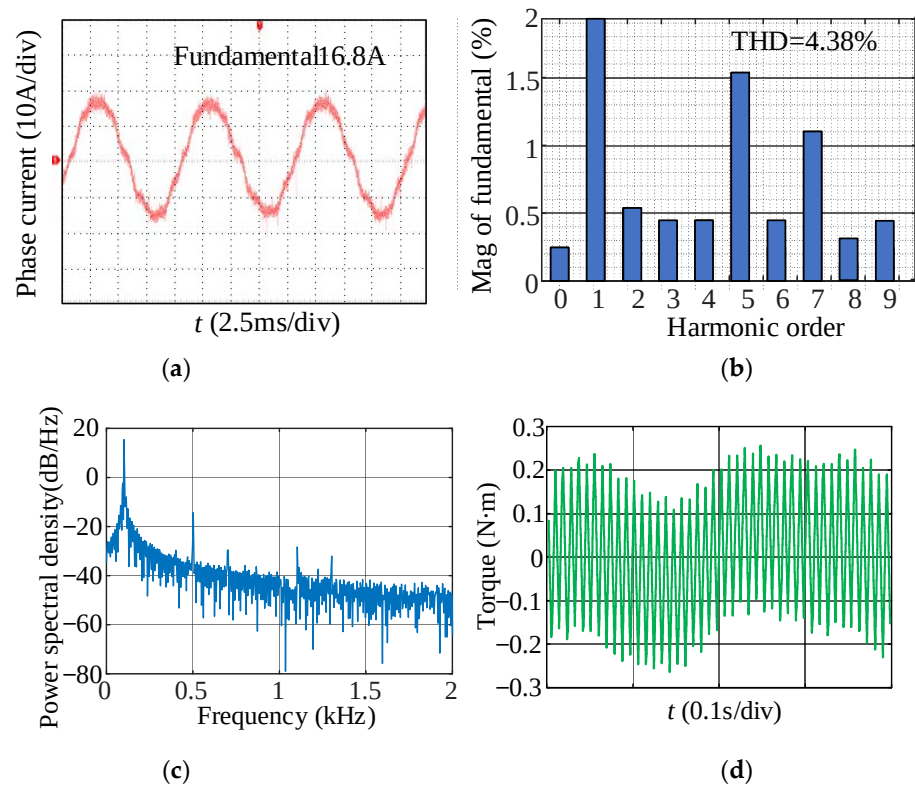


Figure 18. Experimental waveforms under proposed dead-time free modulation when IM operates at 3000 r/min and 0 N·m. (a) Phase current. (b) Harmonic analysis results. (c) Power spectral density. (d) Torque.

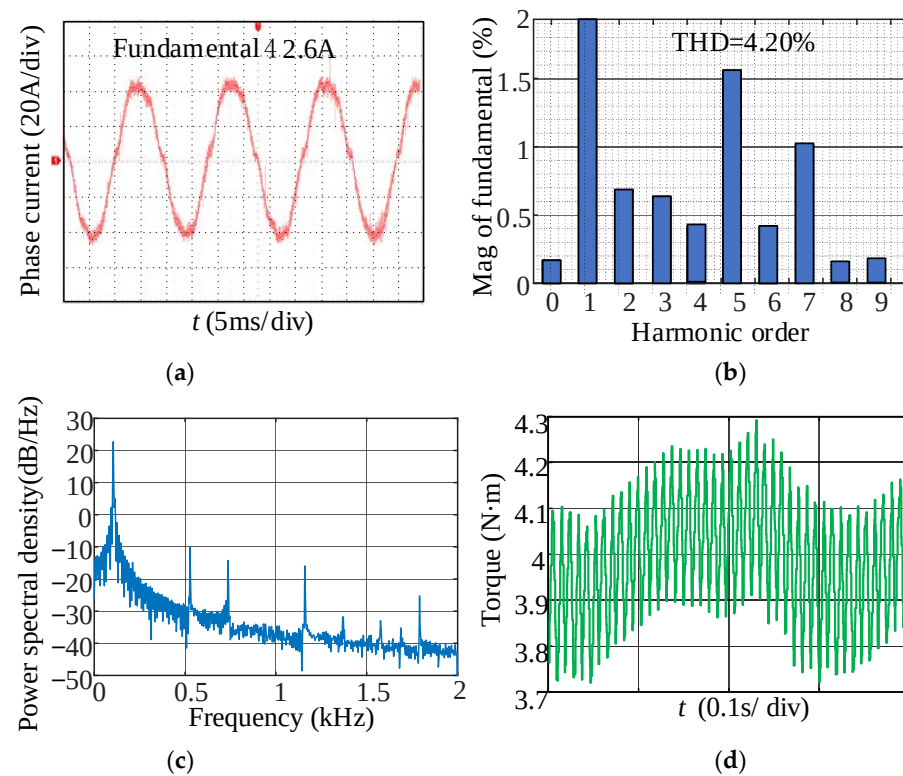


Figure 19. Experimental waveforms under compensation of the pulse duration when IM operates at 1500 r/min and 4 N·m. (a) Phase current. (b) Harmonic analysis results. (c) Power spectral density. (d) Torque.

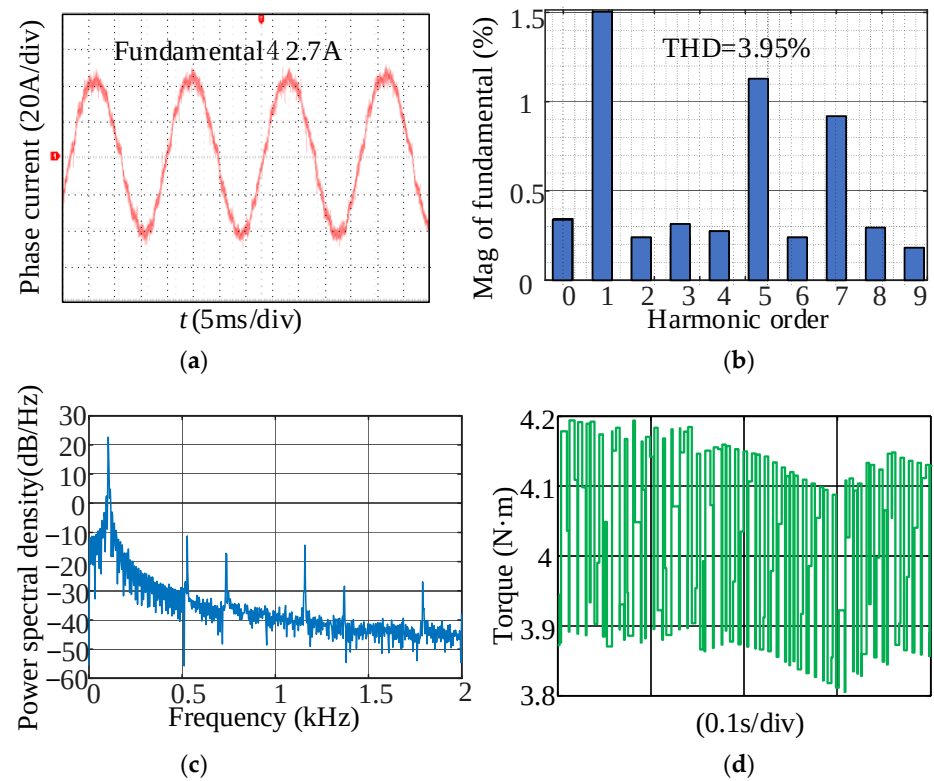


Figure 20. Experimental waveforms under inverter nonlinearity feedforward compensation when IM operates at 1500 r/min and 4 N·m. (a) Phase current. (b) Harmonic analysis results. (c) Power spectral density. (d) Torque.

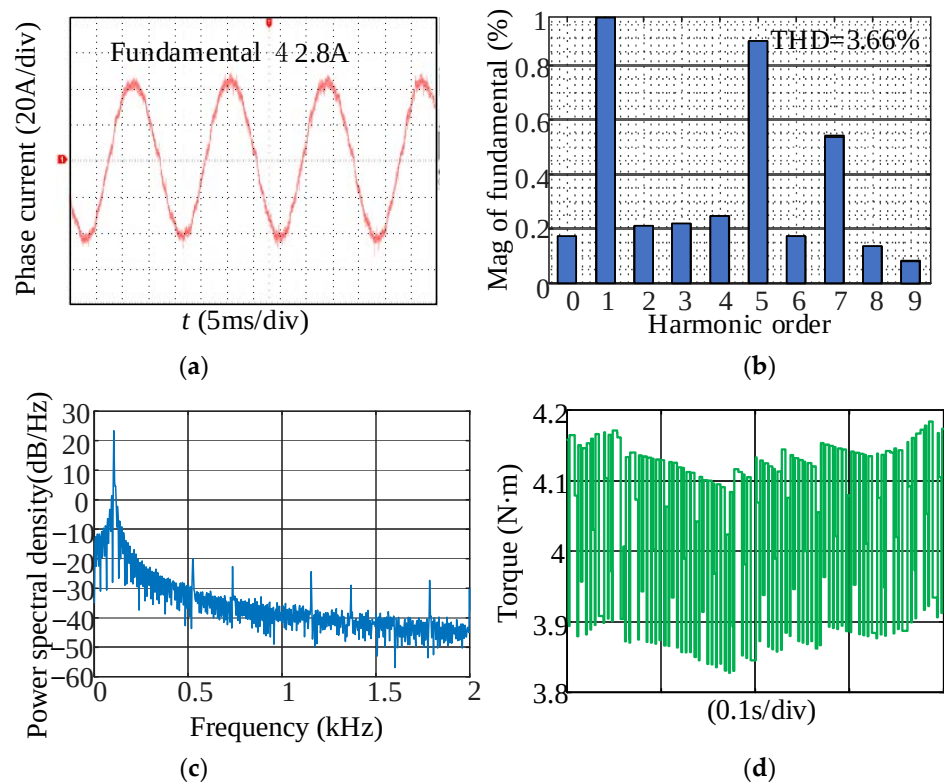


Figure 21. Experimental waveforms under proposed dead-time free modulation when IM operates at 1500 r/min and 4 N·m. (a) Phase current. (b) Harmonic analysis results. (c) Power spectral density. (d) Torque.

The experimental results under the above two operating conditions indicate that the dead-time free modulation proposed in this paper can achieve better steady-state performance. Meanwhile, on the premise of accurately sampling the phase current in real-time, the two proposed modulation schemes with the switching principle are correct and feasible.

7.2. Discussion and Analysis of the Experimental Results

Firstly, the relationship between voltage harmonics, current harmonics, and torque ripple is discussed. According to Reference [19], in an ideal situation, the line voltage using SVPWM modulation only contains the fundamental and the high-order harmonics near the fundamental frequency, so the phase current has little low-order harmonic, and the frequency of torque ripple is consistent with the switching frequency. However, the nonlinear factors such as dead-time and tube conduction voltage drop will generate the fifth and seventh harmonics of the output voltage, which leads to the fifth and seventh harmonics occurring in the phase current, and the sixth ripple occurring in the torque.

Traditional compensation methods consider the dead-time, turn-on delay, turn-off delay, and conduction voltage drop of the switching tube and diode to compensate for pulse duration, but the compensation accuracy is not high, so the steady-state performance of the IM is the worst. The inverter nonlinearity feedforward compensation proposed in [11] decomposes the voltage error into two parts (ΔV_{an_cond} and ΔV_{an_dt}), ΔV_{an_cond} is caused by the conduction voltage drop, and ΔV_{an_dt} is formed in the dead-time stage. Its calculation model is expressed as follows:

$$\begin{cases} \Delta V_{an_cond} = V_s \text{sign}(i_a) \\ \Delta V_{an_dt} = \frac{2}{\pi} V_{dt} \text{atan}(k_{dt} i_a) \end{cases} \quad (12)$$

The conduction voltage drop V_s does not change significantly with the temperature and can be set as a constant according to the data manual. V_{dt} represents the voltage error caused by the dead-time, and k_{dt} is related to the parameters of the snubber capacitor, which requires multiple experimental tests to be obtained. ΔV_{an_cond} and ΔV_{an_dt} are compensated to the voltage references on the d - q axis.

The diagram of the inverter nonlinearity feedforward compensation is shown in Figure 22, when $i_a > 0$, where V_{an}^* represents the ideal voltage under SVPWM in a switching period, V_{an} is the actual voltage considering dead-time, turn-on delay, turn-off delay, and conduction voltage drop of the switching tube and body diode. V_{an_com} represents the output voltage after nonlinear voltage feedforward compensation. ΔV_{an} represents the voltage error between V_{an}^* and V_{an_com} . Although the average error can be eliminated by the nonlinear voltage feedforward compensation, two pulses occur in the waveform of ΔV_{an} in every switching period, which leads to the low-order harmonics in the phase current. In addition, due to the existence of the dead-time, the zero current clamping effect cannot be suppressed significantly.

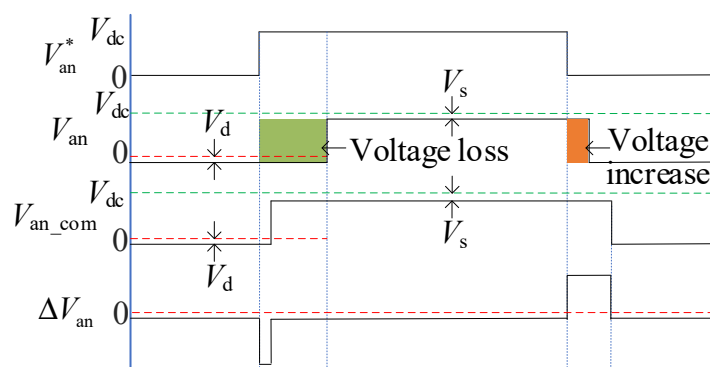


Figure 22. The diagram of the inverter nonlinearity feedforward compensation.

Due to the elimination of the dead-time, the output voltage V_{an} under the proposed dead-time free modulation has few differences from the ideal voltage V_{an}^* , and the zero current clamping effect can be suppressed by making the phase current crossing zero in advance. Therefore, in the comparative experiment results of the above three operating conditions, the best steady-state performance of the IM can be obtained by the proposed dead-time free modulation.

8. Conclusions

To reduce the harmonic distortion and torque ripple caused by the dead-time, a novel dead-time free modulation scheme is proposed in this paper. Utilizing the freewheeling characteristics of the body diodes, only one switching tube remains action state in one phase leg, and another one remains off-state. To suppress the zero current clamping effect when the phase current crosses zero, another modulation scheme for the phase current crossing zero in advance is proposed. The dead-time is eliminated during all switching periods. Finally, the feasibility and effectiveness are verified by experiments, and the following conclusion are formed:

- (1) In the non-zero crossing region of the phase current, due to only one tube in the upper and lower bridge arms being in action, the deadtime is eliminated. The nonlinear error between the actual output voltage and the ideal voltage is very little, so the fifth and seventh harmonics of the output voltage can be reduced from the root. The fifth and seventh harmonics and the THD in the phase current under the proposed dead-time free modulation are less than those under other compensation schemes, and the torque ripple minimization can be achieved;
- (2) Near the zero crossing point, the inverter remains in the switching state that can output the maximum voltage whose polarity is the same as the changing direction of the phase current, which accelerates the phase current crossing zero. Compared to other compensation schemes, this method is more effective in suppressing the zero current clamp effect, and the dead-time is avoided.

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