

Article

Novel Single-Loop Control Strategy for 400 Hz Voltage Source Inverter with LC Filter

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Abstract

The control of 400 Hz Ground Power Units (GPUs) in the range of several hundreds of kW poses distinct challenges, as the switching frequency (f_{sw}) must be constrained to limit switching losses. This constraint typically results in low ratios of the switching and LC filter natural frequencies (f_n) relative to the fundamental frequency. Notably, without mitigation, such systems often face stability issues or non-minimum phase behavior when $f_n < f_s/3$ (where f_s is the sampling frequency). To address these challenges, this paper introduces a single-loop voltage control strategy for a 400 Hz voltage-source inverter (VSI) featuring a robust voltage decoupling scheme. Crucially, this decoupling allows the system to maintain minimum phase characteristics and operate with positive gains even when $f_n < f_s/3$, effectively solving the stability problems inherent to this operating region. The proposed architecture employs a proportional-resonant (PR) controller, with parameters systematically tuned to achieve maximum system damping based on stability regions dependent on the ratio between the sampling and natural frequencies. Validated through simulation and experimental procedures, the proposed method demonstrates precise voltage tracking and a robust dynamic response, proving its suitability for high-power, high-fundamental-frequency applications.

Keywords: control systems; damping; decoupling; GPU; PR controller; robust control; single loop; stability; voltage control

1. Introduction

Power supply systems are critical components in the aerospace industry, primarily serving as Ground Power Units (GPUs) to provide external energy to aircraft while they are parked. The design of the voltage control strategy for 400 Hz GPUs in the range of several hundreds of kW is challenging. The switching frequency (f_{sw}) cannot be high to limit the switching losses; this results in a ratio of switching to fundamental frequency being low in many cases. The combination of a high fundamental frequency ($f_o = 400$ Hz) and inherent digital implementation constraints, such as computational and modulation delays, makes this application particularly challenging [1–10]. To address these challenges, several authors have proposed multi-loop architectures that utilize observers to estimate system states and compensate for processing lags [3,5], while others suggest multiresolution strategies that partition control tasks to optimize digital signal processor efficiency [2]. In contrast to these cascaded methods, single-loop strategies employing proportional-resonant (PR) controllers or resonant (R) controllers have been developed to offer a balance of simplicity and dynamic



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performance [1,10]. Due to the high bandwidth requirements of a 400 Hz GPU, single-loop voltage controllers are often preferred over double-loop structures [10]. In a single-loop design, the converter's output current is usually measured for safety reasons, allowing it to be tripped if the current exceeds the maximum permissible value.

PR and R controllers are employed in power converter control strategies to maintain precise reference tracking and system stability when the converter faces disturbances [11,12]. These controllers provide predictable phase characteristics, which enable a stable operation in a wide range of operating conditions. Consequently, researchers have focused on optimizing these designs to eliminate stability gaps and ensure robust operation during mode transitions, highlighting the common goal of these controllers to secure a stable operating region across various grid-connected and islanded applications [1,13,14].

The stability region of power converters with an LC filter is determined by the relationship between the sampling frequency (f_s) and the filter's natural or resonant frequency (f_n), specifically their ratio (f_s/f_n). Many techniques have been proposed in research publications aiming to enhance damping and expand the stability region, specifically for single-loop voltage control [1,15]. In those publications, the stability region with PR controllers was considered to be $f_n > f_s/3$. In [16] it was shown that this is due to using positive proportional gains, and that with negative proportional gains the region is $f_n < f_s/3$, but that a non-minimum phase system is obtained. This approach leads to a stability region that is markedly different from that achieved with a positive proportional gain. When a negative proportional gain is used, the stability requirement shifts, mandating that the filter's resonant frequency be lower than one-third of the sampling frequency ($f_n < f_s/3$). Conversely, PR controllers with positive proportional gain necessitate the LC filter's resonant frequency to be higher than one-third of the sampling frequency (i.e., $f_n > f_s/3$), according to [16]. However, a consequence of using negative proportional gains is the creation of a non-minimum phase system, which will introduce right-half plane zeros, potentially causing system undershoot. In [17–19] the common goal is to enhance the stability and control performance of LC-filtered voltage-source inverters through the analysis and optimization of control strategies, including accurate discretization methods and resonance damping techniques.

In the case of a resonant (R) controller, the natural frequency needs to be higher than $f_s/6$ [17]. In [17], it is shown that negative resonant gains for the R controller will result in an unstable system. Therefore, the stability region for the single-loop voltage control with an R controller is defined as $f_n > f_s/6$, which ensures a minimum-phase system. In [17], it is demonstrated that the advantage of decoupling the capacitor voltage when a PR controller is used lies in its ability to enable the use of positive proportional gains when f_n is either above or below $f_s/3$. Therefore, a minimum-phase system is always achieved, thereby improving system performance compared to existing approaches. However, these advantages cannot be obtained using the decoupling technique with an R controller. Therefore, in this work, a single-loop voltage control with a PR controller and capacitor voltage unitary decoupling is designed.

This paper presents the design of a single-loop voltage control with a PR controller and voltage decoupling in 400 Hz medium-power converters, where the switching frequency is closer to the fundamental one compared to 50 or 60 Hz applications. Using voltage decoupling, a minimum-phase system is achieved independently of the resonant frequency of the LC filter (below or above $f_s/3$). The stability region of the single-loop voltage control in the discrete-time domain is covered in [17], where the authors define the minimum and maximum values for the controller gains but do not include a methodology for selecting the controller gains based on a particular key performance index. The gain selection criteria in this paper proposes a method to select the gain to achieve the highest damping.

The main contributions of this paper are as follows:

1. The development and analysis of a voltage control tuning strategy for 400 Hz GPUs, consisting of a single-loop voltage control with a PR controller and capacitor voltage unitary decoupling. The design is based on stability region analysis and is shown to achieve effective AC voltage regulation, especially in systems that operate with a low ratio of switching frequency to fundamental frequency (around 10–15).
2. By using maximum damping as the key performance index for gain selection in the PR controller, the system dynamics of the 400 Hz GPU are improved, resulting in better overall performance of the voltage regulation.

2. System Specifications

The system under investigation is a three-phase VSI equipped with an output LC filter, as depicted in Figure 1. The parameters L_f and C_f denote the filter inductance and capacitance, while R_f signifies the inductor's equivalent series resistance (ESR) along with the VSI's equivalent loss resistance. For the purpose of stability analysis, the study will assume that the filter and converter ESR is negligible. This assumption is made to evaluate the system under the least stable conditions, as the presence of this resistance would introduce damping, thereby expanding the region of stability. The currents flowing through the inductor, capacitor, and load are designated as i_L , i_C , and i_O , respectively. The voltage across the capacitor, v_C , serves as the controlled variable in this system.

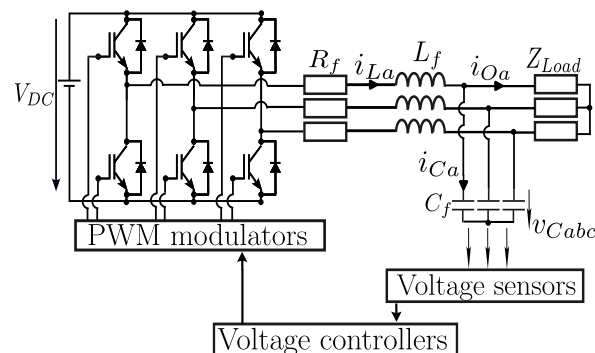


Figure 1. Three-phase VSI with LC filter and controllers.

Figure 2 illustrates a simplified block diagram representing the system's operation within a stationary reference frame, featuring a single-loop voltage control mechanism with capacitor voltage decoupling. In Figure 2, the system's plant model is represented in the s -domain, whereas the voltage controller $G_v(z)$ and the computational delay are depicted in the z -domain. The control loop reference signal is denoted as $V_{C\alpha\beta}^*$, while the actual measured capacitor voltage is $V_{C\alpha\beta}$. The inductor current and capacitor current are represented as $I_{L\alpha\beta}$ and $I_{C\alpha\beta}$, respectively. The output current, $I_{O\alpha\beta}$, is treated as a disturbance affecting the system. The converter's output voltage is expressed as $V_{i\alpha\beta}$. The plant model for the voltage controller is

$$G_{pv}(s) = \left. \frac{V_{C\alpha\beta}}{V_{i\alpha\beta}} \right|_{I_{O\alpha\beta}=0} = \frac{\omega_n^2}{s^2 + \omega_n^2}, \quad (1)$$

where

$$\omega_n = \frac{1}{\sqrt{L_f C_f}}. \quad (2)$$

ω_n is the natural frequency of the filter expressed in rad/s. A one-sample-period delay, T_s , also known as the computational delay, accounts for the time needed for signal sampling

and computational processes. For analysis in the discrete-time domain, the computational delay is represented by z^{-1} . The impact of PWM is considered by discretizing the plant using a zero order hold (ZOH) method. This method allows for a discrete-time analysis that fully incorporates the delay effect associated with the PWM. The resulting discrete-time transfer function of the plant, using the ZOH discretization method, is

$$G_{pv}(z) = \frac{(z+1)(1-\cos(\omega_n T_s))}{z^2 - 2z \cos(\omega_n T_s) + 1}. \quad (3)$$

The voltage control loop uses a PR controller specifically tuned to the fundamental frequency of 400 Hz (being denoted by f_o). The continuous-time domain expression of the PR controller is given by

$$G_{PR}(s) = K_{PV} + K_{RV} \frac{s}{s^2 + \omega_0^2}. \quad (4)$$

ω_0 is expressed in rad/s. The term K_{PV} represents the proportional gain, while K_{RV} is the resonant gain. To convert the controller for use in a discrete-time system, the Tustin method is applied. Using prewarping at the resonant frequency ensures the discrete-time controller preserves a high gain at such frequency. As outlined in [18], this approach ensures that the resulting digital controller closely mirrors the performance characteristics of its original analog version. This gives the discrete-time transfer function shown below.

$$G_v(z) = K_{PV} + K_{RV} \frac{\sin(\omega_o T_s)(z^2 - 1)}{2\omega_o(z^2 - 2z \cos(\omega_o T_s) + 1)}. \quad (5)$$

For stability analysis, a PR voltage controller can be approximated as a simpler proportional controller [16], since the resonant component of the PR controller only influences the vicinity of the fundamental frequency.

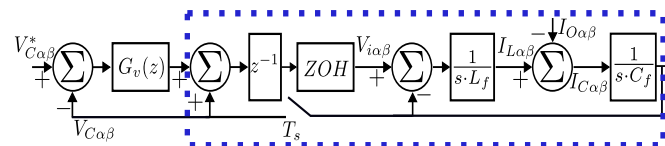


Figure 2. Block diagram of a single-loop voltage control system with unitary decoupling of the capacitor voltage. The plant, PWM and computational delay models are delimited by the dotted box.

3. The 400 Hz PR Voltage Controller Design

The investigation presented in the following sections focuses on a voltage control strategy specifically designed for a 400 Hz GPU, operating under the notable condition of a low switching-to-fundamental frequency ratio (approximately 10–15). The natural frequency of the filter must maintain sufficient separation from the switching frequency to ensure adequate attenuation of harmonics ($f_n < f_{sw}$). In addition, it must also remain separated from the fundamental frequency ($f_n > f_o$). Therefore, an LC filter should be designed to satisfy the condition $f_o < f_n < f_{sw}$. In power electronic applications, converters typically operate at low switching frequencies to minimize power losses. A specific example can be found in GPUs for aerospace applications, which operate at power levels in the hundreds of kW. In these systems, the switching frequency is generally limited to 2.5–5 kHz to reduce switching losses, while the fundamental frequency (f_o) is 400 Hz. Even when applying a double update strategy ($f_s = 2f_{sw}$), the filter's resonant frequency must remain sufficiently separated from the fundamental frequency. For example, with $f_o = 400$ Hz, $f_{sw} = 2.5$ kHz, and $f_s = 5$ kHz, the value of $f_s/6$ is approximately 833 Hz. In this case, to ensure proper separation from the fundamental frequency ($f_n > 3f_o$), a filter with a resonant frequency of at least 1 kHz–1.2 kHz is recommended. As a result, it becomes almost

inevitable to operate above $f_s/6$. Thus, the filter must be designed with a natural frequency above $\frac{f_s}{6}$. Furthermore, to effectively attenuate switching harmonics, it is advisable to operate with $f_n < \frac{f_s}{3}$ (i.e., $f_n < \frac{2f_{sw}}{3}$). Consequently, the filter should be designed to operate within the range $\frac{f_s}{6} < f_n < \frac{f_s}{3}$. Therefore, to obtain a resonant frequency in that range, multiple combinations of L_f and C_f are valid. Table 1 shows the parameters to fulfil this requirement.

Table 1. Nominal system parameters.

Component	Value
Filter Inductor	$L_f = 2.5 \text{ mH}$
Filter Capacitor	$C_f = 5 \text{ } \mu\text{F}$
Converter and inductor	$0 \text{ } \Omega$ (for control design)
ESR (R_f)	$1 \text{ } \Omega$ – $3 \text{ } \Omega$ (for experiment)
Natural Frequency	$f_n = 1423 \text{ Hz}$
Switching Frequency	$f_{sw} = 5000 \text{ Hz}$
Sampling Frequency	$f_s = 5000 \text{ Hz}$
Line-to-Line Voltage	200 V
DC Bus Voltage	400 V

In Section 3.1, the stability region applicable to the designated 400 Hz GPU under investigation is determined. In Section 3.2, the selection of the PR controller gain is explained. The system without load will be analyzed because it is worth noting that if a load with a resistive component is used, additional damping will occur, leading to larger stability regions. As a result, the stability regions used here represent the worst-case scenario in this specific design case application in the context of 400 Hz GPU.

3.1. Stability Region

The system under study has a natural frequency $f_n < \frac{f_s}{3}$, so capacitor voltage unitary decoupling is now considered for the single-loop capacitor voltage control analysis. In a single-loop voltage control with a PR controller, unitary decoupling of the capacitor voltage makes it possible to use positive proportional gains when the filter's natural frequency is below $f_s/3$, while always maintaining a minimum-phase system. In [17], the closed-loop transfer function of the system of Figure 2 is analyzed and it is concluded that the stability region for the single-loop voltage control with capacitor voltage decoupling is

$$\begin{cases} 0 < f_n < \frac{f_s}{4} & \rightarrow 0 < K_{PV} < 1 \\ \frac{f_s}{4} < f_n < \frac{f_s}{3} & \rightarrow \frac{3 \cos(\omega_n T_s)}{\cos(\omega_n T_s) - 1} < K_{PV} < 1 \\ \frac{f_s}{3} < f_n < \frac{f_s}{2} & \rightarrow 1 < K_{PV} < \frac{3 \cos(\omega_n T_s)}{\cos(\omega_n T_s) - 1} \end{cases} \quad (6)$$

In [17], the value of proportional controller gain K_{PV} is chosen primarily to facilitate a direct comparison of the system's performance with and without decoupling. In this paper the K_{PV} gain is selected to obtain maximum damping. This damping-focused selection then directly determines the optimum gain, uniquely configured for the requirements of each specific design scenario.

3.2. Root Locus and Selection of the PR Controller Gains

To simplify the complex process of selecting the optimal gain from the available closed-loop poles, the system's damping property is used as the definitive benchmark. In [17], the authors present the range of allowable gains, but they do not explain how to select the

optimum gain in order to provide a maximally damped system. In this paper, it is explained how to select the gain in order to achieve the maximum admissible damping. The gain selection process that allows achieving the maximum admissible damping is based on the understanding of the system's root locus. The parameters outlined in Table 1 are considered to explain the proposed method. Figure 3a shows the root locus of the single-loop voltage control with capacitor voltage unitary decoupling that employs a PR controller tuned at 400 Hz with a ratio $\frac{K_{RV}}{K_{PV}} = 30$. Appropriate selection of the resonant action is important for the proper operation of the PR controller, since excessive resonant action will create unnecessary deviation in the root locus [17]. As can be seen in Figure 3a, there are five open-loop poles and three zeros. The open-loop pole caused by the computational delay is consistently located at $z = 1$ (without decoupling it is at $z = 0$), whereas the open-loop zero resulting from the plant's discretization continues to lie at $z = -1$. The PR controller adds a pair of complex conjugate poles and a pair of complex conjugate zeros near $z = 1$, which are responsible for its resonance at 400 Hz. The open-loop complex conjugate poles of the LC filter are outside the unit circle, making the open-loop system unstable. Using the parameters listed in Table 1, it can be concluded that the filter's natural frequency falls within the second range specified in expression (6), where f_n lies between $f_s/4$ and $f_s/3$. As can be concluded from (6), the decoupling of the capacitor voltage implies that, when $f_n > \frac{f_s}{4}$, the open-loop system is unstable (K_{PV} must be greater than a certain value above 0). The use of (6) lead to a stable gain interval of $0.532 < K_{PV} < 1$. This gain interval is related to the complex conjugate poles of the LC filter, which must be inside the unit circle for system stability. As can be seen in Figure 3a, the only two loci that influence the system's damping are the green and blue loci (located on the left semicircle), which are associated with the LC filter. Therefore, system stability and achievable damping are both related to the position of the complex conjugate poles of the LC filter. Based on the root locus presented in Figure 3a, the trajectories described by the blue and green loci indicate that the achievable damping is very limited. The selected gain is chosen to achieve the highest possible damping. It is concluded that the proportional gain that allows achieving the maximum damping is $K_{PV} = 0.827$. The tuning of the PR controller and the damping achieved can be seen in Table 2. The closed-loop poles and zeros of the system with this tuning of the PR controller can be seen in Figure 3b. The zoomed view in Figure 3b demonstrates that the controller introduces zeros that remain within the unit circle, indicating a minimum-phase system. As a result, the issue that arises with the case of no decoupling when $f_n < \frac{f_s}{3}$ is resolved.

Figure 4 shows the closed-loop frequency response of the system for the range of allowable gains defined by expression (6). As shown in the reference tracking transfer function (Figure 4a), the voltage controller exhibits a gain of 0 dB (unity gain) and a phase of 0° at the fundamental frequency of 400 Hz, demonstrating its capacity to achieve zero steady-state error at this frequency. As observed in Figure 3b, the designated closed-loop poles of the LC filter, indicated by the two blue crosses on the left semicircle, provide a limited amount of damping. The consequence of this is evident in the frequency response shown in yellow in Figure 4, where maximum damping occurs at the resonant frequency of the LC filter. But the resonance is not completely attenuated, as can be seen in Figure 4b. Figure 4b demonstrates that the selected gain allows one to achieve the maximum damping. The green and blue closed-loop frequency responses are associated with proportional controller gains that are close to the maximum and minimum admissible proportional gains, while the yellow closed-loop frequency response is associated with the optimum PR voltage controller proportional gain within the allowable interval. The optimal frequency response, shown in yellow color, demonstrates a significant improvement in damping the resonance

in comparison with all other frequency responses demonstrated in Figure 4b. The damping is lower (higher resonance) when K_{PV} is higher and lower than the optimum K_{PV} .

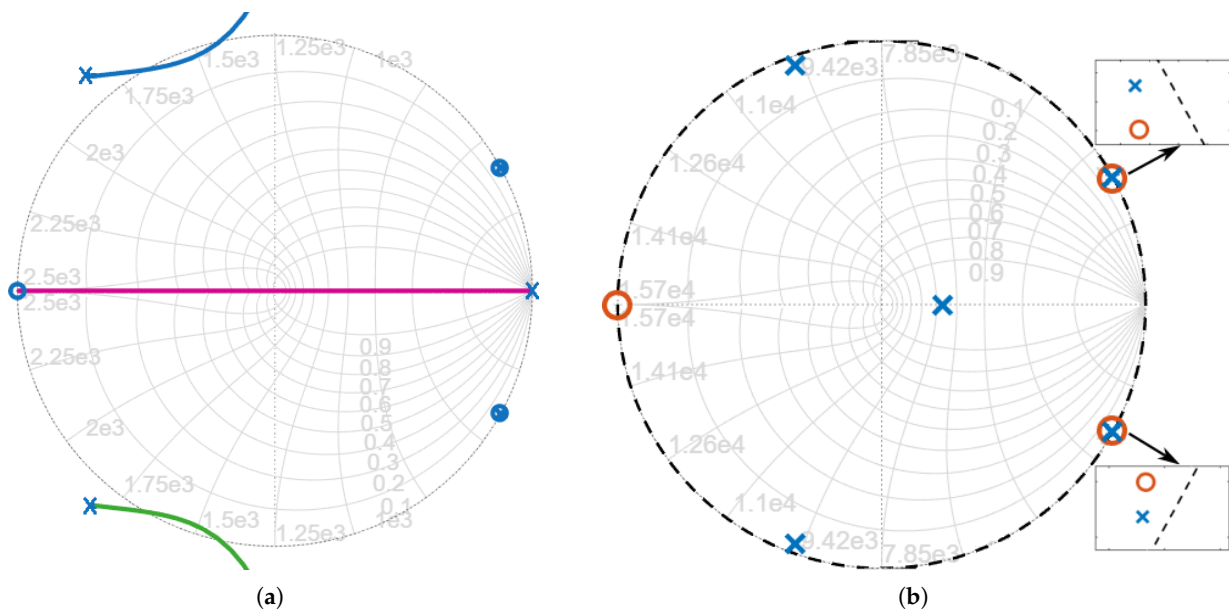


Figure 3. Root locus of the single-loop voltage control with PR controller and unitary decoupling of the capacitor voltage for the system of Table 1 with fundamental frequency of 400 Hz. (U) Loci of the system with positive proportional gains K_{PV} . (b) Locations of the selected closed-loop poles based on the gain selection criteria.

Table 2. Profile of the 400 Hz PR voltage controller with capacitor voltage decoupling.

Parameters	Values
K_{PV} of PR controller	0.827
K_{RV} of PR controller	30
Highest damping of LC filter resonance	0.0183

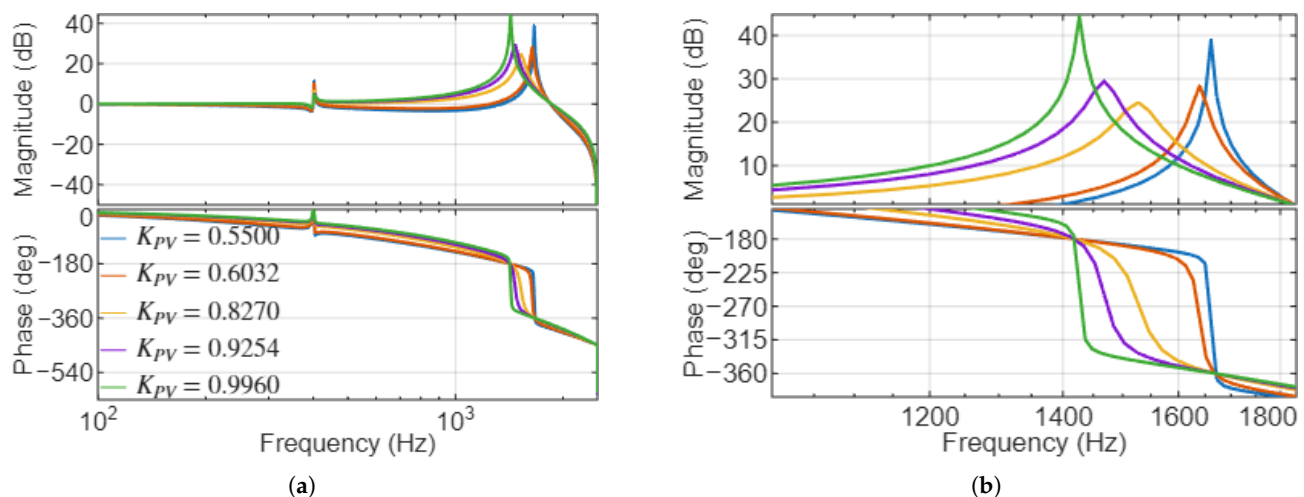


Figure 4. Closed-loop frequency responses of the single-loop voltage control with PR controller and unitary decoupling of the capacitor voltage for different proportional gains, including the resonant action at 400 Hz. (a) Full discrete frequency range. (b) Zoomed frequency range around LC filter resonance.

4. Simulation and Experiment

4.1. Simulation

The MATLAB/SIMULINK R2026A environment was used to perform the simulations. The specifications outlined in Table 1 are used. The specifications in Table 2 are used for the controllers. To evaluate the system's ability to follow a target value, its reference tracking performance was tested. This was achieved without any load connected, by suddenly changing the desired capacitor voltage. The results of the 400 Hz GPU system with capacitor voltage decoupling exhibit a fast transient response, as expected. Figure 5 shows the system's dynamic response to a step change in the voltage reference under no-load conditions, highlighting the capacitor voltage waveform with decoupling.

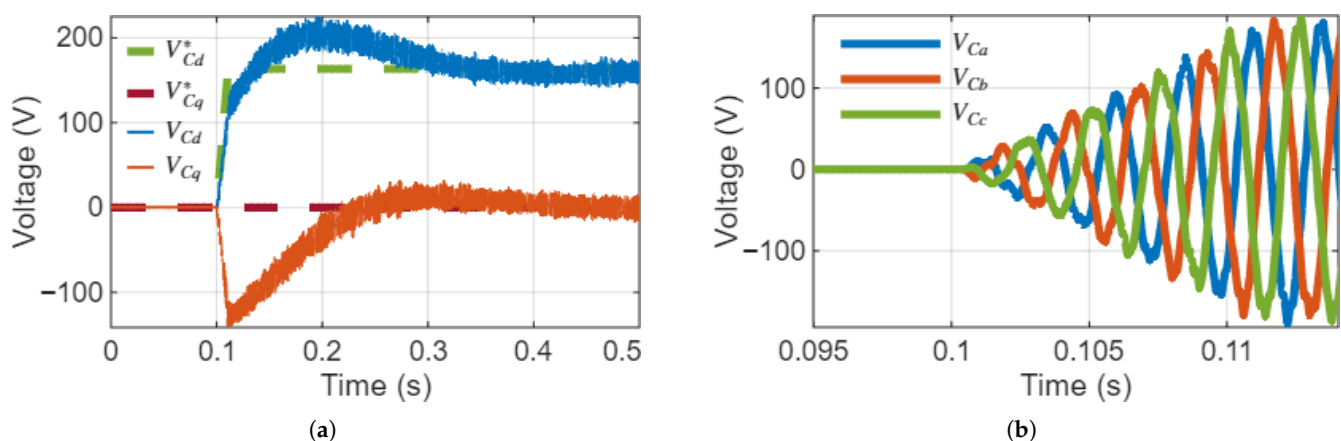


Figure 5. Simulation results for the case of the 400 Hz system with decoupling for a reference step under no load. (a) Capacitor phase voltages in dq reference frame. (b) Capacitor phase voltages in abc reference frame.

As can be seen in Table 2, the proportional gain of the PR controller with capacitor voltage decoupling is chosen to be the optimal gain based on the damping performance outlined in the gain selection criteria. This results in a better transient response in terms of overshoot, settling time of the capacitor voltage and voltage tracking as shown in Figure 5. The zeros in Figure 3 are observed to be located within the stable region of the unit circle. Therefore, a relatively fast transient response is expected due to the minimum-phase system behavior. As shown in Figure 5a, the direct (d) and quadrature (q) axis components of the capacitor voltage successfully exhibit this behavior. The zoomed view of capacitor phase voltages in abc reference frame is shown in Figure 5b.

Analysis of the disturbance rejection capability was conducted through connecting a $100\ \Omega$ resistive load. Figure 6 shows what happens when the R load is connected to the system at time $t = 0.5\text{ s}$ in terms of the disturbance rejection capability. When the load is connected, the reference tracking is still maintained very well. As can be seen, while there is a small variation in the d component of the voltage during stand-alone operation, it does not degrade the overall performance of the voltage regulation maintained by the PR controller. Figure 6a,b show the capacitor voltage and the load current at the time of the connection event. As can be seen, a slight decrease in the capacitor voltage is observed.

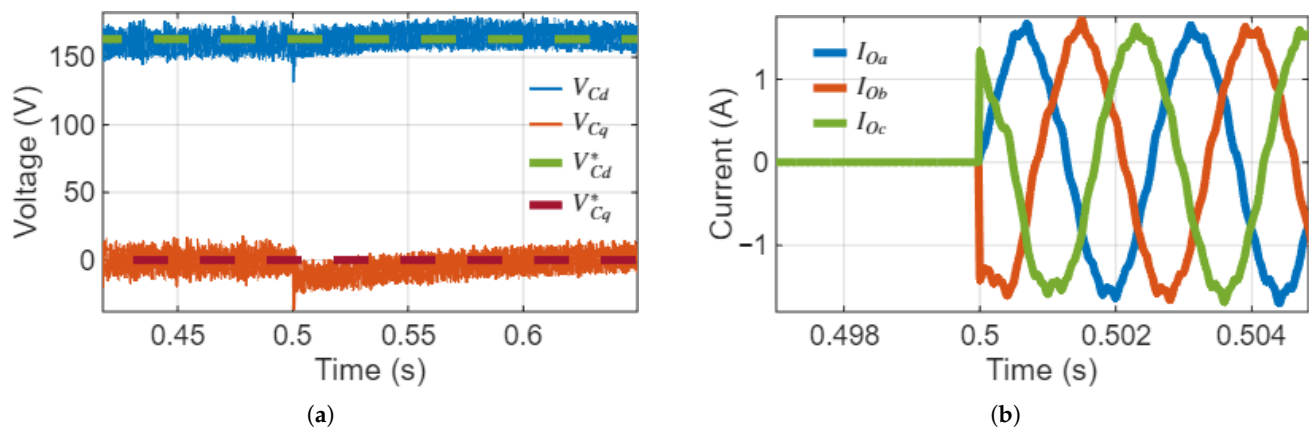


Figure 6. Simulation results for a load step change for the single-loop voltage control in the 400 Hz GPU using PR controller with capacitor voltage decoupling during the connection of the R load. (a) Capacitor phase voltages in dq reference frame. (b) Load phase currents in abc reference frame.

4.2. Experiment

The experimental equipment used for the validation of the proposed method is shown in Figure 7. The equipment was configured using a dSPACE 1202 platform with the ControlDesk experiment software environment. A three-phase, two-level inverter was used for the experiment. The developed control algorithm was implemented using dSPACE. To achieve a more accurate data acquisition, the ControlDesk software environment was used to capture signals. This method provided less switching noise than a conventional oscilloscope and yielded measurements with substantially higher fidelity. The LC filter described in Table 1 was used in the experiment. The switching and sampling frequencies were chosen to be the same as those in the simulation, both set at 5 kHz. For this particular filter arrangement, a 400 V DC bus was chosen to provide the required voltage for the proper operation of the VSI with 400 Hz fundamental frequency. The system's ability to track a reference signal was assessed by introducing a sudden 163.3 V change to the peak capacitor phase voltage setpoint, all while the system was not connected to the load. The experimental results demonstrate that a fast transient response was obtained for the 400 Hz GPU by applying the proposed gain selection criteria for the unitary decoupling of the capacitor voltage. The disturbance rejection test was conducted by using a manual switch to connect a resistive load of 100 Ω to the system. The proposed controller's performance was then evaluated by monitoring the capacitor voltage in the dq and abc reference frames. This test revealed how effectively the controller adapted to the connected load.

The PR controller was tuned for a fundamental frequency of 400 Hz by applying the proposed method to its proportional and resonant components, using the data from Table 2. The no-load step response of the capacitor's dq -frame voltages is depicted in Figure 8a. Upon applying a step to the d -axis reference, V_{Cd}^* , at $t = 0.1$ s, the measured voltage V_{Cd} exhibits a swift and stable response, settling at the reference value after a brief overshoot. Specifically, the absence of an initial inverse response in V_{Cd} validates the system's minimum-phase characteristics. The controller also demonstrates robust regulation by quickly suppressing the transient induced in the q -axis voltage, V_{Cq} . Figure 8b shows the capacitor phase voltages in abc reference frame under a no-load reference step.

Figure 9a,b demonstrate the disturbance rejection test conducted when connecting the resistive load to the terminals of the filter capacitor. As seen in Figure 9a, at $t = 0.5$ s, the load is connected to the system, causing a small drop in the d -component of the capacitor voltage. However, the controller quickly adapts to the designated reference value. This rapid adoption arises from selecting an optimal controller gain for the proportional

component of the PR voltage controllers. Figure 9b presents the experimental results for the three-phase load current, demonstrating the system's dynamic performance under a sudden load disturbance. Prior to $t = 0.5$ s, the system operates under no-load conditions, and the load current is zero. When the $100\ \Omega$ resistive load is connected directly to the terminals of the LC filter capacitor at $t = 0.5$ s, a minor, well-damped transient is observed, after which the currents rapidly converge to a balanced, sinusoidal steady-state waveform with a peak amplitude of approximately 1.5 A. The smooth and swift transition from no-load to full-load conditions, with minimal overshoot and a fast settling time, validates the robustness and effective disturbance rejection capability of the PR voltage controller that was designed based on the proposed method.

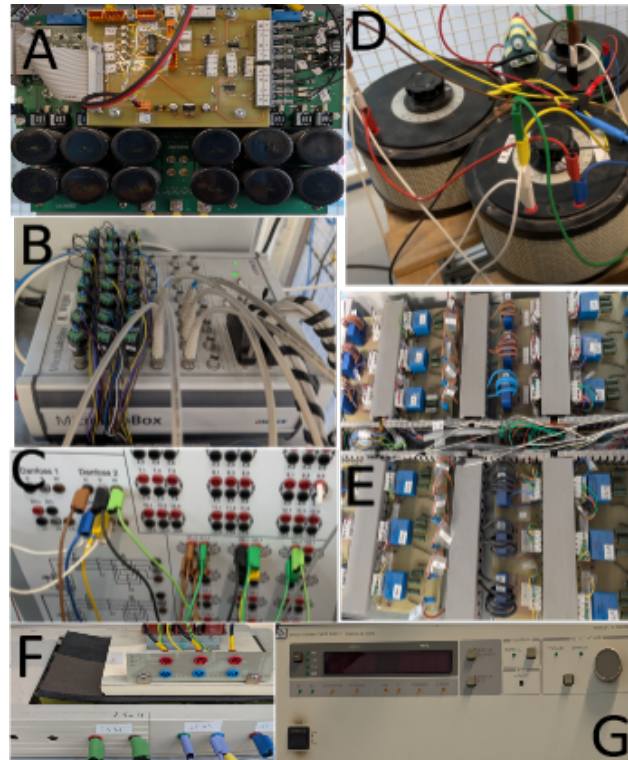


Figure 7. Experimental setup of the 400 Hz LC-filtered VSI. (A) Inverter, (B) dSPACE MicroLabBox, (C) front input interface to acquire analog signals, (D) load with the capacitor modules, (E) voltage sensors, (F) inductor modules and (G) power supply.

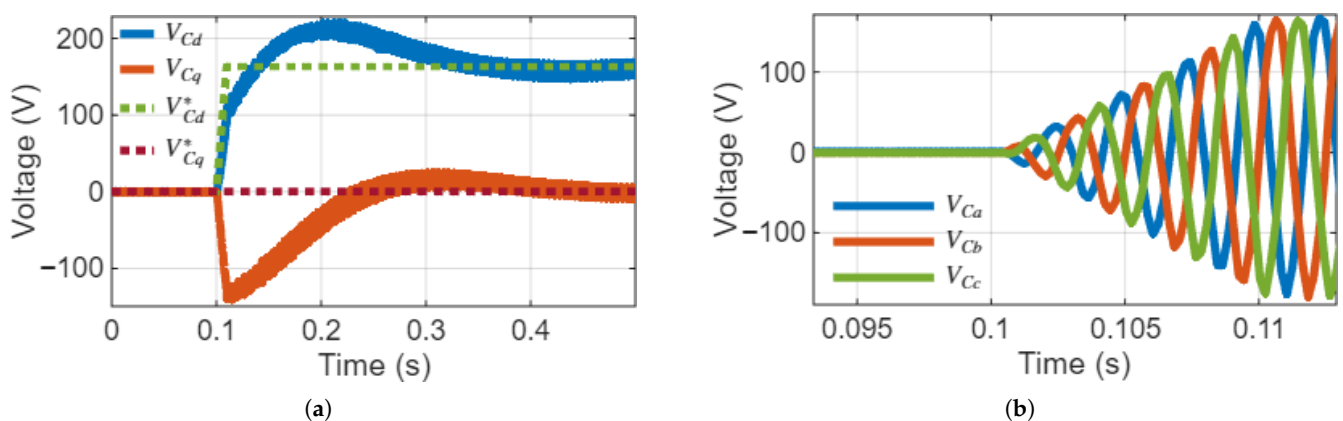


Figure 8. Experimental capacitor phase voltages under a no-load reference step: (a) in the dq reference frame, (b) in the abc reference frame.

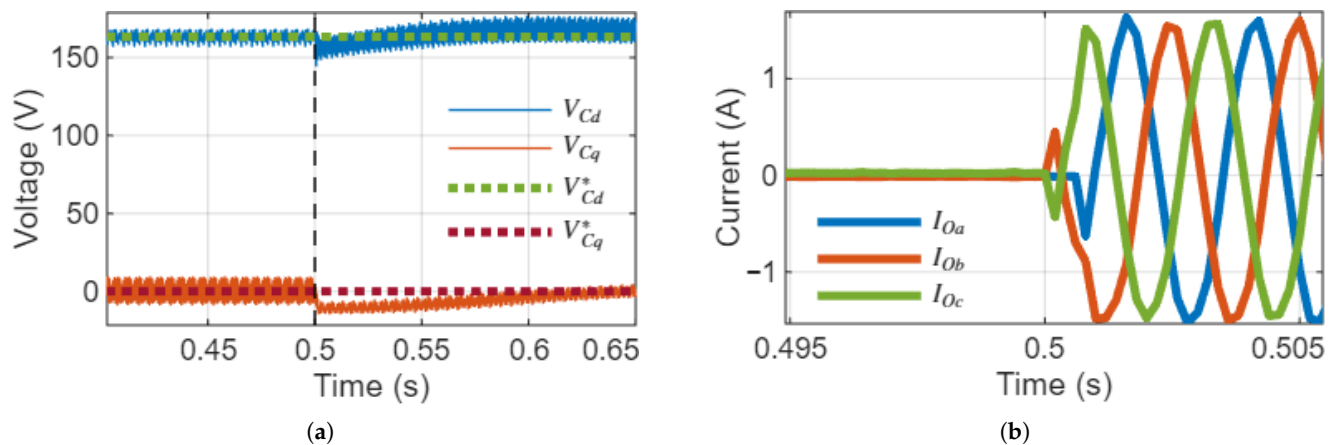


Figure 9. Experimental disturbance rejection during a resistive load connection: (a) Capacitor phase voltages in the dq reference frame. (b) Load phase currents in the abc reference frame.

5. Conclusions

This paper developed a voltage control strategy for 400 Hz VSI equipped with LC filters, specifically designed to meet the rigorous demands of GPU applications. To address the specific challenges highlighted in the Introduction, namely the stability limitations imposed by a low switching-to-fundamental frequency ratio and digital implementation constraints, the proposed control architecture employs a single-loop PR controller enhanced with capacitor voltage unitary decoupling. This configuration allows the system to be tuned for the highest possible damping, providing a robust solution where conventional tuning methods face limitations due to bandwidth constraints. A key contribution of this work is resolving the stability gap associated with LC filters in implementations; the unitary decoupling of the capacitor voltage significantly enhances the dynamic response, enabling stable operation with positive proportional gains even when the filter's natural frequency lies in the critical range of $\frac{f_s}{6} < f_n < \frac{f_s}{3}$. Consequently, this approach ensures a minimum-phase system is achieved, avoiding the right-half plane zeros that typically characterize designs relying on negative proportional gains in this region. Both simulation and experimental results confirm that this method effectively mitigates the identified control challenges, ensuring accurate AC voltage regulation under the realistic operating conditions of 400 Hz GPUs.

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Conflicts of Interest: The authors declare no conflicts of interest.

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