

Article

Full-Bridge Intermediate-Frequency Converter with Low Voltage and Current Stress on Auxiliary Switching Devices

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Abstract

The DC converter constitutes a pivotal component within medium-voltage direct current (MVDC) collection systems, performing functions such as voltage boosting, isolation, and power transmission. To accommodate the demand for high-capacity DC converters in MVDC collection systems for new energy sources, a full-bridge medium-frequency converter featuring low voltage and current stress on auxiliary switching devices is proposed. Based on the principles of dual-transformer configuration and component sharing, this converter employs a half-bridge circuit and a full-bridge circuit sharing two switching devices. Utilizing mixed-frequency modulation, the full-bridge main circuit operates at medium frequency to transmit the majority of power, while the half-bridge auxiliary circuit regulates overall power and voltage through high-frequency chopping control. This achieves zero-current switching for the medium-frequency switching devices across the entire load range, significantly reducing switching losses in the converter. This paper details the converter's operating principles and analyzes key parameter design methodologies. Finally, a 240–6000 V/7200 W prototype was constructed to validate the proposed converter's performance.

Keywords: medium-voltage DC collection; DC converter; mixed-frequency modulation; dual-transformer; zero-current switching



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1. Introduction

With the escalating severity of issues such as the energy crisis, the greenhouse effect, and environmental pollution, new energy sources have garnered widespread global attention and seen increasingly extensive application. According to the China Power Industry Annual Development Report 2023 [1], China's electrification process is projected to enter a mid-term transition phase by 2030, accelerating the pace of green and low-carbon transformation in the power sector. Non-fossil energy sources will account for approximately 60% of installed power generation capacity, contribute nearly 50% of total electricity generation, and provide around 90% of the incremental electricity demand growth across society. As renewable energy generation capacity continues to expand both domestically and globally, technologies for aggregating and transmitting this energy have garnered significant attention. The adoption of Medium-Voltage Direct Current (MVDC) collection for renewable energy generation represents a significant future development direction [2]. As early as

2016, China's National Key R&D Program for Smart Grids established a dedicated project titled 'Research and Development of Key Technologies and Equipment for DC Step-Up Collection and Grid Integration of Large-Scale Photovoltaic Power Stations' within its inaugural batch of initiatives [2,3].

The core equipment for MVDC collection systems in renewable energy generation is the high-power, high-voltage-ratio DC converter, which elevates the DC from the renewable energy side to the medium-voltage DC level. In high-power applications, IGBTs serve as the primary power devices. Achieving Zero Current Switching (ZCS) in IGBTs is crucial for reducing switching losses, enhancing efficiency, and enabling more effective utilization of renewable energy [4]. Parameters such as the converter's input voltage, output voltage, and rated transmission power influence the selection of its fundamental topology, which in turn affects the realization of soft switching in power semiconductor devices [5]. Researchers worldwide have conducted extensive studies on DC boost converters, including LC resonant converters [6–8]. Reference [9] comprehensively considered semiconductor device selection and arrangement, resonant capacitor selection and structural layout, and high-power high-frequency transformer design. It theoretically designed a novel LC series resonant full-bridge converter and conducted loss assessments, predicting efficiencies exceeding 98.5%.

To reduce voltage stress on switching devices, multilevel circuits may be employed [10,11]. In commonly used three-level circuits [12–14], the voltage stress on switching devices is only half the input voltage.

The authors in [15] proposed a dual full-bridge converter based on a dual-transformer structure. This comprises a main circuit and an auxiliary circuit. By designing the transformer turns ratio, the main circuit transmits the majority of the power. The main circuit operates in open-loop mode, whilst closed-loop control of the auxiliary circuit regulates the converter's voltage and power. This approach simplifies control and facilitates ZCS implementation. However, the dual full-bridge configuration increases the number of switching devices and introduces insulation challenges for the high-voltage-side inductors.

The author's work in references [16–20] proposes a multiplexed bridge arm combination ZCS full-bridge converter. Based on the principle of device multiplexing [21–23], by combining two full-bridge circuits to reduce two switches. This achieves zero-current turn-on and turn-off for the main circuit's four switches, whilst the two auxiliary switches enable zero-voltage turn-on and turn-off. It also eliminates the high-voltage-side filter inductor, resolving insulation concerns associated with high-voltage inductors. However, during the auxiliary circuit's mid-voltage-side freewheeling period, it does not transfer energy to the secondary side. This increases unnecessary switch conduction losses and reduces converter efficiency.

In summary, DC/DC converters within new energy MVDC collection systems require substantial capacity. However, high-frequency (typically referring to frequencies significantly higher than line frequency, such as several tens of kHz and above) DC/DC converters struggle to achieve large capacities, necessitating multiple modules in parallel—a solution that incurs higher costs.

This paper proposes a full-bridge medium-frequency converter with low voltage and current stress on auxiliary switching devices. Employing a medium-high frequency hybrid modulation technique, the current waveform approximates a discontinuous trapezoidal wave, significantly reducing current stress on switching components. Furthermore, the transformer operates at a medium frequency of 500 Hz, facilitating the design and manufacture of higher power ratings. Based on dual-transformer and component-sharing principles, power and voltage regulation across the entire converter is achieved by adjusting the duty cycle of the high-frequency switching transistor. Zero-current switching (ZCS) is realized

during both turn-on and turn-off across the full load range, whilst the four main circuit switching transistors operate in a fixed duty cycle mode, offering the advantage of simplified control. By designing the main transformer's step-up ratio such that the main circuit handles the majority of power transfer while the auxiliary circuit manages a minor portion, the current flowing through the high-frequency switching transistors is reduced. This significantly lowers the switching losses within the converter.

2. Transformer Topology and Working Principle

As shown in Figure 1, the proposed full-bridge medium-frequency converter topology features low voltage and current stress on auxiliary switching devices. Transistors Q_1 to Q_4 , transformer T_{r1} , and its leakage inductance L_{t1} form a full-bridge main circuit. The voltage-dividing capacitors C_{in1} and C_{in2} , freewheeling diodes D_{c1} and D_{c2} , switch transistors Q_1 , Q_2 , Q_5 , and Q_6 , transformer T_{r2} and its leakage inductance L_{t2} form an auxiliary half-bridge circuit. Switching transistors Q_1 and Q_2 serve as common switches for both the main circuit and auxiliary branch. The output side comprises a rectifier circuit, with the secondary windings of T_{r1} and T_{r2} directly connected in series to form its input.

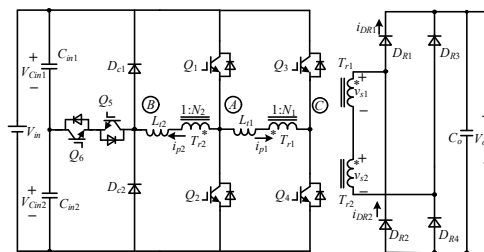


Figure 1. Topology of full-bridge converter with low voltage and current stress.

Figure 2 shows the main operating waveforms of the proposed full-bridge medium-frequency converter with low voltage and current stress on the auxiliary switches. Auxiliary switches Q_5 and Q_6 employ PWM chopping control and operate in high-frequency mode, while Q_1 , Q_2 , Q_3 , and Q_4 operate at 500 Hz. To achieve ZCS, they are driven with a fixed 50% duty cycle rather than PWM control. Q_1 and Q_4 turn on and off simultaneously, while Q_2 and Q_3 turn on and off together. Consequently, the main power circuit operates in an open-loop state, with the entire converter achieving port voltage and power transfer control through the chopping of auxiliary switches Q_5 and Q_6 .

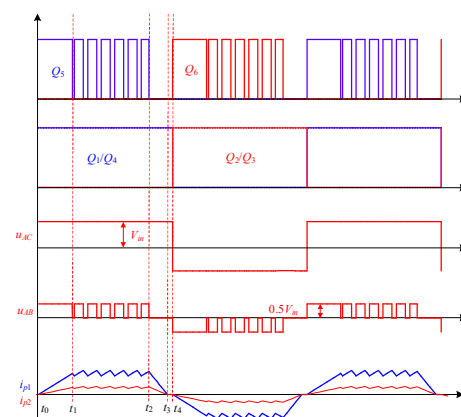


Figure 2. Typical working waveform.

Before detailed analysis, the following assumptions are made:

1. All switches, diodes, inductors, and capacitors are ideal components.

2. The input voltage-dividing capacitors C_{in1} and C_{in2} are equal and sufficiently large, so $V_{Cin1} = V_{Cin2} = V_{in}/2$; capacitors C_{in1} and C_{in2} are equal and sufficiently large.
3. The leakage inductance of transformer T_{r2} is sufficiently small and negligible.

As shown in Figure 2, this converter exhibits four distinct modes within half a medium-frequency switching cycle. These are Mode 1 $[t_0-t_1]$, Mode 2 $[t_1-t_2]$, Mode 3 $[t_2-t_3]$, and Mode 4 $[t_3-t_4]$. Mode 1 $[t_0, t_1]$: The current path for this mode is shown in Figure 3a. Since no current flows through any switching transistors before time t_0 , Q_1 , Q_4 , and Q_5 achieve ZCS turn-on. At this point, the main circuit portion forms a loop consisting of V_{in} , Q_1 , L_{t1} , T_{r1} , and Q_4 . The auxiliary branch forms a loop with V_{in} , Q_1 , L_{t2} , T_{r2} , Q_5 , and the reverse-parallel diodes of Q_6 . The current flowing through switch Q_1 is the sum of the currents in both loops. The equivalent circuit of this mode converted to the secondary side is shown in Figure 4a. In this mode, the voltage between points A and B is $V_{in}/2$. Therefore, the voltage across the secondary winding of auxiliary transformer T_{r2} auxiliary winding voltage is $N_2 V_{in}/2$, the T_{r1} auxiliary winding voltage is $V_o - N_2 V_{in}/2$, and the voltage across the leakage inductance L_{t1} is

$$v_{Lt1} = V_{in} - \frac{V_o - N_2 V_{in}/2}{N_1}, \quad (1)$$

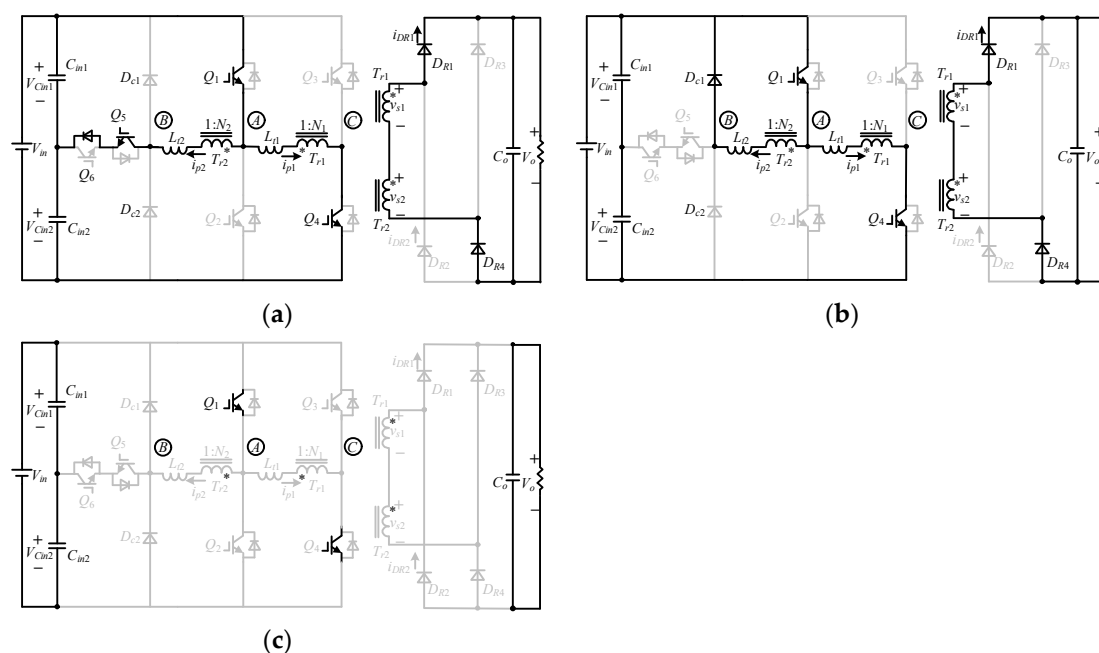


Figure 3. Current flow diagram. (a) Current rise; (b) Current drop; (c) Zero current.

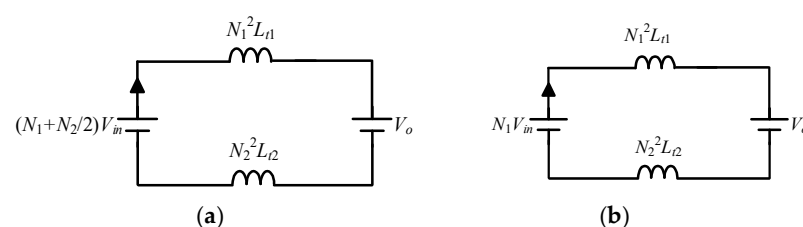


Figure 4. Equivalent circuit. (a) Current rise; (b) Current drop.

The currents flowing into the main transformer and auxiliary transformer, i_{p1} and i_{p2} , respectively, are

$$\begin{cases} i_{p1} = \frac{V_{in} - \frac{V_o - N_2 V_{in}/2}{N_1}}{L_{t1}}(t - t_0) , \\ i_{p2} = \frac{N_2}{N_1} i_{p1} \end{cases} \quad (2)$$

For the current in this mode to rise to its steady-state value, $v_{Lt1} > 0$ must be satisfied, yielding

$$N_1 + \frac{N_2}{2} > \frac{V_o}{V_{in}}, \quad (3)$$

Mode 2 [t_1, t_2]: This mode employs high-frequency chopping via switching transistor Q_5 to oscillate the current near its steady-state value. When high-frequency switching transistor Q_5 is turned on, the current increases linearly, with the current path as shown in Figure 3a. When high-frequency switching transistor Q_5 is turned off, the current decreases linearly. At this time, the current path in the auxiliary branch consists of D_{C1} , Q_1 , L_{t2} , and T_{r2} , while the current path in the main circuit remains unchanged, as shown in Figure 3b. The current flowing through switch Q_8 remains the sum of the two loops. When high-frequency switch Q_5 turns off, the voltage between points A and B equals zero. The equivalent circuit on the secondary side, as shown in Figure 4b, indicates that the voltage across the secondary winding of auxiliary transformer T_{r2} is also zero. Therefore, the voltage across the secondary winding of T_{r1} equals V_o , and the voltage across the leakage inductor L_{t1} is

$$v_{Lt1} = V_{in} - \frac{V_o}{N_1}, \quad (4)$$

To allow the current to fluctuate near its steady-state value, it is necessary to satisfy $v_{Lt1} < 0$, from which we obtain

$$N_1 < \frac{V_o}{V_{in}} \quad (5)$$

Mode 3 [t_2, t_3]: The current path for this mode is shown in Figure 3b. At time t_2 , switch Q_5 turns off, causing the current to decrease linearly. By time t_3 , the current drops to zero. The secondary-side rectifier diodes D_{R1} and D_{R4} naturally turn off. This mode operates identically to Mode 2 when the high-frequency switch Q_5 turns off.

Mode 4 [t_3, t_4]: The current flow diagram for this mode is shown in Figure 3c. Although the medium-frequency switching transistors Q_1 and Q_4 are in the on state, the inductor current remains zero throughout. Time t_4 marks the end of the upper switching cycle and the start of the lower switching cycle. At t_4 , Q_1 and Q_4 achieve ZCS turn-off. After a fixed dead time, Q_2 , Q_3 , and Q_6 achieve ZCS turn-on due to the transformer leakage inductance suppressing rapid current rise.

3. Parameter Design

This section presents parameter design using the following operating parameters: input voltage $V_{in} = 1500$ V, output voltage $V_o = 20$ kV, rated power $P_N = 500$ kW, medium-frequency switching frequency $f_M = 500$ Hz, and high-frequency switching frequency $f_H = 10$ kHz.

(a) Main Transformer Turns Ratio N_1

Assuming no losses during power transmission, the total power transmitted by the converter during the upper half-cycle is obtained from Figure 3 as

$$P_{tot} = \frac{2}{T_s} V_o \int_{t_0}^{t_4} i_{DR1} dt = \frac{2V_o}{T_s} \int_{t_0}^{t_3} i_{DR1} dt, \quad (6)$$

Similarly, the power transmitted by the main circuit is

$$P_m = \frac{2V_{in}}{T_s} \left(\int_{t_0}^{t_3} i_{p1} dt + \int_{t_3}^{t_4} 0 dt \right) = \frac{2N_1 V_{in}}{T_s} \int_{t_0}^{t_3} i_{DR1} dt, \quad (7)$$

From Equations (6) and (7), the ratio of the power transmitted by the main circuit to the total power is

$$\frac{P_m}{P_{tot}} = \frac{N_1 V_{in}}{V_o}, \quad (8)$$

From Equation (8), it can be seen that the proportion of power transmitted by the main circuit is proportional to the main transformer's turns ratio N_1 . That is, the larger N_1 is, the more power is transmitted by the main circuit. Since the switching transistors in the main circuit can achieve ZCS turn-off, it is desirable for the main circuit to transmit a larger proportion of power. Setting $P_m:P_{tot} = 0.9$ yields the condition required for the main circuit to transmit 90% of the power:

$$N_1 = 0.9 \frac{V_o}{V_{in}}, \quad (9)$$

(b) Auxiliary transformer turns ratio N_2

From Equations (3) and (9), we obtain

$$\begin{cases} N_1 + \frac{N_2}{2} > \frac{V_o}{V_{in}} \\ N_1 = 0.9 \frac{V_o}{V_{in}} \end{cases}, \quad (10)$$

Solving the above equation yields the range for N_2 :

$$N_2 > 0.2 \frac{V_o}{V_{in}}, \quad (11)$$

Referring to Figure 2, applying the volt-second balance principle to the leakage inductance L_{t1} of the main transformer during modes 1 and 3 yields

$$\left(V_{in} - \frac{V_o - N_2 V_{in}/2}{N_1} \right) t_{on} + \left(V_{in} - \frac{V_o}{N_1} \right) t_{off} = 0, \quad (12)$$

where t_{on} denotes the time interval from t_0 to t_1 , and t_{off} denotes the time interval from t_2 to t_3 .

From Equation (12), we obtain

$$t_{off} = \frac{\left(N_1 + \frac{N_2}{2} \right) V_{in} - V_o}{V_o - N_1 V_{in}} t_{on}, \quad (13)$$

Based on Equation (13), the total power transmitted by the converter during the upper half-cycle is expressed as

$$P_{tot} = \frac{V_o}{T_s} \left(T_s - t_{on} - \frac{V_{in} \left(N_1 + \frac{N_2}{2} \right) - V_o}{V_o - N_1 V_{in}} t_{on} \right) \sqrt{\left(\frac{V_{in} \left(N_1 + \frac{N_2}{2} \right) - V_o}{N_1^2 L_{t1} + N_2^2 L_{t2}} t_{on} \right)^2 - t_{on}^2}, \quad (14)$$

Neglecting the auxiliary transformer leakage inductance L_{t2} , Equation (14) simplifies to

$$P_{tot} = \frac{V_o}{T_s} \left(T_s - t_{on} - \frac{V_{in} \left(N_1 + \frac{N_2}{2} \right) - V_o}{V_o - N_1 V_{in}} t_{on} \right) \sqrt{\left(\frac{V_{in} \left(N_1 + \frac{N_2}{2} \right) - V_o}{N_1^2 L_{t1}} t_{on} \right)^2 - t_{on}^2}, \quad (15)$$

Solving Equation (15) yields the relationship between the rise time t_{on} and the auxiliary transformer turns ratio N_2 and the main transformer leakage inductance L_{t1}

$$t_{on} = \frac{T_s - \sqrt{T_s^2 - M}}{N_2 V_{in} / (V_o - N_1 V_{in})}, \quad (16)$$

where

$$M = \frac{2T_s L_{t1} N_1^2 N_2 V_{in} P}{V_o (V_o - N_1 V_{in}) \sqrt{((N_1 + N_2/2) V_{in} - V_o)^2 - (L_{t1} N_1^2)^2}}, \quad (17)$$

According to Equations (2) and (16), the steady-state values of the current i_{p1} flowing into the main transformer and the current i_{p2} flowing into the auxiliary transformer are

$$\begin{cases} I_{p1} = \frac{V_{in} - \frac{V_o - N_2 V_{in}}{N_1}}{L_{t1}} \\ \frac{T_s - \sqrt{T_s^2 - M}}{N_2 V_{in} / (V_o - N_1 V_{in})} \\ I_{p2} = \frac{N_2}{N_1} I_{p1} \end{cases}, \quad (18)$$

Equation (18) enables plotting the variation curves of I_{p1} and I_{p2} with respect to the auxiliary transformer turns ratio N_2 and the main transformer leakage inductance L_{t1} , as shown in Figures 5 and 6.

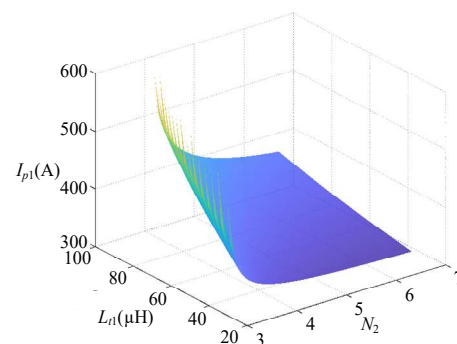


Figure 5. The curve of I_{p1} with N_2 and L_{t1} .

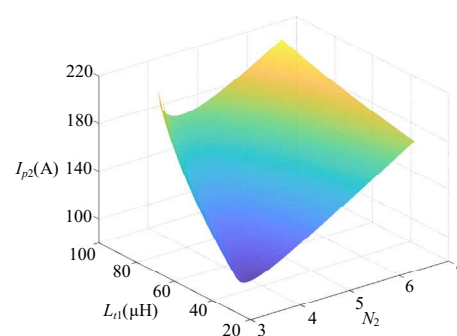


Figure 6. The curve of I_{p2} with N_2 and L_{t1} .

As shown in Figure 5, when $N_2 < 4$, the steady-state value of the current flowing into the main transformer, I_{p1} , decreases rapidly with increasing N_2 . When $N_2 > 4$, the trend of I_{p1} decreases more gradually as N_2 increases. The primary loss source in the power devices of the converter proposed in this paper is the conduction loss of the intermediate frequency switching transistor. Therefore, to reduce the overall loss of the converter, it

is necessary to minimize the conduction loss of the intermediate frequency switching transistor. This requires the steady-state current flowing into the main transformer, I_{p1} , to be as small as possible. Consequently, the turns ratio N_2 of the auxiliary transformer should be set to a larger value. However, as shown in Figure 6, the steady-state current I_{p2} flowing into the auxiliary transformer increases rapidly with the increase in the auxiliary transformer turns ratio N_2 . This leads to a rapid increase in the switching losses of the high-frequency switching transistor. Therefore, N_2 cannot be set too large. After comprehensive consideration, $N_2 = 4$ is selected.

(c) For the leakage inductance L_{t1} of the main transformer

Applying the volt-second balance principle to both ends of the inductance L_{t1} in Mode 2 yields

$$\left(V_{in} - \frac{V_o - N_2 V_{in}/2}{N_1}\right)D + \left(V_{in} - \frac{V_o}{N_1}\right)(1-D) = 0, \quad (19)$$

Solving Equation (19) yields the duty cycle D of the high-frequency switching transistor in mode 2 as

$$D = \frac{2(V_o - N_1 V_{in})}{N_2 V_{in}}, \quad (20)$$

From this, the current ripple ΔI_p during the plateau phase can be calculated. The relationship between V_{in} and L is given by

$$\Delta I_{p1} = \frac{\left(N_1 + \frac{N_2}{2}\right)V_{in} - V_o}{N_1 L_{t1}} \cdot \frac{2(V_o - N_1 V_{in})}{N_2 V_{in}} \cdot \frac{1}{f_H}, \quad (21)$$

According to Equations (18) and (21), the peak currents of i_{p1} and i_{p2} are obtained as

$$\begin{cases} i_{p1_peak} = \frac{\left(N_1 + \frac{N_2}{2}\right)V_{in} - V_o}{N_1 L_{t1}} \left[\frac{(V_o - N_1 V_{in})}{N_2 V_{in}} \cdot \frac{1}{f_H} + \frac{T_s - \sqrt{T_s^2 - M}}{N_2 V_{in} / (V_o - N_1 V_{in})} \right] \\ i_{p2_peak} = \frac{\left(N_1 + \frac{N_2}{2}\right)V_{in} - V_o}{N_1^2 L_{t1}} \left[\frac{(V_o - N_1 V_{in})}{V_{in}} \cdot \frac{1}{f_H} + \frac{T_s - \sqrt{T_s^2 - M}}{V_{in} / (V_o - N_1 V_{in})} \right] \end{cases}, \quad (22)$$

Based on the converter's operating principle, the sum of i_{p1_peak} and i_{p2_peak} represents the peak current flowing through the common switch transistor Q_1 . According to Equation (22), the peak currents i_{p1} , i_{p2} and the peak current i_{Q1_peak} flowing through the common switch transistor Q_1 relative to the leakage inductance L_{t1} as shown in Figure 7.

It can be seen that i_{p1_peak} and i_{p2_peak} and the peak current i_{Q1_peak} flowing through the common switch transistor Q_1 , all exhibit a consistent trend with the variation in the main transformer leakage inductance L_{t1} . They initially decrease and then increase as L_{t1} increases, reaching a minimum at $L_{t1} = 43 \mu\text{H}$. Since i_{p1_peak} and i_{Q1_peak} increase, the conduction losses of the medium-frequency switch transistor also increase, which is unfavorable for its selection. Similarly, the larger i_{p2_peak} becomes, the greater the switching losses of the high-frequency switch transistor. Therefore, it is desirable for all three values to be as small as possible. Hence, $L_{t1} = 43 \mu\text{H}$ is selected.

(d) Selection of Light-Load Switching Power P_s

When the transmitted power decreases, the converter's current waveform reduces overall. Based on $i_{p1(t1)} = \Delta I_{p1}/2$, the critical continuous power is obtained as

$$P_s = \frac{V_o(V_o - N_1 V_{in})(2T_s f_H - 1)}{4T_s L_{t1} N_1^2 N_2 V_{in} f_H^2} \sqrt{(2V_o - (N_2 + 2N_1)V_{in})^2 - (2L_{t1} N_1^2)^2}, \quad (23)$$

When the converter's transmitted power is less than or equal to P_s , the operating frequency of the high-frequency switching transistor is also reduced to 500 Hz.

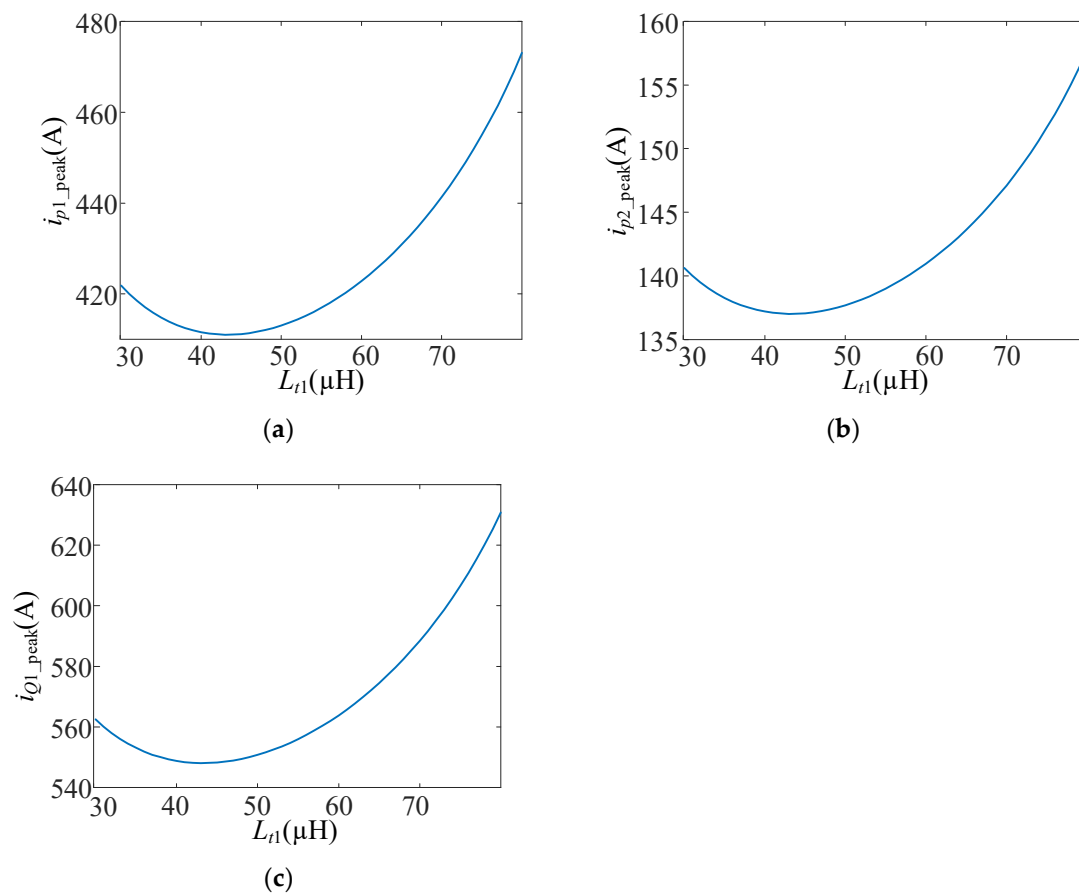


Figure 7. The curve of partial current peak with L_{t1} . (a) The relationship curve between i_{p1_peak} and L_{t1} ; (b) the relationship curve between i_{p2_peak} and L_{t1} ; (c) the relationship curve between i_{Q1_peak} and L_{t1} .

4. Simulation Verification

Based on the results of the parameter design, the converter parameters are obtained as shown in Table 1. To verify the working principle of the proposed converter, its circuit model and thermal simulation model were constructed in PLECS.

Table 1. Simulation Parameters.

Parameter	Symbol	Data
Input voltage	V_{in}	1500 V
Output Voltage	V_o	20 kV
Rated Output Power	P_N	500 kW
Main transformer turns ratio	N_1	12
Auxiliary transformer turns ratio	N_2	4
Main transformer leakage inductance	L_{t1}	43 μH

Figure 8 shows steady-state simulation waveforms under (a) full-load conditions and (b) light-load conditions (15% P_N). The simulation waveforms align with theoretical waveforms.

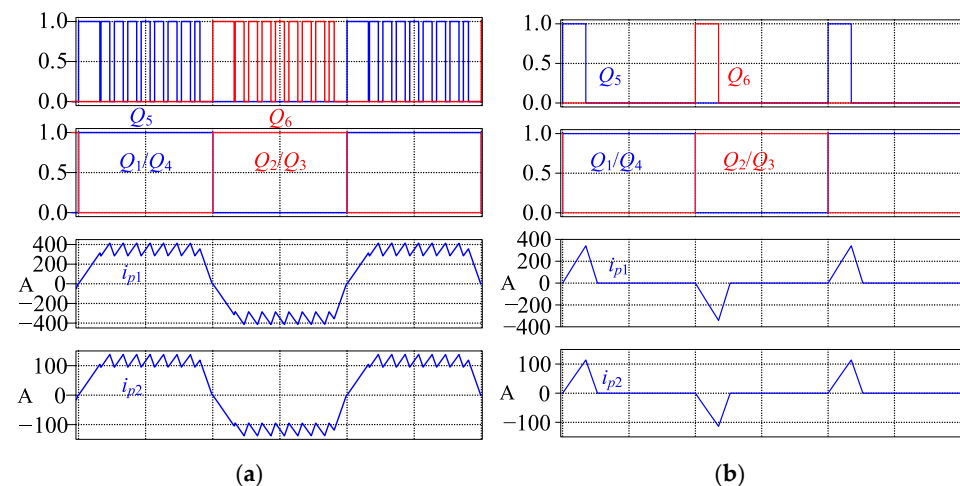


Figure 8. Steady-state simulation waveform of each working condition. (a) Full load; (b) light load.

To verify the soft-switching characteristics of the intermediate frequency switching devices, Figure 9 presents the drive voltages and current waveforms for the main circuit switching devices Q_3 and Q_4 as well as the common switching device Q_1 and Q_2 under full load (100% P_N) and light load (15% P_N) conditions. Before each intermediate frequency switch turns off, the current flowing through it decreases to zero, achieving ZCS turn-off. Before each intermediate frequency switch turns on, the current flowing through it remains zero, and the current rises slowly upon turn-on, achieving ZCS turn-on.

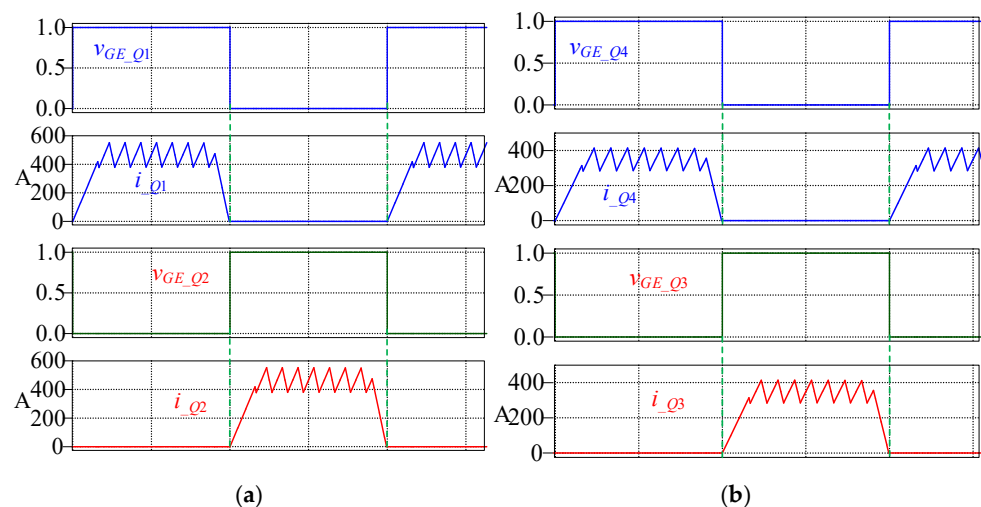


Figure 9. If switch device soft switching waveform. (a) Common switch transistor; (b) main circuit switch transistor.

Based on the simulation results, Table 2 presents the peak and RMS current values flowing into each switching device. Since the main circuit undertakes 90% of the power transfer, the conduction current of each switching device in the main circuit is significantly higher than that of the switching devices in the auxiliary circuit.

To provide a detailed comparison of the loss characteristics of the power devices, device selection and thermal simulations were performed for this converter. For the high-frequency chopping switch, the IKQ120N120CS7 IGBT (Infineon Technologies AG, Neubiberg, Germany) was selected. This IGBT has a maximum RMS current rating of 144 A (@T_c = 100 °C), and its anti-parallel diode is rated for a maximum RMS current of 125 A (@T_c = 100 °C). Therefore, the diodes D_{c1} and D_{c2} can directly utilize the anti-parallel diode

of this IGBT. For the common switch and the main circuit switches, the FF450R33T3E3 (1200 V/450 A, Infineon Technologies AG, Neubiberg, Germany) was chosen.

Table 2. Current through each power device (A).

Device	Peak Current	RMS Current
Q_1/Q_2	552.45	298.02
Q_3/Q_4	414.34	223.74
Q_5/Q_6	138.113	86.10
D_{c1}/D_{c2}	138.113	43.03

By setting the junction temperature of the power devices at a stable 100 °C, the simulated loss results are summarized in Table 3. As can be seen, Q_1/Q_2 and Q_3/Q_4 operate with zero-current switching (ZCS), resulting in negligible switching losses. Although Q_5/Q_6 and D_{c1}/D_{c2} are hard-switched, the current flowing through them is relatively small, so their switching losses account for a low proportion—only 9.7% of the total device losses.

Table 3. Simulation Results of Converter Losses (A).

Device	Conduction Loss	Switching Loss (Reverse Recovery Loss)	Total Loss
Q_1/Q_2	1118.36	0	1118.36
Q_3/Q_4	730.52	0	730.52
Q_5/Q_6	214.20	198.72	412.92
D_{c1}/D_{c2}	50.34	34.56	84.90

5. Experimental Verification

Based on the above theoretical analysis, a low-power experimental platform was constructed to further validate the proposed converter's operating principles and performance, as depicted in Figure 10. Key parameters are shown in Table 4.

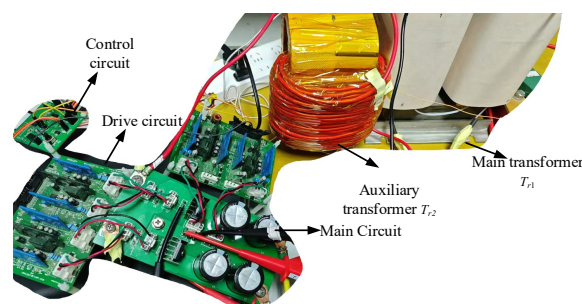


Figure 10. Experimental prototype.

Table 4. Experimental Parameters.

Parameter	Symbol	Data
Input voltage	V_{in}	240 V
Output Voltage	V_o	6 kV
Rated Output Power	P_N	7.2 kW
Main transformer turns ratio	N_1	22
Auxiliary transformer turns ratio	N_2	11
Main transformer leakage inductance	L_{t1}	196 μ H

Figure 11 shows the drive signal v_{GE_Q1} for the shared switch transistor Q_1 under full load (7.2 kW), half load (3.6 kW), and light load (1150 W) conditions, the drive voltage v_{GE_Q5} for the high-frequency chopping switch Q_5 , the current i_{p1} flowing through the main transformer, and the current i_{p2} flowing through the auxiliary transformer. Comparing the waveforms of i_{p1} and i_{p2} under various operating conditions reveals that the peak value of i_{p2} is significantly smaller than that of i_{p1} . This indicates that the currents during hard switching and turn-on of the high-frequency chopping switch Q_5 are very small, resulting in minimal switching losses.

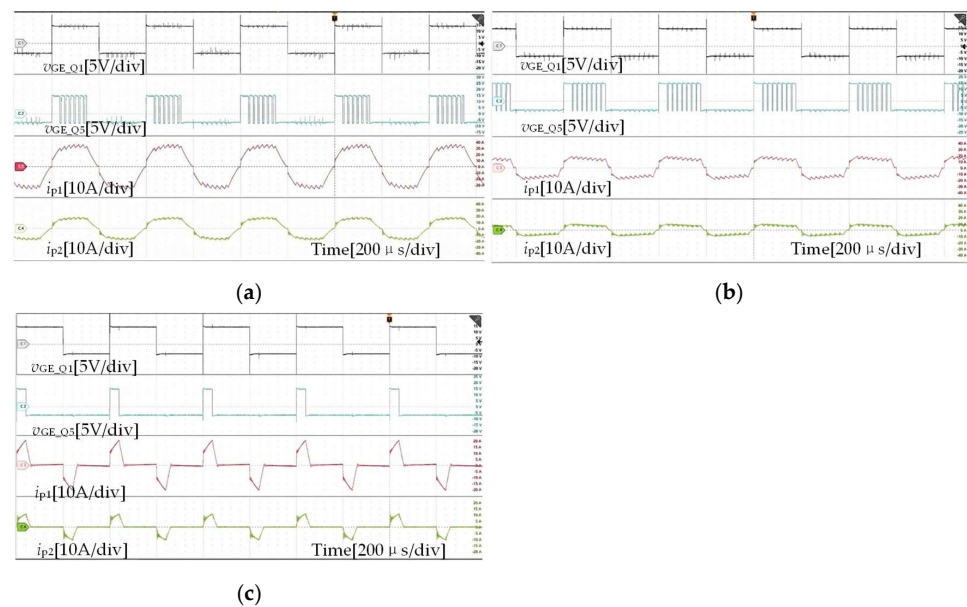


Figure 11. Steady state waveform under each working condition. (a) full load; (b) half load; (c) light load.

The current flowing through the shared switches Q_1 and Q_2 is the sum of the two branch currents. The current flowing through the main circuit switches Q_3 and Q_4 is the main transformer current i_{p1} . Figure 12 shows the terminal voltage v_{Q1} to v_{Q4} and the current waveforms flowing through them under full-load conditions. Observing that i_{p1} and i_{p2} are zero at the switch turn-off instant demonstrates that Q_1 to Q_4 achieve ZCS turn-off.

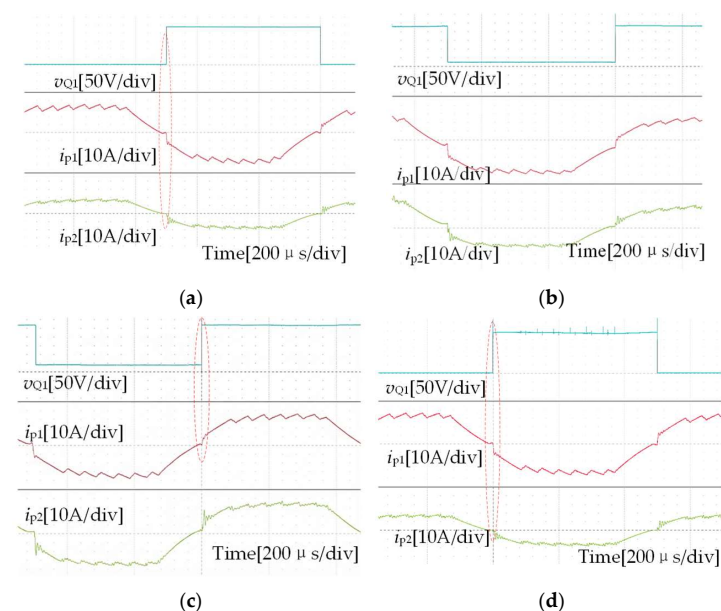


Figure 12. Waveforms of v_Q and current of i_p under full load condition. (a) Q_1 ; (b) Q_2 ; (c) Q_3 ; (d) Q_4 .

Figure 13 shows the terminal voltages v_{Q1} to v_{Q2} of switching transistors Q_1 to Q_4 under light load conditions for the current waveforms and the corresponding current waveforms. Observing that i_{p1} and i_{p2} drop to zero at the switch turn-off instant demonstrates that ZCS turn-off is also achievable for $Q_1 \sim Q_4$ under light load conditions.

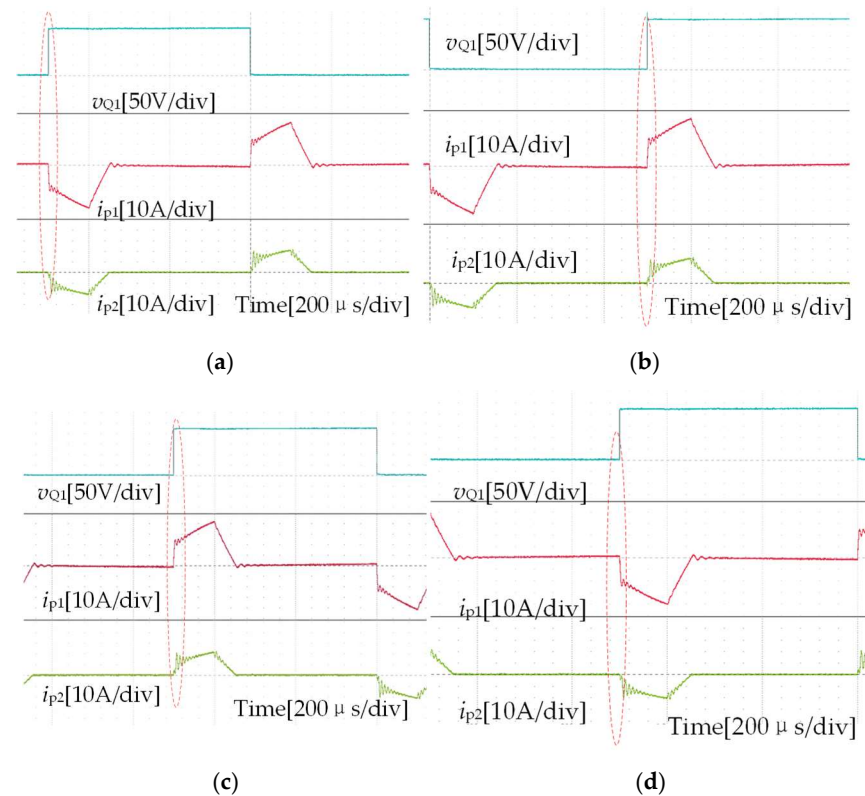


Figure 13. Waveforms of v_Q and current of i_p under light load condition. (a) Q_1 ; (b) Q_2 ; (c) Q_3 ; (d) Q_4 .

Regarding the efficiency characteristics of the proposed converter, prototype efficiency was tested at different output powers. Figure 14 shows the efficiency curves of the converter at various output powers. It can be seen that due to the introduction of an auxiliary branch for small-current high-frequency chopping, combined with the main circuit switches operating in ZCS mode, actual switching losses are minimal. Efficiency exceeds 97% across a wide power range.

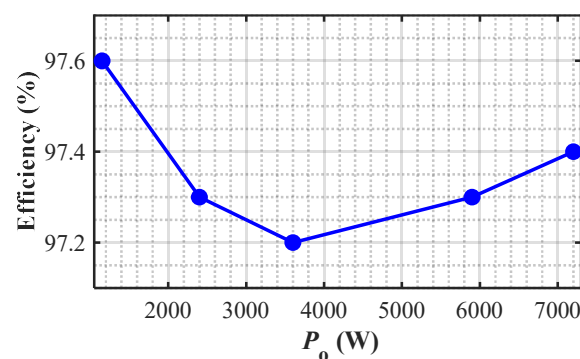


Figure 14. Converter efficiency.

6. Conclusions

This paper proposes a full-bridge medium-frequency converter based on mixed-frequency modulation, featuring low voltage and current stress on the auxiliary switches.

The main work involves integrating a dual-transformer structure and component reuse to construct a main circuit and an auxiliary branch consisting of four medium-frequency switches, two high-frequency switches, and two shared medium-frequency switches.

The key contributions of this scheme are reflected in the following aspects: First, power and voltage regulation of the entire converter is achieved solely by adjusting the duty cycle of the chopper control for the two high-frequency switches in the auxiliary branch. This allows all medium-frequency switches to operate in a fixed duty cycle mode, thereby simplifying the control system. Second, this modulation method enables zero-current switching for both turn-on and turn-off of the medium-frequency switches, effectively reducing switching losses. Furthermore, by rationally designing the turns ratio of the main transformer, the majority of power is transmitted through the main circuit. The auxiliary transformer is designed with a smaller step-up ratio and is responsible for transmitting only a small portion of the power, which helps reduce the peak current of the switches and further improves efficiency.

Finally, experimental studies validate the feasibility and excellent performance of the proposed converter, confirming the correctness of the above theoretical analysis.

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