

Article

Adaptive Harmonic Impedance Control and Flexible Compensation Method for AI Data Centers

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Abstract

The stochastic fluctuations of AI computational loads inject harmonic currents into the DC bus, amplifying bus voltage ripples and weakening the power quality. Existing strategies typically rely on high-gain control strategies to minimize harmonic output impedance, aiming at full absorption of harmonic currents. However, such designs rarely consider engineering constraints such as capacity and current boundaries, which impose inherent limits on harmonic absorption. To address these issues, this paper proposes an adaptive harmonic impedance control and flexible compensation method for AI data centers. By integrating DC bus voltage feedforward with output current feedback, a virtual harmonic impedance control channel is constructed to enable real-time impedance shaping. Then, an adaptive gain regulation mechanism is developed to adjust harmonic impedance according to the available capacity and current margin. Compared with traditional strategies relying on fixed high gains or resonant links, the proposed method allows for the continuous regulation of harmonic impedance over a wide range. This enables the dynamic matching of harmonic absorption capability with the available capacity, effectively suppressing the risks of overcurrent, saturation, and stability degradation. Simulation and 8 kW experimental results verify the correctness and effectiveness of the proposed analysis and control strategy.

Keywords: AI data center; adaptive harmonic impedance; flexible compensation; impedance reshaping

1. Introduction

In recent years, the rapid advancement of artificial intelligence (AI) has driven a continuous increase in the power density and capacity of AI data centers (AIDC) [1–3]. Large-scale GPU/TPU computing clusters exhibit pronounced stochastic and fast-varying load characteristics, which inject wideband harmonic currents into the DC bus [4–7]. This harmonic injection amplifies DC bus voltage ripple, degrades power quality, and poses increasing challenges to the stability and reliability of the power delivery system [8,9].

To mitigate DC bus ripple and absorb harmonic currents, existing research has primarily developed along three technical routes: passive filtering, additional compensation devices, and impedance reshaping.

Firstly, passive approaches, e.g., large electrolytic capacitors or LC filters, are straightforward but suffer from large volume, high cost, and limited effectiveness across wide frequency ranges, which makes them less attractive for high-density AIDC applications [10].



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As for additional compensation devices, one class of research achieves active ripple throughput by constructing additional energy channels, including active capacitor technologies [11–14] and active power decoupling (APD) [15–20]. These methods can significantly reduce DC bus capacitance requirements, but they suffer from complex hardware structures, limited modulation depth, and compensation capabilities that easily reach limits under large-amplitude load disturbances. Another class of research relies on DC active power filters (DC-APF) to reduce bus ripples through harmonic current detection and injection compensation. However, conventional DC-APF is susceptible to measurement noise, filtering-induced phase lag, and DC bus coupling, causing ripple suppression performance and stability to vary with operating conditions. Meanwhile, under severe disturbances or low-frequency pulsations, the required peak compensating current and energy buffering increase, further leading to higher device stress and losses. Ref. [21] introduces a first-order inertial link in the voltage loop to achieve synergy between voltage control and harmonic extraction, but the inertial link may sacrifice dynamic response speed, limiting suppression capability under severe operating conditions. Ref. [22] employs sliding mode active disturbance rejection control to enhance DC-APF disturbance rejection performance and dynamic response, but the complexity of sliding mode chattering and parameter tuning still constrains its engineering application.

Thirdly, with the development of impedance modeling and frequency-domain control theory, harmonic suppression methods based on impedance reshaping have received widespread attention in recent years. These methods realize the diversion and redistribution of harmonic currents by regulating the output impedance in specific frequency bands. Specifically, Ref. [23] incorporates a bandpass filter into the inductor current feedback to increase impedance in the target frequency band, guiding harmonic currents to the bus capacitor. Ref. [24] reduces bus voltage ripples by lowering the output impedance of the bidirectional DC/DC converter (BDC), but the associated optimization algorithms present difficulties in engineering implementation. Ref. [25] proposes an adaptive sliding mode control-based output impedance shaping method that enhances the source-side converter's output impedance at twice the line frequency. However, this approach relies on sparse communication networks and does not account for communication delays. Additionally, the chattering inherent in sliding mode control and the complexity of parameter tuning increase the difficulty of engineering implementation. Ref. [26] proposes a frequency-selective droop strategy to provide high gain at specific frequencies for precise impedance reshaping, but the parameter design is complex. For comparison, this paper summarizes the characteristic differences between typical DC bus harmonic suppression methods in Table 1.

Table 1. Comparison of different DC bus voltage harmonic suppression methods.

Method Category	Additional Power Devices	Adjustable Output Impedance	Risk of Modulation Saturation	Operating Constraints Considered
Passive filtering	×	×	×	×
Additional compensation devices	✓	✓	✓	×
Impedance Shaping	×	✓	✓	×
Proposed method	×	✓	×	✓

Overall, existing active harmonic suppression methods mostly employ high-gain controllers, resonant links, or intelligent optimization strategies to minimize the equivalent harmonic impedance of the compensation device, thereby forming a “low impedance point” on the bus side to absorb harmonic currents. These impedance-shaping methods typically use fixed gains, which result in a fixed equivalent harmonic impedance and, consequently, an unchanged harmonic absorption capability. When the data center capacity continues to expand and load disturbances become more severe, compensation strategies with fixed or excessively high gains easily trigger problems like overcurrent, over-modulation, or control saturation, further causing a reduction in stability margin or even system instability. Therefore, for high-dynamic, high-power-density AIDC scenarios, there is an urgent need for a novel control method that explicitly considers engineering constraints and allows for the flexible regulation of compensation capability.

To bridge the above-mentioned gap, this paper proposes an adaptive harmonic impedance control method for flexible compensation in AIDC. Unlike DC-APF solutions that require additional power devices, the proposed approach reuses the energy-storage BDC already deployed in the data center as the actuator. By integrating DC bus voltage feedforward with output current feedback, a virtual harmonic impedance control channel is constructed to enable real-time impedance shaping. In addition, an adaptive gain regulation mechanism is developed. Different from fixed-gain impedance-shaping methods, the proposed approach adjusts the harmonic impedance according to the converter’s available capacity and current margin, so that harmonic absorption capability can be flexibly allocated while avoiding overcurrent, modulation saturation, and stability degradation. The main contributions are summarized as follows:

- (1) Control framework: An adaptive harmonic impedance control architecture is proposed for AI data center DC buses, which realizes flexible ripple compensation through impedance shaping without requiring additional power devices.
- (2) Constraint-aware regulation: A capacity- and current-margin-aware adaptive gain regulation mechanism is established to continuously tune the equivalent harmonic impedance, enabling dynamic matching between harmonic absorption capability and available converter margins, and improving safety and stability under large disturbances.
- (3) Verification: The simulation and 8 kW experiment results demonstrate that the proposed method can regulate the equivalent harmonic output impedance of the BDC over a wide range, achieving dynamic matching between compensation capability and converter available capacity, and effectively suppressing DC bus voltage ripples while ensuring system stability.

The remainder of this paper is organized as follows: Section 2 details the principle and implementation structure of adaptive harmonic impedance control; Section 3 presents the unified design framework for the adaptive gain coefficient k ; Section 4 verifies the effectiveness of the proposed strategy through simulation and experimental results; Section 5 concludes the paper and looks forward to future work.

2. Proposed Adaptive Harmonic Impedance Control

2.1. Typical Architecture and Control Strategies of AIDC

Figure 1 illustrates a typical DC microgrid power supply topology for AIDC. The system consists of distributed power sources, energy storage units, and AIDC loads. In Figure 1, the 54 V (and 12 V) rails are load-side buses, typically generated by dedicated load-side DC-DC modules in the AIDC power chain. It should be noted that the topology adopted in this paper is not intended for the AI power-supply stage that steps down an 800 V DC bus to 54 V; instead, it is designed for the DC/DC converter in the energy storage

unit within an AIDC architecture. In an AIDC architecture, some DC/DC or AC/DC converters are responsible for regulating and maintaining the DC bus voltage, and these units can be regarded as equivalent DC voltage sources, also called “power source side” [27]. In addition, components such as AI loads, AC loads, DC loads, and certain bidirectional DC/DC converters in energy storage systems typically achieve power regulation by controlling their output currents; these units can therefore be treated as equivalent DC current sources [27]. To reduce DC bus voltage ripples, this paper integrates the ripple suppression function as an additional control objective into the BDC, equipped with active filtering capabilities, achieving “flexible compensation without adding power devices”.

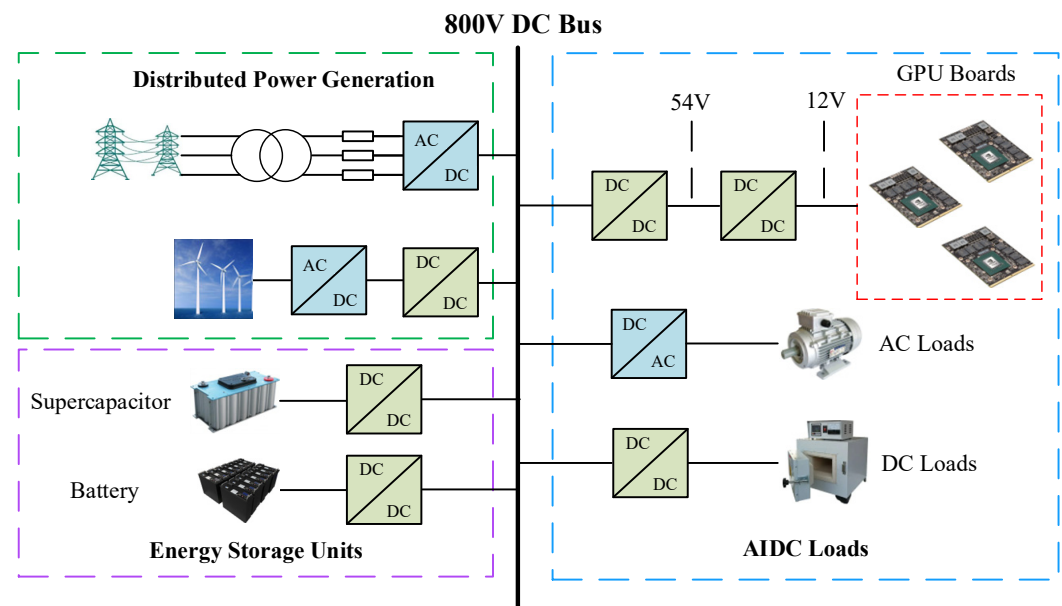


Figure 1. Typical topology of the power supply system in an AIDC.

To enhance power density while balancing low ripple, low loss, and high reliability, BDCs in AIDC typically employ an interleaved parallel structure as the energy hub between the DC bus and the storage side. The basic principle is to electrically parallel multiple identical power phases and apply a fixed phase difference in modulation to drive them interleaved. This increases the equivalent switching frequency on the bus side to N times, significantly reducing inductor current ripple and the ripple current stress on the bus capacitor [28,29]. In addition, advanced interleaved topologies, such as the interleaved cascaded non-inverting buck–boost converter, have also been reported to further improve power density and performance [30]. However, the focus of this paper is the harmonic suppression strategy and its impedance-shaping mechanism. Therefore, to simplify the modeling and highlight the control principle, the converter stage is represented by the simplest three-phase interleaved Buck-based consideration in this work, without loss of generality for the proposed control concept. As shown in Figure 2, the three-phase interleaved parallel BDC consists of three power phases. Each phase includes synchronous half-bridge switching devices S_i and an inductor L_i . The input side connects to the storage voltage u_s , and the output side parallels the DC bus voltage u_{dc} , where C_1 is the input-side capacitor, C_2 is the bus-side capacitor, and i_{L_i} is the inductor current of each phase.

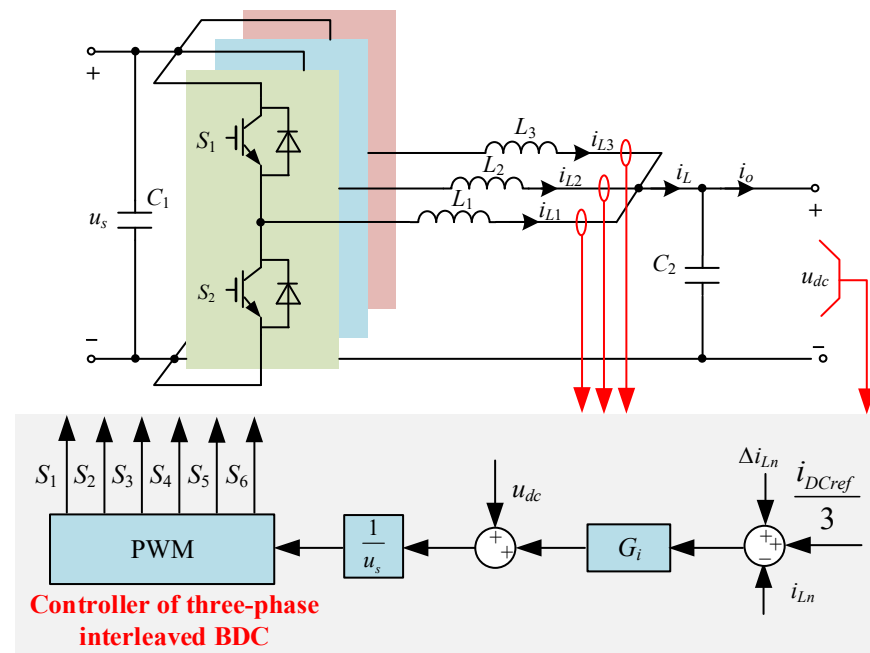


Figure 2. Circuit topology and control strategy of the three-phase interleaved BDC.

In terms of control strategy, this paper adopts the current source control mode shown in Figure 2, using an inductor current closed loop for fast current tracking. A current sharing loop is configured for each phase to ensure $i_{Li} \approx i_{DCref}/N$, where G_i is the current loop transfer function, i_{DCref} is the current reference value, and Δi_{Ln} denotes the current-balancing compensation term. As shown in Figure 3, the three-phase interleaved DC/DC converter adopted in this paper employs three PWM modules to drive and control the three phase legs, respectively. For each phase, the corresponding PWM module triggers the inductor current sampling. The sampling trigger is placed at the peak/valley of the PWM carrier waveform, so that the mid-point value of the phase inductor current can be captured, and this sampled value is used as the feedback signal for control. Interleaved modulation is achieved by setting the phase difference in the carrier or switching function of each phase to $2\pi/N$. Under ideal current-sharing conditions, the N -phase inductor current ripples cancel each other out on the bus side, theoretically reducing the output current ripple amplitude as N increases; meanwhile, the increased equivalent ripple frequency helps reduce bus capacitance requirements. It is noted that, in practical interleaved systems, nonidealities such as inductance tolerances, device parameter dispersion, and sensor gain/offset errors may lead to imperfect current sharing; dedicated current-balancing/equalization strategies have been reported to enhance the robustness of branch current distribution [31].

To characterize the formation mechanism of DC bus ripples from the perspective of “impedance reshaping”, this paper establishes an equivalent circuit model in the frequency domain, as illustrated in Figure 4. The equivalent circuit modeling in Figure 4 follows the commonly adopted impedance-based/Thevenin–Norton representation for DC microgrids and converter-interfaced systems [32]. Specifically, the impedances used in this paper are derived from a formal small-signal linearization around a given steady-state operating point, yielding the corresponding port output/input impedances in the frequency domain. In practice, these impedances can also be obtained (or validated) via standard impedance measurement/identification procedures, e.g., injecting small-amplitude sinusoidal (or broadband) perturbations and measuring the resulting port voltage/current responses.

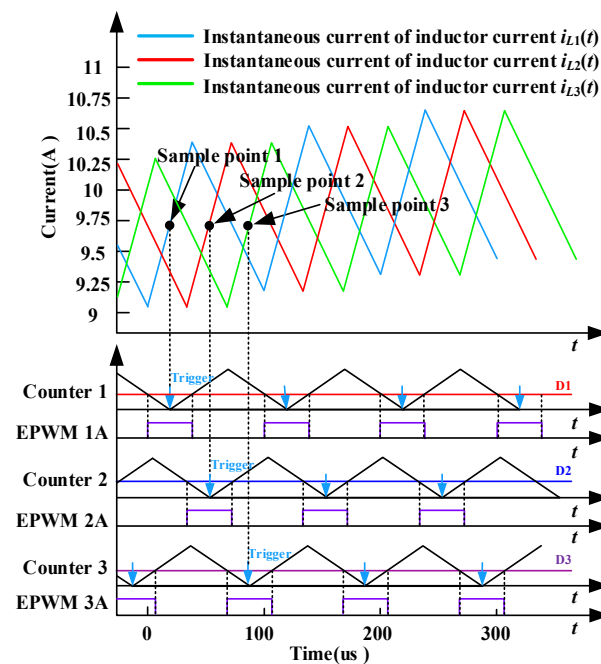


Figure 3. Timing diagram illustrating the instantaneous current waveform and the sampled current sequence.

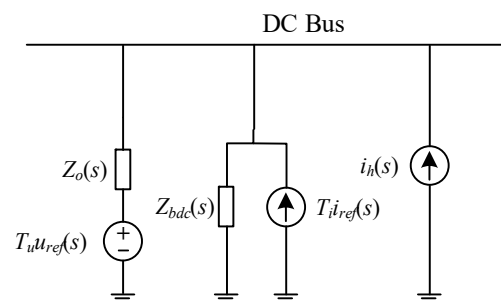


Figure 4. System equivalent circuit.

The power source side is modeled as a series connection of a controlled voltage source $T_u u_{ref}(s)$ and an output impedance $Z_o(s)$, the AI load is equivalent to a current source $i_h(s)$ being injected into the Point of Common Coupling (PCC) in the harmonic frequency band, and the BDC is equivalent to a parallel connection of a controlled current source $T_i i_{ref}(s)$ and an output impedance $Z_{bdc}(s)$. When the system lacks a ripple compensation device, the ripple current is shared by the load connected to the DC bus and the converter. Analyzing the schematic of Figure 4 in the harmonic frequency domain yields the equivalent circuit shown in Figure 5.

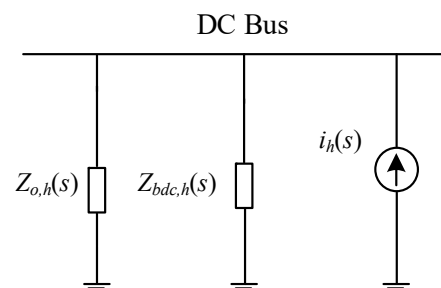


Figure 5. System equivalent circuit in the harmonic frequency domain.

This model provides a unified description of “how harmonic currents are distributed among $Z_{o,h}(s)$ and $Z_{bdc,h}(s)$ ”, laying the foundation for subsequent stability and compensation capability analysis. Under this equivalent model, the harmonic voltage ripple at the bus can be written as

$$V_h(s) = Z_{eq}(s) \cdot i_h(s) \quad (1)$$

where

$$Z_{eq}(s) = \frac{1}{\left(\frac{1}{Z_{o,h}(s)} + \frac{1}{Z_{bdc,h}(s)}\right)} \quad (2)$$

Therefore, one of the fundamental ways to reduce bus ripple is to make $Z_{bdc,h}(s)$ present a “controllable low impedance” in the target frequency band, thereby prioritizing the diversion of $i_h(s)$ to the BDC. Conversely, when the system’s available margin is insufficient or participation in compensation is undesirable, $Z_{bdc,h}(s)$ can be raised to a “high impedance” to reduce harmonic current sharing.

2.2. The Proposed Adaptive Harmonic Impedance Control Method

Existing control approaches based on the DC bus harmonic voltage or the converter harmonic output current typically introduce a tunable factor to generate the harmonic current or harmonic voltage reference, which is then tracked by the current or voltage controller. By adjusting this factor, the harmonic output impedance of the BDC can be continuously regulated. However, to achieve highly flexible tuning, the factor often needs to vary over a wide range, which substantially amplifies the feedforward or feedback gains; excessive gains may lead to overcurrent, saturation, and a reduced stability margin. To address these issues, this paper proposes an adaptive harmonic impedance control and flexible compensation method for AIDC. The proposed strategy constructs a virtual-impedance path within the control loop using the DC bus harmonic voltage and the converter output harmonic current, thereby enabling online dynamic reconstruction of the reference voltage. With this method, the harmonic output impedance of the BDC can be flexibly set over a wide range without excessively amplifying feedforward or feedback gains, thus avoiding overmodulation and instability. The modified harmonic voltage command can be expressed as

$$u_{dc_h}^* = k(u_{dc_h} - Z_v i_{o_h}) \quad (3)$$

where Z_v represents the virtual impedance and k is the gain coefficient.

To achieve precise suppression of bus voltage ripples, a multi-resonant controller is employed in the control channel to track the reference voltage:

$$G_h = \sum_h K_r \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_r^2} \quad (4)$$

where K_r is the resonant gain, ω_r is the resonant frequency, and the cutoff frequency ω_c determines the control bandwidth. In this work, the target frequency set is explicitly selected as $f_i \in \{20, 50, 100, 150\}$ Hz, and the resonant branches are designed with $\omega_{r,i} = 2\pi f_i$ to provide targeted suppression at these representative disturbance components. The resonant gains $K_{r,i}$ and the bandwidth parameter ω_c are selected according to widely adopted tuning guidelines [33]. This controller can respond rapidly to harmonic components at specific frequencies, effectively mitigating periodic voltage ripple on the DC bus.

Figure 6 depicts the control scheme of the BDC based on adaptive harmonic impedance. The specific implementation of the adaptive harmonic impedance control module is shown in Figure 7.

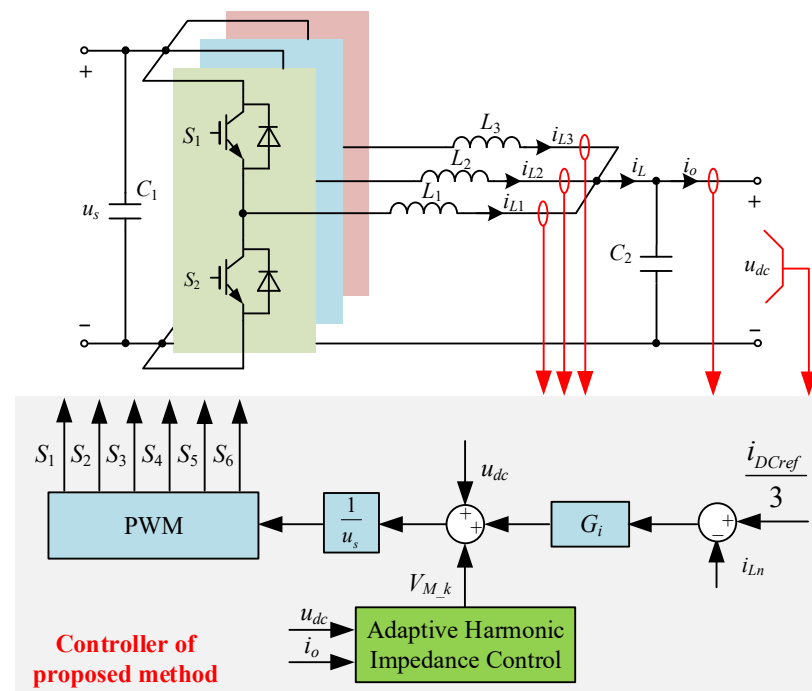


Figure 6. Control scheme of the BDC based on adaptive harmonic impedance control.

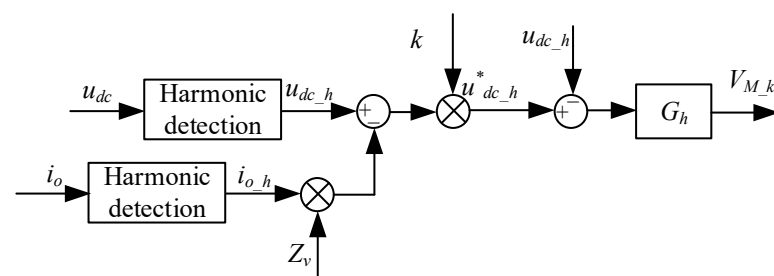


Figure 7. Adaptive harmonic impedance control module.

2.3. Equivalent Harmonic Output Impedance Analysis

The harmonic voltage reference value obtained in Equation (3) will be tracked by a voltage controller based on a resonant loop. It should be noted that an ideal resonant element in the continuous-time domain provides theoretically high gain at ω_r ; however, in digital implementation, this gain becomes finite due to ω_c , sampling/computation delays, and discretization effects. Therefore, ω_c is introduced to limit the resonant peak and bandwidth, ensuring implementation feasibility and robustness. Under zero-static-error tracking conditions at this resonant frequency, the harmonic voltage reference becomes equal to the actual harmonic voltage, which leads to the following relation:

$$u_{dc_h} = u_{dc_h}^* = k(u_{dc_h} - Z_v i_{o_h}) \quad (5)$$

Consequently, the equivalent harmonic output impedance of the BDC can be expressed as

$$Z_{o_h} = \frac{u_{dc_h}}{-i_{o_h}} = \frac{k}{1-k} Z_v \quad (6)$$

From Equation (6), the BDC's equivalent harmonic impedance is mainly determined by the gain coefficient k and the virtual impedance Z_v , where the design of Z_v can follow

Ref. [34]. It should be noted that the virtual impedance Z_v adopted in this paper is a purely resistive type. The corresponding design guideline is as follows:

$$Z_v = \frac{(\alpha U_{dcref})^2}{\eta P_{bn}} \quad (7)$$

where α is the maximum ripple coefficient on the DC bus, P_{bn} is the rated power of the BDC, and η is the harmonic compensation coefficient.

When k approaches 0, the BDC equivalent harmonic output impedance approaches zero, allowing the BDC to actively absorb harmonic currents in the system and thus effectively suppress DC bus voltage ripple; physically, this corresponds to a “strong-compensation” operating mode, but in a real converter, the achievable absorption is ultimately limited by current ratings, the modulation margin, and thermal constraints. When k approaches 1, the equivalent harmonic output impedance tends to infinity, and the BDC response to DC bus voltage disturbances becomes negligible; this can be interpreted as a “weak-compensation” mode in which the converter intentionally reduces harmonic participation to avoid saturation or overcurrent when the available margin is insufficient. Therefore, the BDC equivalent harmonic output impedance can be continuously tuned over a wide range. Furthermore, as indicated by Equation (6), when k varies within the interval (0, 1), the gains of the voltage feedforward and current feedback paths remain within a reasonable range without excessive amplification, which improves system stability and helps avoid oscillations and instability caused by control-loop overmodulation or gain coupling.

When the BDC is interfaced to the DC bus of the AIDC as a current-source-type unit and the proposed control strategy is applied, its equivalent control block diagram is as shown in Figure 8.

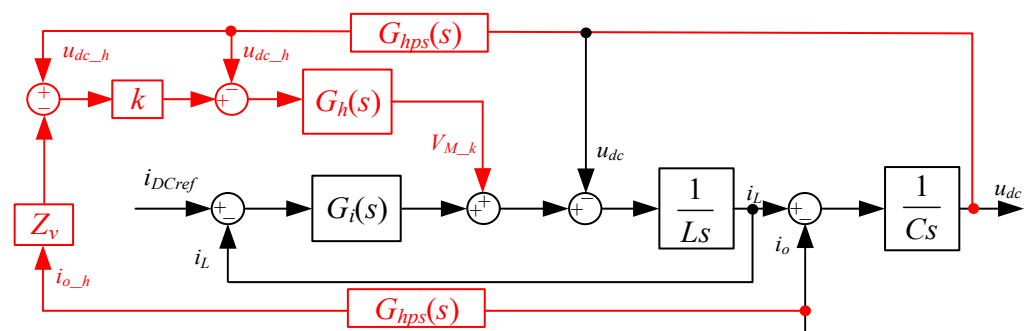


Figure 8. Equivalent control block diagram of the proposed compensation strategy.

From the control block diagram, the expression of the output impedance of the BDC can be derived as

$$Z_{bdc}(s) = \frac{u_{dc}}{-i_o} = \frac{Ls + G_i(s) + G_h(s)G_{hps}(s)kZ_v}{1 + Cs(Ls + G_i(s)) - G_h(s)G_{hps}(s)(k-1)} \quad (8)$$

where $G_{hps}(s)$ is the high-pass filter used for harmonic extraction, and its transfer function is given by

$$G_{hps} = \frac{s}{s + \omega_{hpf}} \quad (9)$$

where ω_{hpf} is the cutoff frequency and is typically selected as 15–30 rad/s.

To investigate the influence of the gain coefficient k on the BDC output impedance, taking the 20 Hz harmonic component as an example, the Bode plots of the output impedance under different values of k are drawn, as shown in Figure 9. Meanwhile, to illustrate the

influence of the virtual impedance Z_v on the impedance-shaping effect, the Bode plots of the BDC output impedance under different Z_v values are presented in Figure 10.

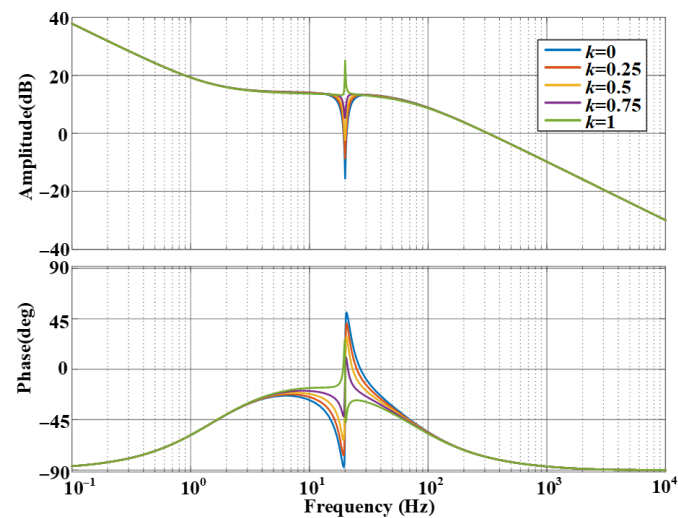


Figure 9. Bode plots of the output impedance of the current-source-type BDC as gain k varies from 0 to 1.

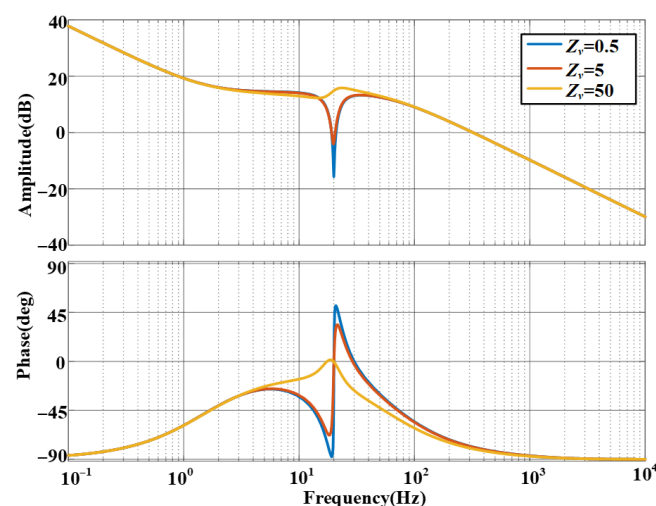


Figure 10. Bode plots of the output impedance of the current-source-type BDC for different Z_v values.

From the Bode plots in Figure 9, it can be seen that as the gain k gradually increases from 0 to 1, the output impedance of the BDC at the frequency point increases accordingly. This indicates that the gain k can regulate the BDC output impedance, thereby changing the magnitude of the harmonic current absorbed by the BDC. As can be observed from Figure 10, as the virtual impedance Z_v increases, the BDC's equivalent harmonic impedance at the selected frequency correspondingly increases. Consequently, the ripple suppression capability is weakened, and the compensation current decreases. Therefore, in practical design, Z_v should not be chosen excessively large. Simultaneously, the phase in Figures 9 and 10 remains consistently between -90° and 90° , demonstrating that the impedance shaping process does not introduce abnormal phase characteristics.

According to the characteristic equation of the system output impedance, the loop gain of the system can be obtained as

$$D(s) = \frac{kZ_v G_h(s) G_{hps}(s)}{Ls + G_i(s)} \quad (10)$$

The stability of the system is determined by the loop gain $D(s)$. From Equation (10), it can be observed that the poles of the loop gain are independent of k and Z_v . First, the pole distribution of $D(s)$ is examined to evaluate the open-loop stability of the BDC; when all poles of the transfer function $D(s)$ lie in the left half of the complex plane, the open-loop system is stable. Figure 11 shows the pole distribution of $D(s)$; it can be observed that there are no poles with positive real parts, indicating that the open-loop system is stable under the selected parameters. From Figure 11 and the denominator term of Equation (10), it can be seen that the factors affecting open-loop stability include only the bandwidth of the resonant controller, the parameters of the current-loop controller, and the circuit parameters of the BDC. Assuming the BDC component parameters (e.g., capacitance and inductance) are properly designed, the open-loop stability condition is satisfied only when the resonant-controller bandwidth is positive and the current-loop controller parameters are appropriately selected; this premise always holds for the method proposed in this paper.

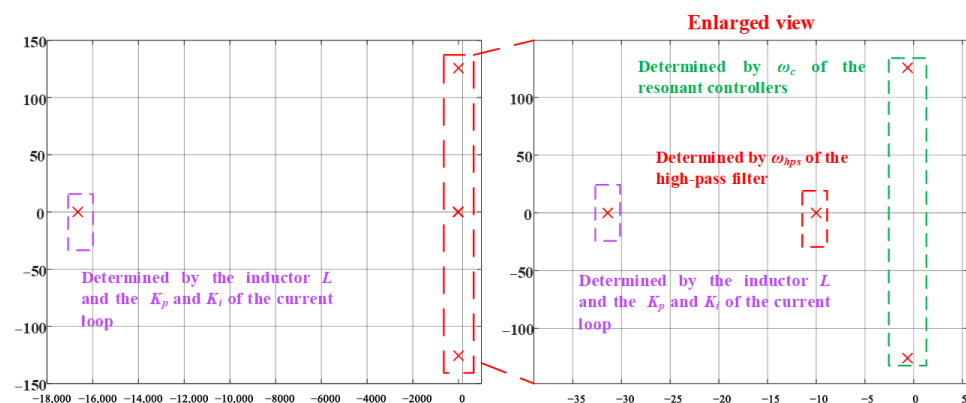


Figure 11. Pole map of $D(s)$.

Therefore, within the variation range of $k \in [0, 1]$, the system remains open-loop stable, and no unstable poles are introduced, nor is stability compromised by tuning k . Meanwhile, the bandwidth of the adaptive update channel for k is designed to be far lower than that of the inner current loop, meaning that the variation in k is a slow-variable adjustment and will not cause a “rapid gain jump” on the fast dynamic timescale dominated by the current loop, thereby avoiding transient instability or a significant reduction in stability margin due to fast gain variations.

2.4. Stability Analysis of the Proposed Strategy in a Parallel-Converter System

To analyze the stability of the proposed strategy in a parallel-converter scenario, a parallel system consisting of a voltage-source BDC and a current-source BDC is constructed, and the proposed strategy is applied to this system. The impedance model of the parallel system is shown in Figure 12.

The control block diagram of the voltage-source BDC is shown in Figure 13.

Its equivalent output impedance is given by

$$Z_o(s) = \frac{u_{dc}}{-i_o} = \frac{Ls + G_i(s)}{1 + Cs(Ls + G_i(s)) + G_i(s)G_v(s)} \quad (11)$$

The Nyquist criterion based on the impedance ratio $T_m(s)$ is an effective method for assessing interaction stability between two subsystems in a cascaded network. If the Nyquist plot of $T_m(s)$ encircles the point $(-1, 0)$, the overall system becomes unstable. The expression of $T_m(s)$ is given by

$$T_m(s) = \frac{Z_o(s)}{Z_{bdc}(s)} \quad (12)$$

Figure 14 shows the Nyquist plots of $T_m(s)$ under the proposed strategy for $k = 0, 0.25, 0.75$, and 1 . As observed in Figure 14, when k varies from 0 to 1 , none of the Nyquist curves of the parallel system encircle the point $(-1, 0)$. Therefore, the choice of k within this range does not compromise the system's stability.

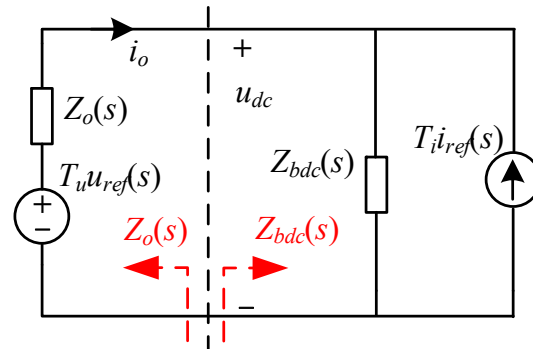


Figure 12. Impedance model of the parallel system comprising a voltage-source BDC and a current-source BDC.

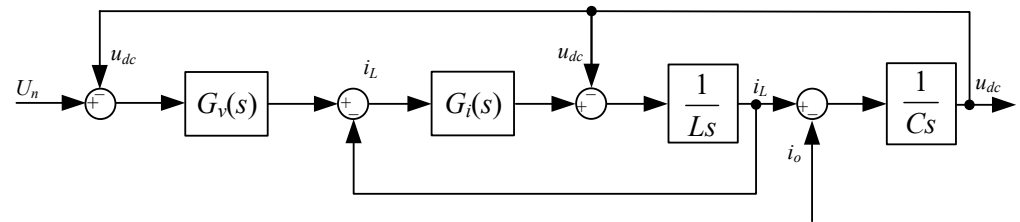


Figure 13. Control block diagram of the voltage-source BDC.

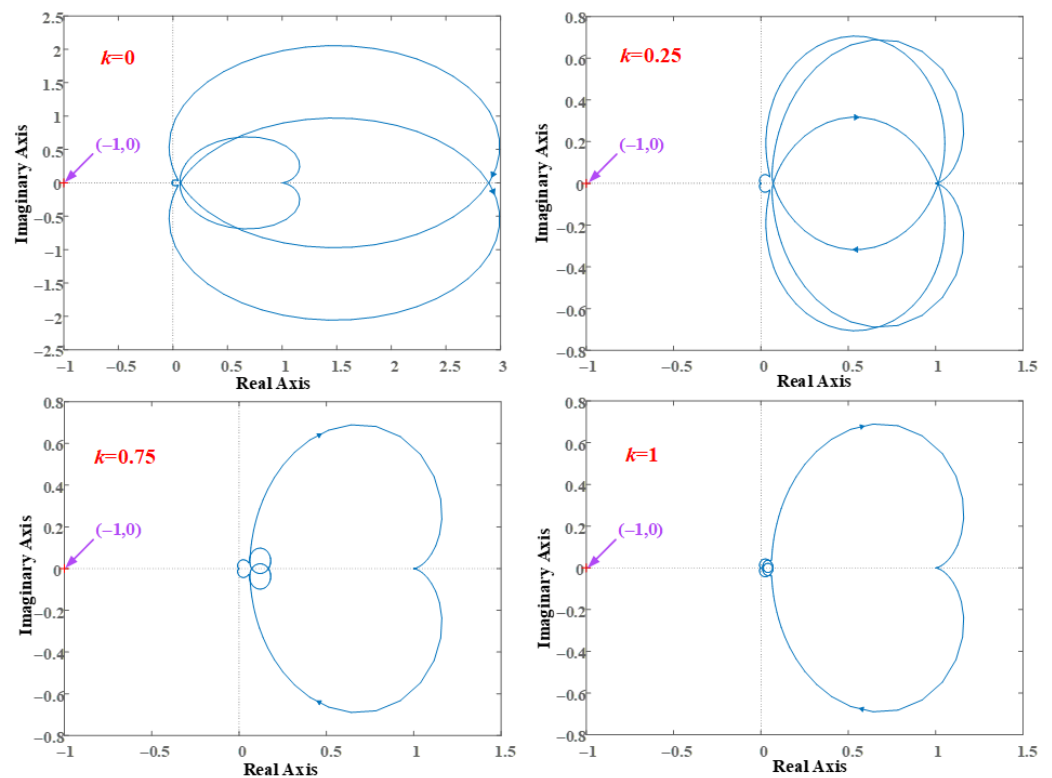


Figure 14. Nyquist Plots of $T_m(s)$ for $k = 0, 0.25, 0.75$, and 1 .

3. Develop an Adaptive Gain Adjustment Mechanism

In practical engineering applications, converters are typically subject to constraints such as power limits, current limits, modulation margin, and thermal losses. To explicitly associate the gain coefficient k with these constraints, this paper proposes a unified design framework for an adaptive gain coefficient and introduces a capacity and current boundary-based adaptive gain regulation mechanism, thereby enabling real-time shaping and on-demand tuning of the equivalent harmonic impedance of the BDC. The proposed framework exhibits good scalability, allowing new influencing factors to be incorporated flexibly without changing the overall architecture. It mainly consists of four modules: normalization and available margin calculation, piecewise-differentiable gating mapping, multi-indicator geometric aggregator, and linear mapping. The detailed flowchart is shown in Figure 15.

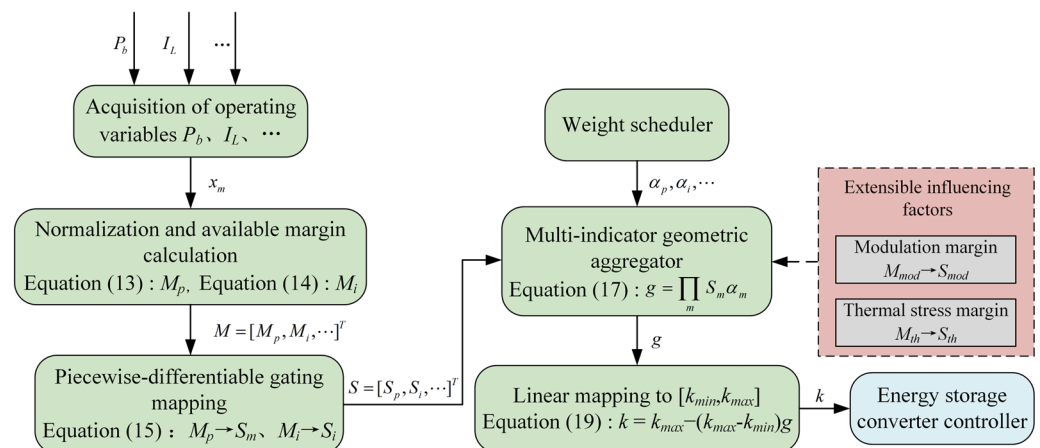


Figure 15. Design flowchart of the adaptive gain coefficient k .

3.1. Normalization and Available Margin Calculation

First, dimensionless “available margin” indices $M_m \in [0, 1]$ are computed for various constraint quantities to characterize the safety degree of the current operating point relative to the rated limits. We take power and current available margins as examples.

The power availability margin is defined as

$$M_p = \frac{P_n - |P_b|}{P_n}, 0 \leq M_p \leq 1 \quad (13)$$

where P_n is the rated power of the device and P_b is the current active power (or power command). Specifically, P_b is obtained by multiplying the measured instantaneous DC bus voltage and output current to compute the instantaneous power, and then applying a low-pass filter to generate a smoothed estimate, so as to mitigate the influence of switching ripple and measurement noise on the adaptive decision. When the output power approaches the rated value, M_p approaches 0, indicating that the power capacity is gradually being exhausted; when the output is far below the rated power, M_p approaches 1, characterizing sufficient regulation space on the power side.

Similarly, the current availability margin is defined as

$$M_i = \frac{I_{Lmax} - |I_L|}{I_{Lmax}}, 0 \leq M_i \leq 1 \quad (14)$$

where I_{Lmax} is the maximum allowable current and I_L is the inductor current. Likewise, M_i decreases from 1 to 0 as the current constraint is gradually approached. Specifically, I_L is

obtained by applying a low-pass filter to the measured inductor current signal, so as to reflect the available current margin and the proximity to the current constraint.

The filtering stages used to compute P_b and I_L , together with the update channel of k , form a slow adaptive loop whose bandwidth is designed to be much lower than that of the inner current loop. As a result, the adaptation does not introduce rapid gain jumps on the fast time scale dominated by the current loop, thereby avoiding transient instability or a significant reduction in stability margins caused by fast parameter variations.

3.2. Piecewise-Differentiable Gating Mapping

To effectively suppress chattering or abrupt changes near the threshold caused by measurement noise or small perturbations, thereby preventing high-frequency switching or oscillations of the gain k in the vicinity of the operating boundary, a smooth cubic gating function $S(x; x_0, x_1)$ is introduced to nonlinearly map the available margin:

$$S(x; x_0, x_1) = \begin{cases} 0, & x \leq x_0 \\ \left(\frac{x-x_0}{x_1-x_0}\right)^2 \left(3 - 2\frac{x-x_0}{x_1-x_0}\right), & x_0 < x < x_1 \\ 1, & x \geq x_1 \end{cases} \quad (15)$$

where x_0 and x_1 are the thresholds at which the regulation starts to take effect and is fully released, respectively. Within the interval (x_0, x_1) , the function is a cubic smooth curve, and both the function value and its first derivative are continuous at (x_0, x_1) . This guarantees a smooth transition of the tuning coefficient k and its rate of change, thus preventing control chattering induced by small fluctuations in the margins.

For each available margin M_m (such as M_p , M_i , etc.), a corresponding adjustable margin factor S_m is obtained through the gating function

$$S_m = S(M_m; m_{m0}, m_{m1}) \in [0, 1] \quad (16)$$

The thresholds (m_{m0}, m_{m1}) can be flexibly set according to the importance of each physical quantity, thereby determining the start point and width of the transition region for its regulation effect.

3.3. Multi-Indicator Geometric Aggregator

After obtaining the adjustable margin factors S_m for each constraint, they are combined using a geometric-weighted form:

$$g = \prod_m S_m^{\alpha_m} \quad (17)$$

where $\alpha_m > 0$ is the weight exponent of each influencing factor, typically chosen such that $\sum_m \alpha_m = 1$, ensuring that the aggregated factor g remains within $[0, 1]$. For example, when considering only power and current available margins, one has

$$g = S(M_p; m_{p0}, m_{p1})^{\alpha_p} \cdot S(M_i; m_{i0}, m_{i1})^{\alpha_i} \quad (18)$$

The proposed geometric weighting method exhibits excellent consistency, sensitivity, and scalability. When any critical available margin is severely insufficient, causing the corresponding S_m to approach 0, the weighted product g will decrease rapidly. This makes the final regulation coefficient more sensitive to the “weakest link”, enabling the timely reinforcement of protection or limiting actions. If other constraint factors, such as modulation margin or thermal loss margin, need to be considered subsequently, it is only necessary to define new M_j and S_j , following the same steps, and introduce the

corresponding $S_j^{\alpha_j}$ term into the product, without altering the original control framework. Meanwhile, by adjusting the weight coefficients α_m , the relative importance of different constraints to system safety can be flexibly characterized based on engineering experience or optimization results.

3.4. Linear Mapping

The comprehensive influence factor g is linearly mapped to the regulation coefficient interval $[k_{\min}, k_{\max}]$:

$$k = k_{\max} - (k_{\max} - k_{\min})g \quad (19)$$

Since $g \in [0, 1]$, it directly follows that

$$k \in [k_{\min}, k_{\max}] \quad (20)$$

When the system operates with sufficient available margins, each M_m is large, resulting in $S_m \approx 1$ and thus g approaches 1. In this case,

$$k \approx k_{\min} \quad (21)$$

At this point, the equivalent harmonic output impedance of the BDC is very small, providing strong equivalent harmonic absorption capability for the DC bus. Conversely, when certain constraints approach their limits and the available margin decreases, the relevant S_m decreases significantly, causing g to approach 0. It can be obtained that

$$k \approx k_{\max} \quad (22)$$

At this point, the regulation coefficient automatically increases, resulting in a larger harmonic output impedance of the BDC and reduced harmonic absorption capability. This forces the system operation to retreat towards the safe region, achieving adaptive protection against operational risks under multi-constraint conditions.

In summary, this method constructs normalized available margins, employs smooth gate functions for interval mapping, and utilizes geometric weighting to fuse multiple influence factors. Ultimately, the comprehensive quantity g is mapped to the adaptive gain coefficient k , flexibly altering the equivalent harmonic output impedance of the BDC.

3.5. Example of Extended Constraints

In practical PWM converters, the harmonic compensation path is implemented as an auxiliary signal superimposed on the modulation waveform (or the duty-cycle command). When the compensation demand becomes large, the modulation command may move closer to the saturation boundary, which can induce overmodulation and nonlinear distortion. Consequently, the achievable impedance-shaping capability is inherently bounded in practice. To explicitly capture this engineering limitation and to enable an online constraint-aware capping of the compensation strength, the modulation margin is introduced as an illustrative constraint and incorporated into the unified framework.

For PWM modulation (or duty-cycle control), the unsaturated modulation command is denoted as $m^*(t)$, and it is constrained within the admissible range $[m_{\min}, m_{\max}]$. Based on this, a normalized index describing the available modulation margin, $M_{\text{mod}}(t)$, is defined as

$$M_{\text{mod}}(t) = \text{sat}_{[0,1]} \left(\frac{m_{\max} - |m^*(t)|}{m_{\max} - m_{\text{safe}}} \right) \quad (23)$$

where m_{safe} represents a reserved safety margin threshold selected to avoid pronounced nonlinear distortion when operating near saturation. With this definition, $M_{\text{mod}}(t)$ decreases as

$|m^*(t)|$ approaches m_{max} , indicating an insufficient modulation margin; conversely, $M_{mod}(t)$ remains close to unity when $|m^*(t)|$ is well below m_{max} , indicating a sufficient margin.

To prevent abrupt variations and potential chattering when the operating point is close to the margin boundary, $M_{mod}(t)$ is further transformed into a modulation margin factor, S_{mod} , through a smooth gating function:

$$S_{mod} = S(M_{mod}) \quad (24)$$

The gating function $S(M_{mod})$ can adopt the cubic smooth form used in the unified framework, ensuring consistency with the gating design applied to the power and current margin constraints.

Subsequently, the modulation margin factor is incorporated into the multi-indicator geometric aggregation to form the composite influence factor g :

$$g = \prod_m S_m^{\alpha_m} \Rightarrow g = S_p^{\alpha_p} S_i^{\alpha_i} S_{mod}^{\alpha_{mod}} \quad (25)$$

where $\alpha_{mod} > 0$ denotes the weighting exponent associated with the modulation margin constraint and reflects its relative importance. The established linear mapping from g to k over the range $[k_{min}, k_{max}]$ is preserved. Under a reduced modulation margin, the value of $M_{mod}(t)$ becomes smaller, which leads to a smaller S_{mod} and consequently a smaller aggregated factor g . In this case, the coefficient k is adaptively increased, which raises the equivalent harmonic impedance and weakens the participation of harmonic compensation. In this way, the proposed formulation provides an explicit, constraint-aware cap on the compensation strength and helps avoid overmodulation and saturation.

The online computation of the modulation margin index typically requires no additional sensors and primarily relies on controller-internal variables and routinely measured signals. Specifically, the controller can directly provide the modulation command $m^*(t)$, the corresponding limits m_{max} and m_{min} , and the safety threshold m_{safe} determined by engineering settings. If a formulation based on the modulation index and DC bus voltage is adopted, the DC bus voltage u_{dc} (which is normally sampled) and the relevant normalization base values or per-unit scaling factors of the modulator may also be used. These signals support a complete online closed-loop procedure that sequentially performs margin evaluation, smooth gating, multi-indicator aggregation, and coefficient update, thereby integrating modulation margin constraints into the unified framework.

4. Simulation and Experimental Verification

To verify the effectiveness and practical feasibility of the proposed adaptive harmonic impedance control and flexible compensation strategy, a simulation model of a DC micro-grid with two parallel-connected BDCs is first established in Matlab/Simulink based on the parameters listed in Table 2, as shown in Figure 16. Here, U_{dcref} denotes the reference voltage of the DC bus; U_b is the reference voltage on the high-voltage side of the BDC; C_b and L_b are the BDC filter capacitor and filter inductor, respectively; P_{bn} is the rated power of the BDC; m_{p0} and m_{p1} represent the lower and upper limits of the available power margin, respectively; R_{ac} is the resistance of the single-phase AC load; P_{acl} is the rated power of the single-phase AC load; C_{dc} is the DC-link filter capacitor; f_{sw} and f_s are the switching frequency and sampling frequency, respectively; U_{acref} is the reference voltage of the single-phase AC output; f_{ac} is the rated frequency of the single-phase AC load; and C_{ac} and L_{ac} are the AC-side filter capacitor and filter inductor, respectively (used in the AC-side filtering stage). In this setup, BDC 1 adopts voltage source control to establish and regulate the DC bus voltage, whereas BDC 2 employs current source control and incorporates the proposed strategy to provide harmonic compensation capability. It should be noted that the

proposed harmonic mitigation method is applied only to BDC 2, while the control strategy of BDC 1 remains unchanged.

Table 2. System parameters.

Symbol	Value	Symbol	Value
$U_{dc\text{ref}}$	350 V	U_b	500 V
C_b	500 μF	L_b	300 μH
P_{bn}	8 kW	m_{p0}	0.1
m_{p1}	0.3	P_{acl}	8 kW
R_{ac}	6.05 Ω	C_{dc}	1000 μF
f_{sw}	10 kHz	f_s	20 kHz
$U_{ac\text{ref}}$	220 V	f_{ac}	50 Hz
C_{ac}	25 μF	L_{ac}	300 μH

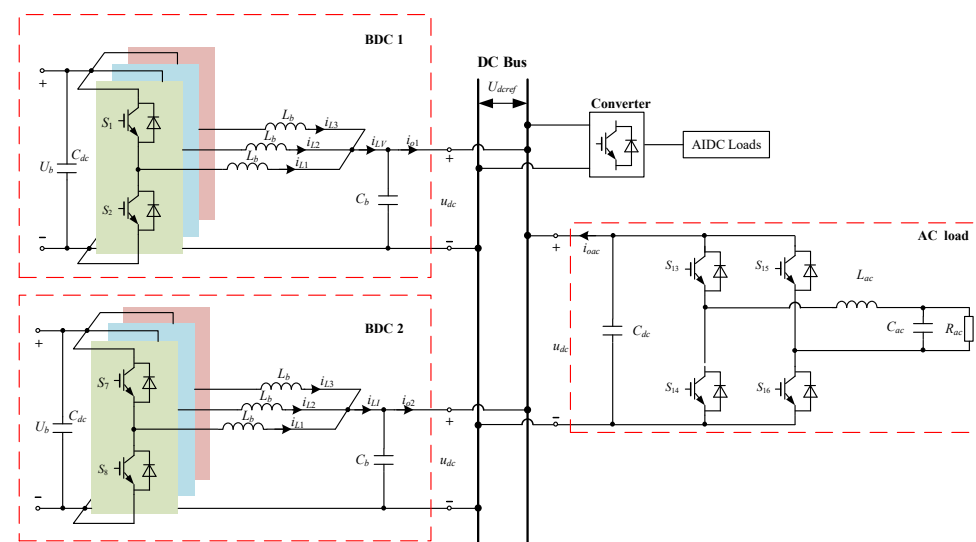


Figure 16. System simulation structure.

In the simulations, harmonic currents at 20 Hz, 50 Hz, 100 Hz, and 150 Hz are injected into the DC bus to emulate random fluctuations of the AIDC load, where the selection of these frequency points is justified as follows:

- (i) Public engineering analyses indicate that large-scale AI training loads, due to the synchronized “computation–communication” iterations of GPU clusters, exhibit second-scale low-frequency power swings whose spectral energy can extend over approximately the 0.1–20 Hz band [35,36]; thus, 20 Hz is chosen as a representative point within this low-frequency disturbance range to cover relatively faster components and to evaluate the adaptive harmonic suppression capability of the proposed method under different compensation strengths.
- (ii) In practical AIDC power-supply chains, power electronic interfaces such as UPSs, PFC stages, and inverters may couple the AC-side fundamental frequency-related disturbances and their integer-multiple-related components into the DC side [37,38]. When the DC bus supplies a single-phase AC load through an inverter, a typical double-line-frequency ripple appears on the DC side; moreover, among low-order harmonics, the third harmonic corresponds to 150 Hz in a 50 Hz system and is commonly observed in scenarios involving nonlinear loads such as computers/UPSs [39].

This set of frequency points is selected for representative validation. The proposed control framework is not limited to these specific frequencies; in practical applications, it can be

extended and its parameters can be tuned according to the measured harmonic/disturbance spectra on site. Accordingly, the above-outlined injected frequency components are used to evaluate the harmonic suppression performance and adaptive regulation capability under different compensation strengths and operating conditions.

4.1. Simulation Results Analysis

Without the proposed control strategy, the DC bus voltage ripple amplitude is 27.4 V, and the voltage THD is 3.06%. The ripple current mainly flows into BDC 1 with an amplitude of 71.5 A, whereas the ripple current of BDC 2 is only 7.7 A (see Figure 17). This is because, in a paralleled converter system, the sharing of harmonic currents is mainly determined by the closed-loop output impedances of the branches, and ripple currents tend to flow into the branch with the smaller output impedance. In the low-frequency range of interest, the closed-loop output impedance of the current-source-type converter BDC 2 is much higher than that of the voltage-source-type converter BDC 1. Therefore, the harmonic current primarily flows into BDC 1, which has the smaller closed-loop output impedance.

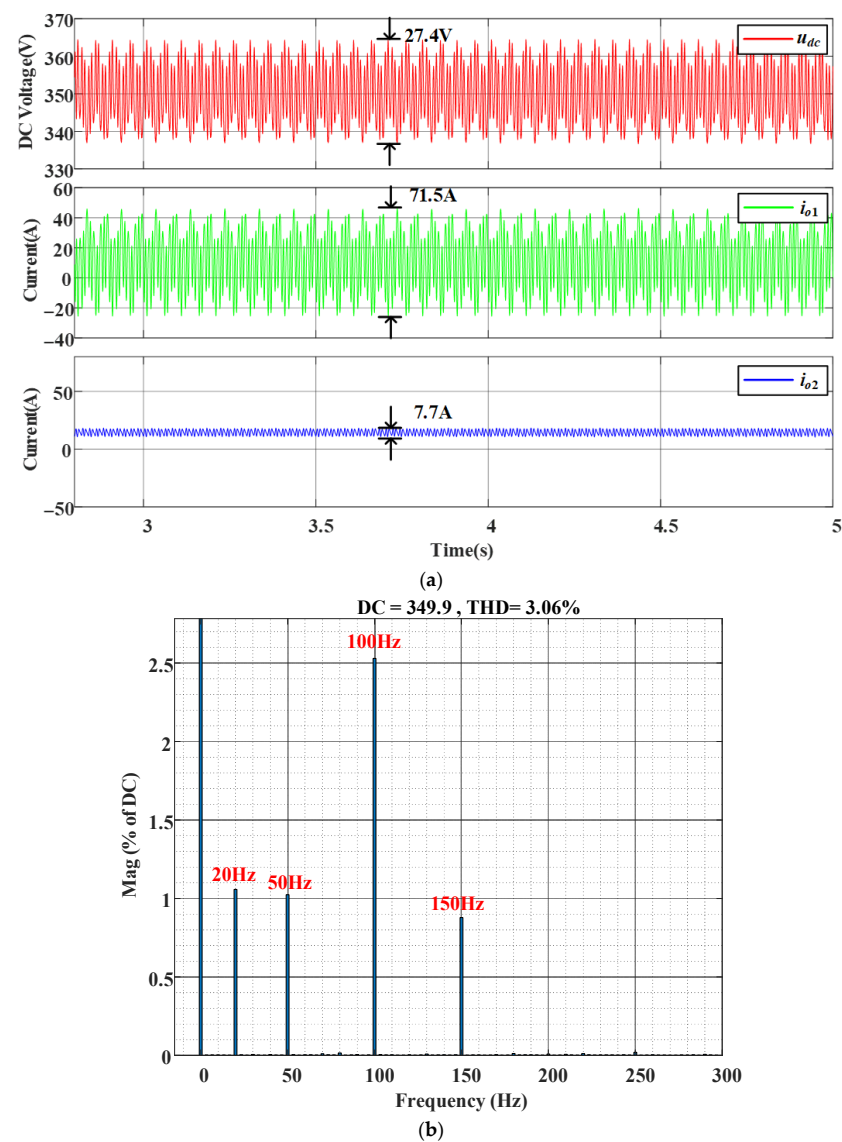


Figure 17. Simulation results and FFT analysis without the proposed compensation strategy. (a) DC bus voltage and BDC current waveforms without the proposed compensation strategy. (b) FFT analysis of DC bus voltage without the proposed compensation strategy.

4.1.1. Harmonic Suppression Performance

When $k = 0$, the equivalent harmonic output impedance of the BDC 2 approaches zero and is much smaller than the output impedance of BDC 1, so BDC 2 assumes the main harmonic current compensation. At this time, the bus ripple amplitude drops from 27.4 V to 8.4 V, voltage THD drops from 3.06% to 0.89%, and BDC 1 ripple current drops from 71.5 A to 19.3 A, while the ripple current of BDC 2 increases from 7.7 A to 56 A (see Figure 18), demonstrating an extremely strong ripple suppression effect.

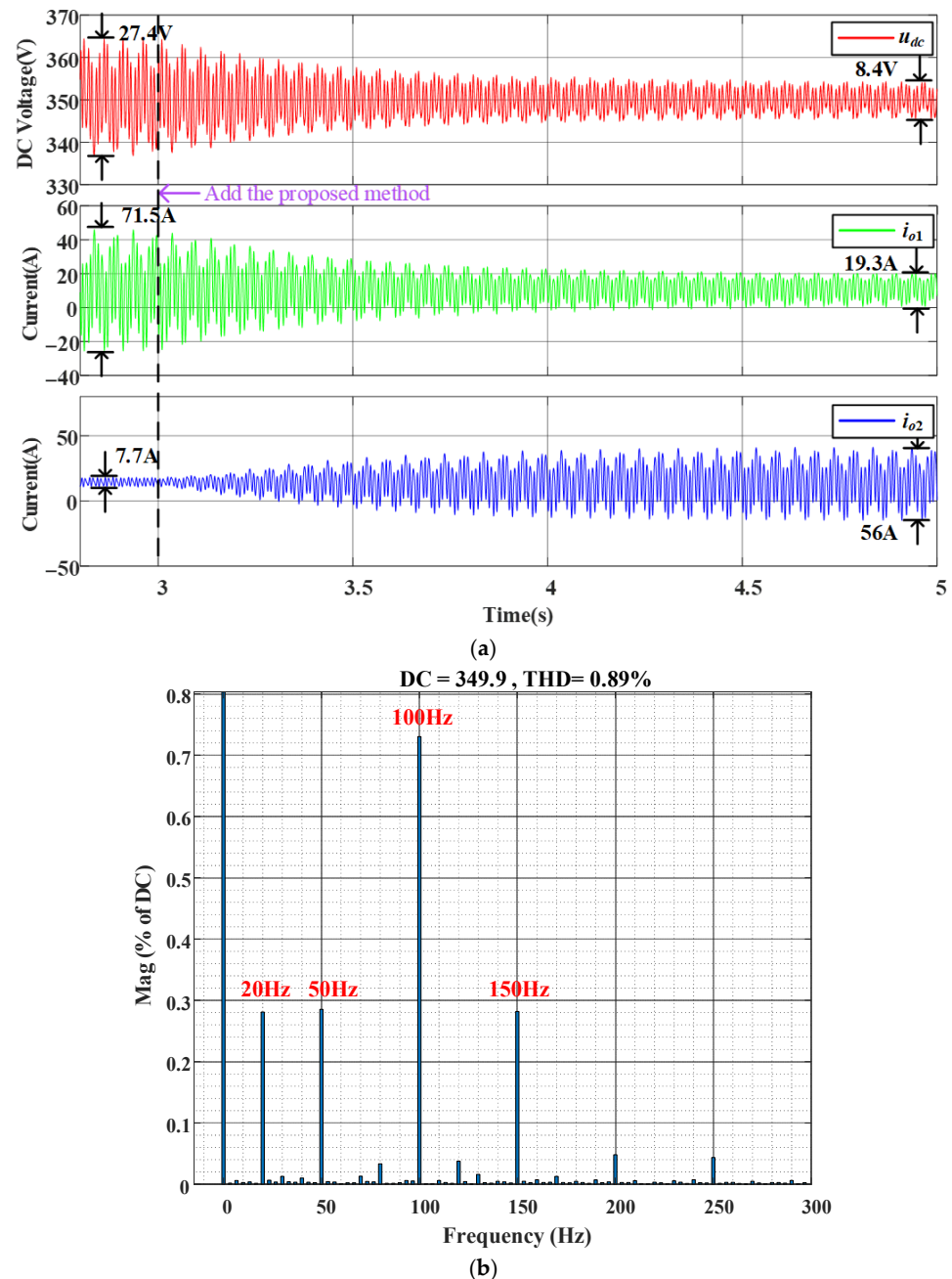


Figure 18. Simulation results and FFT analysis with the proposed compensation strategy ($k = 0$). (a) DC bus voltage and BDC current waveforms with the proposed compensation strategy ($k = 0$). (b) FFT analysis of DC voltage with the proposed compensation strategy ($k = 0$).

To demonstrate the steady-state suppression performance, Figure 19 presents the simulated waveforms obtained using the frequency-selective control strategy in [26]. As shown, the DC bus voltage ripple is reduced from 27.4 V to 10.5 V, and the voltage THD

decreases from 3.06% to 1.19%. Since the frequency-selective control reduces the output impedance of BDC 2, most of the ripple current is guided to the BDC 2 branch. As a result, the ripple current of BDC 1 is reduced from 71.5 A to 25.1 A, while the ripple current absorbed by BDC 2 increases from 7.7 A to 48.7 A.

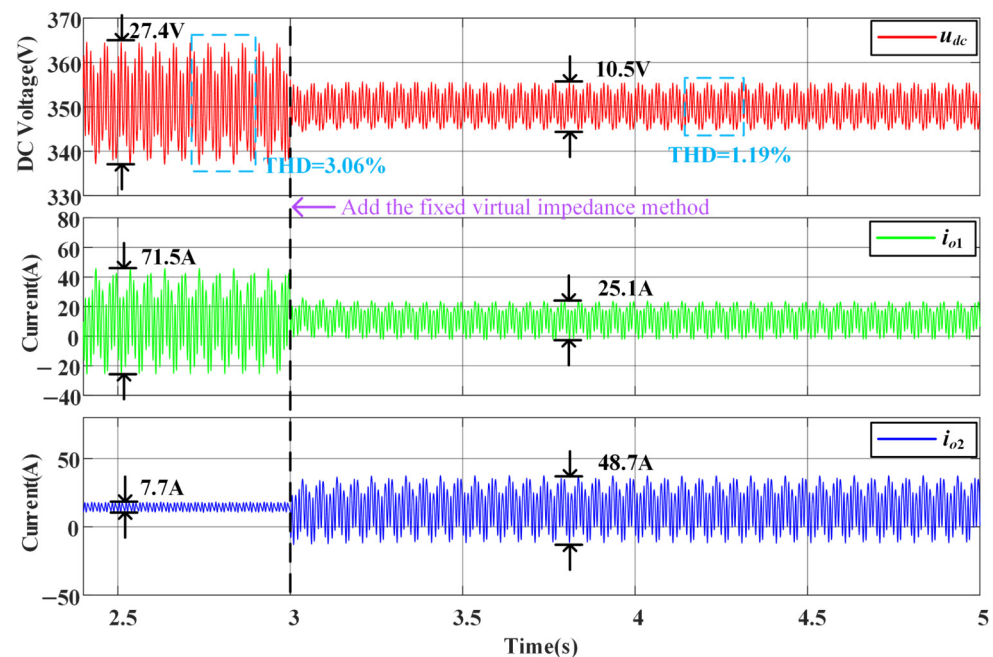


Figure 19. Simulation results for comparison using the previous control method reported in [26].

To further compare the implementation performance of the proposed strategy with the method in [26], Figure 20 presents a quantitative comparison of key metrics for different methods with respect to the conventional current-source control baseline. The metrics include the bus-voltage ripple amplitude, voltage THD, and the peak-to-peak current of BDC 1. As shown in Figure 20, the proposed strategy achieves better improvement in all the above metrics than the method in [26].

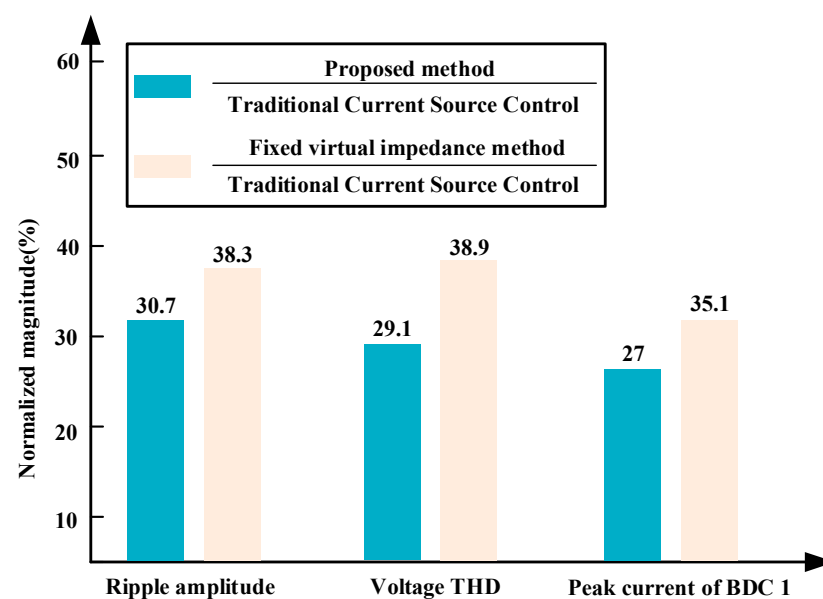


Figure 20. Comparison results of various performance metrics between the proposed method and the method in [26].

When $k = 0.5$, the BDC 2 equivalent harmonic impedance increases moderately. The bus ripple amplitude rises to 12.9 V, THD is 1.45%, and the BDC 1 ripple current amplitude rises to 29.4 A (see Figure 21). Results indicate that as gain k increases, harmonic absorption capability weakens, and bus power quality declines accordingly.

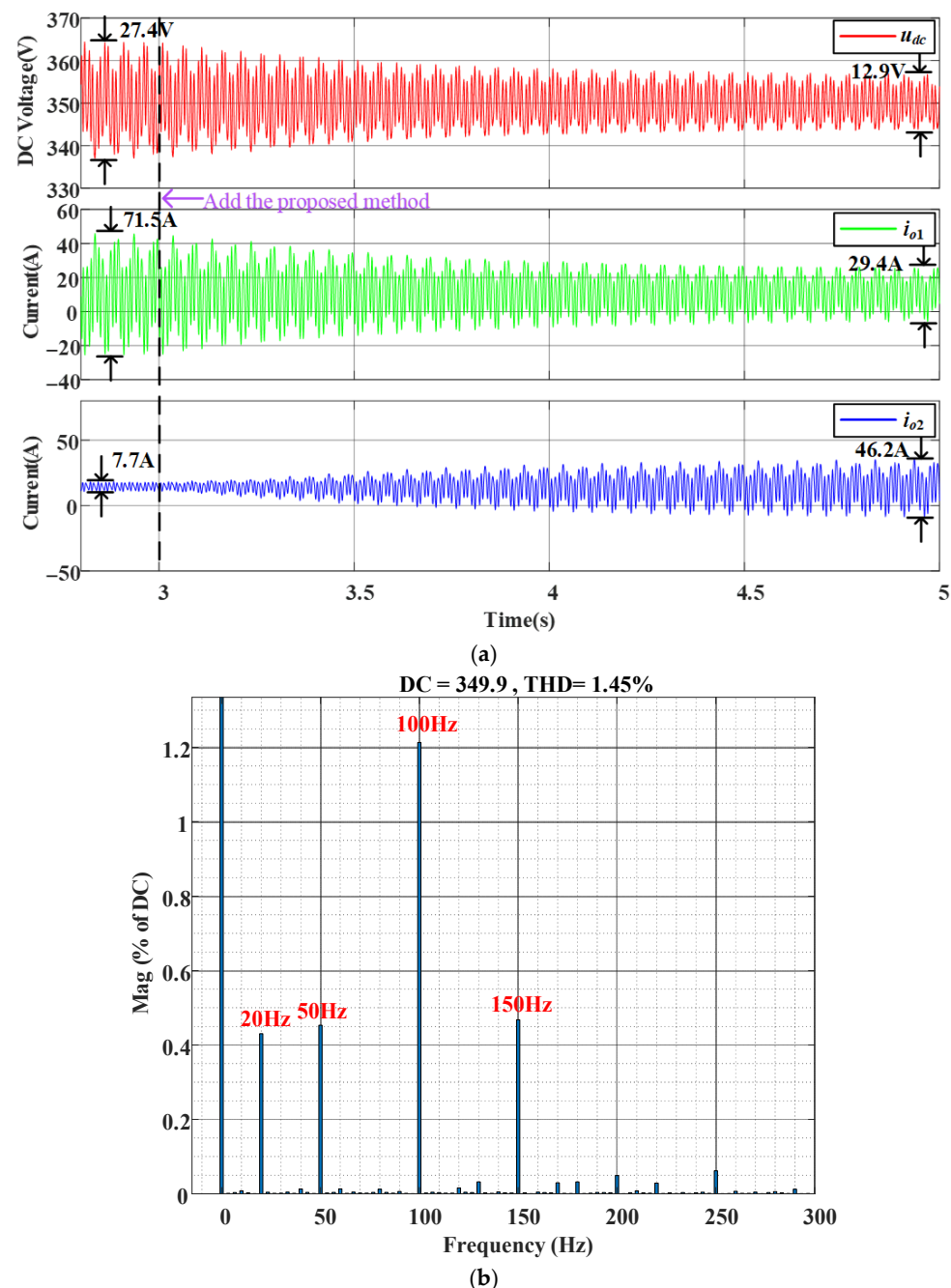


Figure 21. Simulation results and FFT analysis with the proposed compensation strategy ($k = 0.5$). (a) DC bus voltage and BDC current waveforms with the proposed compensation strategy ($k = 0.5$). (b) FFT analysis of DC voltage with the proposed compensation strategy ($k = 0.5$).

When $k = 0.8$, the output impedance of BDC 2 becomes close to that of BDC 1, but it remains smaller than the output impedance of BDC 1. The bus ripple amplitude is 19.4 V, THD is 2.22%, and the BDC 1 ripple current amplitude is 47.8 A (see Figure 22). Although compensation capability is markedly reduced, the overall performance remains superior to the baseline condition without the compensation strategy.

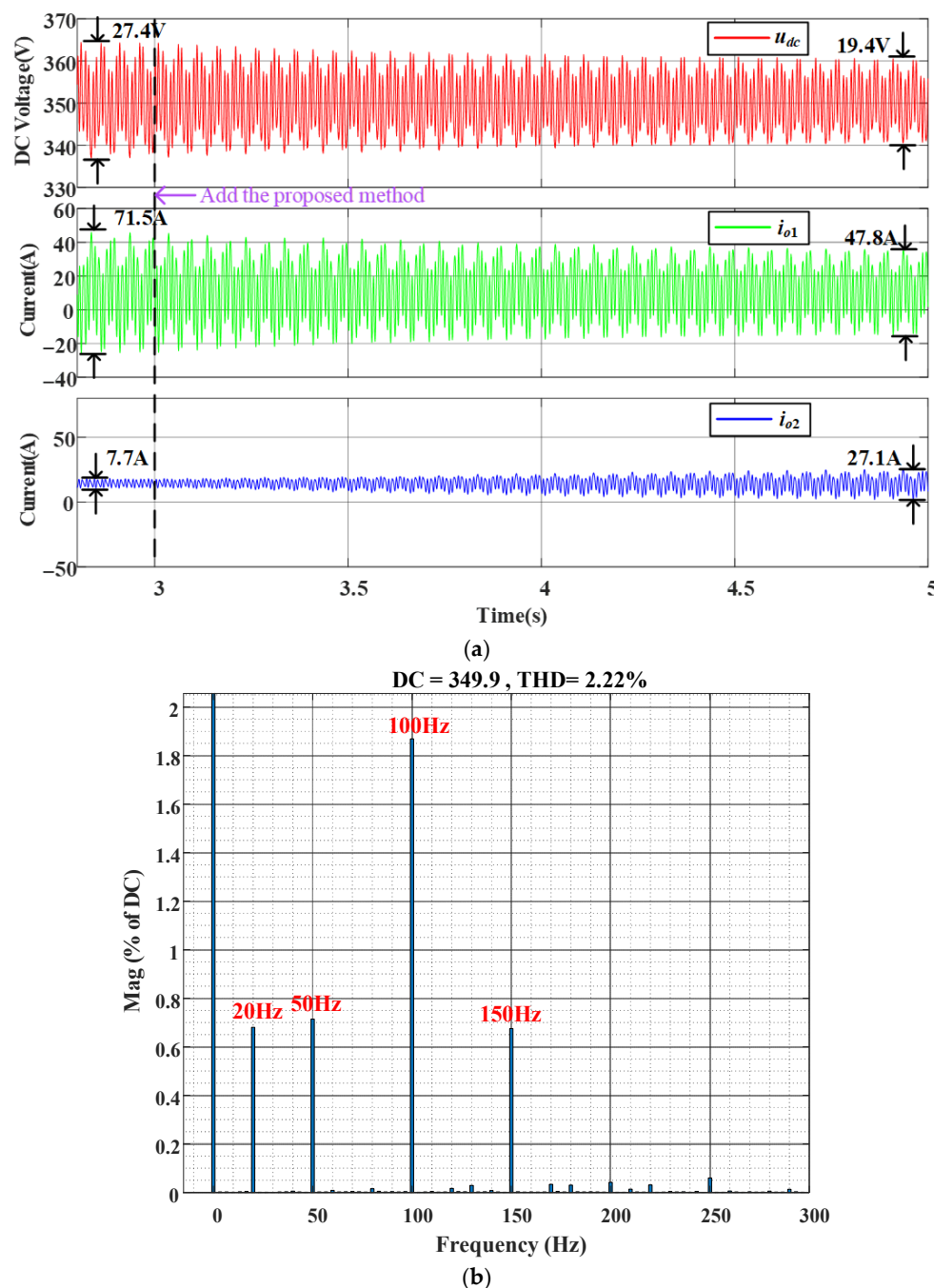


Figure 22. Simulation results and FFT analysis with the proposed compensation strategy ($k = 0.8$). (a) DC bus voltage and BDC current waveforms with the proposed compensation strategy ($k = 0.8$). (b) FFT analysis of DC voltage with the proposed compensation strategy ($k = 0.8$).

4.1.2. Dynamic Adaptive Adjustment Performance

To further verify the online regulation capability of the proposed adaptive mechanism under varying available capacity, a step change in the output power of BDC 2 is set.

Power Surge ($t = 5$ s): The system initially operates in strong compensation mode ($k = 0$), with bus voltage THD maintained at 0.89%. At $t = 5$ s, a sudden increase in BDC 2 output power causes the power available margin to decrease. The adaptive mechanism drives k to rise smoothly from 0 and stabilize at 0.38 (Figure 23b). Correspondingly, the converter's equivalent harmonic impedance increases, the compensation current is actively limited, and the bus ripple amplitude increases from 8.4 V to 10.5 V, with THD rising to 1.17% (Figure 23a). This process demonstrates that when the converter's power

available margin is insufficient, the controller prioritizes ensuring the converter does not overcurrent or overload at the cost of sacrificing some power quality, achieving dynamic matching between compensation capability and available capacity.

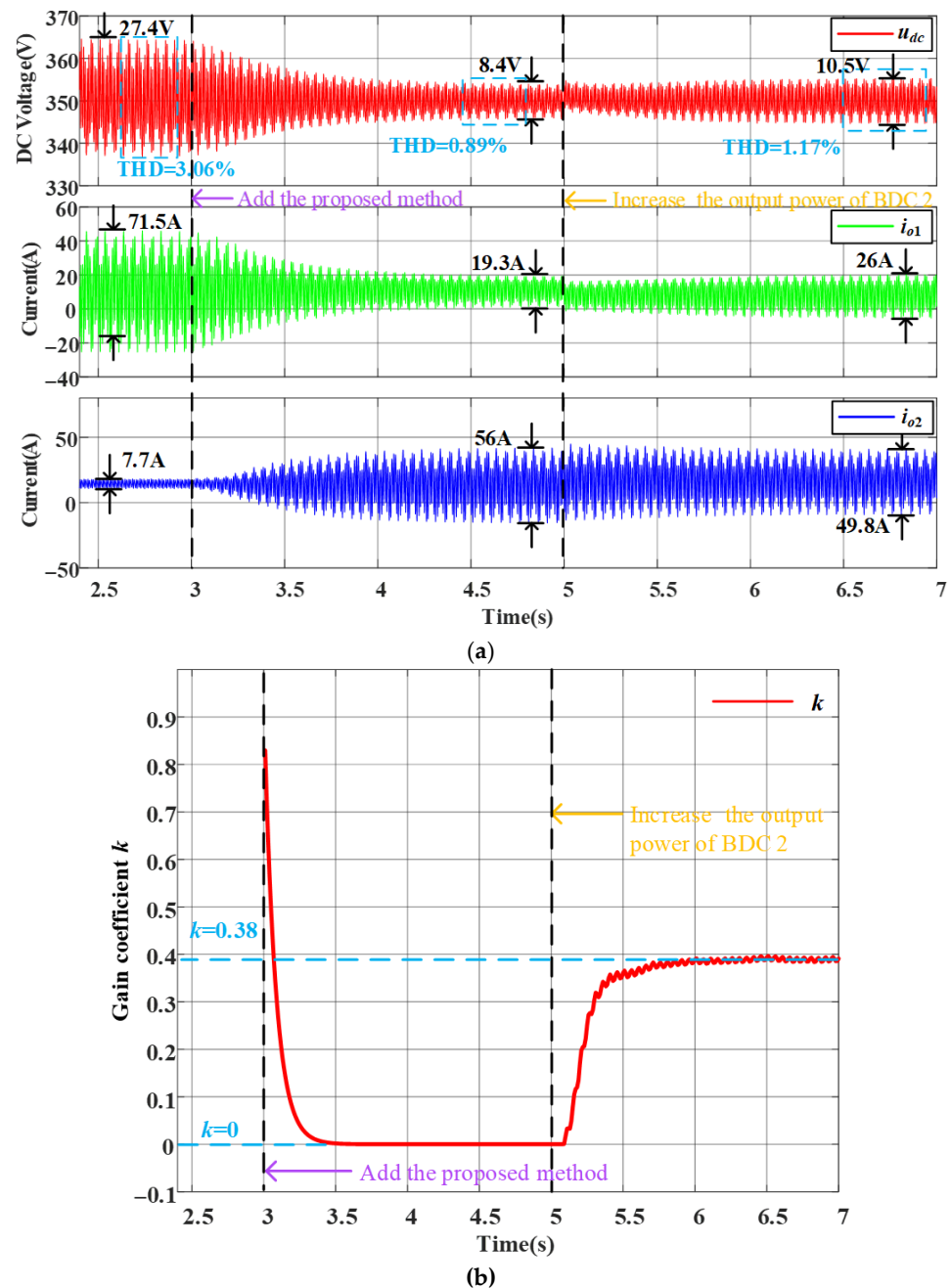


Figure 23. Simulation results and variation curve of gain coefficient k when BDC 2 output power increases at $t = 5$ s. (a) DC bus voltage and BDC current waveforms when BDC 2 output power increases at $t = 5$ s. (b) Variation curve of gain coefficient k when BDC 2 output power increases at $t = 5$ s.

Power Drop ($t = 5$ s): The system runs in semi-compensation mode with $k = 0.54$, and bus voltage THD is 1.59%. At $t = 5$ s, a sudden decrease in BDC 2 output power causes the power available margin to increase. The adaptive mechanism drives k to decrease smoothly from 0.54 and finally fall back to 0 (Figure 24b). After compensation capability is enhanced, the bus ripple amplitude drops from 14.2 V to 8.4 V (Figure 24a). This result indicates that

when device capacity is sufficient, the proposed method automatically enhances harmonic absorption capability, unifying power quality improvement with margin utilization.

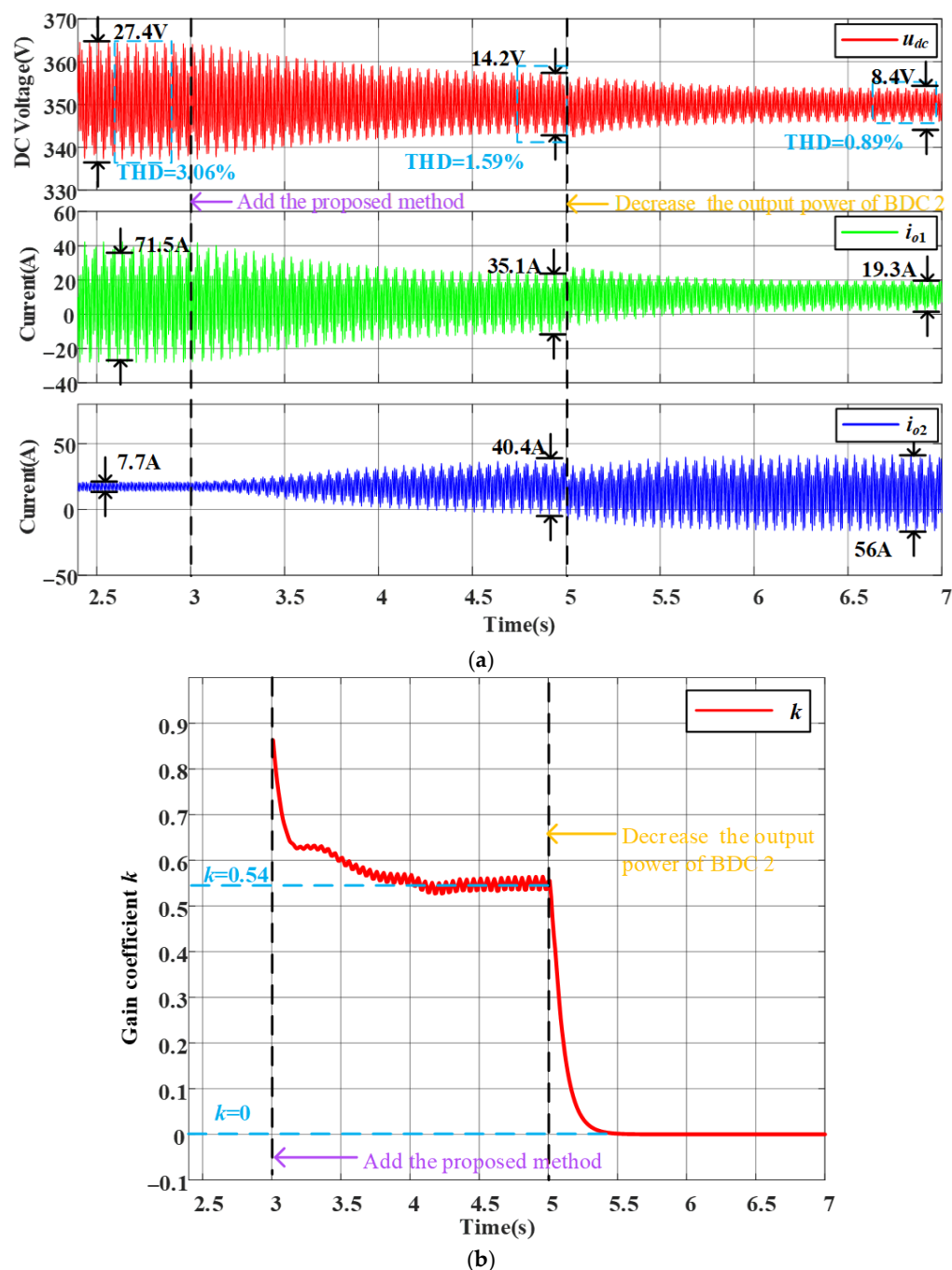


Figure 24. Simulation results and variation curve of gain coefficient k when BDC 2 output power decreases at $t = 5$ s. (a) DC bus voltage and BDC current waveforms when BDC 2 output power decreases at $t = 5$ s. (b) Variation curve of gain coefficient k when BDC 2 output power decreases at $t = 5$ s.

To highlight the advantage of the proposed method over the impedance-shaping approach in [26] (which uses a fixed gain to reduce the output impedance of BDC 2), the output power of BDC 2 is increased at $t = 6$ s in the simulation. As shown in Figure 25a, because a fixed gain is used in [26], the output impedance remains constant, and the peak value of the absorbed harmonic current is also fixed. When the active current is superimposed with the harmonic current, the inductor current can easily reach the current

limit and trigger overcurrent protection. In contrast, as shown in Figure 25b, the proposed method automatically computes the current margin and adaptively increases k when the current is about to hit the limit (see Figure 25c), thereby increasing the output impedance of BDC 2 and reducing the absorbed harmonic current.

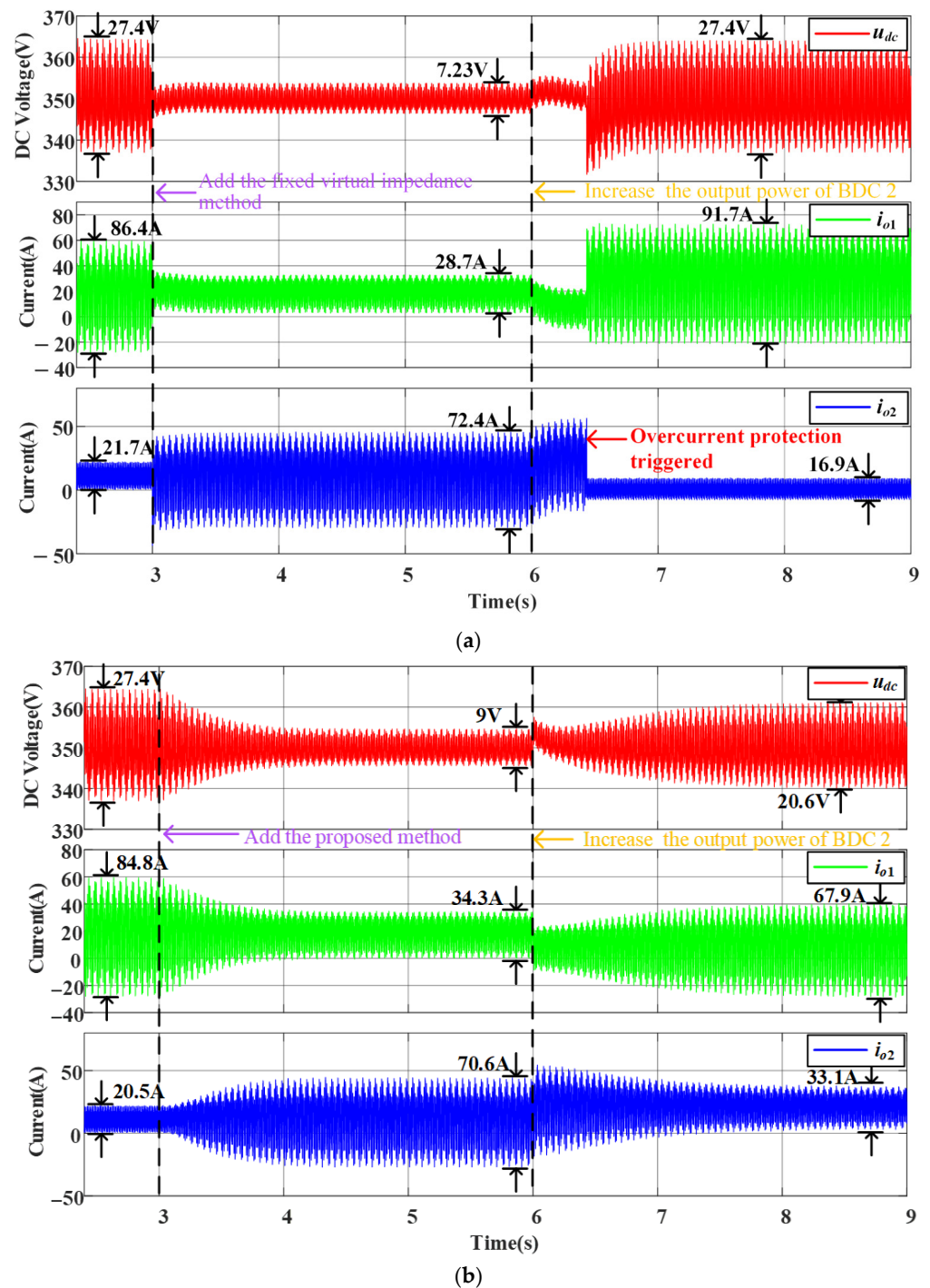


Figure 25. Cont.

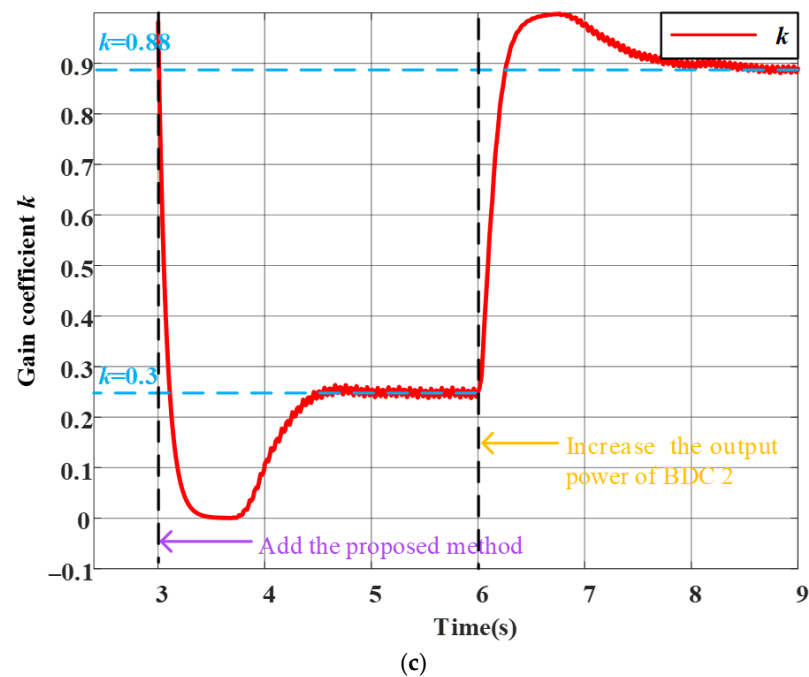


Figure 25. Simulation results comparing the method in [26] and the proposed method, and the variation curve of the gain coefficient k when the output power of BDC 2 decreases at $t = 6$ s. (a) DC bus voltage and BDC current waveforms using the method in [26] when the output power of BDC 2 decreases at $t = 6$ s. (b) DC bus voltage and BDC current waveforms using the proposed method when the output power of BDC 2 decreases at $t = 6$ s. (c) Variation curve of gain coefficient k when BDC 2 output power increases at $t = 6$ s.

4.2. Experimental Results Analysis

To further validate the engineering applicability of the proposed method, experiments are conducted on a hardware platform, with the experimental parameters kept consistent with the simulation settings. Since the random fluctuations of an AIDC load are difficult to reproduce in a laboratory environment, a single-phase load is connected to the DC bus through an inverter to intentionally introduce a second-harmonic voltage ripple on the bus, thereby verifying the effectiveness of the proposed strategy. Figure 26 illustrates the configuration of the experimental platform, where the core control algorithm is implemented and executed in real time on a TI TMS320F28376S digital signal processor (DSP) manufactured by Texas Instruments (Dallas, TX, USA).

From Figure 27, without the proposed control strategy, the DC bus voltage ripple amplitude is 28 V, and the voltage THD is 4.14%; the ripple current mainly flows into BDC 1, with the BDC 1 ripple current amplitude at 26 A and BDC 2 at 13.7 A.

4.2.1. Harmonic Suppression Performance

From Figure 28, when the proposed strategy is introduced with $k = 0$, the DC bus voltage ripple amplitude is suppressed to 4 V, the BDC 1 ripple current amplitude is suppressed to 5.6 A, the BDC 2 ripple current amplitude increases to 44 A, and the voltage THD decreases to 0.76%. Experimental results verify that BDC 2's equivalent harmonic impedance approaches zero at this time, presenting ideal voltage source characteristics and demonstrating extremely strong ripple suppression effects.

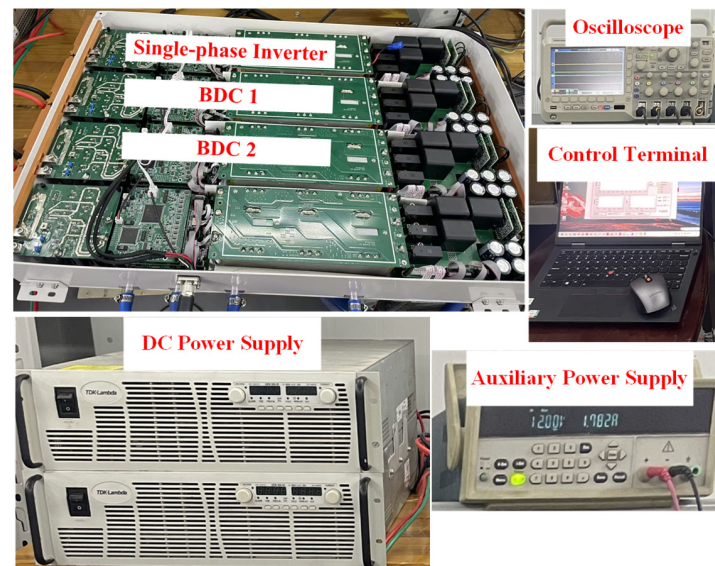
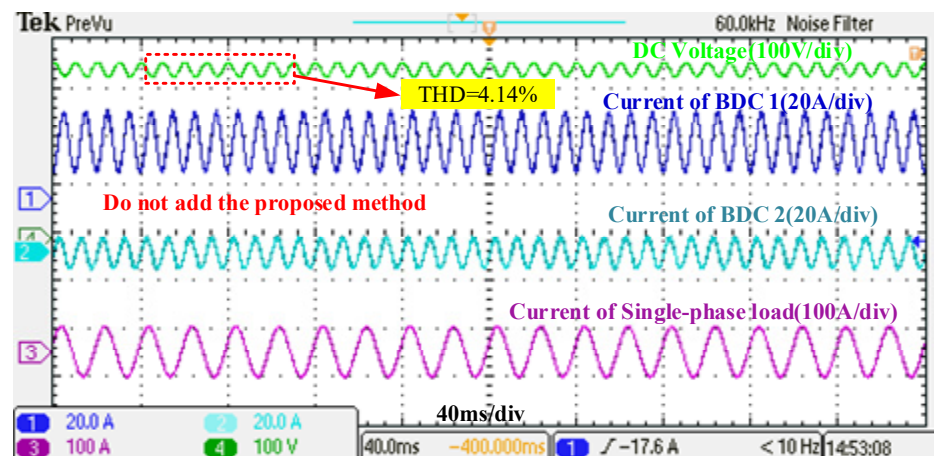
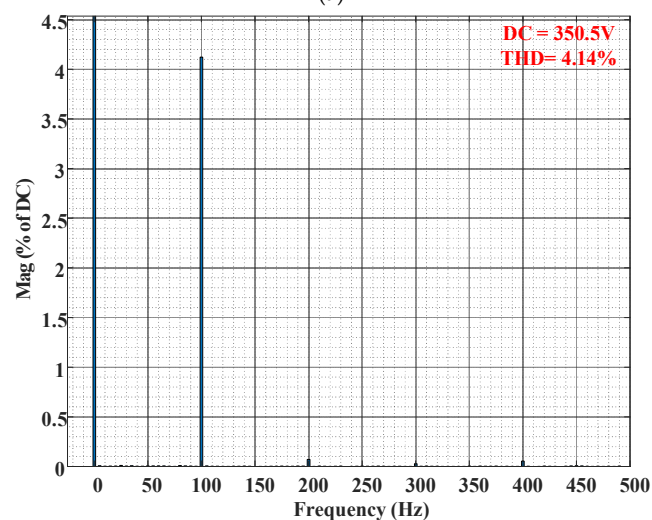


Figure 26. Configuration of the experimental platform.



(a)



(b)

Figure 27. Experimental waveforms and FFT analysis without the proposed strategy. (a) Waveforms of DC bus voltage, BDC output current, and single-phase AC load current without the proposed strategy. (b) FFT analysis of DC bus voltage without the proposed strategy.

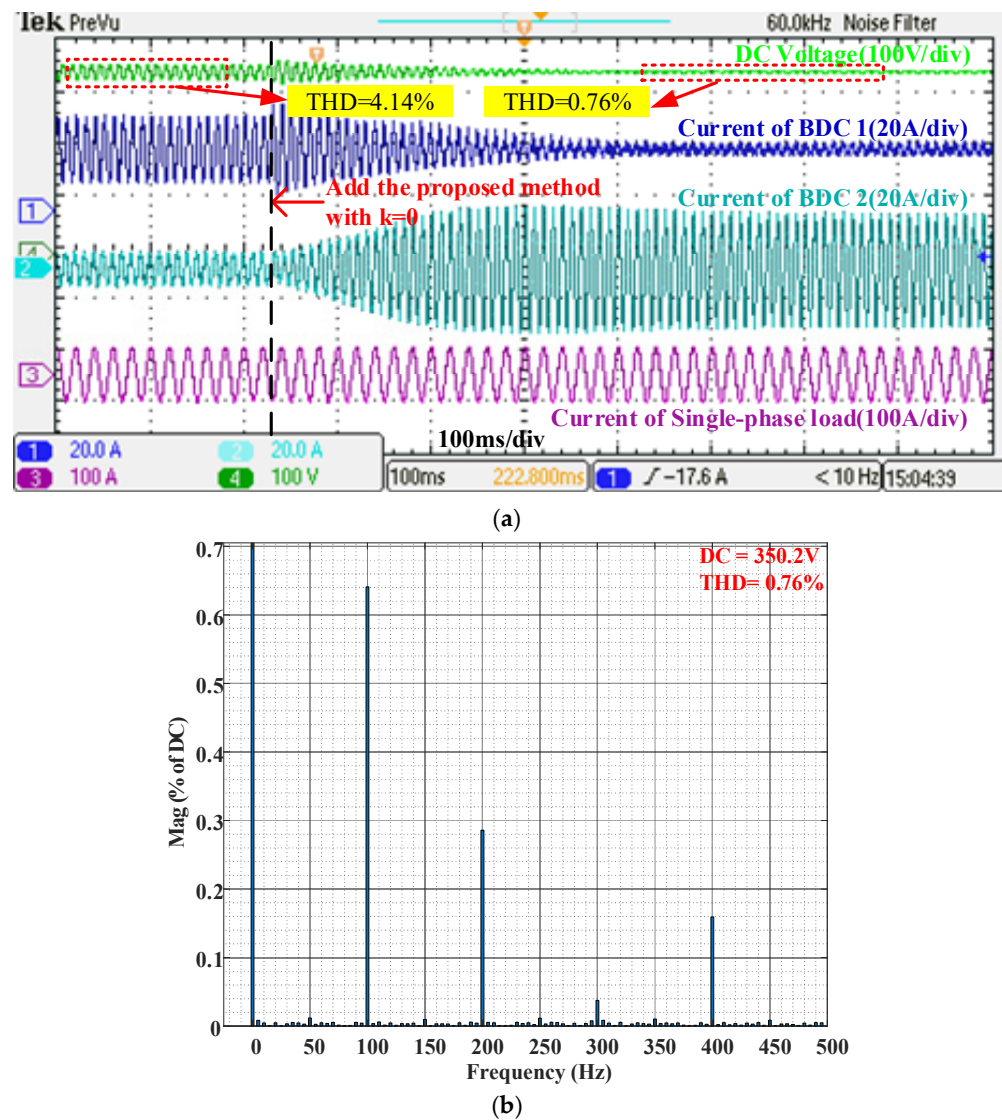


Figure 28. Experimental waveforms and FFT analysis with the proposed strategy ($k = 0$). (a) Waveforms of DC bus voltage, BDC output current, and single-phase AC load current with the proposed strategy ($k = 0$). (b) FFT analysis of DC bus voltage with the proposed strategy ($k = 0$).

From Figure 29, when k increases to 0.5, the converter's equivalent harmonic impedance increases moderately. DC bus voltage ripple amplitude rises to 8 V, voltage THD increases to 1.26%, BDC 1 ripple current amplitude rises to 8.7 A, and BDC 2 ripple current amplitude decreases to 41.6 A. Experimental results show that as k increases, harmonic absorption capability weakens, and bus power quality declines.

From Figure 30, when $k = 0.9$, the converter approaches a high-impedance state, and its suppression effect on bus harmonics weakens. Bus ripple amplitude increases to 20 V, voltage THD increases to 3.1%, BDC 1 ripple current amplitude rises to 19.7 A, and BDC 2 ripple current amplitude decreases to 20.4 A. Experimental results indicate that although compensation capability is significantly reduced, the overall performance is still better than the baseline condition without compensation.

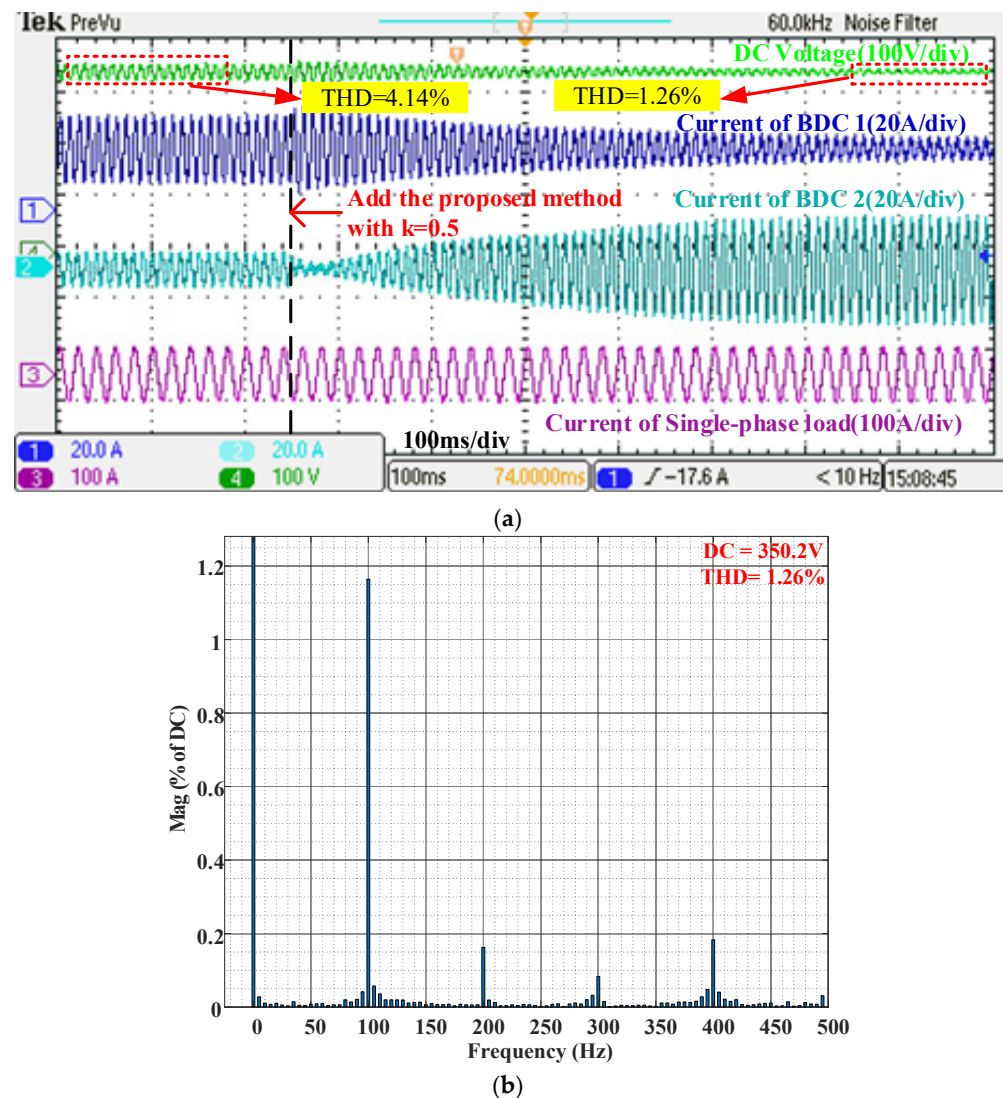


Figure 29. Experimental waveforms and FFT analysis with the proposed strategy ($k = 0.5$). (a) Waveforms of DC bus voltage, BDC output current, and single-phase AC load current with the proposed strategy ($k = 0.5$). (b) FFT analysis of DC bus voltage with the proposed strategy ($k = 0.5$).

4.2.2. Dynamic Adaptive Regulation Performance

Figures 31 and 32 show experimental results under a sudden increase and decrease in BDC 2 output power, respectively, verifying the online regulation capability under varying available capacity.

From Figure 31, when the BDC 2 output current is 5 A with the proposed strategy, BDC 2 has maximum remaining capacity and the lowest equivalent harmonic impedance. When the bus ripple amplitude is suppressed to 4 V, THD decreases to 0.76%, the ripple current into BDC 1 decreases to 5.6 A, and the ripple current absorbed by BDC 2 increases to 44 A. When the BDC 2 output current is suddenly increased to 15 A, BDC 2 adjusts its equivalent harmonic output impedance according to remaining capacity. At this point, the ripple voltage amplitude increases to 12 V, THD increases to 1.91%, the ripple current into BDC 1 increases to 8 A, and the ripple current absorbed by BDC 2 decreases to 35.4 A.

From Figure 32, when the BDC 2 output current is 15 A with the proposed strategy, BDC 2 adjusts its equivalent harmonic output impedance according to the remaining capacity. When the bus ripple amplitude is suppressed to 8.1 V, THD decreases to 1.36%, the ripple current into BDC 1 decreases to 7.2 A, and the ripple current absorbed by BDC 2 increases to 39.8 A. When the BDC 2 output current is suddenly decreased to 5 A, BDC 2

has the maximum remaining capacity and the lowest equivalent harmonic impedance. At this point, the ripple voltage amplitude is further reduced to 4 V, THD decreases to 0.76%, the ripple current into BDC 1 decreases to 5.6 A, and the ripple current absorbed by BDC 2 increases to 44 A.

Experimental results demonstrate that when the converter's available capacity is restricted, the proposed strategy prioritizes ensuring that the converter does not overcurrent or overload at the cost of sacrificing some power quality; when the converter's available capacity is sufficient, the proposed method automatically enhances harmonic absorption capability, thereby achieving dynamic matching between compensation capability and available capacity.

Due to the limitations of the experimental setup, the experiments in this paper mainly validate the DC bus power-pulsation condition caused by a single-phase load. To complement operating conditions that are difficult to realize on the current test bench, the simulation study further considers a harmonic source composed of multiple superimposed frequency components for a more comprehensive evaluation.

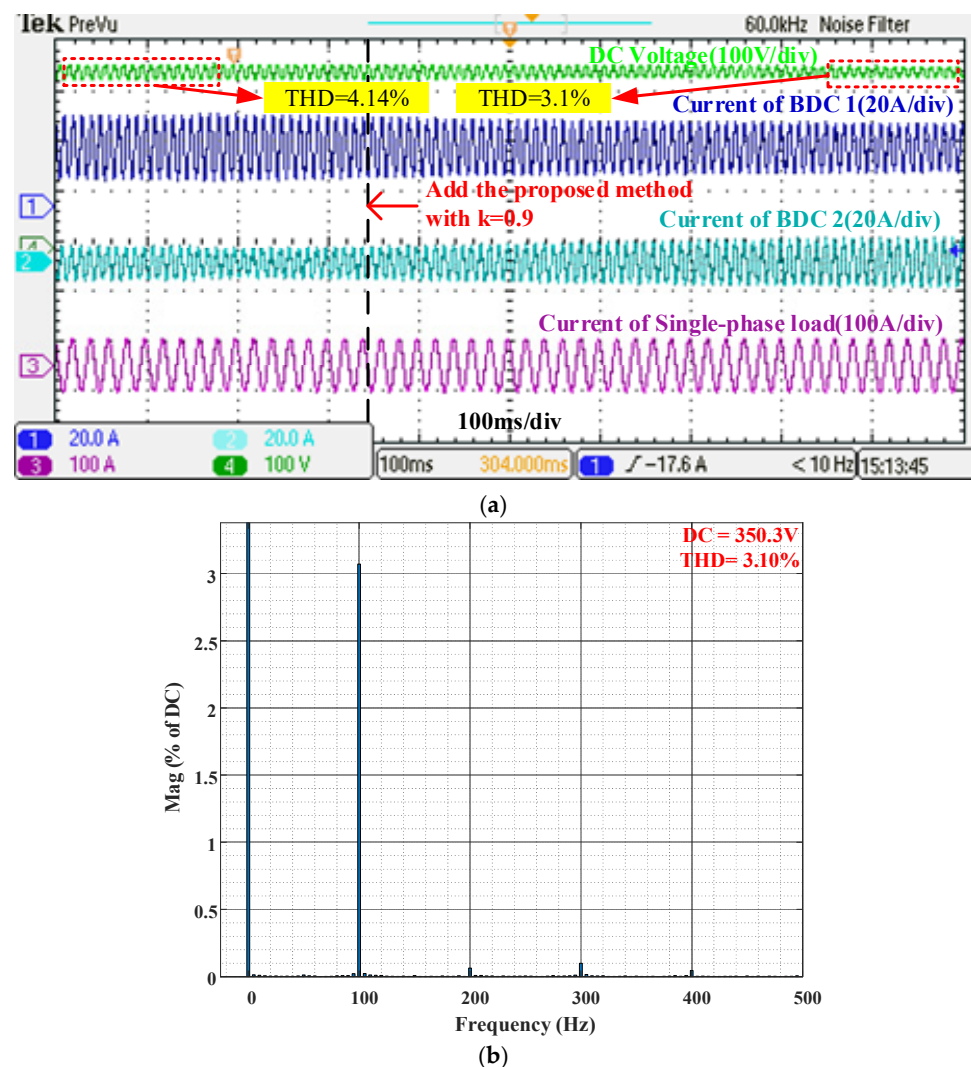


Figure 30. Experimental waveforms and FFT analysis with the proposed strategy ($k = 0.9$). (a) Waveforms of DC bus voltage, BDC output current, and single-phase AC load current with the proposed strategy ($k = 0.9$). (b) FFT analysis of DC bus voltage with the proposed strategy ($k = 0.9$).

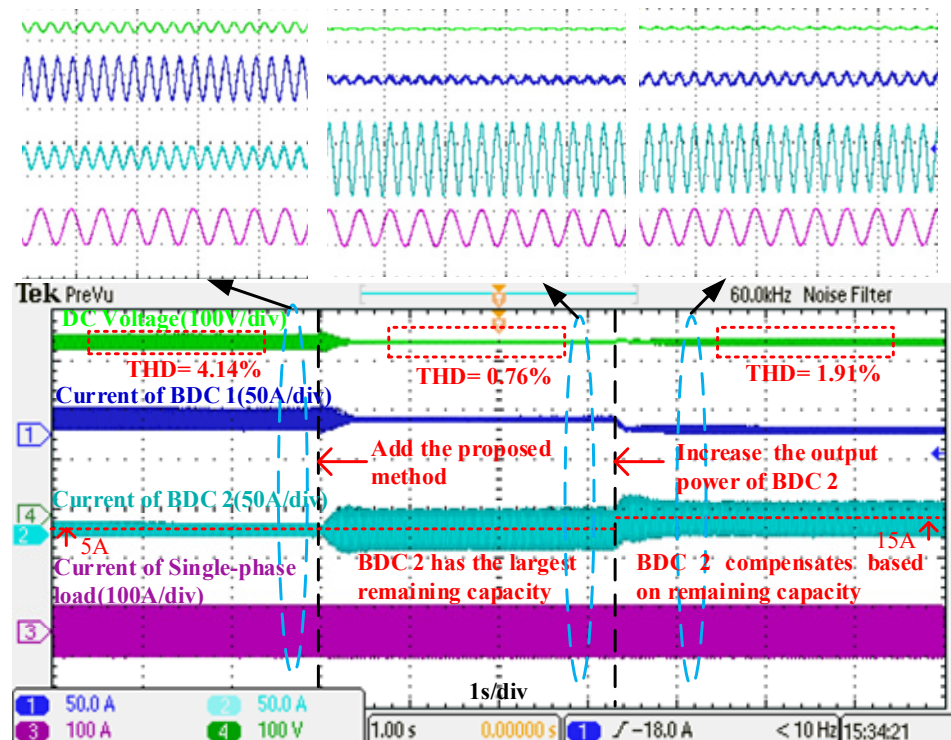


Figure 31. Experimental waveforms and FFT analysis results when BDC 2 output power suddenly increases.

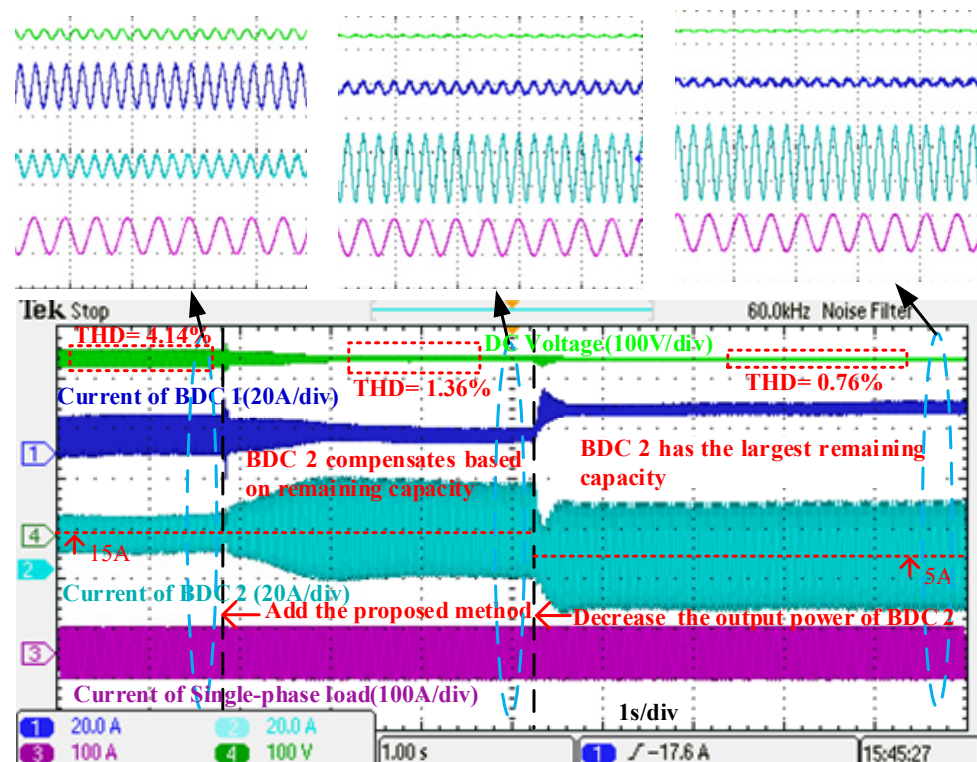


Figure 32. Experimental waveforms and FFT analysis results when BDC 2 output power suddenly decreases.

5. Conclusions

Addressing the issues of DC bus voltage ripple and power quality degradation caused by the stochastic fluctuation of AI computing loads, this paper proposes an adaptive harmonic impedance control and flexible compensation method. The main conclusions are as follows:

- (1) A virtual impedance control architecture combining bus voltage feedforward and output current feedback is constructed. Without relying on extremely high gains or narrow-band resonant links, controllable harmonic output impedance in the target frequency band is achieved through virtual impedance reshaping.
- (2) An adaptive adjustment mechanism considering converter capacity and current boundaries is established. By monitoring the power margin and current margin in real-time and dynamically adjusting the gain coefficient k , on-demand shaping of the BDC's equivalent harmonic impedance is realized.
- (3) Simulation and experimental results verify that the proposed method can smoothly transition between “strong compensation/low impedance” and “weak compensation/high impedance” modes according to the converter's operating state. This method not only effectively suppresses voltage ripples under steady-state conditions but also automatically limits compensation intensity under extreme conditions, achieving a good balance between improving power quality and ensuring system stability.

At present, the proposed method targets a control improvement for a single converter, and its applicability and performance in multi-converter systems remain to be further validated.

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