

Article

Triple-Voltage Gain and Self-Balancing in a New Switched-Capacitor Seven-Level Inverter for Microgrid Integration

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Abstract

In the context of power electronic interfaces in photovoltaic (PV), fuel cell, battery, and microgrid applications, the low output voltage of the DC source necessitates a voltage-boosting inverter. This paper proposes a single-source seven-level switched-capacitor boost inverter, particularly for low-voltage applications. The proposed inverter has the capability to produce seven different output voltage levels, i.e., intermediate boosted levels, with a total gain of three times the input voltage. The inverter has the advantage of a reduced number of power switches, diodes, and a switched-capacitor unit, which allows for single-stage operation without the need for a second DC-DC converter. The operating principle of the proposed inverter is explained in detail with a complete switching state analysis, conduction path analysis, and output voltage generation. The capacitor size is calculated using a charge balance-based equation. The self-balancing capability is validated for mismatched initial voltages with a bounded steady-state ripple. To evaluate the performance of the proposed inverter in a more realistic scenario, the effects of non-ideal device characteristics are considered, and the efficiency of the inverter is estimated using a loss model. A predictive current control technique is applied to control the output current under inductive load conditions. The simulation results obtained in MATLAB/Simulink software validate the proper seven-level operation of the inverter, the self-balancing capability of the capacitors, improved output waveform quality, and current control. The proposed inverter can be extended to grid-connected applications, where conventional output filters can be applied to meet the harmonic standards.

Keywords: seven-level boost inverter; switched-capacitor structure; PV system; low voltage stress; switch capacitor; multilevel inverter



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1. Introduction

Power electronic converters known as multilevel inverters (MLIs) are frequently used to convert DC voltage into AC voltage in numerous fields, including renewable energy systems, electric vehicles, microgrids, and power transmission and distribution systems [1]. When compared with the conventional two-level inverter, MLIs offer numerous advantages, including better voltage quality, reduced harmonic distortion, lower electromagnetic

interference, and higher reliability [1,2]. However, the use of MLIs also involves some disadvantages, including the complexity of the circuit, the use of more power electronic devices, and the voltage regulation of capacitors. Despite the disadvantages of MLIs, numerous researchers are interested in the use of MLIs because they are capable of overcoming the disadvantages of conventional two-level converters.

In the family of MLIs, the use of extensible multilevel inverters has been recognized as one of the promising power electronic converters for use in power systems where the voltage level and power rating are required to be changed frequently. The use of switched-capacitor-based multilevel converters enables the voltage boosting of the DC voltage without the use of any magnetic component and the need for an additional DC-DC conversion stage [1,3]. The use of switched-capacitor-based multilevel converters allows for the generation of multiple voltage levels using a DC voltage source, with the ability to increase the voltage level using the switched-capacitor cells [4–6].

In switched-capacitor-based multilevel converters, capacitors are used to store energy temporarily and discharge the energy during the switching time to generate the AC voltage with multiple levels [7]. The use of capacitors allows the generation of AC voltage with multiple levels using switched-capacitor cells without the use of any magnetic component. However, the use of switched-capacitor-based multilevel converters also has some disadvantages, including the regulation of capacitor voltage, higher current stress on the capacitor during the capacitor charging time, and the efficiency of the switched-capacitor-based multilevel converters [8–10].

Some other boost-capable multilevel inverter topologies with reduced switch count have also been reported. For example, a seven-level boost-capable multilevel inverter based on the packed U-cell configuration was reported in [11], in which active control of the capacitor voltage was required. A nine-level hybrid multilevel inverter using the H-bridge configuration for polarity reversal was reported in [12]. The switched-capacitor-based hybrid multilevel inverter reported in [13] requires reverse-blocking switches, and the packed E-cell configuration reported in [14] is not boost-capable. A diamond-shaped hybrid multilevel inverter was also reported in [15]. The configuration reported in this paper requires a higher number of voltage levels at the expense of a higher number of capacitors, diodes, and switches. A nine-level multilevel inverter using different voltage ratings for the capacitors was reported in [16] to achieve a higher voltage gain. However, this configuration also increases the design constraints.

In addition, various single-input and dual-source multilevel inverter configurations have been reported in the literature. For example, multilevel inverters were reported in [17–21]. In these studies, the voltage gain and the number of voltage levels increase at the expense of a higher number of components. Dual-source switched-capacitor-based multilevel inverters were reported in [22–27]. In these studies, the voltage levels increase at the expense of a higher number of voltage sources or non-boosting sources. Additionally, the voltage stress increases as the number of components increases in the configuration reported in [26,27].

Despite the extensive research carried out on boost-capable multilevel inverters, there are certain limitations that have been identified with the existing topologies. Some of the existing topologies require a higher number of components, complex hybrid structures, and the use of different voltage-rated capacitors. Moreover, in certain topologies of switched-capacitor-based inverters, the capacitor voltage balancing is not inherently ensured. This requires additional sensing and control of the capacitor voltages. This adds additional control complexity and reduces the converter's reliability. Certain existing topologies have also been implemented with hybrid H-bridge structures and reverse-blocking switches. This results in increased voltage stress on the switches and also increases the cost of the

converter. Moreover, certain existing topologies have not clearly described all the operating modes and conduction paths of the converters for the intermediate voltage levels. This adds additional complexity to the reproduction of the converter.

Boost inverters are commonly used in photovoltaic systems. The low output voltage of the PV panel needs to be boosted to a higher level that is suitable for grid-connected inverters. Single-stage boost multilevel inverters have the potential to reduce the size and losses of the system. The multilevel output of the converter reduces the harmonic distortion of the output current. This reduces the filter requirements of the system. The converter can be designed to meet the harmonic standards of the grid with the addition of a suitable filter. Moreover, the operating principle of the switched capacitor is a conceptual step towards the adaptation of the converter for energy storage-embedded converter configurations [28].

Inspired by the above explanations, this paper presents a new configurable switched-capacitor multilevel inverter with the capability to produce seven different voltage levels with a total gain of around three, utilizing a single DC source. Compared to existing multilevel inverters, the proposed topology is unique due to the following reasons: fewer components are used; capacitor voltage balancing is achieved naturally; the maximum voltage rating of the components is fixed; and the operating modes for all seven voltage levels are clearly explained. Moreover, the proposed topology is also suitable for extending the configuration with the help of switched-capacitor blocks to obtain higher voltage gain with the same operating principle.

The rest of the paper is organized as follows: Section 2 explains the proposed topology and its operating principle. Section 3 explains the modulation and control techniques. Section 4 explains the simulation and performance analysis for different operating conditions. Section 5 explains the comparison with existing topologies. Finally, Section 6 concludes the paper with future work.

2. Proposed Topology

The suggested multilevel inverter topology is composed of one DC voltage source and a switched-capacitor component. The suggested topology is presented in Figure 1. The topology is composed of two capacitors represented as C_1 and C_2 , two diodes represented as D_1 and D_2 , and eight active power switches represented as S_1 to S_8 . The left part of the topology is the switched-capacitor boosting network, while the right part is the single-phase inverter bridge.

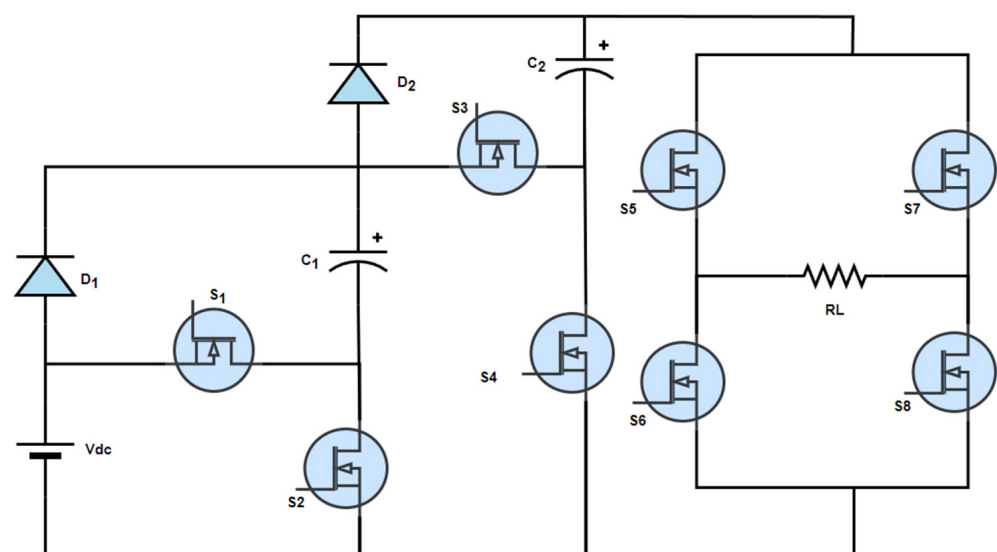


Figure 1. Proposed topology for the triple-boost input with a seven-level output.

The main purpose of the switched-capacitor network is to provide the voltage-boosting function. The capacitors C_1 and C_2 are selectively connected to the DC voltage source through different states. The capacitors can be connected individually or together in series with the DC voltage source. The generation of multiple voltage levels is achieved without the requirement of an additional DC-DC converter. The diodes D_1 and D_2 provide a unidirectional path for the current. This path is essential for proper capacitor charging.

Through the appropriate coordination of the switching states, the proposed inverter is able to produce seven different discrete output voltage levels, i.e., $0V_{dc}$, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$. The intermediate voltage levels are achieved by connecting one of the switched capacitors in series with the DC source, while the maximum voltage levels are achieved by connecting both capacitors in series with the DC source. The zero-voltage level is achieved through the freewheeling states of the inverter bridge, thus allowing the current to flow continuously during the supply of inductive loads.

A significant advantage of the proposed inverter topology is that the charging and discharging times of the two capacitors, i.e., C_1 and C_2 , are complementary, constituting one fundamental cycle. This ensures that the capacitor voltages will converge to their rated values, thus providing the advantage of self-balancing without the need for additional voltage sensors. Moreover, the blocking voltage of the power switches is bounded by the boosted DC-link voltage, thus improving the scalability of the proposed inverter topology.

2.1. The Operating Principle of the Seven-Level Boost Inverter

Table 1 below shows a summary of valid switching states of the proposed SCMLI and their associated voltage levels. It is evident from Table 1 that the proposed SCMLI has the capability to generate seven different voltage levels. The seven levels comprise zero-voltage levels, positive and negative levels of the input voltage, intermediate levels of boosting, and the maximum levels of boosting. In Table 1, “+,” “−,” and “idle” refer to the state where the corresponding capacitor is in the process of charging, discharging, or neither charging nor discharging, respectively.

Table 1. Switching configurations and resulting output voltages of the proposed topology.

S1	S2	S3	S4	S5	S6	S7	S8	C	Vector	Output
0	0	0	0	1	0	1	0	idle	V0	0
0	1	0	1	1	0	0	1	+	V1	+V _{dc}
0	0	1	0	1	0	0	1	−	V2	+2V _{dc}
1	0	1	0	1	0	0	1	−	V3	+3V _{dc}
0	0	0	0	0	1	0	1	idle	V4	0
0	1	0	1	0	1	1	0	+	V5	−V _{dc}
0	0	1	0	0	1	1	0	−	V6	−2V _{dc}
1	0	1	0	0	1	1	0	−	V7	−3V _{dc}

In order to simplify the explanation of the operating principle of the proposed SCMLI, the following assumptions are made:

- (1) The input voltage is considered to be constant.
- (2) The voltages across the capacitors in the proposed SCMLI circuit are considered to be at their normal values.
- (3) The power semiconductor devices in the SCMLI circuit are considered to be ideal.

Note that these assumptions are made for analytical purposes only.

2.1.1. Zero-Voltage Level Operation

The zero-voltage level is achieved using two different switching states that allow for bidirectional current flow in the presence of an inductive load. When the voltage level is zero, the load current flows through the freewheeling path provided by the appropriate inverter switches. During this operating mode, both capacitors are in an idle state, and no interaction with the capacitors occurs. This operating mode ensures a smooth flow of current and stable operation with an inductive load.

2.1.2. Positive Voltage Levels

The positive fundamental voltage level, $+V_{dc}$, is achieved by connecting the DC source to the load through the inverter switches, with both capacitors either in charging mode or idle state. During this operating mode, the inverter circuit operates as a conventional voltage-source inverter with one DC source connected to the load.

The intermediate voltage level, $+2V_{dc}$, is achieved by connecting one switched capacitor in series with the DC source. During this operating mode, one capacitor discharges to support the load voltage, with the other capacitor either in charging mode or an idle state. This operating mode is specifically included in Table 1 and is essential in achieving the true seven-level inverter.

The maximum boosted voltage level, $+3V_{dc}$, can be achieved by connecting both capacitors in series with the DC source. In this configuration, both capacitors will discharge and supply voltage to the load.

2.1.3. Negative Voltage Levels

Negative voltage levels are achieved by using the same operating principle but with opposite current flow in the inverter switches. The zero-voltage level in the negative half-cycle is achieved by an alternative configuration in freewheeling mode.

The $-V_{dc}$ voltage level is achieved by simply connecting the DC source in series with the load, but with a reversed polarity. In this configuration, the capacitors are either in a charging mode or idle. The $-2V_{dc}$ voltage level is achieved by simply combining the DC source with a discharging capacitor in series with the load. Finally, the $-3V_{dc}$ voltage level is achieved by discharging both capacitors in series with the DC source.

2.1.4. Inductive Load Compatibility and Self-Balancing Behavior

For all operating modes, a closed current path is provided by the proposed inverter. Thus, inductive load compatibility is ensured by the proposed inverter. The capacitors' charging/discharging intervals are complementary in a fundamental cycle. Thus, capacitor voltage self-balancing is inherently achieved without using additional control blocks.

The switching states corresponding to each voltage level are provided in Table 1. The conduction paths for positive and negative voltage levels are shown in Figures 2 and 3.

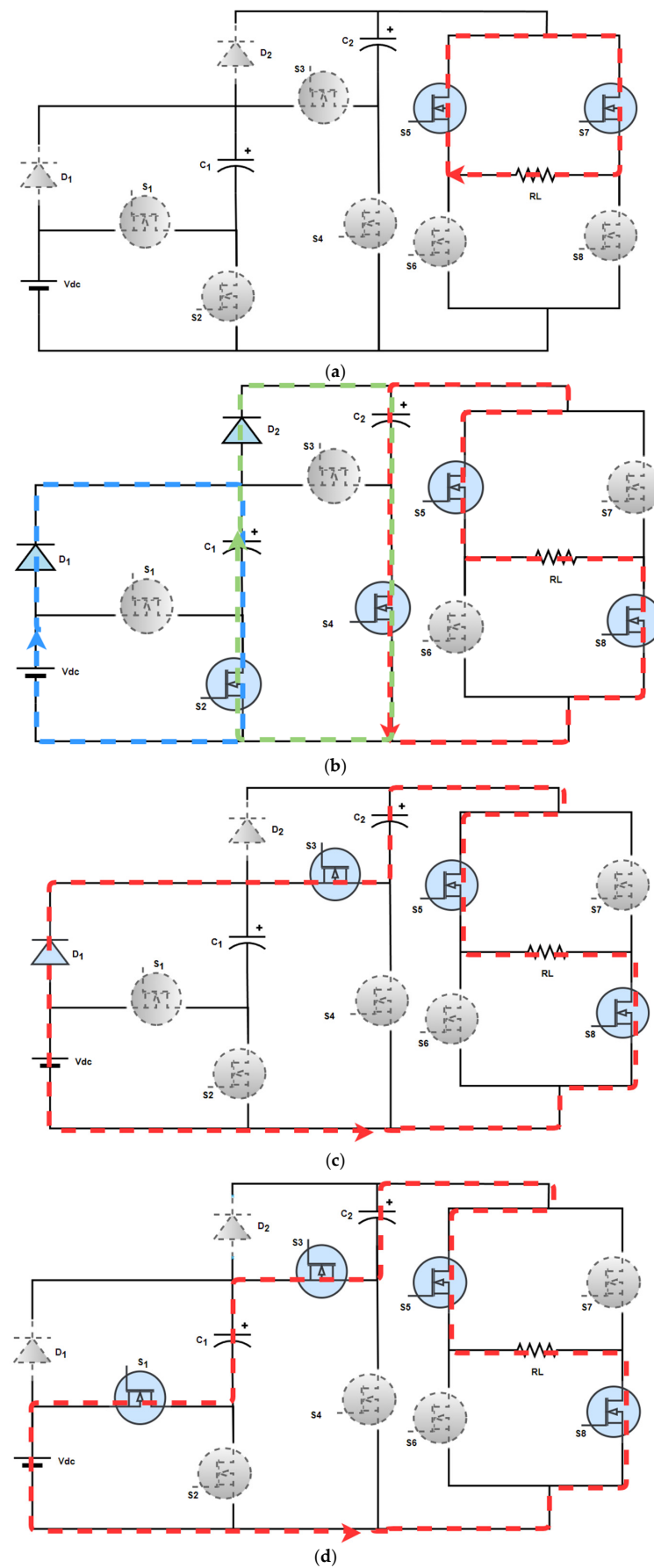


Figure 2. Positive sequence operation of the proposed topology: (a) $V_o = 0$, (b) $V_o = V_{dc}$, (c) $V_o = 2V_{dc}$, and (d) $V_o = 3V_{dc}$.

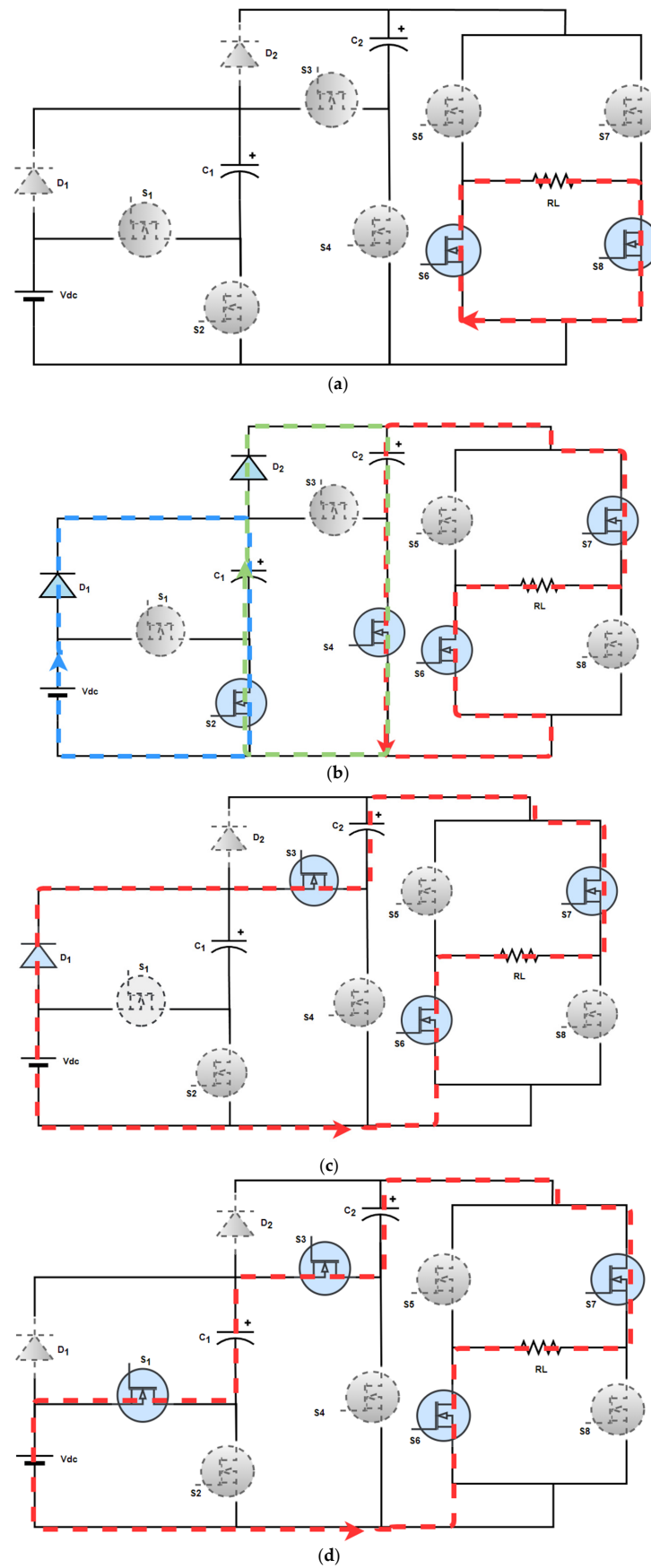


Figure 3. Negative sequence operations of the proposed topology: (a) $V_o = 0$, (b) $V_o = -V_{dc}$, (c) $V_o = -2V_{dc}$, and (d) $V_o = -3V_{dc}$.

2.2. Design of the Capacitor

The selection of an appropriate capacitance value is critical in controlling the voltage ripple across the switched-capacitor network and generating stable multilevel voltages. The voltage ripple across the capacitor can result in distortion of the multilevel voltage, increased current stress, and degradation of the inherent self-balancing characteristics. Therefore, the capacitor selection should be based on the actual charging and discharging characteristics observed during the inverter operation.

At the initial condition, the capacitor is assumed to be uncharged, which can be expressed as follows:

$$\left. \begin{array}{l} V_c(0) = 0 \\ i_c(0) = 0 \end{array} \right\} \quad (1)$$

During the charging interval (as shown in the figures illustrating the charging modes of the operating principle), the capacitor is connected to the input source. In this case, the voltage of the capacitor is equal to the DC voltage of the input, and the current of the capacitor depends on the difference between the input current and the load current:

$$\left. \begin{array}{l} V_c = V_{dc} \\ i_c = i_{in} - i_{load} \end{array} \right\} \quad (2)$$

During the discharging period, the capacitor contributes to the output voltage level. In this mode of operation, the capacitor voltage contributes to the generation of the output voltage, and the capacitor current is mainly equal to the load current.

$$\left. \begin{array}{l} V_c = V_o - V_{dc} \\ i_c = i_{in} \end{array} \right\} \quad (3)$$

The capacitor voltage ripple is governed by the fundamental capacitor equation, which relates the voltage variation to the net transferred charge:

$$\Delta V_c = \frac{1}{C} \int_{t_1}^{t_2} i_c(t) dt \quad (4)$$

To obtain a useful design equation, the capacitor current during the worst-case charging or discharging period may be taken as its average value. The minimum capacitance value may therefore be expressed as follows:

$$C \geq \frac{I_{c,avg} T_{eff}}{\Delta V_c} \quad (5)$$

Here, $I_{c,avg}$ represents the average capacitor current during the effective charge or discharge interval, T_{eff} represents the duration of the corresponding switching state within one switching period, and ΔV_c is the allowable peak-to-peak capacitor voltage ripple.

The worst-case ripple occurs in situations of high load current and in modes where intermediate levels of boosted voltage are generated. Therefore, it is important that the capacitor value is determined with consideration of the maximum load current and the longest discharge time. The equivalent series resistance of the capacitor is another factor that contributes to additional voltage ripple and power loss. Therefore, it is important that low-ESR capacitors are used, along with a design margin.

2.3. Current and Voltage Stresses

Table 2 presents a summary of the voltage and current stresses experienced by the power switches in the proposed seven-level boost inverter. The voltage stress experienced

by each power switch in the proposed inverter depends on the location of the particular switch in the switched-capacitor network and the inverter bridge. The current stress on each power switch in the proposed inverter depends on the active conduction path for a given switching state.

In the proposed inverter, power switches S5, S6, S7, and S8 form part of the inverter bridge. As a result, these power switches are subjected to the highest voltage stress in comparison with other power switches in the proposed inverter. The voltage stress experienced by these power switches in the proposed inverter occurs during inverter operation at the highest voltage level. Consequently, these power switches are subjected to a voltage stress equal to three times the input DC voltage. The voltage stress experienced by power switches S1, S2, and S3 in the proposed inverter is due to the input DC voltage, while S4 experiences twice that voltage.

Table 2. Voltage and current stresses on power switches.

Switches	Voltage Stress	Current Stress
S1	Vdc	Load/Iin
S2	Vdc	Load/Iin
S3	Vdc	Load/Iin
S4	2Vdc	Load/Iin
S5	3Vdc	Load/Iin
S6	3Vdc	Load/Iin
S7	3Vdc	Load/Iin
S8	3Vdc	Load/Iin

The current stress on the power switches in the proposed inverter depends on the load current through a particular active conduction path. During operation of the proposed inverter at boosted voltage levels, the power switches forming part of the series-connected capacitors are subjected to a current stress equal to the inverter DC-link current supplied to the load. Consequently, to ensure the safe operation of the proposed inverter, all power switches should be rated for a current stress equal to the inverter current.

2.4. Loss Analysis

This section aims to quantify the power losses of the proposed inverter topology by taking into consideration the major non-ideal characteristics of semiconductor devices and the switched capacitors used in the topology. The total power loss is calculated as the sum of the individual power losses due to (i) switch conduction loss, (ii) switch switching loss, (iii) diode conduction loss, and (iv) capacitor ESR loss. Since the proposed topology does not use inductors, magnetic losses are not considered.

2.4.1. Total Loss Model

The total converter loss is defined as the sum of the following: (i) total switch conduction loss, (ii) total switching loss, (iii) diode conduction loss, and (iv) capacitor ESR loss. It can be expressed as

$$P_{\text{loss}} = P_{\text{cond,sw}} + P_{\text{sw}} + P_{\text{d}} + P_{\text{ESR}} \quad (6)$$

The efficiency is given by

$$\eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \quad (7)$$

2.4.2. Switch Conduction Loss

For a MOSFET implementation, the conduction loss of switch j is

$$P_{\text{cond},j} = R_{\text{ds(on)},j} I_{j,\text{rms}}^2, \quad (8)$$

and thus,

$$P_{\text{cond,sw}} = \sum_{j=1}^8 P_{\text{cond},j}. \quad (9)$$

(For an IGBT, $P_{\text{cond},j} \approx V_{\text{CE(sat)},j} I_{j,\text{avg}}$).

2.4.3. Switching Loss

The switching loss of switch j can be estimated using datasheet switching energies:

$$P_{\text{sw},j} = f_{\text{sw},j} (E_{\text{on},j} + E_{\text{off},j}), \quad (10)$$

and the total switching loss is

$$P_{\text{sw}} = \sum_{j=1}^8 P_{\text{sw},j}. \quad (11)$$

For PD-PWM, $f_{\text{sw},j} \approx f_{\text{sw}}(\text{fixed})$. For FS-MPC, $f_{\text{sw},j}$ is the effective switching rate extracted from the switching events per second.

2.4.4. Diode Conduction Loss

For each diode $k \in \{1, 2\}$,

$$P_{\text{d},k} = V_{f,k} I_{d,k,\text{avg}}. \quad (12)$$

Hence,

$$P_{\text{d}} = \sum_{k=1}^2 P_{\text{d},k}. \quad (13)$$

2.4.5. Capacitor ESR Loss

The ESR loss in capacitor $m \in \{1, 2\}$ is

$$P_{\text{ESR},m} = r_{\text{ESR},m} I_{c,m,\text{rms}}^2, \quad (14)$$

and thus

$$P_{\text{ESR}} = \sum_{m=1}^2 P_{\text{ESR},m}. \quad (15)$$

The RMS/average currents $I_{j,\text{rms}}$, $I_{d,k,\text{avg}}$, $I_{c,m,\text{rms}}$ are obtained from simulation waveforms over one fundamental cycle, ensuring that all seven voltage levels (including the intermediate levels) are included in the loss estimation. The loss model is used to estimate converter efficiency under realistic operating conditions; experimental validation is planned for future work.

3. Model Predictive Control of the Proposed Seven-Level Boost Inverter

To control the output current of the proposed seven-level boost inverter, the finite control set model predictive control strategy is used. The strategy directly exploits the inverter's discrete switching states and predicts the future behavior of the output current

for each voltage level. For the single-phase RL load connected to the output of the inverter, the continuous-time dynamic model of the load current can be articulated as follows:

$$\frac{di_o}{dt} = \frac{1}{L}(v_o - Ri_o) \quad (16)$$

where i_o is the output current, v_o is the inverter output voltage, R is the load resistance, and L is the load inductance.

Using a forward Euler discretization with sampling interval T_s , the discrete model of the output current can be written as follows:

$$i_o(k+1) = i_o(k) + \frac{T_s}{L}(v_o(k) - Ri_o(k)) \quad (17)$$

At each sampling instant, the inverter can generate a finite set of output voltage levels corresponding to its switching states. For the proposed topology, the available voltage level is

$$V_i \in \{V_0, V_1, \dots, V_7\} \quad (18)$$

where each voltage level V_i corresponds to a specific switching vector of the seven-level inverter.

Using the discrete-time model in (17), the future output current is predicted for each candidate voltage level V_i , yielding

$$i_o(k+1) = i_o(k) + \frac{T_s}{L}(V_i - Ri_o(k)) \quad (19)$$

In order to find the optimal switching state, a cost function is defined to evaluate the tracking error between the predicted output current and the reference current. A basic form of the cost function is given by

$$J_i = \left| i_{ref}(k+1) - i_o^{(i)}(k+1) \right| \quad (20)$$

where $i_{ref}(k+1)$ is the reference current at the next sampling instant.

To improve control performance and reduce excessive voltage transitions, a weighted cost function can be employed as

$$J_i = \alpha \left| i_{ref}(k+1) - i_o^{(i)}(k+1) \right| + \beta |V_i| \quad (21)$$

where α and β are weighting factors that balance current tracking accuracy and switching effort.

Finally, the minimized cost of choosing a vector V_{opt} can be expressed as

$$V_{opt} = \underset{i}{\operatorname{argmin}} J_i \quad (22)$$

The switching state related to V_{opt} is subsequently applied to the inverter in the following sampling period. This predictive control technique enables a prompt dynamic response, precise current control, and direct control of the discrete voltage levels related to the proposed seven-level inverter.

4. Modulation Strategy

To show the effectiveness of the dynamic performance and tracking ability of the finite set model predictive control (FS-MPC) method, a conventional phase disposition PWM (PD-PWM) method is employed as a baseline comparison method. Multilevel inverters can be controlled using various pulse-width modulation techniques to produce stepped waveforms with reduced harmonic distortion. Various modulation techniques

for multilevel inverters have been proposed in the literature, such as sinusoidal PWM, space-vector PWM, and selective harmonic elimination PWM. SVPWM is reported to produce satisfactory results for inverters with a small number of voltage levels [26]. However, the complexity of the SVPWM technique is reported to increase with the number of levels in the inverter. The SHE-PWM technique is reported to produce satisfactory results by improving the utilization of the DC link voltage and reducing the number of switching cycles. However, the use of the SHE-PWM technique is limited due to the non-linear equations involved in the modulation index calculations, as well as the parameter sensitivity of the technique. Therefore, the carrier-based sinusoidal PWM technique has been widely used for the modulation of multilevel inverters due to its simplicity and robustness.

In this work, the proposed seven-level boost inverter is modulated using the phase disposition PWM technique, which is a well-established carrier-based sinusoidal PWM technique for the modulation of multilevel inverters. In the PD-PWM technique, the carrier signals are of the same frequency and amplitude, with a phase difference of zero degrees between the carrier signals.

For the proposed seven-level inverter, six triangular carrier signals are required for the modulation of the inverter. As shown in Figure 4a, six triangular carrier signals, denoted as V_{cr1} – V_{cr6} , are compared with a sinusoidal signal denoted as V_{ref} . The amplitude of the sinusoidal signal is denoted as A_{ref} , while the frequency of the sinusoidal signal is denoted as f_{ref} . The modulation index is defined as the ratio of the amplitude of the sinusoidal signal to the amplitude of the carrier signal, with the modulation index set to 0.9 in this work.

The comparison between the reference signal and the six carriers produces gating signals for the generation of the seven different voltage levels. Depending on the instantaneous position of the reference signal relative to the carrier bands, the inverter output switches between the different voltage levels 0, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$. The two intermediate voltage levels, $\pm 2V_{dc}$, naturally occur when the reference signal is between the two carrier thresholds. This naturally produces the seven-level inverter output.

The gating signals for the switches S1–S8 for a fundamental cycle are shown in Figure 4b. Because of the symmetry in the proposed topology, the switches S1–S4 operate synchronously to control the switched-capacitor network, and the inverter bridge switches operate in pairs, (S5, S7) and (S6, S8), to produce positive and negative voltage levels. This reduces the total gate drivers required compared to conventional multilevel inverter configurations.

The output voltage waveform is shown in Figure 4c, where all seven voltage levels can be observed. The stepped waveform follows the sinusoidal reference signal closely, verifying the effectiveness of the proposed PD-PWM strategy in generating a high-quality output voltage and fully utilizing the voltage-boosting potential of the proposed topology.

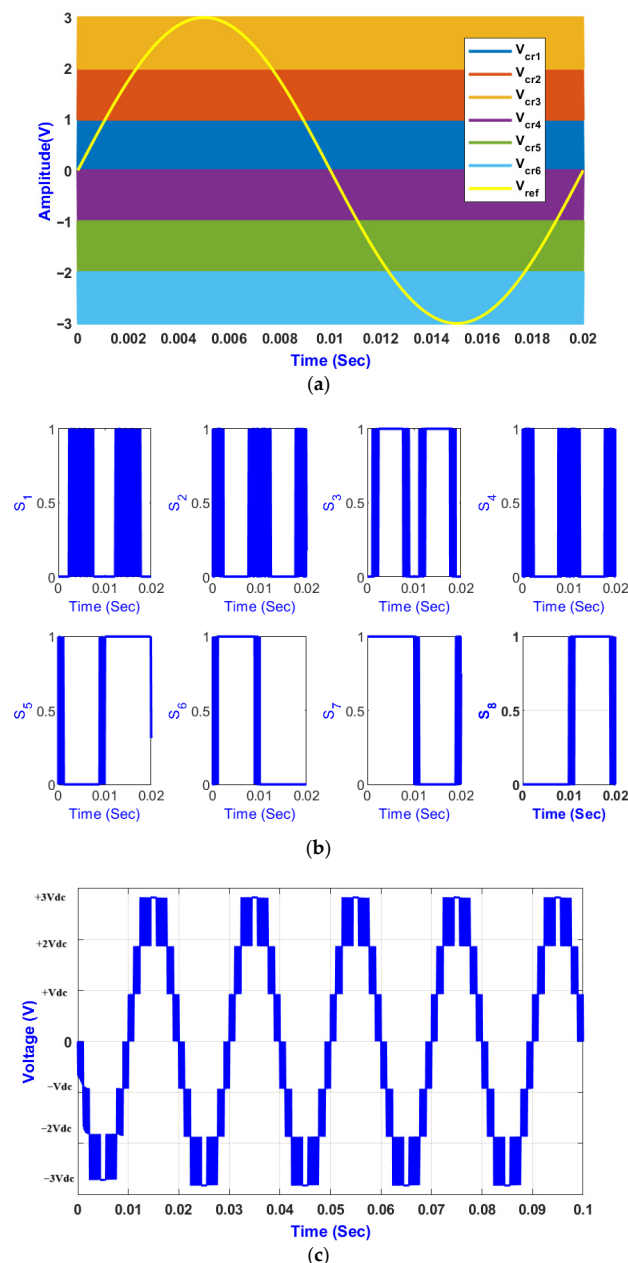


Figure 4. (a) Modulation signals, (b) switching signals, and (c) output voltage.

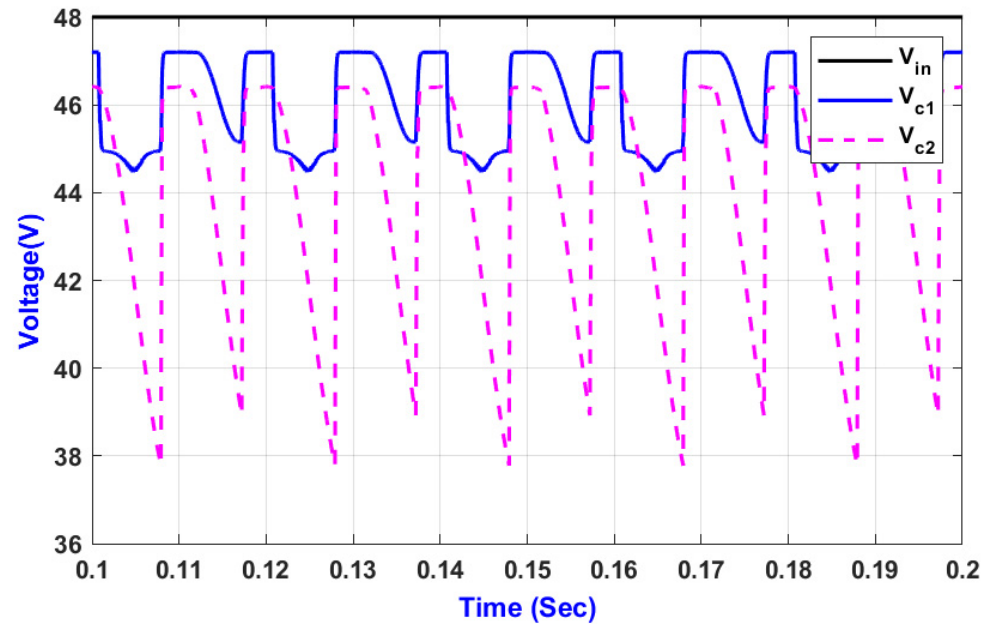
5. Simulation Results

A comprehensive simulation model of the proposed seven-level switched-capacitor boost inverter was developed using MATLAB/Simulink to verify the topology as well as the modulation and control strategies used. The parameters used in the simulation model are given in Table 3.

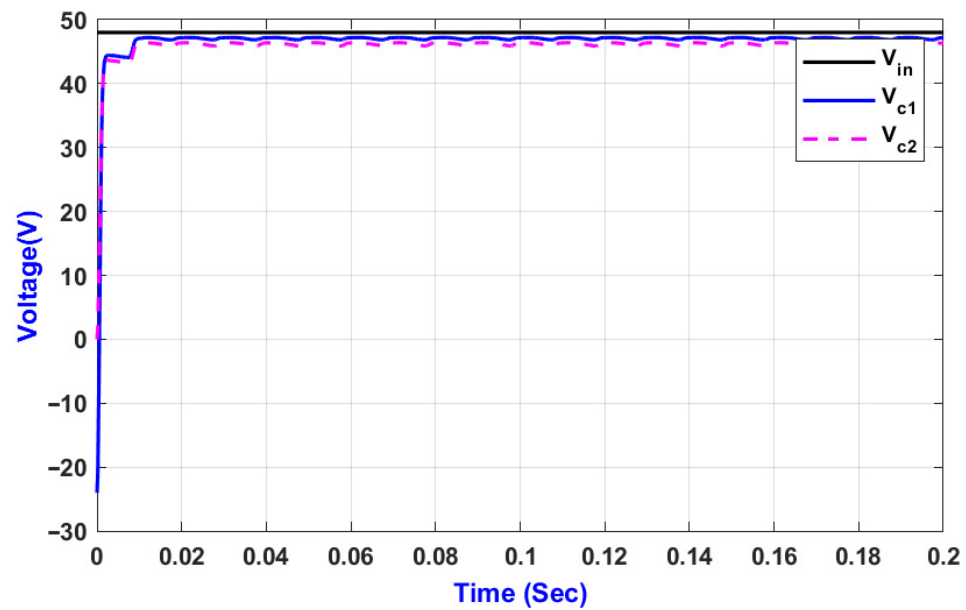
Table 3. The simulation parameters of the proposed topology.

Parameters	Values
Input voltage	48 V
Switching Frequency	20 kHz
Modulation index	0.9
capacitor	2200 μ f
Resistive, inductive load	25 Ω –20 mH

The simulation results are presented in Figures 5–9. Figure 5a,b show the capacitor voltage waveforms obtained with RL loading by adopting the PD-PWM and FS-MPC control methods. In both instances, it is evident that the capacitor voltage is steady and remains centered around the input DC voltage of 48 V. This is an inherent feature of the proposed topology. The peak-to-peak voltage ripple is limited and remains within the acceptable value of less than 2.7 V.



(a)



(b)

Figure 5. The voltage across the switched boost capacitor: (a) PD-PWM and (b) MPC.

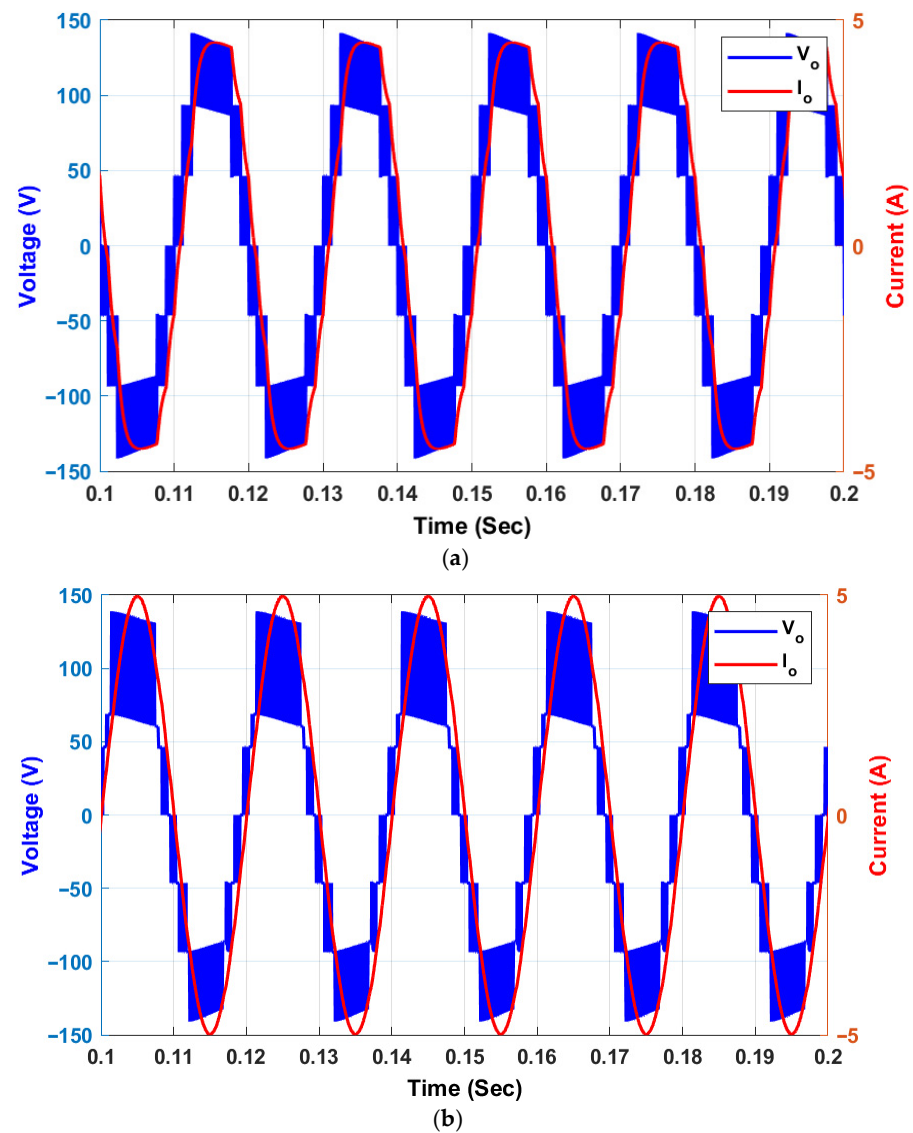


Figure 6. The waveforms of output voltage and current: (a) PD-PWM and (b) MPC.

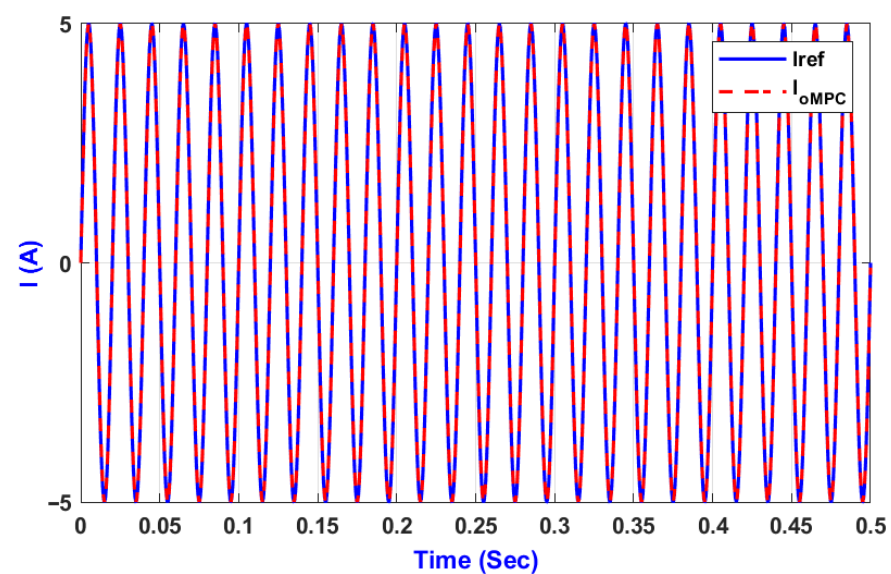


Figure 7. Output current response under finite-set model predictive control (FS-MPC) compared with the reference current.

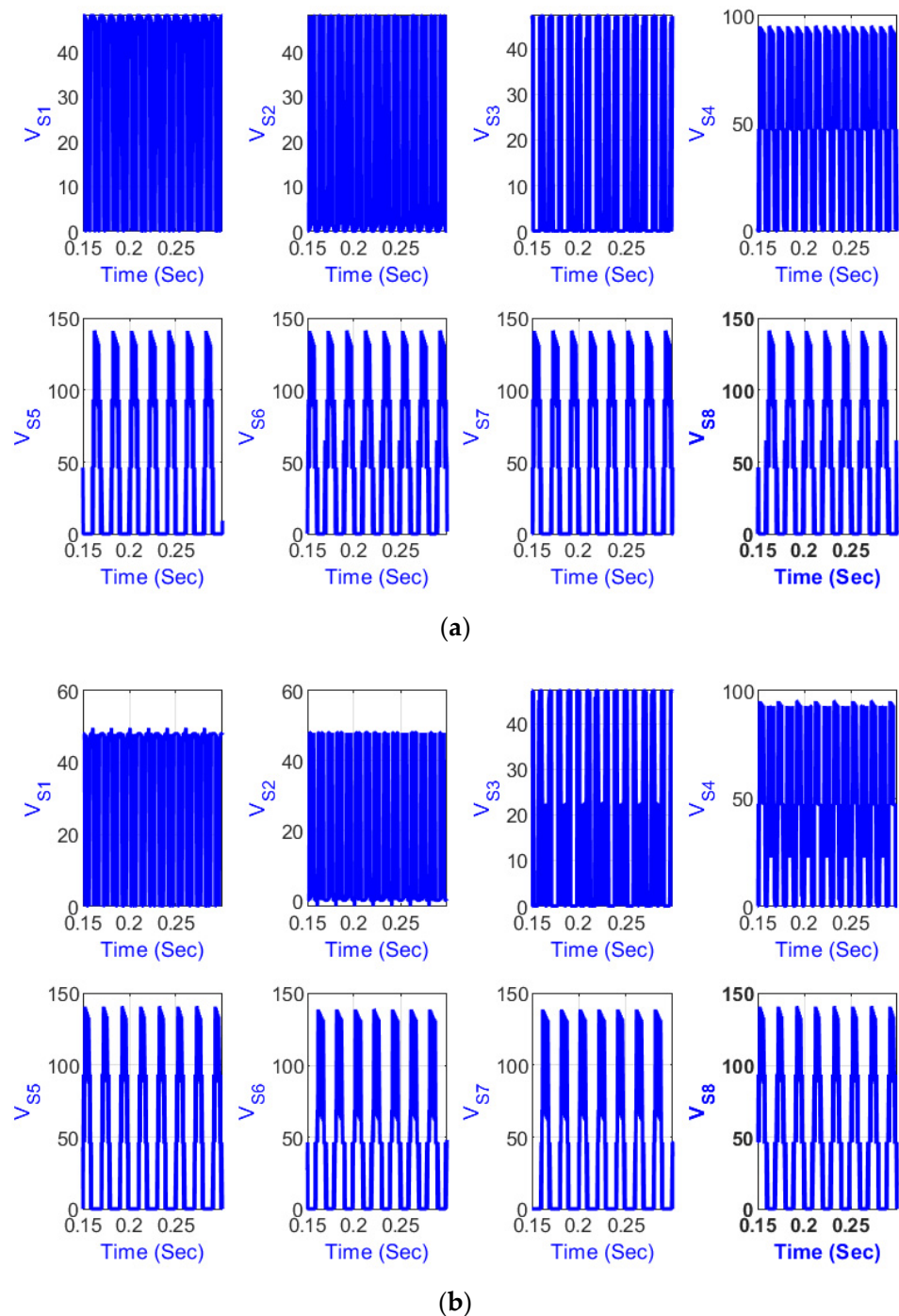


Figure 8. The voltage stress across switching: (a) PD-PWM and (b) MPC.

Figure 6a,b show the output voltage and load current waveforms for the PD-PWM and FS-MPC control methods, respectively. As can be observed, the output voltage has seven distinct levels: 0 , ± 48 V, ± 96 V, and ± 144 V, which are consistent with the theoretical values of 0 , $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$, respectively. On the other hand, the load current has a nearly sinusoidal waveform, which is consistent with the expected performance of the inverter, especially for inductive loads. This shows that the boosted output voltage is indeed achieved by the series connection of capacitors during certain operating states, with each capacitor regulated to the input voltage.

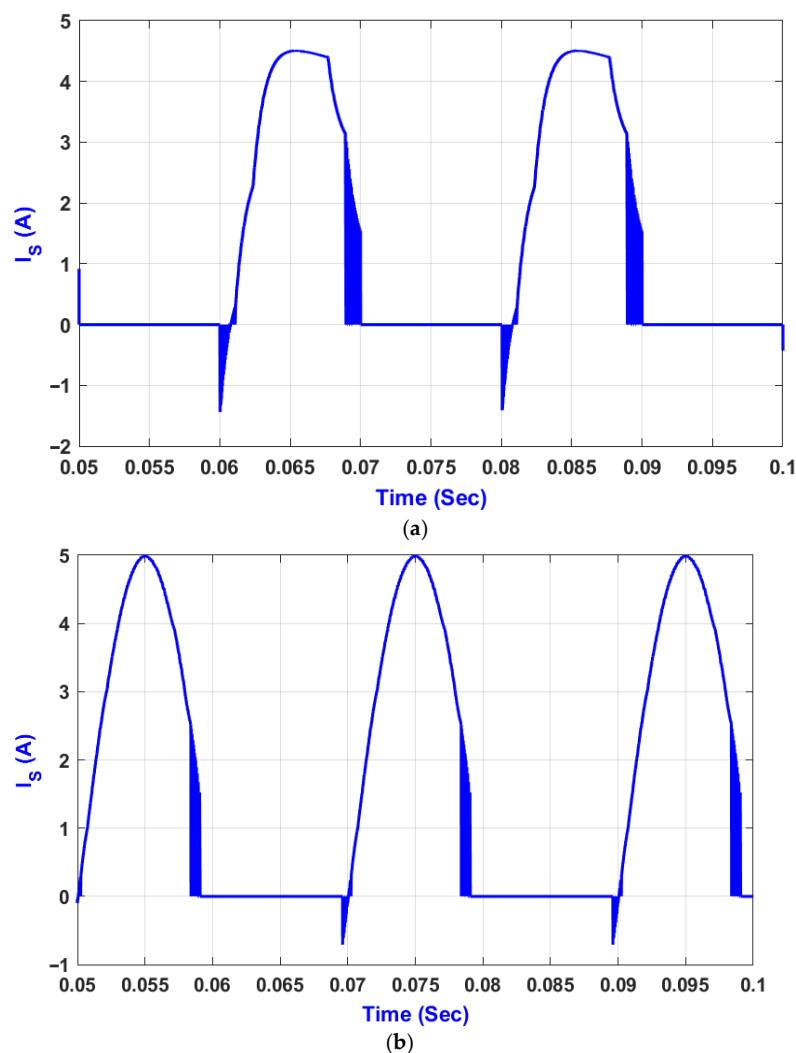


Figure 9. The current stress of switching: (a) PD-PWM and (b) MPC.

In addition, Figure 7 shows the performance of the finite-set model predictive current control strategy in terms of the inverter output current relative to the reference current during steady-state operation. As indicated in the figure, there is a close relationship between the reference current and the inverter output current. This indicates that the FS-MPC algorithm can select the optimal state at each sampling instant based on the model. In addition, there is no significant phase difference between the reference current and the inverter output current. This indicates accurate current regulation. In addition, there is no significant overshoot in the current waveforms. This indicates that there is a fast dynamic response of the FS-MPC algorithm, which is due to the fact that FS-MPC does not use any predefined modulation pattern and is able to evaluate all possible states. This is different from carrier-based PWM techniques. This result is in agreement with the fast dynamic response of the FS-MPC algorithm, as indicated in the simulation results.

Figure 8a,b present the voltage stress across the inverter switches under PD-PWM and FS-MPC control, respectively. It can be observed that switches S5–S8 experience the highest voltage stress, equal to three times the input DC voltage, whereas switches S1–S3 are subjected only to the input voltage, while S4 is subjected only to the input voltage. This bounded voltage stress characteristic validates the analytical stress analysis and demonstrates the suitability of the proposed inverter for practical implementation with appropriately rated devices.

Figure 9a,b show the current stress on the inverter switches for purely resistive and resistive-inductive loads, respectively. It is noticed that the current stress level varies with the active switching state and load type. All the current stress levels are within the expected range. This shows the inverter's ability to operate with different types of loads while maintaining the voltage level.

The comparison between PD-PWM and FS-MPC further indicates that, whereas the fixed switching frequency operation is ensured by PD-PWM, improved dynamic response is provided by FS-MPC through the selection of states.

6. Comparative Study

In this paper, a seven-level switched-capacitor boost inverter is proposed, which provides a balanced trade-off in terms of voltage gain, component count, and voltage stress. To compare different multilevel inverter topologies, two voltage stress indicators, the maximum blocking voltage (MBV) and the total standing voltage (TSV), are used. The MBV refers to the maximum voltage stress applied to any single power switch in the inverter, normalized with respect to the DC input voltage. It directly affects the voltage rating of the semiconductor devices used in the inverter. On the other hand, the TSV is defined as the sum of the maximum blocking voltage of all active switches in the inverter topology. It is used to measure the voltage stress applied to semiconductor devices, with a lower TSV indicating better voltage stress distribution.

As shown in Table 4, the proposed inverter configuration requires merely two capacitors, two diodes, and eight active switches. Therefore, a total of twelve components is required in this inverter configuration. By using a parallel connection for capacitor charging and a series connection for capacitor discharging, a triple-voltage gain is achieved by a single DC source. Moreover, the inherent voltage self-balancing capabilities of capacitors are maintained in this inverter configuration.

Table 4. Comparison of the proposed topology with related works.

Ref.	No. Capacitors	No. Diodes	No. Switches	No. Levels	Gain	Capacitor Charging Balance	Total Elements	MBV	TSV	THD %	η % Simulation
[29]	3	3	6	3	2	Inherent	12	2 Vdc	12V dc	2.20	97.90
[30]	2	-	10	5	2	Inherent	12	2 Vdc	14V dc	4.60	94.50
[31]	3	2	8	7	3	Inherent	13	>3 Vdc	27V dc	4.13	96.35
proposed	2	2	8	7	3	Inherent	12	3 Vdc	17V dc	3.35	98.45

As compared with the transformerless three-level inverter configuration proposed in [29], a significant improvement in the number of voltage levels and voltage gain has been achieved in the proposed inverter configuration with a similar number of components. In comparison with an extensible SC inverter configuration proposed in [30], a higher voltage gain with improved power quality has been achieved in the proposed inverter configuration with a similar number of components. In comparison with a seven-level triple boost inverter configuration proposed in [31], a similar voltage gain with a higher number of voltage levels has been achieved in the proposed inverter configuration with a lower number of components and a lower TSV.

7. Conclusions

This paper proposes a novel seven-level switched-capacitor boost inverter topology, which is suitable for renewable energy systems and microgrid applications. The proposed topology attains seven levels of output voltage with a voltage gain of approximately three using a single DC source and a reduced number of power switches and passive components. The operation of the proposed topology was explained in detail, along with the switching states of the proposed topology. The capacitor voltage balance method was also discussed,

and the self-balancing of capacitor voltages using the proposed topology was demonstrated using the simulation results.

To evaluate the performance of the proposed topology more accurately, non-ideal device characteristics were also considered, along with the efficiency of the proposed topology. The simulation results of the proposed topology with various inductive loads were obtained, which validate the proper operation of the proposed topology. The proposed topology attains seven levels of voltage with better output waveform quality using predictive current control. The reduced number of components in the proposed topology may reduce the cost of the proposed topology when compared with existing seven-level boost inverter topologies.

The grid connection of the proposed topology was also discussed, and the filtering of the output voltage of the proposed topology was considered suitable for grid-connected systems. Although the analytical modeling of the proposed topology was carried out in this study, the practical implementation of the proposed topology needs to be performed in the future to validate the efficiency of the proposed topology.

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References

1. Hussan, R.; Sarwar, A.; Siddique, M.D.; Mekhilef, S.; Ahmad, S.; Sharaf, M.; Zaindin, M.; Firdausi, M. A novel switched-capacitor multilevel inverter topology for energy storage and smart grid applications. *Electronics* **2020**, *9*, 1703. [\[CrossRef\]](#)
2. Rashid, A.K.; Al-Shamaa, N.K.; Wali, M.K. A New Five-Level Transformerless Boost Inverter for Renewable Energy Applications. In *Proceedings of the 2023 IEEE Jordan International Joint Conference on Electrical Engineering and Information Technology (JEEIT)*; Amman, Jordan, 22–24 May 2023; IEEE: New York, NY, USA, 2023; pp. 300–305.
3. Barath, J.N.; Soundarajan, A.; Stepenko, S.; Husev, O.; Vinnikov, D.; Nguyen, M.-K. Topological review of quasi-switched boost inverters. *Electronics* **2021**, *10*, 1485. [\[CrossRef\]](#)
4. Azizi, M.; Husev, O.; Vinnikov, D. Single-Stage Buck–Boost Inverters: A State-of-the-Art Survey. *Energies* **2022**, *15*, 1622. [\[CrossRef\]](#)
5. Taghvaie, A.; Adabi, J.; Rezanejad, M. A self-balanced step-up multilevel inverter based on switched-capacitor structure. *IEEE Trans. Power Electron.* **2017**, *33*, 199–209. [\[CrossRef\]](#)
6. Siddique, M.D.; Reddy, B.; Meraj, M.; Iqbal, A. A new high-level boost inverter topology with reduced device count. *Int. J. Circuit Theory Appl.* **2022**, *50*, 2777–2792. [\[CrossRef\]](#)
7. Siddique, M.D.; Alamri, B.; Salem, F.A.; Orabi, M.; Mekhilef, S.; Shah, N.M.; Sandeep, N.; Ali, J.S.M.; Iqbal, A.; Ahmed, M.; et al. A single DC source nine-level switched-capacitor boost inverter topology with reduced switch count. *IEEE Access* **2019**, *8*, 5840–5851. [\[CrossRef\]](#)
8. Palanisamy, K.; Mylsamy, K. A Single-Phase Single Source Seven Step Boost Inverter with Soft Charging of Switching Capacitors. *J. Control Eng. Appl. Inform.* **2025**, *27*, 120–130. [\[CrossRef\]](#)
9. Singh, A.K.; Raushan, R.; Mandal, R.K.; Ahmad, W. A New Single-Source Nine-Level Quadruple Boost Inverter (NQBI) for PV Application. *IEEE Access* **2022**, *10*, 36246–36253. [\[CrossRef\]](#)
10. Venkatesan, M.; Basha, S.G.; Ramkumar, A.; Manikandan, R.; Easwaran, M.; Khan, B. Switched Capacitor Based High Step-Up Multilevel Inverter with Self-Balancing Ability and Low Switching Stress. *Int. Trans. Electr. Energy Syst.* **2022**, *2022*, 4150590. [\[CrossRef\]](#)
11. Sathik, M.J.; Bhatnagar, K.; Sandeep, N.; Blaabjerg, F. An improved seven-level PUC inverter topology with voltage boosting. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 127–131. [\[CrossRef\]](#)
12. Liu, J.; Wu, J.; Zeng, J.; Guo, H. A novel nine-level inverter employing one voltage source and reduced components as a high-frequency AC power source. *IEEE Trans. Power Electron.* **2017**, *32*, 2939–2947. [\[CrossRef\]](#)
13. Ngo, B.B.; Nguyen, M.K.; Kim, J.H.; Zare, F. Single-phase multilevel inverter based on switched-capacitor structure. *IET Power Electron.* **2018**, *11*, 1–8. [\[CrossRef\]](#)

14. Sharifzadeh, M.; Al-Haddad, K. Packed E-Cell (PEC) converter topology operation and experimental validation. *IEEE Access* **2019**, *7*, 93049–93061. [\[CrossRef\]](#)
15. Deliri, S.; Varesi, K.; Siwakoti, Y.P.; Blaabjerg, F. Generalized diamond-type single DC-source switched-capacitor based multilevel inverter with step-up and natural voltage balancing capabilities. *IET Power Electron.* **2021**, *14*, 1208–1218. [\[CrossRef\]](#)
16. Hosseini, S.A.; Varesi, K. Hybrid switched-capacitor 9-level boost inverter. In Proceedings of the 2021 12th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC), Tabriz, Iran, 2–4 February 2021.
17. Lee, S.S. A single-phase, single-source, 7-level inverter with triple voltage boosting gain. *IEEE Access* **2018**, *6*, 30005–30011. [\[CrossRef\]](#)
18. Sun, X.; Wang, B.; Zhou, Y.; Wang, W.; Du, H.; Lu, Z. A single DC source cascaded seven-level inverter integrating switched-capacitor techniques. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7184–7194. [\[CrossRef\]](#)
19. Siddique, M.D.; Mekhilef, S.; Shah, N.M.; Ali, J.S.M.; Blaabjerg, F. A new switched capacitor 7L inverter with triple voltage gain and low voltage stress. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 1294–1298. [\[CrossRef\]](#)
20. Sathik, M.J.; Sandeep, N.; Almakhlles, D.; Blaabjerg, F. Improved K type seven-level switched capacitor inverter topology with Self-voltage balancing. *Int. J. Circuit Theory Appl.* **2020**, *48*, 1800–1819. [\[CrossRef\]](#)
21. Sandeep, N.; Sathik, M.J.; Yarangatti, U.R.; Krishnasamy, V.; Verma, A.K.; Pota, H.R. Common-ground-type five-level transformerless inverter topology with full DC-bus utilization. *IEEE Trans. Ind. Appl.* **2020**, *56*, 4071–4080.
22. Raman, S.R.; Cheng, K.W.E.; Ye, Y. Multi-input switched-capacitor multilevel inverter for high-frequency AC power distribution. *IEEE Trans. Power Electron.* **2018**, *33*, 5937–5948. [\[CrossRef\]](#)
23. Liu, J.; Cheng, K.W.E.; Ye, Y. A cascaded multilevel inverter based on switched-capacitor for high-frequency AC power distribution system. *IEEE Trans. Power Electron.* **2014**, *29*, 4219–4230. [\[CrossRef\]](#)
24. Samadaei, E.; Kaviani, M.; Bertilsson, K. A 13-level module (K-type) with two DC sources for multilevel inverters. *IEEE Trans. Ind. Electron.* **2019**, *66*, 5186–5196. [\[CrossRef\]](#)
25. Raman, S.R.; Fong, Y.C.; Yuanmao, Y.; Cheng, K.W.E. Family of multiport switched-capacitor multilevel inverters for high-frequency AC power distribution. *IEEE Trans. Power Electron.* **2018**, *34*, 4407–4422. [\[CrossRef\]](#)
26. Lee, S.S.; Lee, K.B.; Alsofyani, I.M.; Bak, Y.; Wong, J.F. Improved switched-capacitor integrated multilevel inverter with a DC source string. *IEEE Trans. Ind. Appl.* **2019**, *55*, 7368–7376. [\[CrossRef\]](#)
27. Wang, Y.; Yuan, Y.; Li, G.; Ye, Y.; Wang, K.; Liang, J. A T-type switched-capacitor multilevel inverter with low voltage stress and self-balancing. *IEEE Trans. Circuits Syst. I* **2021**, *68*, 2257–2270. [\[CrossRef\]](#)
28. Zhu, Q.; Xiao, H.; Yang, Q.; Yang, P.; Dong, Y.; Zhang, L. General and efficient simulation model for energy storage-embedded MMC with adaptability to multiple submodule topologies. *IEEE Trans. Ind. Appl.* **2025**, *62*, 37–48. [\[CrossRef\]](#)
29. Kurdkandi, N.V.; Marangalu, M.G.; Vala, S.S.; Mohseni, P.; Gharehkhoushan, A.R.Z.; Hosseini, S.H.; Sabahi, M. A new transformerless common grounded three-level grid-tied inverter with voltage boosting capability. *IEEE Trans. Energy Convers.* **2020**, *36*, 1896–1909. [\[CrossRef\]](#)
30. Wang, Y.; Ye, J.; Ku, R.; Wang, Y.; Liang, J. Novel extensible multilevel inverter based on switched-capacitor structure. *J. Power Electron.* **2022**, *22*, 1448–1460. [\[CrossRef\]](#)
31. Srivastava, A.; Seshadrinath, J. A single-phase seven-level triple boost inverter for grid-connected transformerless PV applications. *IEEE Trans. Ind. Electron.* **2022**, *70*, 9004–9015. [\[CrossRef\]](#)

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