

Article

A Reproducible Weak-Grid Benchmark with Switching-Averaged EMT Validation for Battery-Backed Grid-Forming Control in PV Microgrids

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Abstract

Controller comparisons for grid-forming battery inverters are often confounded by simultaneous changes in the plant model, saturation law, measurement filtering, and disturbance envelope. This paper addresses that problem through a reproducible weak-grid benchmark and a switching-averaged EMT validation layer for a battery-backed PV microgrid. Droop, virtual synchronous machine (VSM), and power-synchronization control (PSC) are compared under identical plant data, load disturbance, grid-strength reduction, voltage sag, current limit, and metric-extraction rules. The benchmark reveals a consistent trade-off: VSM provides the best frequency moderation, droop provides the fastest post-fault restoration and the lowest implementation burden, and PSC provides the most balanced compromise across recovery, stability, EMT, and implementation metrics. The averaged EMT layer preserves the low-order restoration ordering and sharpens the waveform trade-off during the fault window. Additional analyses quantify the converter-angle excursions during the sag, clarify the reduced lag tolerance of VSM as the grid becomes weaker, and test the local robustness of the reported ranking against representative tuning perturbations. The resulting message is benchmark-specific but operationally useful: controller selection should follow the dominant project objective—frequency quality, restorative efficiency, or balanced performance—before controller-specific switching EMT, hardware-in-the-loop, and plant-level studies are launched.

Keywords: grid-forming control; battery energy storage; photovoltaic microgrid; weak grid; current limiting; dynamic stability; power synchronization control; virtual synchronous machine; digital implementation



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1. Introduction

Battery-backed grid-forming converters are increasingly expected to stabilize photovoltaic microgrids that operate with limited synchronous support and weak feeder conditions [1–3]. Converter-dominated operation changes the design question from simple power injection to the coordinated delivery of voltage formation, frequency moderation, weak-grid stability, and recoverable current-limited support [4–6]. Recent reviews converge on the same practical issue: controller families are well classified, but matched engineering benchmarks that isolate the controller effect from the surrounding plant assumptions are still comparatively scarce [7–9].

Droop control remains attractive because of its compact structure and implementation transparency [10]. VSM control introduces an additional inertia-like state that can

improve frequency moderation and can be tuned in a language familiar to power-system engineers [11]. PSC, in turn, uses an active-power-driven phase law that is often regarded as a strong candidate for weak-grid operation because it preserves source-forming behavior without a separate inertia state [8,9,12]. The distinctive contribution of the present paper is not another broad taxonomy of these families, but a matched benchmark that keeps the plant, disturbance sequence, current-limit law, voltage loop, measurement-lag structure, and post-processing rules fixed while only the controller-family logic is changed.

Existing reviews already highlight why such a benchmark is needed. Khan et al. synthesize GFM operation and system-stability implications at the power-system level [7]. Qaisar and Fang emphasize weak-grid behavior, current limiting, and the practical trade-offs among GFM implementations [8]. Evald et al. identify implementation realism, validation depth, and low-inertia integration as defining next-step issues rather than settled questions [9]. Meanwhile, current-limiting and protection reviews show that the apparent controller ranking can change once saturation, lag, and post-fault recovery are treated seriously [13–15]. The gap addressed here, therefore, lies between broad review-level synthesis and project-specific EMT design: the paper develops a reproducible benchmark that yields a controller-selection message under matched assumptions and then tests whether that message survives an averaged EMT consistency layer.

The manuscript contributes five elements. First, it defines a reproducible weak-grid benchmark for a battery-backed PV microgrid exposed to a load increase, an SCR reduction, and a current-limited voltage sag. Second, it compares droop, VSM, and PSC under identical plant, filter, and disturbance assumptions. Third, it adds a switching-averaged EMT layer to determine whether waveform-level recovery preserves the low-order ranking. Fourth, it audits the validity of the low-order power-transfer approximation during the deep-sag interval and reports the actual converter-angle excursions reached by each controller. Fifth, it supplements the benchmark with explicit linearization notes, discrete-time implementation steps, and a local tuning-sensitivity analysis so that the benchmark can be reproduced and interpreted more rigorously.

The paper is organized as follows. Section 2 presents the benchmark configuration, controller models, tuning workflow, and EMT validation layer. Section 3 defines the quantitative indicators and the implementation-burden method. Section 4 reports the dynamic, fault-response, EMT, stability, and scorecard results. Section 5 converts the numerical outcomes into controller-selection guidance. Section 6 discusses extrapolation limits and future extensions. Section 7 concludes the paper. Appendix A consolidates the controller equations and the linearization used for the small-signal study, while Appendix B documents the discrete-time implementation sequence, parameter-selection logic, and local sensitivity analysis.

2. Benchmark Configuration and Controller Models

2.1. Single-Bus Benchmark Structure

Figure 1 shows the benchmark used throughout the paper. The studied system is a single-bus microgrid in which a battery energy storage system (BESS) operates as the grid-forming source, a photovoltaic unit is connected as a grid-following source, a local load is supplied at the same bus, and an upstream weak grid is represented by a Thevenin equivalent whose short-circuit ratio (SCR) is varied during the test sequence. This topology is intentionally compact. It concentrates the comparison on the controller family rather than on network-scale modeling details and still preserves the main mechanisms of interest: source formation, weak-grid coupling, fault current limiting, and post-fault recovery.

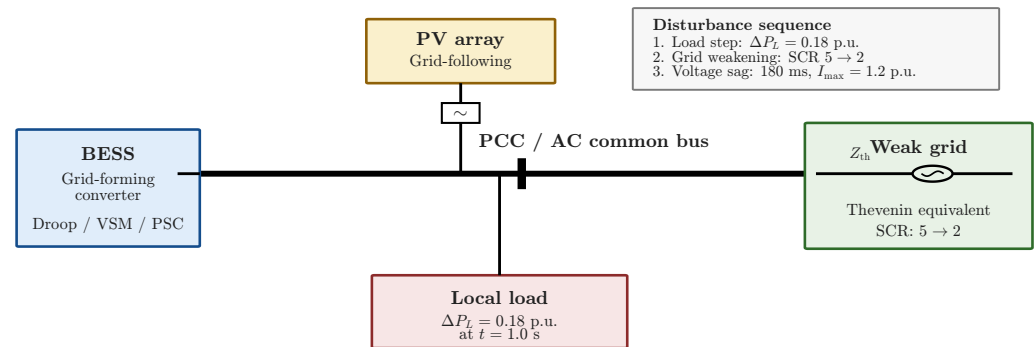


Figure 1. Single-bus benchmark used for the matched controller comparison.

The benchmark sequence contains three events. At $t = 1.0$ s, the local demand increases by 0.18 p.u. At $t = 2.2$ s, the external grid weakens and the post-disturbance SCR drops from 5 to 2. At $t = 3.4$ s, a voltage sag is applied for 180 ms, which forces current limiting at 1.2 p.u. These events were chosen because they collectively stress nominal regulation, weak-grid behavior, and fault recovery in one reproducible sequence. In the reduced benchmark, SCR = 5 represents a moderately stiff upstream grid, whereas SCR = 2 represents a clearly weak grid; for the same nominal voltage base, the associated Thevenin reactance in the reduced model therefore increases by a factor of 2.5 when the benchmark moves from the pre-disturbance to the post-disturbance condition. Table 1 summarizes the benchmark settings.

Table 1. Benchmark configuration and disturbance sequence.

Item	Value	Purpose
Nominal active-power reference P^*	0.58 p.u.	Defines the pre-disturbance operating point of the BESS inverter.
Reactive-power reference Q^*	0.00 p.u.	Keeps the voltage-loop comparison consistent across controllers.
Initial grid strength	SCR = 5.0	Represents a moderately stiff pre-disturbance grid.
Post-disturbance grid strength	SCR = 2.0	Forces a weak-grid operating condition after the network-strength change.
Load increase	0.18 p.u. at $t = 1.0$ s	Excites active-power sharing and frequency support.
Voltage sag	$V_g = 0.40$ p.u. from $t = 3.4$ s to 3.58 s	Forces current limiting and recovery behavior.
Current limit	1.20 p.u.	Represents converter hardware protection.
Power-estimation lag τ_p	40 ms (nominal)	Models filtered active-power estimation in the outer loop.

2.2. Low-Order Benchmark Model

The benchmark uses a low-order model so that each term has a direct engineering meaning. The network-facing active and reactive power are approximated as

$$P = K_P \text{SCR} E V_g \sin \delta + P_L, \quad (1)$$

$$Q = K_Q \text{SCR} (E - V_g \cos \delta), \quad (2)$$

where E is the internal voltage magnitude, δ is the converter angle relative to the upstream grid, V_g is the grid voltage during normal and faulted intervals, and P_L is the active-power demand of the local load. The model is normalized, so all variables are reported in per-unit form. Equations (1) and (2) are nonlinear sinusoidal transfer relations rather than small-angle linearisations; the simplification lies in the use of a lossless single-coupling equivalent, not in truncating the sine or cosine terms.

The converter current magnitude is computed as

$$I = \frac{\sqrt{P^2 + Q^2}}{\max(E, 0.55)}, \quad (3)$$

and current limiting is imposed by a uniform saturation law

$$(P_s, Q_s) = \begin{cases} (P, Q), & I \leq I_{\max}, \\ \frac{I_{\max}}{I}(P, Q), & I > I_{\max}, \end{cases} \quad (4)$$

with $I_{\max} = 1.2$ p.u. The measured powers used by the outer loops are filtered through first-order lags

$$\tau_p \dot{P}_m = P_s - P_m, \quad \tau_q \dot{Q}_m = Q_s - Q_m, \quad (5)$$

which capture the effective estimation delay introduced by signal conditioning and outer-loop processing.

All controllers share the same voltage loop

$$\tau_E \dot{E} = E^* + n_q(Q^* - Q_m) - E, \quad (6)$$

so the comparison remains focused on the active-power and angle-generation mechanisms.

2.3. Compared Control Families

Three control families are benchmarked.

Droop control.

The droop implementation uses a directly regulated phase state:

$$\dot{\delta} = k_d(P^* - P_m) - c_d \delta. \quad (7)$$

This family is compact, easy to tune, and computationally light.

Virtual synchronous machine control.

The VSM implementation introduces a frequency state ω :

$$\dot{\delta} = \omega, \quad (8)$$

$$M \dot{\omega} = P^* - P_m - D_{\text{eff}} \omega, \quad (9)$$

where M is the virtual inertia constant and D_{eff} is the benchmark damping term. In the benchmark, the same nominal VSM parameters are retained while the grid weakens, which is precisely why lag sensitivity becomes visible in the weak-grid envelope.

Power-synchronization control.

The PSC implementation also generates the phase state directly:

$$\dot{\delta} = k_{\text{psc}}(P^* - P_m) - c_{\text{psc}} \delta. \quad (10)$$

Although the reduced PSC law resembles the droop phase law algebraically, its interpretation is different: the controller is tuned and discussed as an active-power-driven synchronization mechanism rather than as a classical frequency-droop loop. The distinguishing choice in this benchmark is therefore the synchronization philosophy and gain placement, not the introduction of an additional inertia state. The adopted PSC form should be read as a reduced-order representative of the active-power-driven phase-synchronization family described in the PSC literature [8,9,12].

Table 2 lists the nominal benchmark parameters.

Table 2. Nominal controller and model parameters used in the benchmark.

Parameter	Value	Interpretation
K_P	1.35	Active-power coupling gain.
K_Q	1.10	Reactive-power coupling gain.
τ_E	0.08 s	Common voltage-loop time constant.
n_q	0.18	Common reactive-power droop coefficient.
k_d	2.8	Droop phase-synchronization gain.
c_d	0.04	Droop phase-restoring term.
M	0.20 s	VSM virtual inertia constant.
D_{eff}	0.75	VSM damping coefficient in the benchmark.
k_{psc}	2.2	PSC synchronization gain.
c_{psc}	0.02	PSC phase-restoring term.
$\tau_p = \tau_q$	0.04 s	Effective power-estimation lag in the outer loop.

Virtual-oscillator control (VOC) is intentionally excluded from the matched benchmark. The present testbed fixes an explicit filtered power-measurement path, a shared voltage-magnitude loop, and a phase-state comparison structure. VOC generates angle and voltage through nonlinear oscillator states, so including it would require a different state definition and parameterization rather than a fourth point in the same benchmark envelope [8,16].

2.4. Parameter Selection, Numerical Integration, and Fair-Comparison Protocol

A benchmark comparison is only useful if the reader can see what was held constant and what was allowed to change. In this study, the plant structure, disturbance sequence, voltage loop, measurement-lag structure, saturation law, and metric extraction rules are fixed across all compared cases. Only the active-power and angle-generation law is changed from droop to VSM or PSC.

The benchmark parameters were obtained through a sequential tuning workflow rather than global optimization. First, the common plant parameters and the shared voltage-loop parameters K_P , K_Q , τ_E , and n_q were selected so that the pre-disturbance operating point remained close to 1.0 p.u. voltage at SCR = 5. Second, the droop and PSC active-power gains were adjusted to achieve stable nominal operation, monotonic recovery after the load event, and comparable voltage-loop aggressiveness. Third, the VSM inertia and damping parameters were selected to provide visibly stronger frequency moderation without changing the plant or protection envelope. The resulting benchmark therefore compares representative tuned implementations rather than controller-specific optimum cases.

The low-order model is solved with a fixed-step fourth-order Runge–Kutta scheme using a 2.5 ms step. This step matches the exported benchmark traces and remains substantially smaller than the smallest outer-loop time constant used in the study. Table 3 summarizes the comparison protocol.

Table 3. Fair-comparison protocol used in the benchmark.

Comparison Aspect	Fixed Across All Cases	Allowed to Change	Purpose
Plant and network model	Same BESS–PV–load structure, same weak-grid equivalent, same K_P , K_Q , τ_E , and n_q	None	Isolates the controller-family effect from plant redesign.
Disturbance sequence	Same load increase, same SCR reduction, same sag duration and depth	None	Applies an identical stress envelope to each controller.
Protection and saturation	Same $I_{\max}$ and same current-limiting law	None	Keeps the fault-response comparison hardware-consistent.
Measurements and filtering	Same P_m and Q_m structure and same nominal $\tau_p = \tau_q$	None	Exposes all families to the same estimation-lag mechanism.
Phase-generation law	Common source-forming objective	Droop, VSM, or PSC state equation	Creates the actual family-to-family contrast.
Tuning basis	Stable nominal operation at SCR = 5 and comparable voltage-loop aggressiveness	Family specific active-power and angle gains	Avoids over-optimizing one family for a single metric.
Metric extraction	Same settling and recovery thresholds	None	Preserves objective post-processing across controllers.
Averaged EMT layer	Same 50 μ s step, same interface-inductor model, same current clamp, same RMS estimator	Only the controller trajectories injected into the EMT layer	Confirms that waveform-level ranking remains tied to the compared family rather than to a different validation setup.
Interpretive scope	Screening benchmark for matched assumptions	None	Prevents the results from being misread as universal rankings.

2.5. Averaged EMT Validation Layer

Low-order benchmarks are attractive because they keep matched comparisons transparent, but they still leave an important practical question unanswered: does the observed controller ordering survive once waveform-level transients are resolved at an electromagnetic-transient time scale? To answer that question without turning the paper into a different tuning contest, the present study adds a balanced three-phase, switching-averaged EMT validation layer around the fault window.

For each controller, the internal phase voltage used by the EMT layer is reconstructed as

$$v_a^{\text{inv}}(t) = \sqrt{2}E(t) \sin(\omega_0 t + \delta_0 + \Delta\delta(t)), \quad \Delta\delta(t) = \int_0^t \omega(\tau) \omega_0 d\tau, \quad (11)$$

with analogous expressions for phases b and c . The upstream grid voltage is represented by the same balanced sag profile used in the low-order benchmark, and the interface current is computed from a common phase-inductor model,

$$L_f(t) \frac{di_a}{dt} = v_a^{\text{inv}}(t) - v_a^g(t) - R_f(t)i_a(t), \quad (12)$$

where $v_a^s(t) = \sqrt{2}V_g(t) \sin(\omega_0 t)$, $X_f(t) = X_0 5/\text{SCR}(t)$, $L_f(t) = X_f(t)/\omega_0$, $R_f(t) = 0.12X_f(t)$, and $X_0 = 0.32$ p.u.

The EMT layer does not re-solve the outer voltage loop. Instead, the low-order benchmark first produces the controller trajectories and then injects them into the EMT layer through time interpolation when Equation (11) is evaluated. The voltage loop in Equation (6) is therefore active only in the benchmark layer; the EMT layer uses the resulting voltage trajectory as a prescribed input so that the validation remains a consistency check rather than a second tuning problem. To remain consistent with the shared hardware envelope, phase-current limiting in the EMT layer is implemented as a hard magnitude saturation with no smoothing function.

Cycle-RMS envelopes are computed over one nominal fundamental period and are used to extract three waveform-level indicators: the peak one-cycle RMS current during and just after the fault, the minimum fault-window RMS voltage, and the recovery time needed for terminal RMS voltage to exceed 0.95 p.u. after sag clearance. A fourth indicator, the maximum $|di_a/dt|$ in the fault window, is included to expose how aggressively each controller drives the interface current once the voltage sag is applied and removed. This EMT layer should therefore be interpreted as a consistency validation of the matched benchmark, not as a replacement for project-specific switching or HIL studies.

3. Performance Indicators and Implementation-Burden Method

The benchmark is evaluated with indicators that are directly observable in the time traces. Table 4 summarizes the metrics used in the paper.

Table 4. Performance indicators used in the benchmark comparison.

Indicator	Definition	Engineering Meaning
Frequency excursion J_f	$\max \omega(t) $ during the load-step window	Measures how strongly the controller departs from the nominal frequency trajectory.
RoCoF proxy J_r	$\max d\omega/dt $ over the full sequence	Quantifies transient aggressiveness of the active-power loop.
Load-step settling time T_s	First, time after $t = 1$ s for which $ P - P_{ss} < 0.02$ p.u. and $ \omega < 0.02$ p.u.	Measures restorative speed after the active-power disturbance.
Fault recovery time T_f	First, time after sag clearance for which $ E - 1 < 0.02$ p.u. and $ \omega < 0.02$ p.u.	Measures post-fault restoration quality.
Fault active-power retention η_P	Mean fault-window power divided by pre-fault power	Quantifies how much active-power service remains during current limiting.
Support-energy excursion J_E	$\int P(t) - P^* dt$	Measures the battery energy swing required by the controller.
Dominant damping ratio ζ	Computed from the linearized dominant eigenvalue	Captures small-signal damping of the low-order benchmark model.
Acceptable lag $\tau_{p,\max}$	Largest lag that still satisfies the benchmark recovery criterion	Measures sensitivity to filtered active-power estimation.
EMT voltage recovery $T_{V,\text{EMT}}$	First, time after sag clearance for which the one-cycle RMS terminal voltage exceeds 0.95 p.u.	Confirms post-fault restoration ordering in the switching-averaged EMT layer.
EMT current slew $S_{I,\text{EMT}}$	$\max di_a/dt $ during fault entry and clearing	Indicates waveform aggressiveness and interface-stress severity.

To condense the evidence without imposing subjective weights, the paper also reports a metric-wise ordinal scorecard. For each metric m and controller c , a benchmark score $r_{c,m} \in \{1, 2, 3\}$ is assigned according to the controller position within the compared set, where 3 denotes the best value for that metric, 2 the middle value, and 1 the weakest value. For lower-is-better metrics, the ranking is computed in ascending order; for higher-is-better metrics, it is computed in descending order. The scorecard therefore preserves metric diversity and makes the final take-away message explicit, while avoiding a single weighted index that could hide the underlying trade-offs.

For the stability-related analysis, the benchmark equations are linearized around the pre-fault operating point at a fixed post-disturbance SCR. The dominant damping ratio is obtained from the eigenvalue with the largest real part. The acceptable lag is defined through the time-domain sequence: the controller passes if the post-fault trajectory returns to $|E - 1| < 0.03$ p.u. and $|\omega| < 0.03$ p.u. within 1.6 s after sag clearance. Appendix A gives the state vectors, the relevant Jacobian entries, and the reduced characteristic polynomials used to interpret the lag-tolerance results.

Implementation burden is estimated for the outer loop only. The counts are reported per control sample and refer only to controller-specific outer-loop calculations. Common PWM, modulation, diagnostics, and hardware protection functions are intentionally excluded. The benchmark also treats the trigonometric evaluations needed for three-phase waveform synthesis as common overhead, so they are not used to differentiate the compared families. The resulting burden metric is therefore a relative integration-overhead indicator rather than a claim that any controller exceeds the capability of a modern DSP.

4. Benchmark Results

4.1. Response to the Load Increase and SCR Reduction

Figure 2 shows the full benchmark sequence. VSM produces the smallest frequency excursion after the load increase, which is consistent with its additional inertia state. Droop and PSC respond more sharply, but they return to the new operating point much faster. Once the SCR drops from 5 to 2 at $t = 2.2$ s, the distinction becomes clearer: the VSM trajectory remains smoother but also more weakly damped in the benchmark, whereas droop and PSC regain the steady regime more quickly.

Table 5 quantifies these observations. The benchmark frequency excursion is 0.295 p.u. for droop, 0.113 p.u. for VSM, and 0.246 p.u. for PSC. The load-step settling times are 0.282 s, 1.098 s, and 0.193 s, respectively. These data make the first benchmark trade-off explicit: VSM moderates frequency most effectively, while droop and PSC restore the operating point far faster after the active-power disturbance.

Table 5. Benchmark results for the three compared control families.

Controller	J_f (p.u.)	J_r (p.u./s)	T_s (s)	T_f (s)	η_P (—)	J_E (p.u. s)
Droop	0.295	23.802	0.282	0.475	0.577	0.142
VSM	0.113	1.088	1.098	1.855	0.495	0.336
PSC	0.246	17.069	0.193	0.565	0.566	0.151

4.2. Fault Response, Current Limiting, and Angle-Validity Audit

Figure 3 zooms into the voltage-sag interval. All three controllers hit the 1.2 p.u. current limit, as intended by the benchmark. The key difference lies in the retained active power and the post-fault restoration path. Droop and PSC retain 0.577 and 0.566 of the pre-fault active power, while VSM retains 0.495. The VSM response also carries the largest

support-energy excursion, which indicates a higher battery swing requirement for the same disturbance sequence.

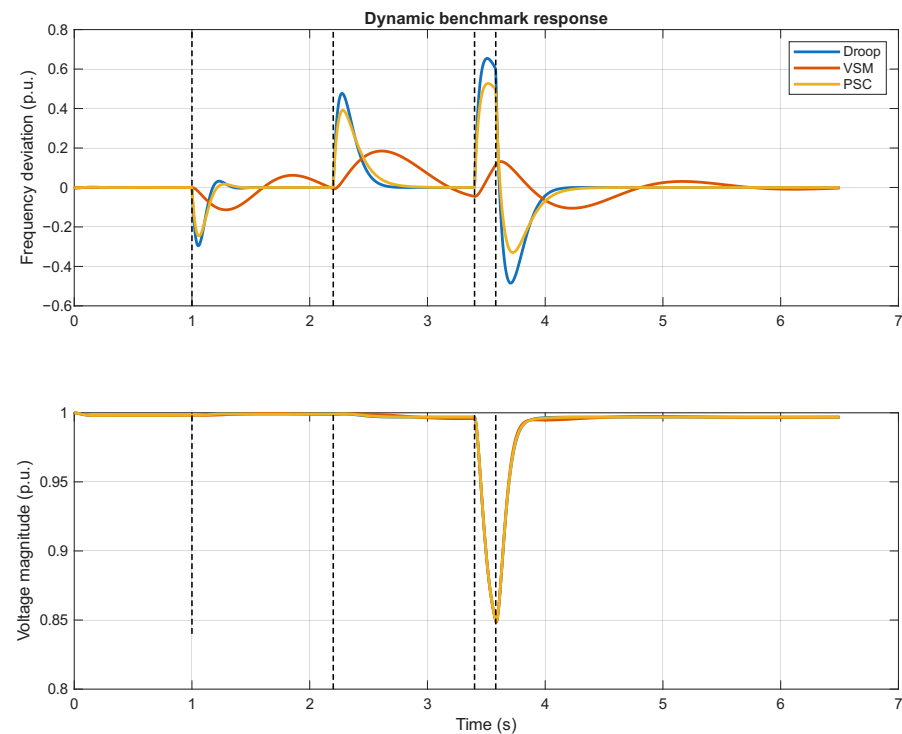


Figure 2. Dynamic benchmark response for frequency deviation and voltage magnitude.

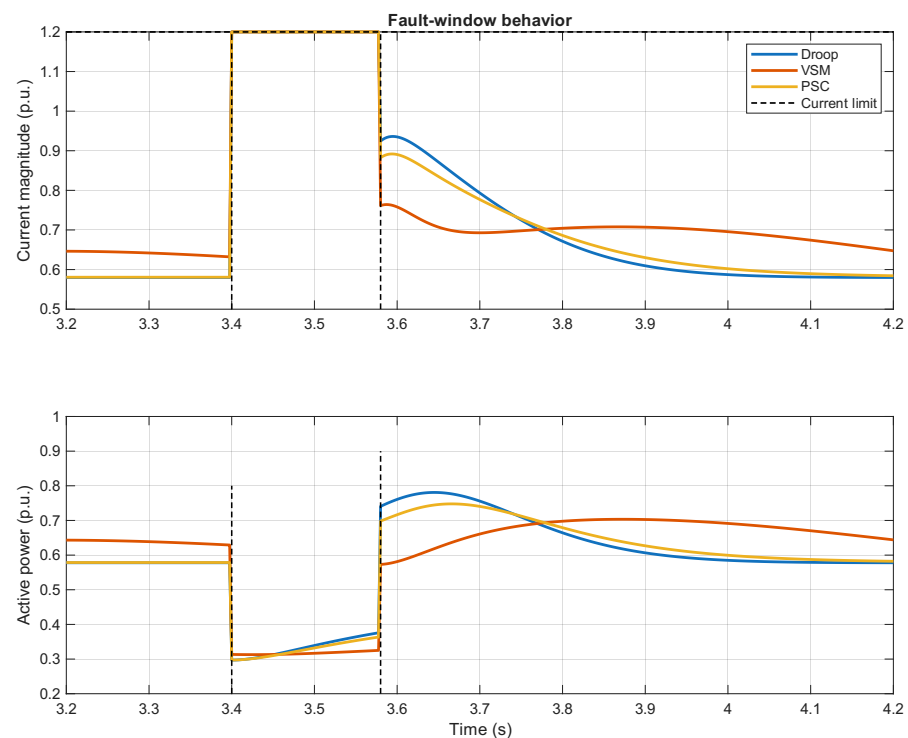


Figure 3. Fault-window current and active-power response under the common sag event.

The post-fault recovery times reinforce the same conclusion. Droop and PSC recover in 0.475 s and 0.565 s, whereas VSM needs 1.855 s. In a battery-backed microgrid, that difference matters because current-limited support must be converted into a recoverable service rather than a long energy excursion.

Table 6 addresses the reviewer concern about low-order validity during the deep sag. The benchmark trajectories keep the absolute converter angle below 14.1 degrees for all three controllers, and the maximum a posteriori relative error that would arise if one linearized the sine term remains below 1.1 percent. The model therefore remains within a moderate-angle regime even during the faulted interval. More importantly, the benchmark equations themselves retain the nonlinear sine and cosine terms, so the reported sag-window results are not obtained from a truncated small-angle model.

Table 6. Sag-window angle audit for the low-order benchmark trajectories.

Controller	Pre-Sag $ \delta $ (Deg)	Sag-Window $ \delta _{\max}$ (Deg)	Incremental Sag Excursion (Deg)	Max. Relative Error of $\sin \delta \approx \delta$
Droop	8.50	14.07	5.56	1.00%
VSM	9.40	9.79	0.39	0.49%
PSC	8.52	12.99	4.48	0.85%

4.3. Averaged EMT Validation of the Fault Window

The switching-averaged EMT layer is designed as a ranking-consistency check rather than as a second tuning contest. Figure 4 resolves the phase-*a* current at fault entry and the smoothed one-cycle RMS current and voltage envelopes across the fault interval. Table 7 summarizes the extracted EMT indicators.

Three observations are technically important. First, the EMT layer preserves the low-order ordering of post-fault restoration: droop restores terminal RMS voltage above 0.95 p.u. in 46.5 ms, PSC in 57.3 ms, and VSM in 71.9 ms. Second, the minimum fault-window RMS voltage is also controller-dependent, with PSC reaching 0.842 p.u., droop 0.826 p.u., and VSM 0.811 p.u.. Third, the waveform layer exposes a trade-off that is only implicit in the low-order envelopes: droop and PSC recover faster, but they do so with higher post-fault RMS current peaks and higher current-slew rates. VSM is slower, yet it also produces the smoothest current trajectory, with the smallest maximum $|di_a/dt|$ in the EMT window.

Table 7. Waveform-level indicators extracted from the switching-averaged EMT validation layer.

Controller	$I_{\text{rms,pk}}^{\text{fault}}$ (p.u.)	$I_{\text{rms,pk}}^{\text{post}}$ (p.u.)	$V_{\text{rms,min}}^{\text{fault}}$ (p.u.)	$T_{V,\text{EMT}}$ (ms)	$S_{I,\text{EMT}}$ (p.u./s)
Droop	0.935	1.134	0.826	46.5	826.8
VSM	0.949	1.022	0.811	71.9	582.7
PSC	0.931	1.100	0.842	57.3	652.0

4.4. Stability-Oriented Comparison and Admissible Operating Region

Figure 5 summarizes the stability-oriented part of the study. The left panel reports the dominant damping ratio of the linearized benchmark model. Under the matched tuning used here, PSC exhibits the strongest damping across the explored SCR range, droop remains second, and VSM is consistently the most weak-grid-sensitive family. The difference is already visible at SCR = 2.0, where the dominant damping ratio is 0.919 for droop, 0.321 for VSM, and 1.000 for PSC.

The right panel converts the lag-tolerance test into an admissible operating envelope in the SCR–lag plane. This representation is more informative than a single lag value because it shows how much timing margin remains available after the grid has weakened. In the present benchmark, droop and PSC remain acceptable up to 100 ms over the explored SCR range, whereas VSM contracts to a markedly smaller envelope and is acceptable up to 30 ms at SCR = 2.0. The reduced VSM lag tolerance follows directly from the benchmark structure.

As SCR falls, the synchronizing coefficient decreases, so the same filtered-power delay represents a larger phase lag relative to restoring torque. Droop and PSC feed that delayed power estimate into a first-order phase law, whereas VSM feeds it into an additional inertial state before phase is recovered. The extra dynamic order therefore loses damping margin sooner when the grid becomes weaker. Appendix A provides the reduced characteristic polynomials that make this mechanism explicit.

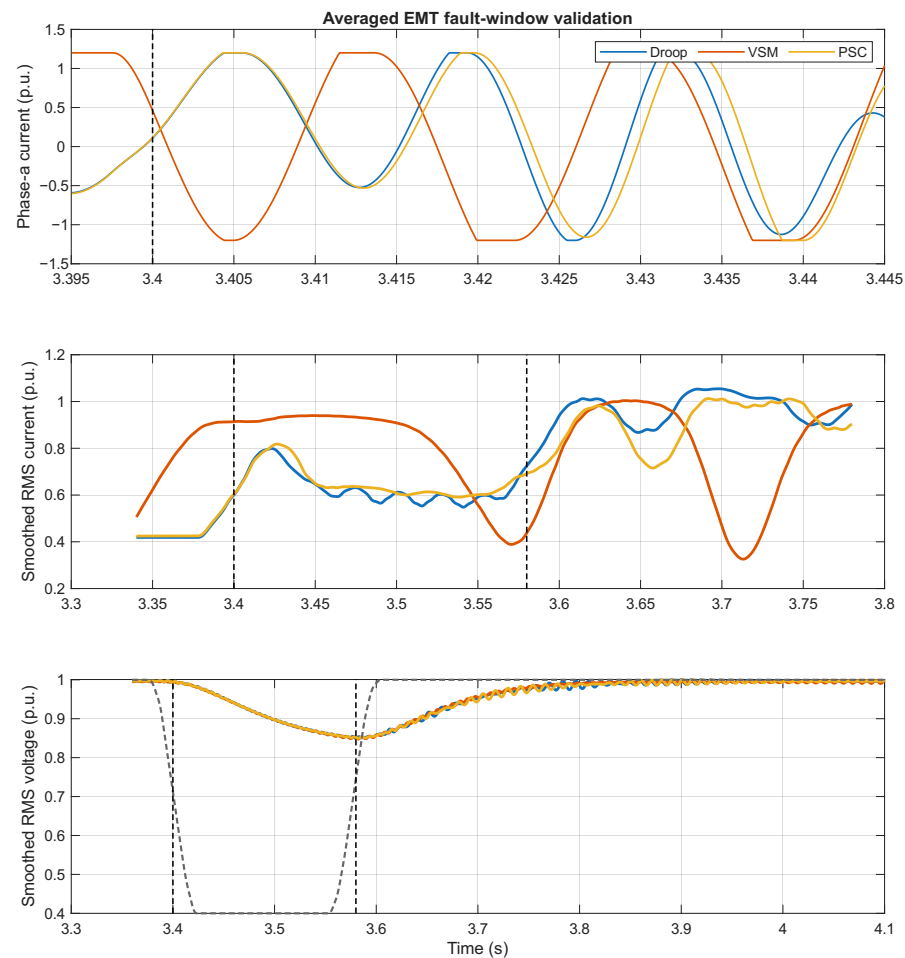


Figure 4. Averaged EMT validation around the fault window.

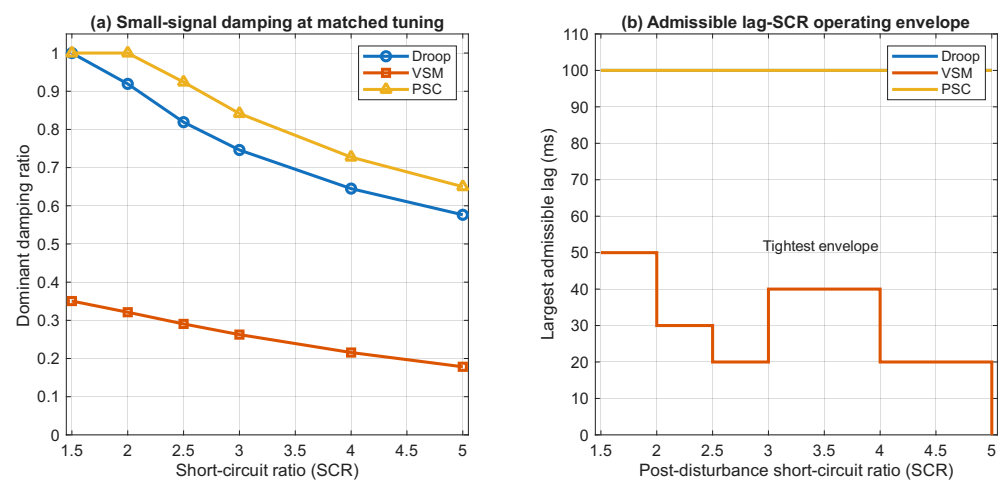


Figure 5. Stability-oriented benchmark results for damping ratio and admissible lag envelope.

4.5. Implementation Burden and Ordinal Scorecard

The outer-loop implementation audit is shown in Figure 6 and Table 8. Droop uses the smallest arithmetic and memory footprint, PSC is slightly heavier, and VSM is clearly the most demanding because it carries the additional frequency state and more outer-loop arithmetic. This ranking is not presented as a feasibility limit on modern DSPs; it is included because practical controller integration in microgrids also depends on code margin, timing robustness, and commissioning simplicity, especially when communication, diagnostics, and protection functions are added around the core control law.

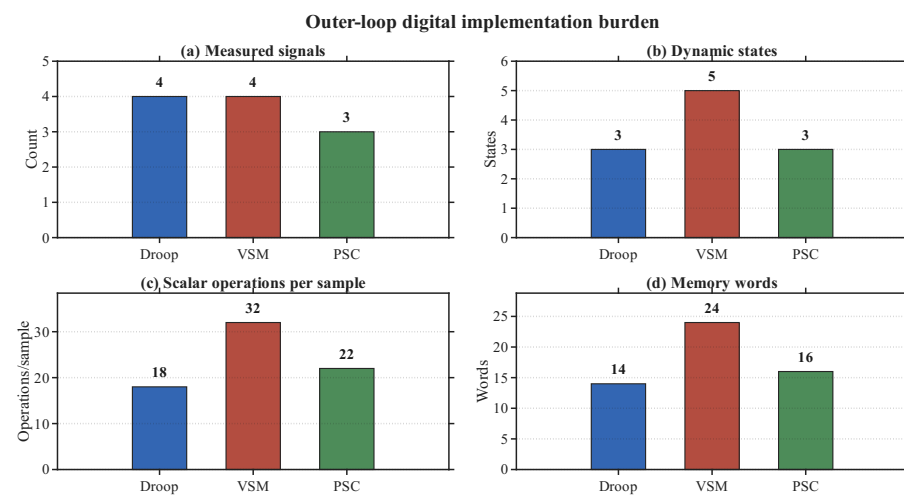


Figure 6. Relative outer-loop implementation burden for the three benchmarked controllers.

Table 8. Estimated outer-loop implementation burden.

Controller	Measured Signals	Dynamic States	Scalar Ops/Sample	Memory Words
Droop	4	3	18	14
VSM	4	5	32	24
PSC	3	3	22	16

The raw metrics are condensed in Figure 7. Droop ranks first in fault recovery, retained fault-window power, energy swing, EMT voltage recovery, and implementation burden, but it ranks third in frequency quality and current-slew smoothness. VSM ranks first in frequency quality and current-slew smoothness, but it ranks third in restoration, lag tolerance, and implementation burden. PSC rarely dominates a single category as strongly as droop or VSM, yet it remains in the best or middle position across all groups. That metric-by-metric balance is the key reason why PSC emerges as the most even compromise in the present benchmark rather than the absolute winner of every individual metric.

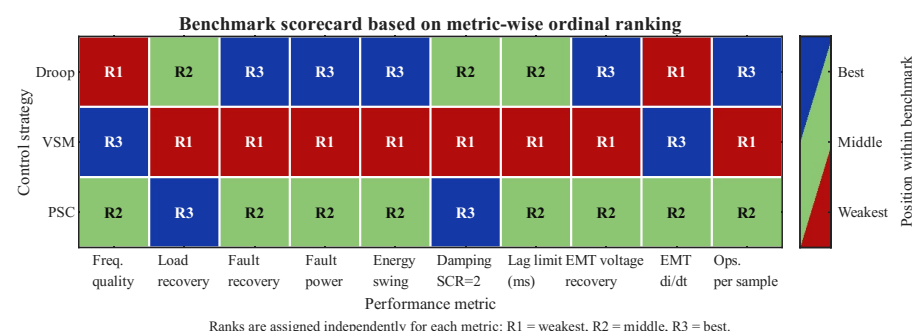


Figure 7. Ordinal benchmark scorecard derived from the reported metrics.

5. Discussion and Design Implications

The benchmark supports a structured controller-selection message rather than a universal ranking.

For frequency-sensitive operation, VSM remains attractive because it produces the smallest frequency excursion and the lowest RoCoF proxy. That advantage is technically meaningful for islanded or low-inertia operation in which frequency quality dominates the design brief. The same benchmark, however, shows that this benefit is coupled to slower recovery, lower lag tolerance, and higher outer-loop burden. A VSM choice is therefore most defensible when the project can enforce tighter timing discipline and can accommodate longer post-fault restoration.

For restoration-centric microgrids, droop provides the strongest evidence. It achieves the shortest post-fault recovery time, the largest retained active power during the sag, the smallest support-energy excursion, and the lightest implementation burden. The EMT layer confirms that the same controller also restores RMS voltage fastest. The trade-off is sharper current forcing during the fault window, which means that droop is best suited to projects that prioritize rapid restorative service and implementation simplicity over waveform smoothness.

PSC occupies the most balanced region of the benchmark. It achieves the fastest load-step settling time, retains short post-fault recovery, preserves the full admissible lag envelope observed for droop, and avoids the high current-slew severity of droop. In practical terms, PSC is the most robust default candidate when the project objective is balanced performance rather than optimization of a single metric.

The benchmark should also be interpreted in relation to broader microgrid topologies. In a multi-inverter microgrid, line-impedance coupling adds collective modes that are absent from the present single-bus study. The restorative ordering observed here is expected to remain informative when one BESS inverter dominates source formation, but the absolute lag margins and damping ratios—especially for VSM—can change once mutual support or inter-unit oscillatory modes appear [17,18]. In addition, distributed primary–secondary coordination introduces communication and restoration dynamics that lie outside the present single-bus benchmark [19]. The present scorecard should therefore be used as a screening result for controller pre-selection, not as a replacement for network-coupled eigenanalysis in multi-converter installations.

The benchmark also suggests a practical validation workflow. A matched low-order study is sufficient to screen controller families and expose their main trade-offs. A switching-averaged EMT layer then checks whether the same ranking remains coherent once waveform-level recovery and current slew are resolved. Only after that second step should controller-specific switching EMT, HIL, or plant-level studies be launched. This staged process is one of the main scientific contributions of the paper: it converts a controller-family comparison into a reproducible validation sequence that engineers can actually reuse.

Adaptive damping work remains relevant to this interpretation. Benchmark-specific controller rankings can change once family-specific enhancement layers are added. Examples include model-matching and energy-shaping extensions, virtual-impedance-aware angle droop, and asymmetrical virtual-impedance stabilization [20–22]. This is precisely why the present paper reports matched baseline families before considering augmented variants. In that sense, the adaptive damping strategy of Khan et al. is best interpreted as a next-step controller enhancement rather than as evidence that the baseline family trade-offs disappear [23].

Table 9 summarizes the resulting application-oriented controller-selection guidance.

Table 9. Application-oriented controller selection matrix derived from the benchmark evidence.

Primary Project Priority	Preferred Controller in the Benchmark	Reason Based on Quantitative Evidence
Smallest frequency excursion and lowest RoCoF proxy	VSM	VSM yields the lowest J_f and J_r , which makes it the strongest frequency-moderating option in the studied benchmark.
Fastest restoration after a load increase	PSC	PSC achieves the shortest load-step settling time ($T_s = 0.193$ s).
Fastest post-fault recovery	Droop	Droop achieves the shortest fault-recovery time ($T_f = 0.475$ s).
Highest retained active power during the sag	Droop	Droop yields the largest η_P among the compared cases.
Smallest battery support-energy excursion	Droop	Droop gives the smallest J_E , which reduces temporary battery energy swing.
Largest admissible lag margin at SCR = 2	Droop or PSC	Both controllers remain acceptable up to 100 ms in the studied benchmark.
Lowest outer-loop implementation burden	Droop	Droop requires the fewest arithmetic operations and memory words.
Best balanced compromise of restoration, stability, and implementation	PSC	PSC remains in the best or middle position across all benchmark categories without the weak extremes seen in the other families.

6. Limitations and Applicability

The benchmark is intentionally compact and should be interpreted within that scope. First, its main comparison layer remains a low-order outer-loop model. That layer does not represent the grid-following PV unit's detailed PLL/filter dynamics, converter-impedance interactions, switching harmonics, inner current-control bandwidths, or filter resonances [24–26]; it also omits sequence components and communication-assisted plant control. Second, the added EMT layer is balanced and switching-averaged. It improves waveform-level observability, but it is not a full switching model, and it does not resolve PWM harmonics, device-level thermal stress, unbalanced faults, or relay algorithm internals [27]. Third, the compared controllers are tuned to provide stable nominal operation and comparable voltage-loop aggressiveness, but they are not globally re-optimized for every metric or every SCR value. The results should therefore be read as a matched-design benchmark rather than a theoretical best-case contest.

Moreover, the benchmark assumes a voltage-source GFM interface and does not cover current-source GFM topologies, whose inherent current-limiting behavior creates a different comparison envelope [28,29].

Appendix B shows that moderate parameter perturbations shift the numerical values of the metrics but do not erase the headline benchmark trade-offs: VSM remains the strongest frequency moderator, droop remains the lightest and fastest post-fault restorer, and PSC remains the most balanced option. At the same time, the study also shows that middle positions can move under retuning, so the scorecard should not be overinterpreted as a universal ranking. The voltage-sag event is implemented as a simplified balanced sag with a common current-limit ceiling. It is sufficient for controller comparison and EMT consistency checking, but it does not replace asymmetrical-fault EMT studies, relay studies, or detailed protection validation. Finally, the benchmark does not certify grid-code compliance [30]. It provides a reproducible screening framework that now includes a switching-averaged EMT layer, but it remains a precursor to utility-specific acceptance testing.

7. Conclusions

This paper presented a reproducible weak-grid benchmark for comparing droop, VSM, and PSC grid-forming control in a battery-backed PV microgrid subjected to a load increase, a reduction in grid strength, and a current-limited voltage sag. The benchmark was designed to isolate the controller-family effect by holding the plant, disturbance sequence, measurement-lag structure, saturation law, and metric extraction rules constant. A switching-averaged EMT layer was then added around the fault window to test whether the low-order ranking remains consistent once waveform-level behavior is resolved.

This manuscript supports six concrete conclusions. First, VSM provides the best frequency moderation in the studied benchmark, but it also exhibits the slowest restoration, the tightest admissible lag envelope, and the highest implementation burden. Second, droop combines the fastest post-fault restoration, the largest retained active power during the sag, the smallest support-energy excursion, and the lowest outer-loop computational footprint. Third, PSC provides the fastest load-step restoration and the most balanced overall position across dynamic, stability-related, EMT, and implementation criteria. Fourth, the low-order benchmark remains technically credible during the deep sag because the governing equations retain their nonlinear sinusoidal form and the observed angle excursions remain moderate, with a worst-case a posteriori small-angle error below 1.1 percent. Fifth, the reduced lag tolerance of VSM under weak-grid conditions is structurally linked to the combination of lower synchronizing stiffness and the additional inertial state through which delayed power information must pass. Sixth, moderate retuning changes metric values but does not remove the main benchmark trade-off between frequency quality, restorative efficiency, and balanced performance.

The practical implication is concise. In the studied weak-grid PV–battery benchmark, VSM is the preferred family when frequency quality dominates, droop is preferred when restorative efficiency and implementation simplicity dominate, and PSC is preferred when the design objective is balanced performance. The scientific value of the paper lies in converting that qualitative design intuition into a transparent benchmark sequence: matched low-order comparison, lag-envelope analysis, averaged EMT consistency check, and application-oriented scorecard. The benchmark package is intended to serve as a reproducible first screening layer before controller-specific switching EMT, HIL, and plant-level validation are undertaken.

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Abbreviations

BESS	Battery energy storage system
DER	Distributed energy resource
EMT	Electromagnetic transients
GFL	Grid-following

GFM	Grid-forming
HIL	Hardware-in-the-loop
PSC	Power-synchronization control
PV	Photovoltaic
RMS	Root mean square
RoCoF	Rate of change of frequency
SCR	Short-circuit ratio
VSM	Virtual synchronous machine
VOC	Virtual-oscillator control
E	Internal voltage magnitude of the grid-forming inverter.
V_g	Grid voltage magnitude imposed by the upstream Thevenin source.
δ	Converter angle relative to the upstream grid.
ω	Converter frequency-deviation state.
P^*, Q^*	Active- and reactive-power references of the BESS inverter.
P_m, Q_m	Filtered active and reactive powers used by the outer loop.
K_P, K_Q	Active- and reactive-power coupling gains of the low-order benchmark.
τ_p, τ_q	Effective measurement-lag constants for active and reactive power.
τ_E	Common voltage-loop time constant.
n_q	Common reactive-power droop coefficient.
k_d, c_d	Droop synchronization and phase-restoring gains.
M, D_{eff}	VSM virtual inertia and damping coefficients.
$k_{\text{psc}}, c_{\text{psc}}$	PSC synchronization and phase-restoring gains.
I_{max}	Converter current-limit threshold in the low-order benchmark.

Appendix A. Consolidated Controller Equations and Linearization Notes

This appendix consolidates the differential equations used in the benchmark and makes the small-signal linearization explicit.

For droop and PSC, the state vector is

$$x_{d/\text{psc}} = \begin{bmatrix} \delta & E & P_m & Q_m \end{bmatrix}^T,$$

and the state equations are obtained from (1)–(10). For VSM, the state vector is

$$x_{\text{vsm}} = \begin{bmatrix} \delta & \omega & E & P_m & Q_m \end{bmatrix}^T,$$

and the state equations are obtained from (1)–(9). In the pre-fault linearization, the current limiter is inactive, so $P_s = P$ and $Q_s = Q$.

The linearization is performed around the selected pre-fault equilibrium. The Jacobian is constructed from the following partial derivatives.

$$\frac{\partial P}{\partial \delta} = K_P \text{SCR} E_0 V_{g0} \cos \delta_0, \quad \frac{\partial P}{\partial E} = K_P \text{SCR} V_{g0} \sin \delta_0, \quad (\text{A1})$$

$$\frac{\partial Q}{\partial \delta} = K_Q \text{SCR} V_{g0} \sin \delta_0, \quad \frac{\partial Q}{\partial E} = K_Q \text{SCR}. \quad (\text{A2})$$

The reported damping ratio is extracted from the dominant eigenvalue of the resulting Jacobian matrix.

The lag-tolerance trend can also be understood from the reduced active-power channel. For droop and PSC, the reduced active-power channel is governed by the following second-order characteristic polynomial.

$$\tau_p s^2 + (1 + c\tau_p)s + (c + kK_s) = 0, \quad (\text{A3})$$

For droop, the parameters are $(k, c) = (k_d, c_d)$, and for PSC they are $(k, c) = (k_{psc}, c_{psc})$. The comparable VSM reduction yields the following third-order characteristic polynomial.

$$M\tau_p s^3 + (M + D_{\text{eff}}\tau_p)s^2 + D_{\text{eff}}s + K_s = 0. \quad (\text{A4})$$

As SCR decreases, the synchronizing coefficient decreases. The additional dynamic order in Equation (A4) therefore loses phase margin faster than the droop or PSC channels, which is consistent with the admissible-lag envelope reported in the main text.

Appendix B. Discrete-Time Implementation, Tuning Workflow, and Local Sensitivity

The controller implementations were evaluated in discrete time on a per-sample basis. The benchmark sequence for all families is

1. read $V_g(t)$, $\text{SCR}(t)$, and the disturbance schedule;
2. evaluate P and Q from (1) and (2);
3. apply the current-limit law in (4);
4. update P_m and Q_m through the first-order measurement lags;
5. update the controller-specific phase law (droop, VSM, or PSC);
6. update the common voltage loop (6);
7. store P , E , ω , and the derived metrics.

The tuning procedure was deliberately simple. The shared plant and voltage-loop parameters were fixed first. The droop and PSC gains were then adjusted to obtain stable nominal operation at $\text{SCR} = 5$ with comparable voltage-loop aggressiveness. The VSM inertia and damping pair was selected to preserve nominal stability while producing visibly stronger frequency moderation. This process was designed to generate representative, reproducible benchmark implementations rather than globally optimized controller variants.

To assess whether moderate retuning would change the headline message of the benchmark, a local single-parameter sensitivity sweep was performed around the published parameter set. For droop and PSC, the main synchronization gains k_d and k_{psc} were perturbed by $\pm 15\%$. For VSM, the virtual inertia M was perturbed by $\pm 15\%$ while the remaining benchmark parameters were held fixed. Table A1 reports the relative change of four key metrics with respect to each controller's own benchmark baseline. Negative changes in J_f , T_s , and J_E are improvements, whereas positive changes in η_P are improvements.

The sensitivity sweep does not eliminate the main benchmark trade-offs. VSM remains the strongest frequency moderator across the explored perturbations, droop remains the lightest and strongest post-fault restorer, and PSC remains the most balanced option. What changes under retuning is the numerical distance between the families, not the basic application-oriented interpretation.

Table A1. Local sensitivity of selected metrics to representative $\pm 15\%$ parameter perturbations around the published benchmark set.

Controller	Parameter	Perturbation	ΔJ_f	ΔT_s	$\Delta \eta_P$	ΔJ_E
Droop	k_d	-15%	-11.6%	$+10.6\%$	-1.3%	$+5.7\%$
Droop	k_d	$+15\%$	$+11.1\%$	$+65.2\%$	$+1.2\%$	-4.4%
VSM	M	-15%	$+5.3\%$	-6.9%	$+0.5\%$	-3.4%
VSM	M	$+15\%$	-4.5%	$+6.6\%$	-0.2%	$+2.8\%$
PSC	k_{psc}	-15%	-11.9%	$+11.7\%$	-1.0%	$+6.5\%$
PSC	k_{psc}	$+15\%$	$+11.4\%$	-7.8%	$+1.0\%$	-4.9%

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