

Article

Design and Validation of a Hybrid Switched Inductor and Switched Capacitor Buck–Boost DC–DC Converter

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Abstract

This paper proposes a new hybrid switched inductor and switched capacitor (HSISC) buck–boost DC–DC converter. For the duty ratio above 28%, the proposed converter operates as a boost converter; otherwise, it acts as a buck converter. Compared with conventional buck–boost converters, incorporating the hybrid switched inductor and switched capacitor (HSISC), the network yields a substantial voltage gain at lower duty ratios. Being a non-isolated topology, high-frequency transformers and the associated issues are absent. Additionally, the proposed topology has the merits of continuous input current, making it suitable for renewable energy integration and vehicle-to-grid (V2G) applications, a wide range of duty ratio for boost operation, and ease of control as there are only two modes of operation with switches operating in a complementary manner. Operational analysis for the two modes, necessary mathematical derivations for component design, and a steady-state analysis of the converter are reported. The experimental findings for the converter, which were conducted at a duty ratio of 0.05 to 0.5 at a switching frequency of 10 kHz, are reported. The presented results provide proof-of-concept validation based on analytical and simulation studies, demonstrating the feasibility and operational characteristics of the proposed converter.

Keywords: buck–boost converter; DC–DC converters; non-isolated configuration; switched capacitor; switched inductor



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1. Introduction

In today's world, a key challenge is that various power sources, energy storage systems, and loads often operate at different DC voltage levels, requiring voltage conversion—either stepping up or down—to ensure proper integration into the system. DC–DC converters find their application in systems involving DC bus regulation. Modern battery-operated consumer gadgets such as smartphones, tablets, Bluetooth speakers, LED flashlights, USB power banks, and more require buck–boost converters. Along with the advantage of regulated output at different input levels, they also offer the extra benefit of boost and buck operation in a single circuit, which makes them perfect for devices with limited space because they use fewer components and are cost-effective.

Primarily, DC–DC converters are classified as isolated and non-isolated topologies. Though isolated topologies offer higher voltage gain with high-frequency transformers (HFTs), they suffer from (i) increased weight and size, (ii) substantial voltage spikes across the switches due to the leakage inductance of HFTs, and (iii) lower efficiency [1,2]. Hence, non-isolated topologies are preferred when isolation is not mandatorily required. In the buck–boost converter, which is a non-isolated topology, the output voltage can be stepped up or down; this desirable feature has led to its applications in fuel cell systems, on-board chargers for electric vehicles, photovoltaic system-based battery charging, LEDs, power factor correction circuits, and portable electronics [3–5]. Buck–boost converters require a duty cycle, D , of 0.8 or higher to achieve a gain of three or higher. Nevertheless, this is not practically viable [6], as the increased D results in higher switch losses and operating temperatures.

This can be circumvented with power Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with higher power ratings, but the ON-state resistance and consequent conduction losses increase. The resulting converter is expensive, bulky, and offers lower efficiency [7]. Furthermore, owing to discontinuous input current, the conventional buck–boost DC–DC converter is not preferred in renewable energy applications [8]. ZETA, Cuk, and Single-Ended Primary-Inductor Converter (SEPIC) converters overcome the discontinuous input current issue; however, to get a significant voltage gain, these converters require a very high D [3]. The converter proposed in [9] has an inverting output and offers lower gain than conventional buck–boost, Cuk and SEPIC converters. A ZETA-based buck–boost DC–DC converter with a gain of $2D/1 - D$ was successfully described in [10], providing a larger gain than a traditional ZETA converter. The topology mentioned in [11] has a gain of $(D/1 - D)^2$ and draws discontinuous current from the source. Likewise, the converter discussed in [12] is quite promising and offers identical gain but draws continuous input current, making it suitable for the application that requires this characteristic. Similarly, the converter stated in [13] has a gain of $3D/1 - D$ and draws continuous current, making it appropriate for fuel cell and renewable energy applications, and is quite popular these days. However, a converter offering similar gain but drawing discontinuous input current is reported in [14]. Both these converters offer much higher gains than the conventional converters.

Reference [15] reported a non-isolated buck–boost DC–DC converter based on the cascading boost converter concept. This converter offers a voltage gain of $D/(1 - D)^2$. It enters boost mode only when $D > 0.38$. A buck–boost DC–DC converter based on cascading a modified boost configuration at the front end, followed by a restructured ZETA converter, is presented in [16]. This converter offers a voltage gain of $D^2/(1 - D)^2$. It enters boost mode only when $D > 0.5$.

References [15,16] have discussed the merits of the reported converters over the quadratic boost converter topologies. Since the majority of the topologies discussed above have the drawback of having lower gain, several voltage-boosting approaches may be employed to increase the gain of buck–boost DC–DC converters. Other different non-isolated step-up DC–DC converter topologies that offer high voltage gain based on voltage lift (VL), multi-stage (MS), switched inductor (SI), switched capacitor (SC), hybrid SI–SC (HSISC), and coupled inductors (CL) are reported in the literature [2,7,17–20]. The merits and demerits of these topologies are summarized in Table 1. From Table 1, it is evident that for obtaining higher gain, the use of passive elements increases in VL, MS, SC, and SI. The use of the CL approach is limited due to the issues resulting from the leakage inductance. HSISC incurs a higher component count but offers the benefits of SC and SI. This paper proposes a new non-isolated buck–boost DC–DC converter wherein SC and SI approaches are combined to create an HSISC configuration for increased voltage gain. This converter acts as a boost converter when the duty cycle is above 0.28; otherwise, it

acts as a buck converter. The merits of this converter are (i) continuous input current; (ii) a wide range of D for boost operation; (iii) ease of control, as there are only two modes of operation; (iv) significantly higher voltage gain even at relatively low duty ratios; (v) absence of high-frequency transformers and associated design complexities. Furthermore, the proposed converter offers continuous input current, which makes it well suited for renewable energy integration and vehicle-to-grid (V2G) applications.

Table 1. Comparison of non-Isolated DC–DC converter topologies.

Approach	Merits and Demerits	
VL [7,17–19]	Merits	High power density, high efficiency, low voltage ripple
	Demerits	For higher gain, the number of passive elements considerably increases
MS [7,17–19]	Merits	Modularity, higher power density, and efficiency
	Demerits	Complex control scheme, high component count, bulky structure, efficiency reduces with higher stages/levels
SC [7,17–19]	Merits	Compact, high power density, fast dynamic response, lower EMI issues, modularity, and cascading capability
	Demerits	Spikes in current during switching transition, reduced efficiency and power density, sensitivity to ESR
SI [7,17–19]	Merits	High boost potential and compatible with other converters
	Demerits	Requires more passive elements and is bulky
HSISC [20]	Merits	High voltage gain, capability of cascading, and modularity
	Demerits	More passive elements are needed; higher power losses
CL [17,19,20]	Merits	Versatile boosting capacity with adjustable turns ratio
	Demerits	High voltage spikes due to leakage inductance require precise magnetic and challenging thermal designs.

Figure 1 depicts the applications of the proposed converter. Due to its ability to draw continuous input current, the converter can be used for the integration of renewable energy sources as well as for vehicle-to-grid (V2G) technology for electric vehicles. The succeeding sections describe the proposed converter's operation, gain calculations, component design, and experimental validation.

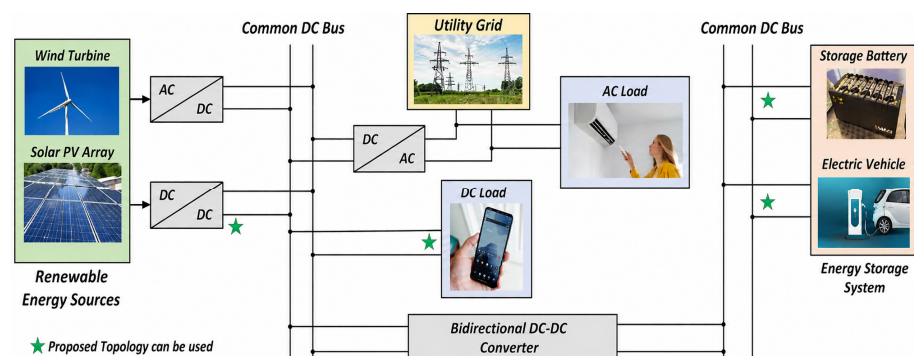


Figure 1. Application of proposed non-isolated HSISC buck–boost converter.

2. Materials and Methods

2.1. Proposed HSISC Buck–Boost Converter

Figure 2 shows the proposed non-isolated HSISC buck–boost converter with HSISC at the front end and buck converter at the load end. The converter comprises a DC source

with voltage of V_{in} , three inductors (L_1, L_2, L_0), five switches ($Q_{Bp}, Q_C, Q_{C1}, Q_{C2}, Q_0$), three capacitors (C_1, C_2, C_0), nine power diodes ($D_{L1}, D_{L2}, D_{L3}, D_{C1}, D_{C2}, D_{C22}, D_{C0}, D_{L0}, D_{Cx}$), and a load resistor (R_0). The proposed converter operates in Modes 1 and 2. The equivalent circuits for the two modes are shown in Figures 3 and 4, respectively. The switching table provided in Table 2 covers the two modes of operation. The five switches are divided into groups. Q_{Bp}, Q_C, Q_0 are part of Group 1, whereas Q_{C1}, Q_{C2} are part of Group 2. When the switches of one group are ON, the other group's switches need to be OFF. Thus, only one gate signal needs to be computed, with another gate signal being its complement. This simplifies the gating requirement. During Mode 1, the gate voltage v_{G1} is provided for Group 1 switches to operate in the ON state. When Group 1 switches are gated, the gate signals for Group 2 switches are inhibited. Similarly, during Mode 2, gate pulses for Group 1 switches are inhibited while ensuring that the gate voltage of Group 2 switches, v_{G2} , is applied such that they are turned ON. The waveforms for the proposed converter based on the theoretical analysis are shown in Figure 5, where v_{L1}, v_{L2} are the instantaneous voltages across L_1, L_2 ; i_{L1}, i_{L2} are the instantaneous currents flowing through L_1, L_2 ; v_{C1}, v_{C2} are the instantaneous voltages across C_1, C_2 ; v_{L0} is the instantaneous voltage across L_0 ; i_{L0} is the current flowing through L_0 ; V_{G1} and V_{G2} are the gate voltages during the ON and OFF state, respectively; T_S is the total time; T_{ON}, T_{OFF} are the periods for which Modes 1 and 2 are active.

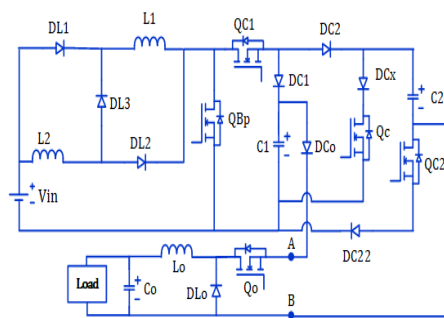


Figure 2. Proposed non-isolated HSISC buck-boost converter.

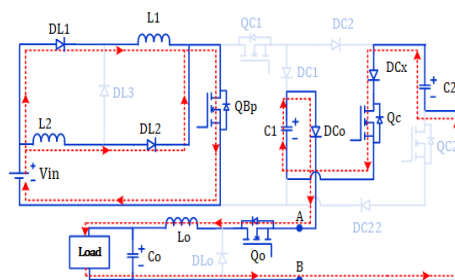


Figure 3. Equivalent circuit of the proposed non-isolated HSISC buck-boost converter for Mode 1.

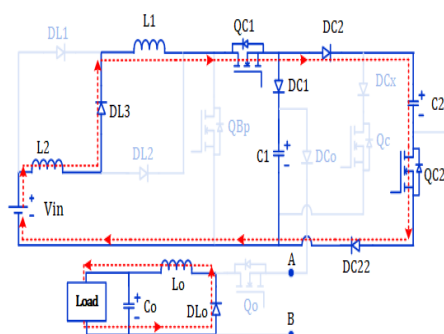
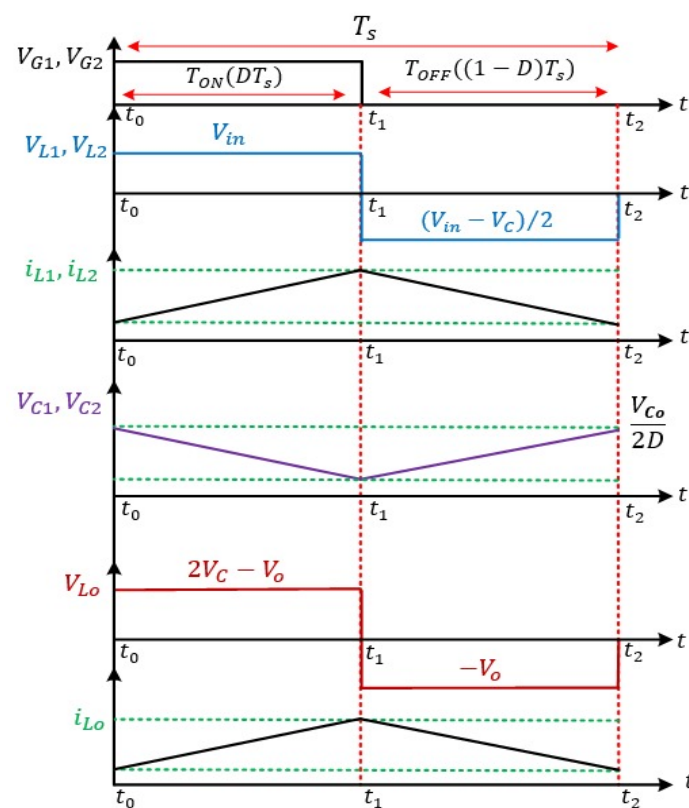


Figure 4. Equivalent circuit of the proposed non-isolated HSISC buck-boost converter for Mode 2.

Table 2. Switching table for the proposed non-isolated HSISC buck–boost converter.

Switch	State	Diodes	State	Path of Flow of Current	Remarks
Mode 1					
Q_{Bp}	ON	D_{L1}	RB		
Q_{C1}	OFF	D_{L2}	RB		
Q_{C2}	OFF	D_{L3}	RB		
Q_c	ON	D_{C1}	RB	(1) through L_1 : $V_{in}-L_1-Q_{Bp}$	L_1, L_2 connected in parallel and energized C_1, C_2 connected in series and discharged
Q_o	ON	D_{C2}	RB	(2) through L_2 : $V_{in}-L_2-Q_{Bp}$	
		D_{C22}	RB	(3) through C_1-C_2 : $C_1-D_{Co}-Q_o-L_o-C_2-Q_c$	
		D_{Lo}	RB		
		D_{Co}	FB		
		D_{Cx}	FB		
Mode 2					
Q_{Bp}	OFF	D_{L1}	RB		
Q_{C1}	ON	D_{L2}	RB		
Q_{C2}	ON	D_{L3}	FB		
Q_c	OFF	D_{C1}	FB	(1) through $L_1-L_2-C_1$: $V_{in}-L_1-L_2-Q_{C1}-D_{C1}-C_1-V_{in}$	L_1, L_2 connected in series and de-energized C_1, C_2 connected in parallel and charged
Q_o	OFF	D_{C2}	FB	(2) through $L_1-L_2-C_2$: $V_{in}-L_1-L_2-Q_{C1}-D_{C2}-C_2-Q_{C2}-D_{C22}-V_{in}$	
		D_{C22}	FB		
		D_{Lo}	FB		
		D_{Co}	RB		
		D_{Cx}	RB		

FB and RB indicate forward biased and reverse biased, respectively.

**Figure 5.** Waveforms for the proposed non-isolated HSISC buck–boost converter based on theoretical analysis.

2.1.1. Analysis of Converter Operation for Mode 1 ($t_0 \leq t < t_1$)

Referring to the waveforms given in Figure 4, the converter operation in Mode 1 exists from t_0 to t_1 . This duration is also termed as the T_{ON} duration. For this duration, the Group 1 switches are turned ON by providing appropriate gate voltage, whereas the Group 2 switches are turned OFF by inhibiting the gate.

In Mode 1, Q_{BP} , Q_C , Q_o are gated so that they operate in the ON state. This results in D_{L1} , D_{L2} , D_{Co} , and D_{Cx} being forward biased and operating in conduction state. On the other hand, switching state results in one of the terminals of D_{C1} - D_{C2} - D_{C22} being disconnected as the switch to which they are connected is in the OFF state. Also, the switching action results in D_{L3} and D_{Lo} being reverse biased. With Q_{BP} ON, the parallel combination of inductors L_1 , L_2 is connected across the input (V_{in}). Consequently, L_1 and L_2 are charged to the same level as the input voltage ($v_{L1} = v_{L2} = V_{in}$). L_1 and L_2 oppose the rate of change of current. Considering linear variation over the small period, i_{L1} and i_{L2} linearly increase, and L_1 and L_2 are energized. With $L_1 = L_2$, i_{L1} and i_{L2} are identical. Also, input current, i_{in} , equals ($i_{L1} + i_{L2}$).

The front-end HSISC network and load-end buck converter are linked via terminals A-B. As Q_C - D_{Co} is conducting and forward biased, the series combination of C_1 - C_2 is connected across the terminals A-B. The voltage across A-B, v_{AB} , is ($v_{c1} + v_{c2}$), where v_{c1} , v_{c2} are the voltages across C_1 , C_2 . A buck converter connects A-B across the load resistor, R_o . With Q_o ON, C_1 and C_2 discharge and transfer the stored energy to R_o . Hence, as shown in Figure 5, during Mode 1, v_{C1} - v_{C2} reduces. With a series connection of C_1 - C_2 acting as a source for the buck converter circuitry and Q_o being ON, i_{Lo} increases, and energy is stored in L_o . For this mode, v_{Lo} is the difference between ($v_{c1} + v_{c2}$) and v_{Co} , the voltage across C_o and load resistor, R_o . At t_1 , Mode 1 ends with the removal of gate pulses for the conducting switches. For this mode, the voltage equations are given in (1)–(3).

$$v_{L1} = v_{L2} = v_L = V_{in} \quad (1)$$

$$v_{C1} + v_{C2} = v_{AB} = 2v_{C1} = v_{Lo} + v_{Co} \quad (2)$$

$$v_{Lo} = 2v_{C1} - v_{Co} \quad (3)$$

2.1.2. Analysis of Converter Operation for Mode 2 ($t_1 \leq t < t_2$)

Referring to the waveforms given in Figure 5, the converter operation in Mode 2 exists from t_1 to t_2 . This duration is also termed as the T_{OFF} duration. Contrary to the earlier mode, for this mode, the Group 1 switches are turned OFF by inhibiting the gate pulse. In contrast, the application of appropriate gate voltages turns ON the Group 2 switches. During this period, Q_{C1} , Q_{C2} and D_{L3} , D_{C1} , D_{C2} , D_{C22} , D_{Lo} are conducting. D_{L1} , D_{L2} are reverse biased and OFF. Alternately, as Q_o , Q_C are OFF, one of the terminals of D_{Co} , D_{Cx} is open. Hence, they do not participate in the circuit operation during this mode. As Q_{C1} , Q_{C2} are ON, C_1 , C_2 are connected in parallel. With Q_{BP} OFF, L_1 , L_2 are connected to this parallel combination. This results in a reduction in i_{L1} , i_{L2} . L_1 - L_2 opposes the rate of change of current. To maintain the current, L_1 - L_2 dissipates the stored energy, and the polarity of v_{L1} - v_{L2} reverses. As a consequence, D_{L1} - D_{L2} is reverse biased and D_{L3} is forward biased. Further, with D_{L3} ON, L_1 and L_2 are connected in series. Also, V_{in} gets connected in series with L_1 - L_2 .

The switching table for the proposed non-isolated HSISC buck-boost converter is presented in Table 2.

Alternately, with Q_{C1} - Q_{C2} ON and D_{C1} - D_{C2} - D_{C22} conducting, C_1 and C_2 are connected in parallel. The series connection of V_{in} - L_1 - L_2 charges the parallel combination of C_1 - C_2 . With Q_{C1} - D_{C1} ON, the positive polarity terminal of the series combination of L_1 - L_2

is connected to the positive terminal of the parallel combination of C_1 - C_2 . Conversely, the negative polarity terminal of the series combination of L_1 - L_2 is connected to the positive terminal of V_{in} . Hence, the voltage across the series connection of L_1 - L_2 is $-(V_{in} - v_c)$, where $v_{c1} = v_{c2} = v_c$. Due to series connection, $i_{in} = i_{L1} = i_{L2}$. Considering linear variation over the given time duration, i_{L1} and i_{L2} tend to reduce as the stored inductor energy is dissipated linearly.

Now, $(V_{in} + v_{L1} + v_{L2})$ appears across the parallel combination of C_1 - C_2 , resulting in C_1 - C_2 getting charged. As i_{L1} - i_{L2} decreases, the energy stored in L_1 - L_2 is transferred to C_1 - C_2 . Considering $v_{L1} = v_{L2} = V_{in}$, at t_2 , C_1 and C_2 are each assumed to be charged to $3V_{in}$. For $D = 0.5$, the capacitor voltages are observed to reach approximately $3V_{in}$, as supported by steady-state analysis and experimental results. Since D_{Cx} - Q_c and D_{Co} - Q_o are not conducting, the HSISC network is disconnected from the terminals A - B . Inductor L_o freewheels to dissipate the stored energy in R_o . During this period, $v_{L_o} = -v_{C_o}$. Also, i_{L_o} linearly reduces as the energy stored in L_o is dissipated in the load. This mode ends with the removal of gate pulses for the conducting switches at t_2 , after which Mode 1 is repeated. The voltage equations for this mode are given as follows:

$$v_{C1} = v_{C2} = V_{in} + v_{L1} + v_{L2} \quad (4)$$

$$v_{L1} = v_{L2} = (V_{in} - v_{C1})/2 = (V_{in} - v_{C2})/2 \quad (5)$$

$$v_{L_o} = -v_{C_o} \quad (6)$$

2.2. Component Design for the Proposed Non-Isolated HSISC Buck-Boost Converter

Equations (7)–(23) show the computations of L_1 , L_2 , L_o ; C_1 , C_2 , C_o ; and D for the proposed converter. By applying the volt-second balance for L_o , the average value of v_{C1} - v_{C2} , denoted as V_{C1} - V_{C2} , is obtained in terms of the average value of output voltage, denoted as V_o , and D as shown in (7). Similarly, by applying the volt-second balance for L_1 - L_2 , V_{C1}/V_{in} and V_{C2}/V_{in} can be determined as per (8). Furthermore, from (8), it is clear that for any positive value of D , which is greater than zero, $V_{C1} > V_{in}$. The relationship between V_{in} and V_{C_o} shown in (9) is established by substituting V_{C1} , V_{C2} from (7) into (8). Analysis of (7)–(9) yields that for $D = 0.28$, $G_1 = 1.778$ and $G_2 = 0.995$. This leads to $V_{C_o} = V_{in}$. With $D > 0.28$, $G_2 > 1$, and the boost action is implemented. Alternately, with $D < 0.28$, $G_2 < 1$, and buck action is implemented. With $L_1 = L_2 = L$, in Mode 1, the parallel connection of L_1 - L_2 is connected in series across V_{in} , and v_{L1} - v_{L2} can be expressed as per (10) and (11). Using (10) and (11), L can be derived as shown in (12). With $T_{ON} = DT_S$ and switching frequency, $f_{sw} = 1/T_S$; L given in (12) can also be expressed as per (13).

$$V_{C1} = V_{C2} = V_{C_o}/2D \quad (7)$$

$$V_{C1}/V_{in} = V_{C2}/V_{in} = \{(1 + D)/(1 - D)\} = G_1 \quad (8)$$

$$(V_{C_o}/V_{in}) = \{2D(1 + D)/(1 - D)\} = G_2 \quad (9)$$

$$v_{L1} = v_{L2} = v_L = V_{in} \quad (10)$$

$$v_L = V_{in} = L(\Delta i_L/T_{ON}) \quad (11)$$

$$L = L_1 = L_2 = V_{in}T_{ON}/\Delta i_L \quad (12)$$

$$L = L_1 = L_2 = V_{in} D/(\Delta i_L f_{sw}) \quad (13)$$

In Mode 2, A - B terminals are disconnected from C_1 - C_2 - V_{in} . L_o freewheels the stored energy to maintain the continuity of supply to the load.

$$\text{During this duration, } V_{L_o} = -V_{C_o} \quad (14)$$

$$\text{and } V_{L_o} = -V_{C_o} = -L_o(\Delta i_{L_o}/T_{OFF}), \quad (15)$$

where Δi_{L_o} is the peak-to-peak current ripple for L_o . With $T_{OFF} = (1 - D)T_s$, L_o can be given as

$$L_o = V_{C_o} (1 - D) / (\Delta i_{L_o} f_{sw}). \quad (16)$$

In Mode 1, with Q_{C1} - Q_{C2} OFF and D_{Cx} - D_{Co} forward biased and conducting, C_1 and C_2 are connected in series. This results in the sum of v_{c1} and v_{c2} being applied across A - B terminals. C_1 and C_2 act as a source and discharge to supply power to the load.

$$\text{During this mode, } I_{C1} = I_{C2} = I_o. \quad (17)$$

Hence, with ΔV_{C1} - ΔV_{C2} as the respective peak-to-peak voltage ripple for C_1 - C_2 , I_o can be mathematically expressed as shown in (18). Further, based on (18), C_1 - C_2 can be determined as per (19) and (20).

$$I_o = C_1(\Delta V_{C1}/T_{ON}) = C_2(\Delta V_{C2}/T_{ON}) \quad (18)$$

$$C_1 = (V_{C_o} \cdot D) / (R_o \cdot \Delta V_{C1} \cdot f_{sw}) \quad (19)$$

$$C_2 = (V_{C_o} \cdot D) / (R_o \cdot \Delta V_{C2} \cdot f_{sw}) \quad (20)$$

Lastly, the output capacitor, C_o , needs to be designed. For designing C_o , the charge stored in C_o , denoted as Q_o , and the peak-to-peak voltage ripple measured across C_o , denoted as ΔV_{C_o} , are considered. In general, Q_o can be expressed as per (21). The theory of buck DC-DC converter is employed for the design of C_o because the circuit configuration between terminals A - B and the load resembles buck DC-DC converter circuitry. Hence, C_o can be designed based on the same logic and theory as that employed for designing the output capacitor for a buck DC-DC converter. Therefore, based on the variations in v_{C_o} , circuit operation, and most importantly, the theory of buck DC-DC converter, Q_o can also be expressed as shown in (22). Using (21) and (22), C_o can be given as per (23). Moreover, based on (7)–(9), D can also be computed as per (24). The design expressions for inductors and capacitors are derived based on permissible current and voltage ripple limits. Lower ripple requirements necessitate higher inductance and capacitance values, which directly influence the size and cost of the converter. Therefore, the selection of passive components represents a trade-off between performance, size, and efficiency. Also, for proper operation of the proposed converter in continuous conduction mode (CCM), the inductor currents must remain non-zero throughout the switching cycle. This condition can be ensured by selecting appropriate inductance values based on load resistance, duty ratio, and switching frequency, thereby avoiding transition into discontinuous conduction mode (DCM).

$$Q_o = C_o \cdot \Delta V_{C_o} \quad (21)$$

$$Q_o = 0.5 (\Delta i_{L_o} / 2) (T / 2) \quad (22)$$

$$C_o = (\Delta i_{L_o} T) / (8 \Delta V_{C_o}) = (\Delta i_{L_o} D) / (8 f_{sw} \Delta V_{C_o}) \quad (23)$$

$$D = (V_{c1} - V_{in}) / (V_{c1} + V_{in}) \quad (24)$$

3. Comparative Analysis

Table 3 presents a comparative analysis of several buck–boost topologies, including the converter that is being proposed. This comparative analysis takes into account the number of components (switches, diodes, capacitors, and inductors); voltage gain; value of duty ratio when gain becomes one or beyond, which the converter operates in boost mode; and type of input current drawn from the source (discontinuous or continuous). The input current nature of the proposed converter and the converter presented in [12,13,15,16] is what distinguishes them from other topologies highlighted in Table 3. These topologies draw continuous current from the source, making them suitable for renewable applications. Figure 6 shows the voltage gain curves for the buck–boost topologies mentioned in Table 3.

Table 3. Comparison of the proposed and existing converters.

Converter Topology	I	C	D	S	Voltage Gain	$G=1, D$	Input Current Conduction
Conventional buck–boost converter	1	1	1	1	$D/1-D$	0.5	Discontinuous
Cuk converter	2	2	1	1	$D/1-D$	0.5	Continuous
SEPIC converter	2	2	1	1	$D/1-D$	0.5	Continuous
Ref. [9]	2	2	3	1	$D/1-D^2$	0.618	Discontinuous
Ref. [11]	2	2	2	2	$(D/1-D)^2$	0.5	Discontinuous
Ref. [10]	3	4	2	1	$2D/1-D$	0.33	Discontinuous
Ref. [14]	3	5	3	1	$3D/1-D$	0.25	Discontinuous
Ref. [12]	3	3	5	1	$(D/1-D)^2$	0.5	Continuous
Ref. [13]	4	6	3	1	$3D/1-D$	0.25	Continuous
Ref. [15]	2	3	3	2	$D/(1-D)^2$	0.38	Continuous
Ref. [16]	3	3	2	2	$D^2/(1-D)^2$	0.5	Continuous
Proposed converter	3	3	9	5	$\frac{2D(1+D)}{(1-D)}$	0.28077	Continuous

I, C, D, and S indicate the number of inductors, capacitors, diodes, and switches, respectively. G indicates the voltage gain of the converter.

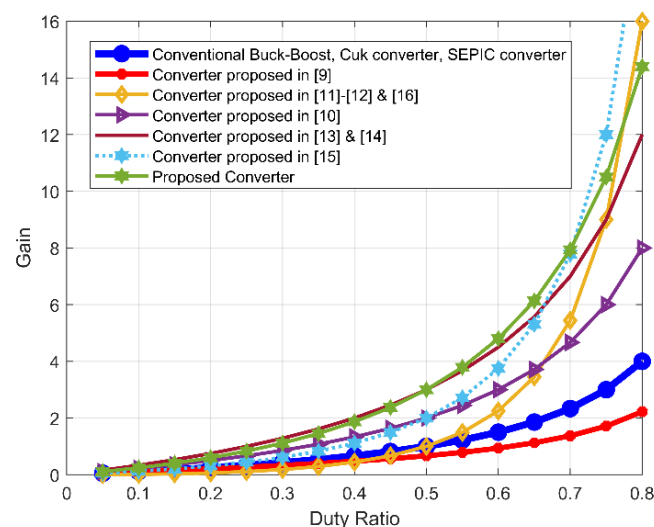


Figure 6. Voltage-gain comparison of the proposed converter and other converters.

The disadvantage of the conventional buck–boost converter is mitigated by the Cuk and SEPIC converters, which draw continuous input current. These converters do not find any practical use, because they have a considerably smaller voltage gain and a limited range of D for boost operation. Similarly, the converter mentioned in [9] deals with similar

detriments. Further, the topologies stated in [11,12,16] function as boost converters after the duty ratio of 0.5. In contrast, the proposed converter offers a gain of three times at this specific duty ratio. Moreover, it provides exponentially higher gain at higher duty ratios, making experimental implementation difficult or impractical. Up to the duty ratio of 0.7, the converter mentioned in [15] provides less gain than the suggested topology. At greater D , it offers more gain. In general, it is not practically feasible to run converters at larger D , considering the significant conduction loss and operating temperature. In contrast to the converter suggested in [10], the proposed topology also has a significantly larger gain. Likewise, the proposed converter yields higher gain at higher values of D in comparison to the topologies discussed in [13,14]. Compared with the other buck–boost topologies listed in Table 3, the proposed converter has a wider bandwidth of D for boost mode, larger gain, and continuous input current. The voltage stress across switches and diodes for different duty ratios has been analyzed and is summarized in Table A1. This analysis provides useful insight for device selection and highlights that the proposed converter operates within practical voltage limits over the intended duty ratio range.

4. Results and Discussion

In this work, the proposed converter is validated through detailed simulation studies to verify its operational characteristics and theoretical analysis. The primary objective is to establish the feasibility of the topology and its steady-state performance. For experimental validation, the laboratory prototype of the proposed non-isolated HSISC buck–boost converter was developed using discrete components. Figure 7 shows a photograph of the developed laboratory prototype. The specifications for the components used in the proposed converter circuitry are given in Table 4. For switches, IRFP640N power MOSFETs are employed. Meanwhile, for diodes, the G and S terminals of IRFP640N are shorted so that the body diode can be exclusively utilized. A TLP 250H-based driver circuit is used to interface the PWM pins of the Arduino Mega 2560 controller with the gate terminals of the respective switches. The prototype was tested for different duty cycles for a constant V_{in} of 20 V. A 100 MHz battery-operated power analyzer, of Agilent Technology make, was used to record the waveforms and perform the measurements. Switching frequency of 10 kHz is considered for prototype testing. The switching frequency of 10 kHz was selected as a representative value for initial validation and to ensure clear observation of converter operation in simulation. The proposed topology is not inherently limited to this frequency and can be extended to higher switching frequencies with appropriate device selection and optimized design.

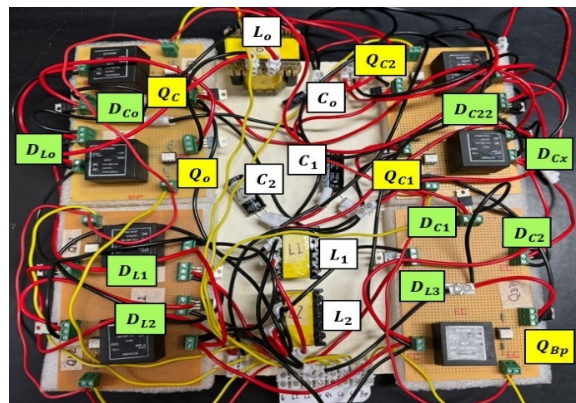
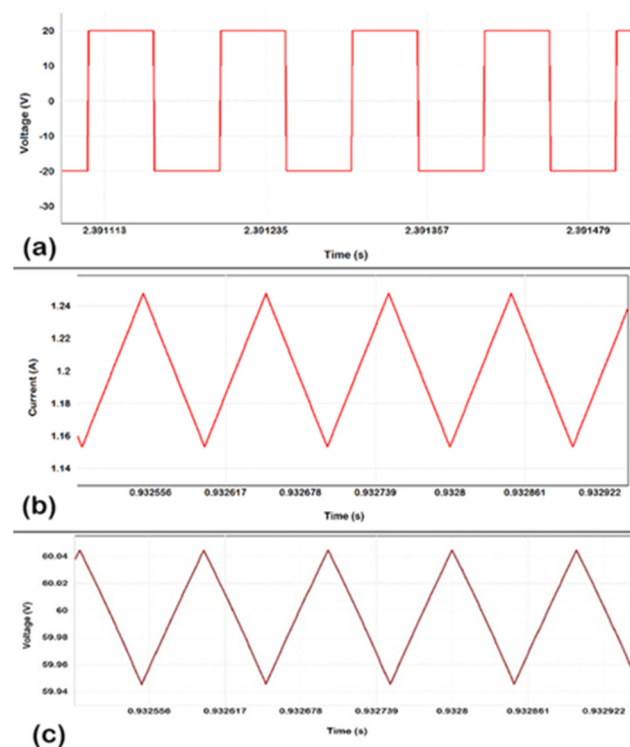


Figure 7. Developed laboratory prototype for the proposed non-isolated HSISC buck–boost converter.

Table 4. Component specifications for the proposed non-isolated HSISC buck–boost converter.

Parameters	L_1 - L_2	C_1 - C_2	L_0	C_0	R_0	f_{sw}
Value	10.56 mH	330 μ F	30.2 mH	22 μ F	100 Ω	10 kHz

The developed prototype was tested with a D of 0.5 in boost mode (resulting in a voltage gain of 3) and 0.2 in buck mode (resulting in a 0.6 gain). The PSIM simulation results for boost (at $D = 0.5$) and buck (at $D = 0.2$) operation are shown in Figures 8–11, respectively. Figures 8a and 10a make it clear that both inductors L_1 and L_2 must be charged to the input voltage of 20 V in accordance with (10). The output of the converter in boost and buck mode should be 60 V and 12 V, respectively, in line with (9), as supported by Figures 9c and 11c. The inductor current i_{L1} - i_{L2} shown in Figures 8b and 10b corresponds to the theoretical waveforms shown in Figure 5 with an average value of 1.2 A for the boost mode and 0.06 A for the buck mode. When inductors L_1 , L_2 discharge in series across the parallel capacitors C_1 , C_2 , both capacitors are charged during Mode 2. According to Equation (7), the capacitor voltages V_{C1} , V_{C2} should be 60 V in boost mode and 30 V in buck mode, as shown in Figures 8c and 10c, respectively. The inductor L_0 is charged during Mode 1 when the fully charged capacitors C_1 , C_2 discharge in series across the lower buck circuit. According to (3), in this way, the inductor L_0 is charged to 60 V in boost mode and 48 V in buck mode. However, during Mode 2, the charged inductor L_0 discharges across the parallel combination of the capacitor C_0 and load. As per (6), the voltage levels need to be -12 V in buck mode and -60 V in boost mode. These results are confirmed for both operating modes in Figures 9a and 11a. The inductor current i_{L0} is shown in Figures 9b and 11b, where the average values are 0.6 A and 0.12 A, respectively. Simulation results were obtained under ideal conditions; the intent was to prove the concept behind the topology and validate the theoretical outcome.

**Figure 8.** Simulation results for boost mode operation of the non-isolated HSISC buck–boost converter with $D = 0.5$: (a) V_{L1} , (b) i_{L1} , and (c) V_{C1} .

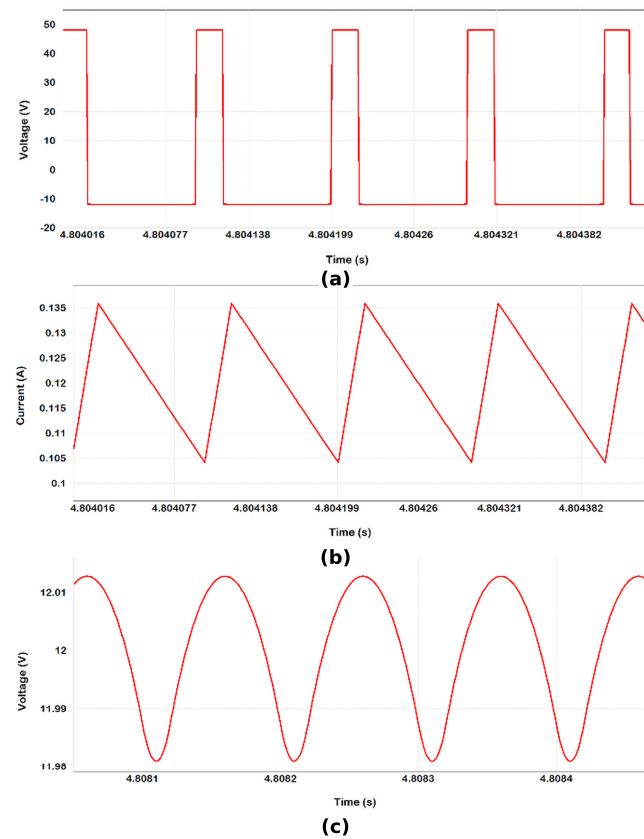


Figure 9. Simulation results for boost mode operation of non-isolated HSISC buck-boost converter with $D = 0.5$: (a) V_{Lo} , (b) i_{Lo} , and (c) V_o .

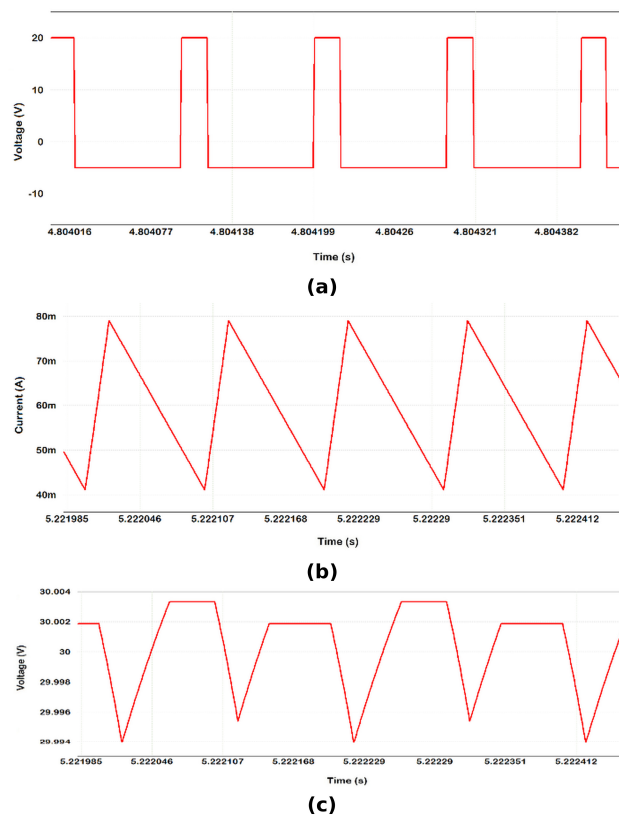


Figure 10. Simulation results for the proposed non-isolated HSISC buck-boost converter operating in buck mode with $D = 0.2$: (a) V_{L1} , (b) i_{L1} , and (c) V_{C1} .

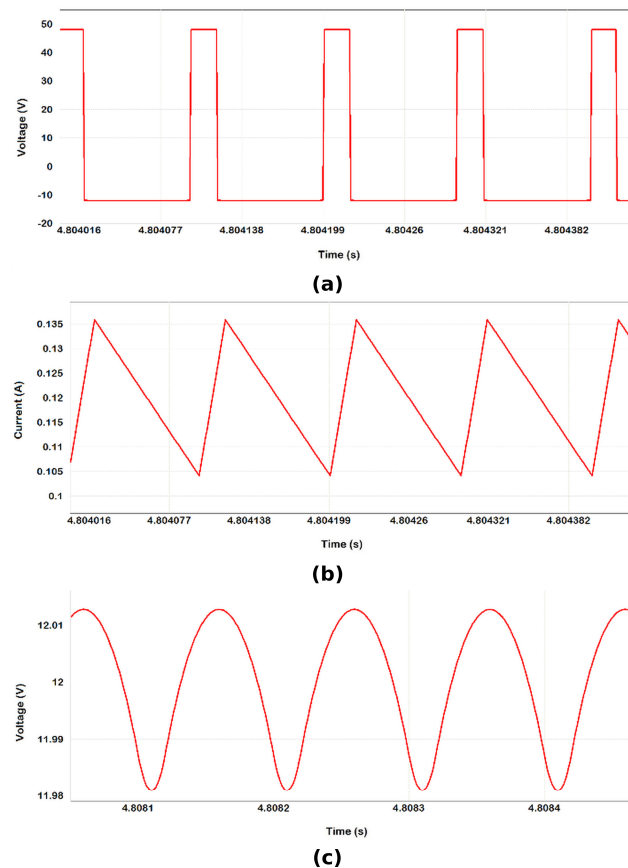


Figure 11. Simulation results for buck mode operation of non-isolated HSISC buck-boost converter with $D = 0.2$: (a) V_{Lo} , (b) i_{Lo} , and (c) V_o .

The experimental results of the converter in both boost and buck modes are shown in Figures 12 and 13, respectively. Figure 12 shows the experimental results for the proposed non-isolated HSISC buck-boost converter operating in boost mode with $D = 0.5$. With $V_{in} = 20$ V, as per (9), the V_{Co} needs to be 60 V. However, the measured value is 49.524 V. The reduction in the measured value is due to the ON-state voltage drop across the conducting switches.

Figure 12b depicts the inductor current $i_{L1}-i_{L2}$, which is in accordance with the theoretical waveforms presented in Figure 5, with the peak-to-peak value of 0.17 A and average value of 1.4 A. Inductors (L_1-L_2) charge in parallel during Mode 1 and discharge in series during Mode 2. According to Figure 12c, V_{C1} has an average value of 49.465 V. During Mode 2, C_2 is connected in parallel with C_1 . C_1-C_2 also charges to the same voltage. Hence, for Mode 2, the voltage across terminals A-B is equal to ($V_{C1} = V_{C2}$). However, during Mode 1, due to the series connection of C_1-C_2 , the voltage across terminals A-B is ($V_{C1} + V_{C2}$) = $2V_{C2} = 98.93$ V, theoretically. To verify the theoretical notion, the voltage across terminals A-B would appear as input to the buck converter at the load side and would give output (V_{Co}) of 49.46 V ($98.93 \times 0.5(D)$), which is nearly equal to the result obtained. With $D < 0.28$, the proposed converter performs buck operation.

Figure 13 shows the experimental results for the proposed non-isolated HSISC buck-boost converter operating in buck mode with $D = 0.2$. With $V_{in} = 20$ V, as per (9), the V_{Co} needs to be 12 V. The corresponding measured value is 11.6 V. Figure 13 shows the experimental results for the proposed non-isolated HSISC buck-boost converter operating in buck mode with $D = 0.2$ and low load condition (<100 ohms). The measured value of output voltage, which is 8.587 V, is illustrated in Figure 13a. Figure 13b depicts $i_{L1}-i_{L1}$, which matches the theoretical waveforms presented in Figure 5, with the Δi_{L1} being positive and negative during Modes 1 and 2, respectively. The peak-to-peak value and average

value of i_{L1} are correspondingly recorded as 0.06 A and 1.084 A. V_{C1} has an average value of 25.31 V, as shown in Figure 13c.

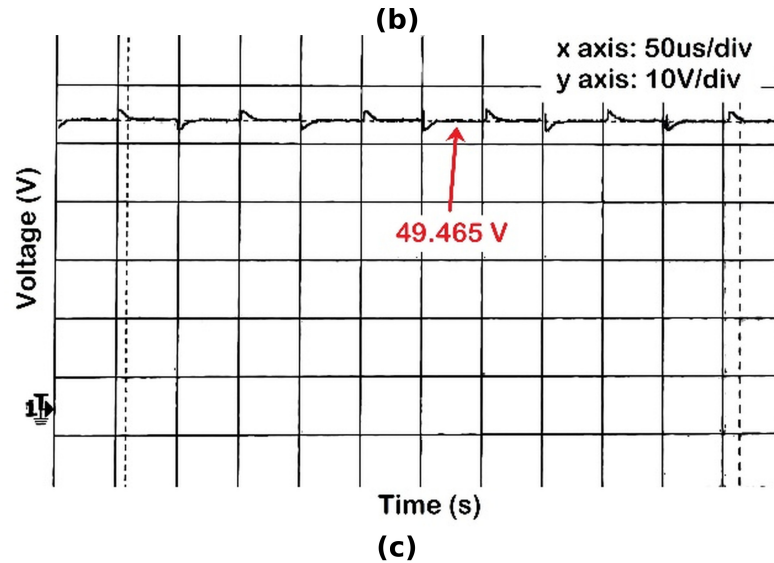
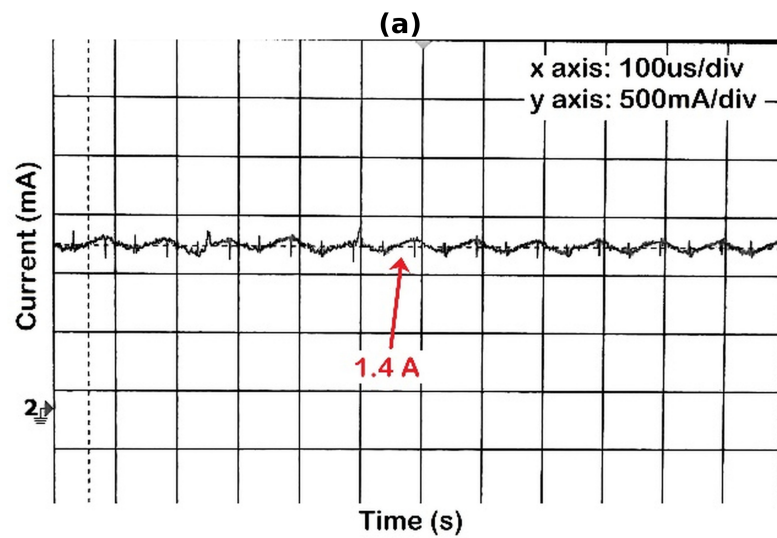
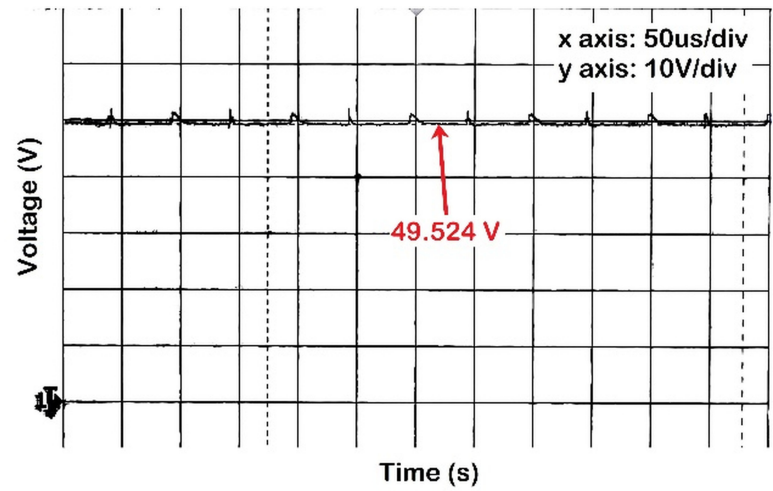


Figure 12. Performance analysis of the proposed non-isolated HSISC buck–boost converter operating in boost mode with $D = 0.5$ (a) V_o , (b) i_{L1} , and (c) V_{C1} .

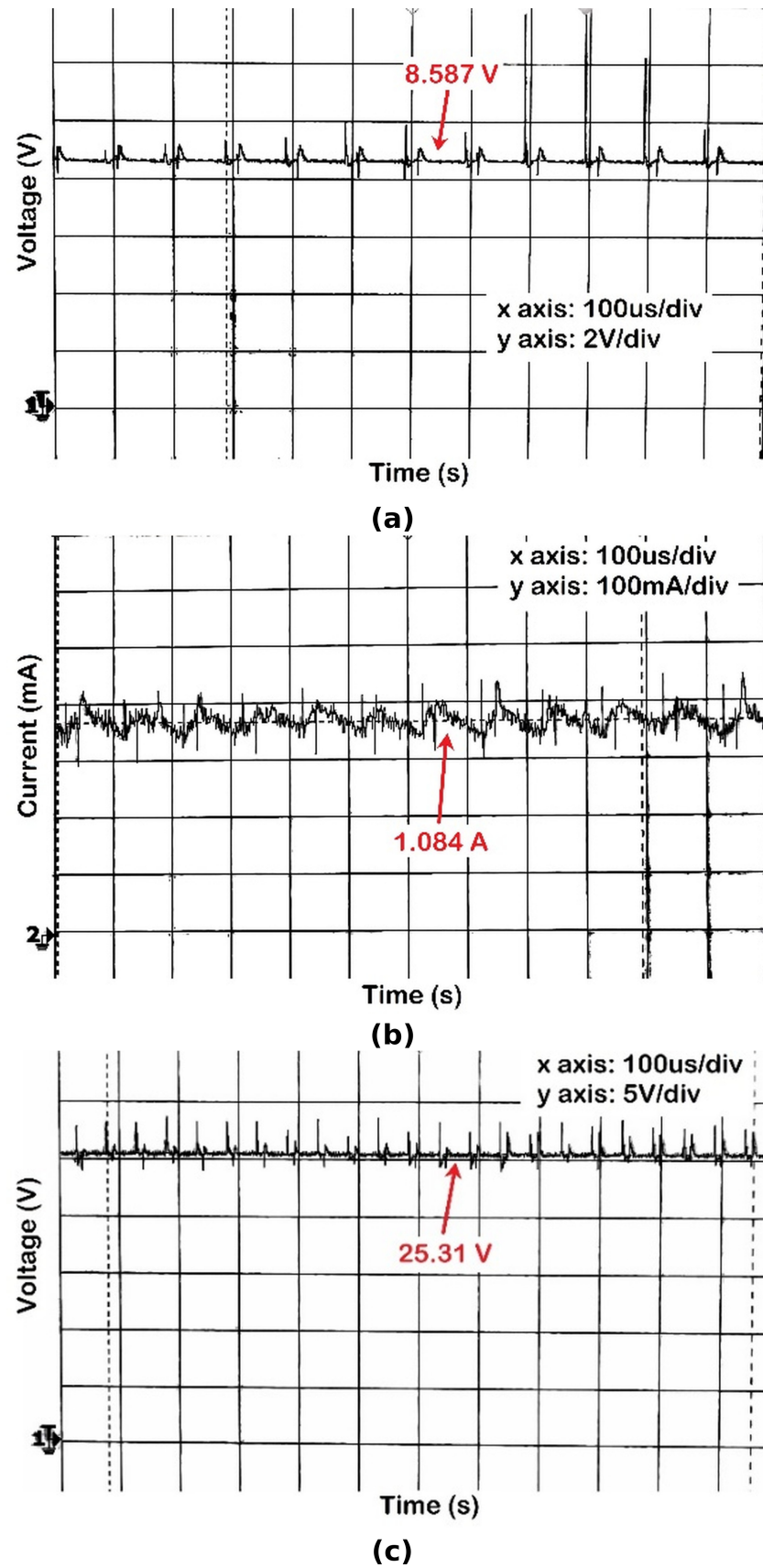


Figure 13. Performance analysis of the proposed non-isolated HSISC buck-boost converter operating in buck mode with $D = 0.2$ (for low load condition ($<100\ \Omega$)): (a) V_o , (b) i_{L1} , and (c) V_{C1} .

Table 5 shows the experimental results at different D . It is evident that the converter performs as a buck converter up to a duty ratio of 0.28 and as a boost converter beyond that, making it appropriate for various applications. The experimental implementation was carried out until the duty ratio of 0.5 because of the limitations of measuring instruments. The primary goal was to verify the simulation findings and assess whether the approach to developing this topology was sound. In practical implementations, non-idealities such as equivalent series resistance (ESR) of capacitors, winding resistance of inductors, and voltage drops across semiconductor devices affect the converter performance. These parasitic elements contribute to additional voltage ripple and reduce the effective voltage gain, which explains the deviation observed between theoretical and experimental results. The practical operating range of the converter is limited by factors such as increased conduction losses at higher duty ratios and voltage stress across components. In this work, experimental validation is carried out up to a duty ratio of 0.5 to ensure reliable operation within safe limits of the employed devices. The present study focuses on validating the topology and its steady-state behavior through analytical modeling and simulation. A comprehensive experimental validation, efficiency analysis, and investigation under dynamic loading conditions are identified as part of future work. Moreover, for higher-frequency operation, the impact of switching losses, parasitic elements, and component optimization must be carefully considered, which forms part of future investigations.

Table 5. Experimental results for the proposed converter.

V_{in} (V)	I_{in} (A)	D	V_{co} (V)		Operating Mode
			Measured	Calculated	
20	0.02	0.05	2.6	2.21	Buck
20	0.03	0.1	4.8	4.88	Buck
20	0.05	0.15	7.9	8.11	Buck
20	0.09	0.2	11.6	12	Buck
20	0.15	0.25	16.1	16.67	Buck
20	0.16	0.26	16.9	17.7	Buck
20	0.2	0.28	19.1	19.9	Buck
20	0.24	0.3	21.4	22.28	Boost
20	0.39	0.35	27.6	29.07	Boost
20	0.62	0.4	35	37.34	Boost
20	0.96	0.45	43.3	47.45	Boost
20	1.47	0.5	49.524	60	Boost

5. Conclusions

In this paper, a novel hybrid switched inductor and switched capacitor (HSISC) buck–boost DC–DC converter, which operates as a boost converter above a duty ratio of 28% and as a buck converter below this value, is proposed. The HSISC network significantly improves voltage gain at lower duty ratios, outperforming traditional buck–boost converters without requiring high-frequency transformers, simplifying the design. The proposed converter’s capability to maintain continuous input current and support a wide range of duty ratios for boost operation is demonstrated through comprehensive theoretical analysis, including operational waveform derivation and component sizing equations. Experimental results at a switching frequency of 10 kHz across duty ratios from 0.05 to 0.5 demonstrate the feasibility and validate the operational concept of the proposed converter and presented

analytical and simulation studies. The merits of this converter can be summarized as (i) continuous input current, (ii) wide range of D for boost operation, and (iii) simplified control, as there are only two operational modes, with the two groups of switches operating in a complementary manner. Although the suggested topology has a higher gain than existing topologies, it has a drawback because it has more passive parts, increasing losses. Nevertheless, the usage of IGBTs, heat sinks, and snubber circuits helps minimize the losses. This work primarily focuses on presenting the concept of the topology, how it works, the equations used to calculate gain, and component design to create a hardware prototype that would verify simulation results. This article significantly expands the scope for conducting loss analysis since the converter has only two modes of operation, making a state space model of the converter simpler. Furthermore, developing a closed-loop control strategy and suggesting a reduced switch topology is much easier.

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Abbreviations

The following abbreviations are used in this manuscript:

HSISC	Hybrid switched inductor and switched capacitor
DC–DC	Direct Current to Direct Current
V2G	Vehicle-to-grid
SI	Switched inductor
SC	Switched capacitor
VL	Voltage lift
MS	Multi-stage
CL	Coupled inductors
HFT	High-frequency transformer
SEPIC	Single-Ended Primary-Inductor Converter
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PWM	Pulse Width Modulation
PSIM	Power Electronics Simulation (software used for simulation results)
EMI	Electromagnetic Interference
ESR	Equivalent series resistance

Appendix A

Appendix A.1 Experimental Results

Table A1 presents the voltage across the switch observed as a part of the simulation studies during ON and OFF states. The switch voltages are presented for duty ratios of 0.2, 0.3, 0.4, 0.5 and 0.6. The mathematical formulation for voltage stress for each switch is also presented in this table. The mathematical equation for voltage stress will be particularly useful for selecting the switch.

Table A1. Voltage stress for switches of the proposed converter.

Switch	Duty Ratio	ON State (V)	OFF State (V)	Voltage Stress
D_{L1}	0.2	0	−5	$\frac{V_{in}-V_{C1}}{2}$
	0.3	0	−8.56	
	0.4	0	−13.35	
	0.5	0	−20	
	0.6	0	−30	
D_{L2}	0.2	0	−5	$\frac{V_{in}-V_{C1}}{2}$
	0.3	0	−8.56	
	0.4	0	−13.35	
	0.5	0	−20	
	0.6	0	−30	
D_{L3}	0.2	−20	0	$-V_{in}$
	0.3	−20	0	
	0.4	−20	0	
	0.5	−20	0	
	0.6	−20	0	
Q_{Bp}	0.2	0	30	V_{C1}
	0.3	0	37.15	
	0.4	0	46.74	
	0.5	0	60	
	0.6	0	80	
$Q_{C1} - D_{C1}$	0.2	−30	0	$-V_{C1}$
	0.3	−37.15	0	
	0.4	−46.74	0	
	0.5	−60	0	
	0.6	−80	0	
Q_C	0.2	0	30	V_{C1}
	0.3	0	37.15	
	0.4	0	46.74	
	0.5	0	60	
	0.6	0	80	
$Q_{C2} - D_{C22}$	0.2	−30	0	$-V_{C1}$
	0.3	−37.15	0	
	0.4	−46.74	0	
	0.5	−60	0	
	0.6	−80	0	
Q_o	0.2	0	30	V_{C1}
	0.3	0	37.15	
	0.4	0	46.74	
	0.5	0	60	
	0.6	0	80	
D_{Lo}	0.2	−60	0	$-2V_{C1}$
	0.3	−74.4	0	
	0.4	−93.34	0	
	0.5	−120	0	
	0.6	−160	0	

Appendix A.2 Power Loss and Efficiency Calculation

Table A2 presents the conduction and switching loss for each switch and diode. Also, total losses are shown in this table. In this table, x is the number of the particular IGBT or diode.

I_L is the average current of inductor L_1 .

I_o is the average output current.

ΔI_L is the peak-to-peak ripple in current flowing through inductor L_1 .

ΔI_{Lo} is the peak-to-peak ripple in current flowing through inductor L_o .

V_{CE0x} is the threshold voltage of the x^{th} IGBT.

R_{CEx} is the dynamic ON-state resistance of the x^{th} IGBT.

V_{Fx} is the forward voltage drop of the x^{th} diode.

R_{Dx} is the dynamic ON-state resistance of the x^{th} diode.

E_{ONx} and E_{OFFx} are the turn-ON and turn-OFF energy losses of the x^{th} IGBT.

E_{rrx} is the reverse recovery energy of the x^{th} diode.

I_{avgx} is the average current of the x^{th} diode or x^{th} IGBT.

I_{rmsx} is the rms current of the x^{th} diode or x^{th} IGBT.

f_{sw} is the switching frequency.

Table A2. Power loss computation for the proposed converter.

Device No. (x)	Device	Average Current I_{avgx}	RMS Current I_{rmsx}	Conduction Loss	Switching Loss
1	Q_{Bp}	$2D I_L$	$2\sqrt{\{D(I_L^2 + \Delta I_L^2/12)\}}$	$P_{condx} = V_{CE0x} \cdot I_{avgx} + R_{CEx} \cdot I_{rmsx}^2$	$P_{swx} = f_{sw}(E_{ONx} + E_{OFFx})$
2	Q_C	$D I_o$	$\sqrt{\{D(I_o^2 + \Delta I_{Lo}^2/12)\}}$	$P_{condx} = V_{CE0x} \cdot I_{avgx} + R_{CEx} \cdot I_{rmsx}^2$	$P_{swx} = f_{sw}(E_{ONx} + E_{OFFx})$
3	Q_{C1}	$(1-D) I_L$	$\sqrt{\{(1-D)(I_L^2 + \Delta I_L^2/12)\}}$	$P_{condx} = V_{CE0x} \cdot I_{avgx} + R_{CEx} \cdot I_{rmsx}^2$	$P_{swx} = f_{sw}(E_{ONx} + E_{OFFx})$
4	Q_{C2}	$(1-D) I_L/2$	$\sqrt{\{(1-D)(I_L^2 + \Delta I_L^2/12)\}}$	$P_{condx} = V_{CE0x} \cdot I_{avgx} + R_{CEx} \cdot I_{rmsx}^2$	$P_{swx} = f_{sw}(E_{ONx} + E_{OFFx})$
5	Q_o	$D I_o$	$\sqrt{\{D(I_o^2 + \Delta I_{Lo}^2/12)\}}$	$P_{condx} = V_{CE0x} \cdot I_{avgx} + R_{CEx} \cdot I_{rmsx}^2$	$P_{swx} = f_{sw}(E_{ONx} + E_{OFFx})$
6	D_{L1}	$D I_L$	$\sqrt{\{D(I_L^2 + \Delta I_L^2/12)\}}$	$P_{condx} = V_{Fx} \cdot I_{avgx} + R_{Dx} \cdot I_{rmsx}^2$	$P_{rrx} = E_{rrx} \cdot f_{sw}$
7	D_{L2}	$D I_L$	$\sqrt{\{D(I_L^2 + \Delta I_L^2/12)\}}$	$P_{condx} = V_{Fx} \cdot I_{avgx} + R_{Dx} \cdot I_{rmsx}^2$	$P_{rrx} = E_{rrx} \cdot f_{sw}$
8	D_{L3}	$(1-D) I_L$	$\sqrt{\{(1-D)(I_L^2 + \Delta I_L^2/12)\}}$	$P_{condx} = V_{Fx} \cdot I_{avgx} + R_{Dx} \cdot I_{rmsx}^2$	$P_{rrx} = E_{rrx} \cdot f_{sw}$
9	D_{C1}	$(1-D) I_L/2$	$\sqrt{\{(1-D)(I_L^2 + \Delta I_L^2/12)\}}$	$P_{condx} = V_{Fx} \cdot I_{avgx} + R_{Dx} \cdot I_{rmsx}^2$	$P_{rrx} = E_{rrx} \cdot f_{sw}$
10	D_{C2}	$(1-D) I_L/2$	$\sqrt{\{(1-D)(I_L^2 + \Delta I_L^2/12)\}}$	$P_{condx} = V_{Fx} \cdot I_{avgx} + R_{Dx} \cdot I_{rmsx}^2$	$P_{rrx} = E_{rrx} \cdot f_{sw}$
11	D_{C22}	$(1-D) I_L/2$	$\sqrt{\{(1-D)(I_L^2 + \Delta I_L^2/12)\}}$	$P_{condx} = V_{Fx} \cdot I_{avgx} + R_{Dx} \cdot I_{rmsx}^2$	$P_{rrx} = E_{rrx} \cdot f_{sw}$
12	D_{Co}	$D I_o$	$\sqrt{\{D(I_o^2 + \Delta I_{Lo}^2/12)\}}$	$P_{condx} = V_{Fx} \cdot I_{avgx} + R_{Dx} \cdot I_{rmsx}^2$	$P_{rrx} = E_{rrx} \cdot f_{sw}$
13	D_{Cx}	$D I_o$	$\sqrt{\{D(I_o^2 + \Delta I_{Lo}^2/12)\}}$	$P_{condx} = V_{Fx} \cdot I_{avgx} + R_{Dx} \cdot I_{rmsx}^2$	$P_{rrx} = E_{rrx} \cdot f_{sw}$
14	D_{Lo}	$(1-D) I_o$	$\sqrt{\{(1-D)(I_o^2 + \Delta I_{Lo}^2/12)\}}$	$P_{condx} = V_{Fx} \cdot I_{avgx} + R_{Dx} \cdot I_{rmsx}^2$	$P_{rrx} = E_{rrx} \cdot f_{sw}$
$\tau = 100 \times P_O / P_{in} = 100 \times P_O / (P_O + \text{Total Losses})$ $\text{Total Losses} = \sum_{x=1}^{14} P_{condx} + \sum_{x=1}^5 P_{swx} + \sum_{x=6}^{14} P_{rrx}$					

Appendix A.3 Voltage Drop Calculation

Equations (A1)–(A5) present the voltage equations for voltage drops due to the MOSFET on-state resistance, body-diode forward voltage, inductor winding resistance, capacitor equivalent series resistance, and equivalent wiring parasitic resistance.

The non-ideal voltage equations have been derived separately for both operating modes by considering the actual current conduction paths of the proposed HSISC buck–boost converter. These equations are then used to estimate the voltage reduction introduced by each conducting semiconductor device and passive parasitic element using the corresponding datasheet values together with the experimentally measured operating currents. Based on the analysis, it is concluded that the inductor winding and the wiring are also significantly contributing to the voltage drop.

Voltage equations considering parasitic elements are given below.

Mode 1:

$$V_L = V_{in} - V_F - \frac{I_{in}}{2}(r_D + R_L + R_{w1}) - V_{in}(R_{DS(on)} + R_{w2}) \quad (A1)$$

$$V_o = 2V_C - I_{Lo}(2R_{DS(on)} + 2R_{ESR} + R_{w3}) - 2V_F - r_D(I_{DCx} + I_{DCo}) - 2I_{Lo}R_{ESR} \quad (A2)$$

Mode 2:

$$V_{C1} = V_{in} - V_{L1} - V_{L2} - 2V_F - \frac{3}{2}I_{in}r_D - I_{in}R_{DS(on)} - I_{in}R_{w4} - \frac{1}{2}I_{in}R_{ESR} \quad (A3)$$

$$V_{C2} = V_{in} - V_{L1} - V_{L2} - 3V_F - \frac{3}{2}I_{in}r_D - \frac{3}{2}I_{in}R_{DS(on)} - I_{in}R_{w5} - \frac{1}{2}I_{in}R_{ESR} \quad (A4)$$

$$V_o = -V_{Lo} - V_F - I_{Lo}(r_D + I_{in}R_{w6}) \quad (A5)$$

Here, R_{w1} – R_{w6} represent the resistance of the inductor winding and the wiring and contact resistances encountered in the current path.

References

1. Venugopal, R.; Chandrasekar, B.; Savio, A.D.; Narayanamoorthi, R.; Aboras, K.M.; Kotb, H.; Ghadi, Y.Y.; Shouran, M.; Elgamli, E. Review on Unidirectional Non-Isolated High Gain DC–DC Converters for EV Sustainable DC Fast Charging Applications. *IEEE Access* **2023**, *11*, 78299–78338. [\[CrossRef\]](#)
2. Revathi, B.S.; Prabhakar, M. Non isolated high gain DC-DC converter topologies for PV applications—A comprehensive review. *Renew. Sustain. Energy Rev.* **2016**, *66*, 920–933. [\[CrossRef\]](#)
3. Yari, K.; Mojallali, H.; Shahalami, S.H. A New Coupled-Inductor-Based Buck–Boost DC–DC Converter for PV Applications. *IEEE Trans. Power Electron.* **2022**, *37*, 687–699. [\[CrossRef\]](#)
4. Nassary, M.; Vidal-Idiarte, E.; Calvente, J. AC/DC Four-Switches Boost Buck Converter for EV Battery Charging. In Proceedings of the IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Tallinn, Estonia, 14–16 June 2023; pp. 1–7.
5. Johnson, L.; Koshy, R.A. Photo Voltaic Application of Two Switch Enhanced Gain Buck Boost Converter in Buck Mode. In Proceedings of the 9th International Conference on Smart Computing and Communications (ICSCC), Kochi, Kerala, India, 17–19 August 2023; pp. 742–747.
6. Gholizadeh, H.; Salehi, M.; Rafiee, Z.; Afjei, E.; Hamzeh, M. A Transformer less Quadratic Buck-Boost Converter with Wide Range of Output Voltage and Low Switch Stresses. In Proceedings of the 2020 11th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC), Tehran, Iran, 4–6 February 2020; pp. 1–6.
7. Alkhalidi, A.; Elkhateb, A.; Laverty, D. Voltage Lifting Techniques for Non-Isolated DC/DC Converters. *Electronics* **2023**, *12*, 718. [\[CrossRef\]](#)
8. Sarikhani, A.; Allahverdinejad, B.; Hamzeh, M. A Nonisolated Buck–Boost DC–DC Converter with Continuous Input Current for Photovoltaic Applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 804–811. [\[CrossRef\]](#)
9. Li, J.; Liu, J. A Novel Buck–Boost Converter with Low Electric Stress on Components. *IEEE Trans. Ind. Electron.* **2019**, *66*, 2703–2713. [\[CrossRef\]](#)

10. Banaei, M.R.; Bonab, H.A.F. A High Efficiency Nonisolated Buck–Boost Converter Based on ZETA Converter. *IEEE Trans. Ind. Electron.* **2020**, *67*, 1991–1998. [[CrossRef](#)]
11. Miao, S.; Wang, F.; Ma, X. A New Transformerless Buck–Boost Converter with Positive Output Voltage. *IEEE Trans. Ind. Electron.* **2016**, *63*, 2965–2975. [[CrossRef](#)]
12. Zhang, N.; Zhang, G.; See, K.W.; Zhang, B. A Single-Switch Quadratic Buck–Boost Converter with Continuous Input Port Current and Continuous Output Port Current. *IEEE Trans. Power Electron.* **2018**, *33*, 4157–4166. [[CrossRef](#)]
13. Banaei, M.R.; Ghabeli Sani, S. Analysis and Implementation of a New SEPIC-Based Single-Switch Buck–Boost DC–DC Converter with Continuous Input Current. *IEEE Trans. Power Electron.* **2018**, *33*, 10317–10325. [[CrossRef](#)]
14. Banaei, M.R.; Bonab, H.A.F. A Novel Structure for Single-Switch Nonisolated Transformerless Buck–Boost DC–DC Converter. *IEEE Trans. Ind. Electron.* **2017**, *64*, 198–205. [[CrossRef](#)]
15. Khuntia, M.R.; Veerachary, M. Extended Boosting Range-Based-Non-Isolated Buck-Boost Converters with Continuous Input Current and Common Grounded Structure. *IEEE J. Emerg. Sel. Top. Ind. Electron.* **2024**, *5*, 813–826. [[CrossRef](#)]
16. Veerachary, M.; Khuntia, M.R. Design and Analysis of Two-Switch-Based Enhanced Gain Buck–Boost Converters. *IEEE Trans. Ind. Electron.* **2022**, *69*, 3577–3587. [[CrossRef](#)]
17. Forouzesh, M.; Siwakoti, Y.P.; Gorji, S.A.; Blaabjerg, F.; Lehman, B. Step-Up DC–DC Converters: A Comprehensive Review of Voltage-Boosting Techniques, Topologies, and Applications. *IEEE Trans. Power Electron.* **2017**, *32*, 9143–9178. [[CrossRef](#)]
18. Tofoli, F.L.; Pereira, D.D.C.; Josias De Paula, W.; Oliveira Júnior, D.D.S. Survey on non-isolated high-voltage step-up dc–dc topologies based on the boost converter. *IET Power Electron.* **2015**, *8*, 2044–2057. [[CrossRef](#)]
19. Forouzesh, M.; Siwakoti, Y.P.; Gorji, S.A.; Blaabjerg, F.; Lehman, B. A survey on voltage boosting techniques for step-up DC–DC converters. In Proceedings of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 18–22 September 2016; pp. 1–8.
20. Tarzamni, H.; Gohari, H.S.; Sabahi, M.; Kyyrä, J. Nonisolated High Step-Up DC–DC Converters: Comparative Review and Metrics Applicability. *IEEE Trans. Power Electron.* **2024**, *39*, 582–625. [[CrossRef](#)]

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