entropy

MDPI

Article

Electronic Implementation of a Deterministic Small-World Network: Synchronization and Communication

Daniel Reyes-De la Cruz [1], Rodrigo Méndez-Ramírez [1], Adrian Arellano-Delgado [2,3,*] and César Cruz-Hernández [1]

[1] Electronics and Telecommunication Department, Scientific Research and Advanced Studies Center of Ensenada, Ensenada 22860, Mexico
[2] National Council of Science and Technology, Ciudad de Mexico 03940, Mexico
[3] Engineering, Architecture and Design Faculty, Autonomous University of Baja California, Ensenada 22860, Mexico
* Correspondence: adrian.arellano@uabc.edu.mx; Tel.: +52-(646)175-07-00 (ext. 64307)

Abstract: In this paper, synchronization and encrypted communication transmissions of analog and digital messages in a deterministic small-world network (DSWN) are presented. In the first instance, we use a network with 3 coupled nodes in a nearest-neighbor (NN) topology, then the amount of nodes is increased until reaching a DSWN with 24 nodes. The synchronization and encrypted communication transmissions using a DSWN are presented experimentally by using Chua's chaotic circuit as node, in both analog and digital electronic implementations, where for the continuous version (CV) we use operational amplifiers (OA), and in the discretized version (DV) we use Euler's numerical algorithm implemented in an embedded system by using an Altera/Intel FPGA and external digital-to-analog converters.

Keywords: deterministic network; small-world network; communication; synchronization; FPGA; Chua's chaotic circuit

Citation: Reyes-De la Cruz, D.; Méndez-Ramírez, R.; Arellano-Delgado, A.; Cruz-Hernández, C. Electronic Implementation of a Deterministic Small-World Network: Synchronization and Communication. *Entropy* **2023**, *25*, 709. https://doi.org/10.3390/e25050709

Academic Editor: Stanisław Drożdż

Received: 17 February 2023
Revised: 10 March 2023
Accepted: 14 March 2023
Published: 25 April 2023

1. Introduction

Many real-life phenomena, such as biological networks, electrical networks, social networks, etc., are modeled as complex dynamical networks that follow certain general and robust patterns, for example, a large number of interconnections among the nodes that integrate the networks. In some cases, the nodes work as team to achieve objectives that would be difficult to reach for a single node. The nodes that integrate these types of networks are modeled as dynamic systems by non-linear differential equations, linear piece-wise, or chaotic maps, and the interactions among the nodes present instantaneous behaviors or with time delays. The synchronization state can converge to a periodic or chaotic trajectories which depend on the initial conditions and/or the parameter values, where in some cases multi-stability can occur.

Recent studies have attempted modeling the behaviors of a particular type of networks, referred to as small-world (SW) networks, with *Watts* and *Strogatz* being pioneers in the study of these type of networks [1]. A model of an SW network starts with a NN topology network, and subsequently, based on a probability p (represented in the interval $0 \leq p \leq 1$), connections are added in the original NN network to obtain an SW network. An SW network presents two main characteristics: a high clustering coefficient and a low average path length. The current literature reports many papers related to SW networks, for example, see [2–7].

Furthermore, Comellas et al. in [8] present a deterministic SW model to streamline the flow of information in wireless communication networks. *Comellas* and *Sampels* present a deterministic SW network as an alternative to stochastic models in order to calculate

relevant parameters of the SW network by using a simplest method [9]. Zhang and Rong [10] present a deterministic model created by edge iterations. In 2010, Zhang et al. published a deterministic model with different weights connections in order to improve the performance in the transmission of packets in communication networks, see [11]. Given the random nature of small-world stochastic networks, they have the disadvantage that the resulting complex network topology is unknown when the number of nodes or connections are varied. For this reason, the DSWN presents an advantageous alternative over the stochastic models, since they allow us a direct calculation of the relevant parameters of the network, for example, average degree, grade distribution, clustering coefficient, average path length, and diameter of the network. On the other hand, the synchronization of complex systems has been studied in regular, irregular, and random networks, see [12–15]; therefore, this study seeks to achieve synchronization in DSWNs.

This work is organized as follows: In Section 2, a brief review on synchronization of complex networks is presented. Section 3 describes the used algorithm to generate a DSWN. In Section 4, synchronization of a DSWN network using Chua's chaotic circuit as node is presented. Section 5 describes the experimental synchronization and communication of a DSWN by using six Chua's circuits as nodes, where the electronic representation in its CV is implemented using operational amplifiers (OA) in order to develop private communications. Section 6 describes the experimental synchronization and communication of a DSWN by using six Chua's circuits as nodes, where its DV is obtained using Euler's numerical algorithm, and a digital communication and its implementation are conducted by using an FPGA as the embedded system. Finally, in Section 7 a conclusion is presented.

2. Brief Review on Synchronization of Complex Networks

2.1. Synchronization of Complex Network

We consider a complex network composed of N identical nodes, linearly and diffusively coupled through the first state of each node. In this network, each node constitutes a *n-dimensional* dynamical system, described as follows:

$$\dot{\mathbf{x}}_i = f(\mathbf{x}_i) + \mathbf{u}_i, \quad i = 1, 2, \ldots, N, \tag{1}$$

where $\mathbf{x}_i = (x_{i1},\ x_{i2},\ \ldots,\ x_{in})^T \in \mathbb{R}^n$ are the state variables of the node i, $\mathbf{u}_i = (u_{i1}, 0,\ \ldots, 0)^T \in \mathbb{R}^n$ is the input signal of the node i, and is defined by

$$\mathbf{u}_i = c \sum_{j=1}^{N} a_{ij} \Gamma \mathbf{x}_j, \quad i = 1, 2, \ldots, N, \tag{2}$$

the constant $c > 0$ represents the *coupling strength* of the complex network and $\Gamma \in \mathbb{R}^{n \times n}$ is a constant $0 - 1$ matrix linking coupled state variables. For simplicity, we assume that $\Gamma = diag(r_1,\ r_2, \ldots, r_n)$ is a diagonal matrix with $r_i = 1$ for a particular i and $r_j = 0$ for $j \neq i$, this means that two coupled nodes are linked through their $i - th$ state variables, whereas $\mathbf{A} = (a_{ij}) \in \mathbb{R}^{N \times N}$ is the *coupling matrix*, which represents the coupling topology of the complex network. If there is a connection between node i and node j, then $a_{ij} = 1$; otherwise $a_{ij} = 0$ for $i \neq j$. The diagonal elements of coupling matrix $\mathbf{A}$ are defined as

$$a_{ii} = -\sum_{j=1,\ j \neq i}^{N} a_{ij} = -\sum_{j=1,\ j \neq i}^{N} a_{ji}, \quad i = 1, 2, \ldots, N, \tag{3}$$

If the *degree* of node i is d_i, then $d_i = -a_{ii}$, $i = 1, 2, \ldots, N$.

Now, suppose that the complex network (1) and (2) is connected without isolated clusters. Then, $\mathbf{A}$ is a symmetric irreducible matrix. In this case, it can be shown that zero is an eigenvalue of $\mathbf{A}$ with multiplicity 1 and all the other eigenvalues of $\mathbf{A}$ are strictly negative [16,17].

Synchronization states of nodes in complex systems can be characterized by the non-zero eigenvalues of **A**. The complex network (1) and (2) is said to achieve (asymptotically) synchronization if [17]

$$\mathbf{x}_1(t) = \mathbf{x}_2(t) = \ \ldots \ = \mathbf{x}_N(t), \text{ as } t \to \infty. \tag{4}$$

The diffusive coupling condition (3) guarantees that the synchronization state is a solution, $\mathbf{s}(t) \in \mathbb{R}^n$, of an isolated node, that is

$$\dot{\mathbf{s}}(t) = f(\mathbf{s}(t)), \tag{5}$$

where $\mathbf{s}(t)$ can be an *equilibrium point*, a *periodic orbit*, or a *chaotic attractor*. Thus, stability of the synchronization state,

$$\mathbf{x}_1(t) = \mathbf{x}_2(t) = \ \ldots \ = \mathbf{x}_N(t) = \mathbf{s}(t), \tag{6}$$

of complex network (1) and (2) is determined by the dynamics of an isolated node, the coupling strength c, the inner linking matrix Γ, and the coupling matrix **A**.

The dynamics of an isolated node are determined by $\bar{d}$, which is a positive constant, such that zero is an exponentially stable point, the n-dimensional isolated system is determined by

$$\begin{cases} \dot{z}_1 = f_1(z) - \bar{d}z_1, \\ \dot{z}_2 = f_2(z), \\ \quad \vdots \\ \dot{z}_n = f_n(z). \end{cases} \tag{7}$$

Note that system (7) corresponds to the mathematical model of an *isolated node* with state feedback $-\bar{d}z_1$.

2.2. Synchronization Conditions

The following theorem gives the conditions to achieve synchronization of the network (1) and (2) as is established in (4).

Theorem 1 ([16,17]). *Consider the dynamical network (1) and (2). Let*

$$0 = \lambda_1 > \lambda_2 \geq \lambda_3 \geq \cdots \geq \lambda_N \tag{8}$$

be the eigenvalues of a coupling matrix **A**. *Suppose that there exists an* $n \times n$, $D > 0$, *and two constants* $\bar{d} < 0$ *and* $\tau > 0$, *such that*

$$[Df(\mathbf{s}(t)) + d\Gamma]^T\mathbf{D} + \mathbf{D}[Df(\mathbf{s}(t)) + d\Gamma] \leq -\tau\mathbf{I}_n \tag{9}$$

for all $d \leq \bar{d}$, *where* $I_n \in \mathbb{R}^{n\times n}$ *is an unit matrix. If, moreover,*

$$c\lambda_2 \leq \bar{d}, \tag{10}$$

then the synchronization state (6) of dynamical network (1) and (2) is exponentially stable.

Since $\lambda_2 < 0$ and $\bar{d} < 0$, inequality (10) is equivalent to

$$c \geq \left|\frac{\bar{d}}{\lambda_2}\right|. \tag{11}$$

Therefore, the synchronizability of (1) and (2) with respect to a specific coupling topology can be characterized by the second-largest eigenvalue of **A**.

3. Generator Algorithm of DSWN

In this work, we use the algorithm introduced by Zhongzhi Zhang et al. in 2006, see [10]. A network is denoted as $N(l)$ after the evolution of l iterations. In this algorithm, the network grows through an iterative procedure. The algorithm is as follows: for $l = 0$ the initial network $N(0)$ is a triangle that contains three coupled nodes in an NN topology, For $l = 1$, the network $N(l)$ is obtained from $N(l-1)$ by adding a new node for each connection created in the step $l-1$ and connecting it to the nearest nodes. The algorithm can be summarized as follows: in each step iteration, for each edge that exists in the network, a new node is added and connected to its two nearest neighbors, see details in [10].

Furthermore, according to [10], the total number of nodes $N_T(l)$ for each iteration l is as follows:

$$N_T(l) = N_T(0) \cdot 2^l, \tag{12}$$

where $N_T(0) = 3$.

With respect to the number of edges $N_e(l)$ added to each iteration, we have the following

$$N_e(l) = N_e(0) \cdot 2^{l+1} - 3, \tag{13}$$

where $N_e(0) = 3$.

Taking into consideration (12) and (13), the average node degree $\langle k \rangle$ of the network for each iteration l is as follows:

$$\langle k \rangle = 2 \cdot \frac{Ne}{N_T} = \frac{2 \cdot (N_e(0) \cdot 2^{l+1} - 3)}{N_T(0) \cdot 2^l} = 4\left(1 - \frac{1}{2^{l+1}}\right). \tag{14}$$

Generally, SW networks can be identified by three main properties: (*i*) the average path length does not increase logarithmically with the size of the network or with the increase in the number of nodes, but it grows or decreases as the number of nodes varies; (*ii*) the average degree of nodes of the network is small, and (*iii*) the network has a high clustering coefficient.

4. Synchronization of a DSWN with Chaotic Chua's Circuits as Node

4.1. Chaotic Chua's Circuit

In this section, we describe the chaotic Chua's circuit that we use as node to construct the DSWNs, see [18]. The Chua's circuit consists of four linear elements (a resistor R, an inductor L, and two capacitors $C1$ and $C2$) and a non-linear element, which is described in [19]. In order to simulate the behavior of the Chua's circuit in a computer, we used the normalized version described below, see details in [20].

$$\begin{cases} \dot{x}_1 = \alpha(x_2 - x_1 - f(x_1)), \\ \dot{x}_2 = x_1 - x_2 + x_3, \\ \dot{x}_3 = -\beta x_2, \end{cases} \tag{15}$$

The non-linearity $f(x_1)$ is defined as

$$f(x_1) = bx_1 + \frac{1}{2}(a-b)(|x_1+1| - |x_1-1|), \tag{16}$$

where with parameter values $\alpha = 15.6$, $\beta = 28$, $a = -1.143$, and $b = -0.714$, Chua's circuit generates the chaotic behavior shown in Figure 1.

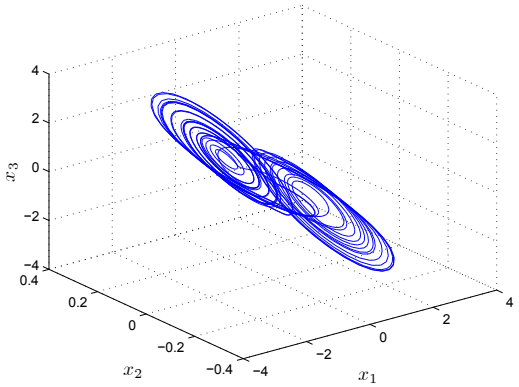

Figure 1. Chaotic attractor generated by the Chua's circuit (15) and (16).

For $\bar{d} = 2.3$ in (7), any isolated chaotic Chua's circuit (15) and (16) is stabilized, see [16,17]. The state equations for N Chua's circuits in complex dynamical networks according to (1) and (2) can be expressed as follows:

$$\begin{aligned} \dot{x}_{i1} &= \alpha(x_{i2} - x_{i1} - f(x_{i1})) + c\sum_{j=1}^{N}(a_{ij}\Gamma x_{j1}), \qquad i = 1, 2, \ldots, N, \\ \dot{x}_{i2} &= x_{i1} - x_{i2} + x_{i3}, \\ \dot{x}_{i3} &= -\beta x_{i2}, \end{aligned} \tag{17}$$

the non-linear functions $f(x_{i1})$, $i = 1, 2, \ldots, N$ are defined as

$$f(x_{i1}) = bx_{i1} + \frac{1}{2}(a-b)(|x_{i1}+1| - |x_{i1}-1|). \tag{18}$$

4.2. Synchronization of 24 Chaotic Chua's Circuits in a DSWN

Now, we present the synchronization of a DSWN for an iteration $l = 3$, which is formed by $N = 24$ chaotic Chua's circuits. The second eigenvalue $\lambda_2 = -0.5501$ of the network $N(3)$ is used and the minimum coupling strength (obtained from (11)) to synchronize the network is obtained as follows:

$$c \geq \frac{|2.3|}{|-0.5501|}. \tag{19}$$

Numerical Simulations of DSWN with 24 Chaotic Chua's Circuits

For the numerical simulations with $N = 24$ chaotic Chua's circuits, the values of initial conditions in the numerical simulations are chosen as follows:

$$\begin{aligned} &0 \leq x_{i1}(0) \leq 1, \\ &0 \leq x_{i2}(0) \leq 1, \quad i = 1, 2, \ldots, 24. \\ &0 \leq x_{i3}(0) \leq 1, \end{aligned} \tag{20}$$

Figure 2 shows the synchronization error dynamics where we can see that the synchronization state for all nodes in the DSWN is convergent.

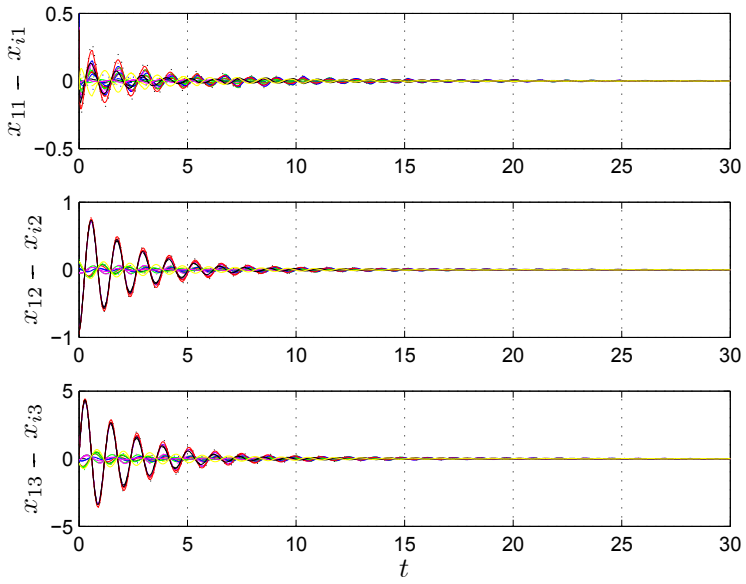

Figure 2. Synchronization error dynamics $x_{11} - x_{i1}$, $x_{12} - x_{i2}$, $x_{13} - x_{i3}$, $i = 1, 2, \ldots, 24$ of the chaotic Chua's circuits with $c = 30$, different colors are used for the sole purpose of differentiating the error synchronization signals.

5. Analog Synchronization of Six Chua's Circuits in a DSWN

This section presents an experimental implementation by using OA and analog components for a potential application with electrical circuits in private communications, by way of illustration we implemented a DSWN for $l = 1$ conformed by the following:

$$N1\begin{cases} \dot{x}_{11} = \alpha(x_{12} - x_{11} - f(x_{11})) + u_1, \\ \dot{x}_{12} = x_{11} - x_{12} + x_{13}, \\ \dot{x}_{13} = -\beta x_{12}, \end{cases} \tag{21}$$

$$f(x_{11}) = bx_{11} + \frac{1}{2}(a-b)(|x_{11}+1| - |x_{11}-1|) \tag{22}$$

$$N2\begin{cases} \dot{x}_{21} = \alpha(x_{22} - x_{21} - f(x_{21})) + u_2, \\ \dot{x}_{22} = x_{21} - x_{22} + x_{23}, \\ \dot{x}_{23} = -\beta x_{22}, \end{cases} \tag{23}$$

$$f(x_{21}) = bx_{21} + \frac{1}{2}(a-b)(|x_{21}+1| - |x_{21}-1|) \tag{24}$$

$$N3\begin{cases} \dot{x}_{31} = \alpha(x_{32} - x_{31} - f(x_{31})) + u_3, \\ \dot{x}_{32} = x_{31} - x_{32} + x_{33}, \\ \dot{x}_{33} = -\beta x_{32}, \end{cases} \tag{25}$$

$$f(x_{31}) = bx_{31} + \frac{1}{2}(a-b)(|x_{31}+1| - |x_{31}-1|) \tag{26}$$

$$N4\begin{cases} \dot{x}_{41} = \alpha(x_{42} - x_{41} - f(x_{41})) + u_4, \\ \dot{x}_{42} = x_{41} - x_{42} + x_{43}, \\ \dot{x}_{43} = -\beta x_{42}, \end{cases} \tag{27}$$

$$f(x_{41}) = bx_{41} + \frac{1}{2}(a-b)(|x_{41}+1| - |x_{41}-1|) \tag{28}$$

$$N5\begin{cases} \dot{x}_{51} = \alpha(x_{52} - x_{51} - f(x_{51})) + u_5, \\ \dot{x}_{52} = x_{51} - x_{52} + x_{53}, \\ \dot{x}_{53} = -\beta x_{52}, \end{cases} \tag{29}$$

$$f(x_{51}) = bx_{51} + \frac{1}{2}(a-b)(|x_{51}+1| - |x_{51}-1|) \tag{30}$$

$$N6\begin{cases} \dot{x}_{61} = \alpha(x_{62} - x_{61} - f(x_{61})) + u_6, \\ \dot{x}_{62} = x_{61} - x_{62} + x_{63}, \\ \dot{x}_{63} = -\beta x_{62}, \end{cases} \tag{31}$$

$$f(x_{61}) = bx_{61} + \frac{1}{2}(a-b)(|x_{61}+1| - |x_{61}-1|) \tag{32}$$

where the inputs signals u_i, $i = 1, 2, \ldots, 6$ are as follows:

$$\begin{aligned} u_1 &= -4x_1 + x_2 + x_3 + x_4 + x_6, \\ u_2 &= x_1 - 4x_2 + x_3 + x_4 + x_5, \\ u_3 &= x_1 + x_2 - 4x_3 + x_5 + x_6, \\ u_4 &= x_1 + x_2 - 2x_4, \\ u_5 &= x_2 + x_3 - 2x_5, \\ u_6 &= x_1 + x_3 - 2x_6 \end{aligned} \tag{33}$$

with parameter values $\alpha = 15.6$, $\beta = 28$, $a = -1.143$, and $b = -0.714$. Figures 3–5 show the electronic diagrams of the six Chua's circuits corresponding to the nodes (21)–(32).

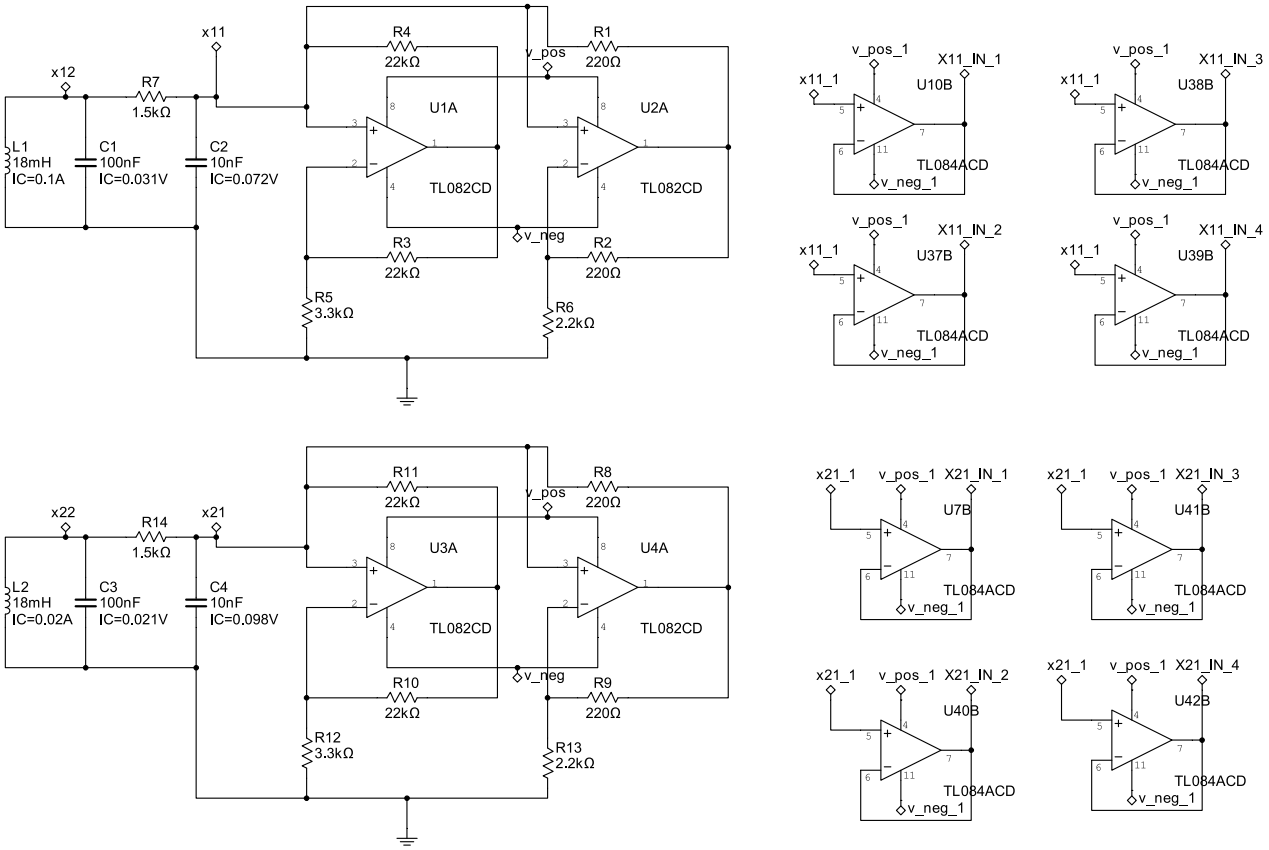

Figure 3. Electrical diagram of the nodes $N1$–$N2$.

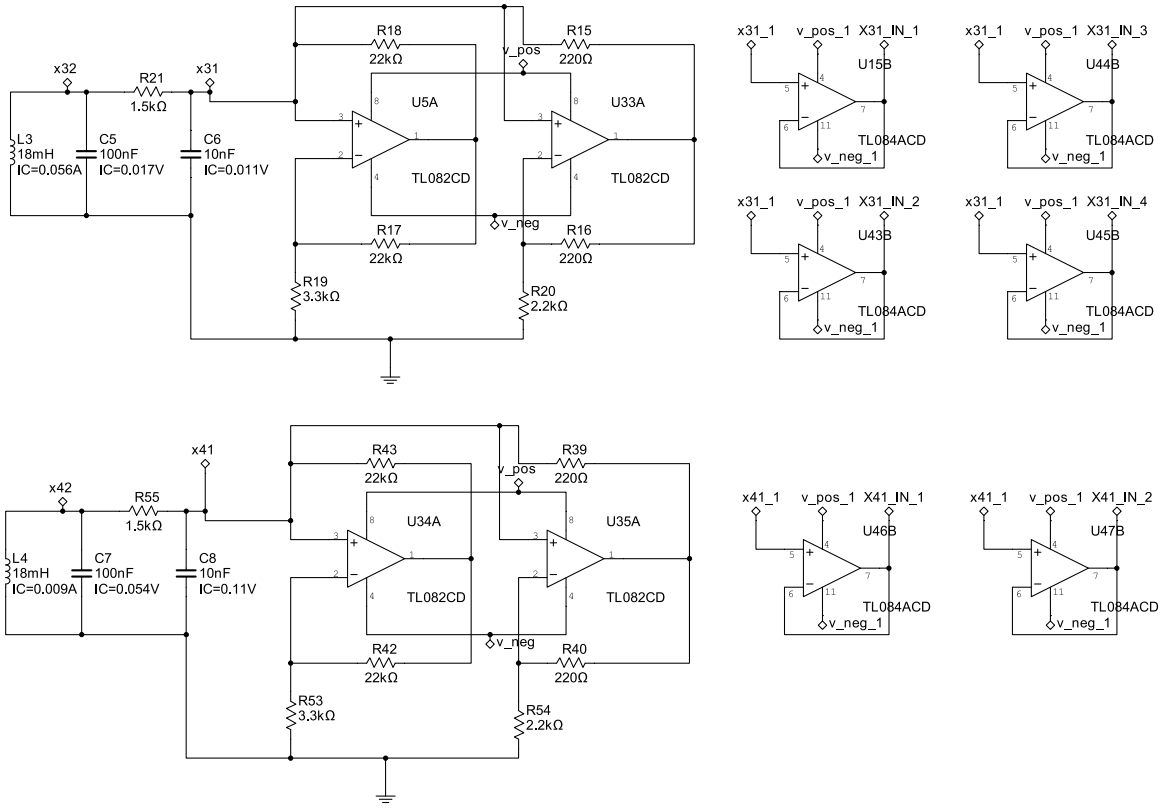

Figure 4. Electrical diagram of the nodes *N*3–*N*4.

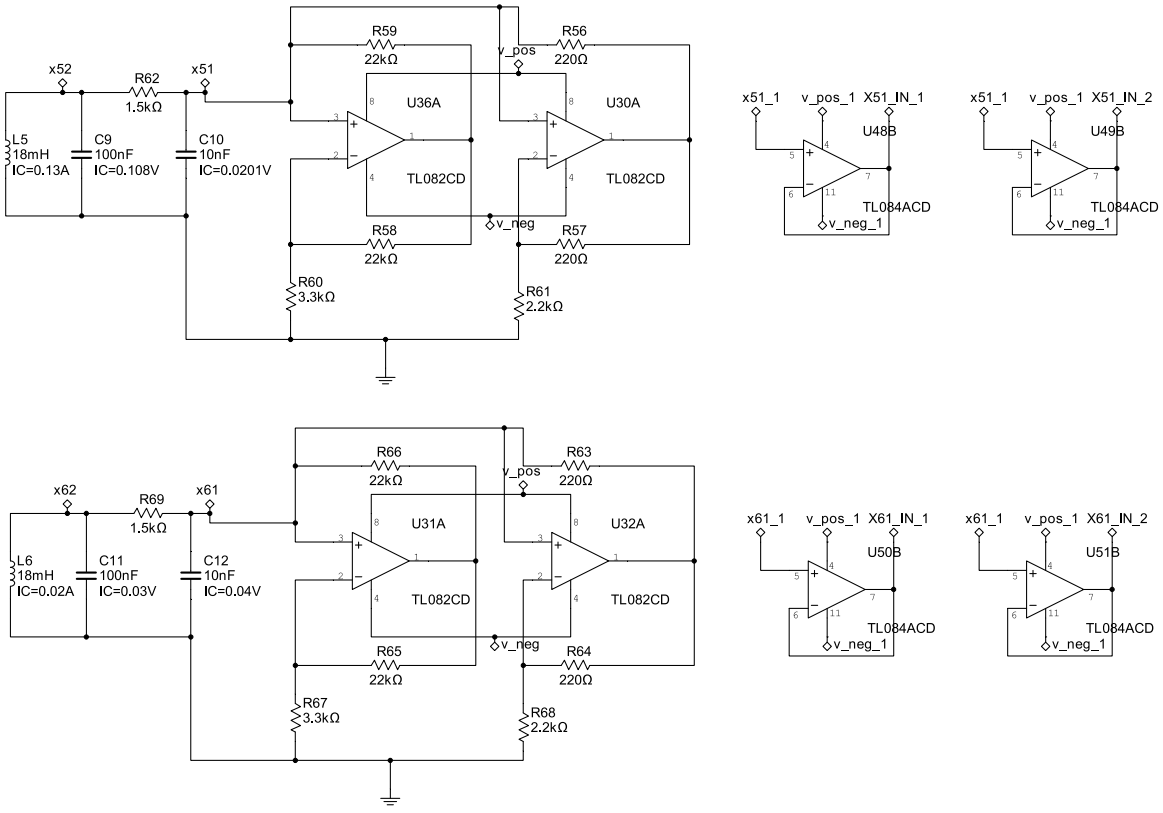

Figure 5. Electrical diagram of the nodes *N*5–*N*6.

The control circuits corresponding to Equation (33) are shown in Figures 6–8.

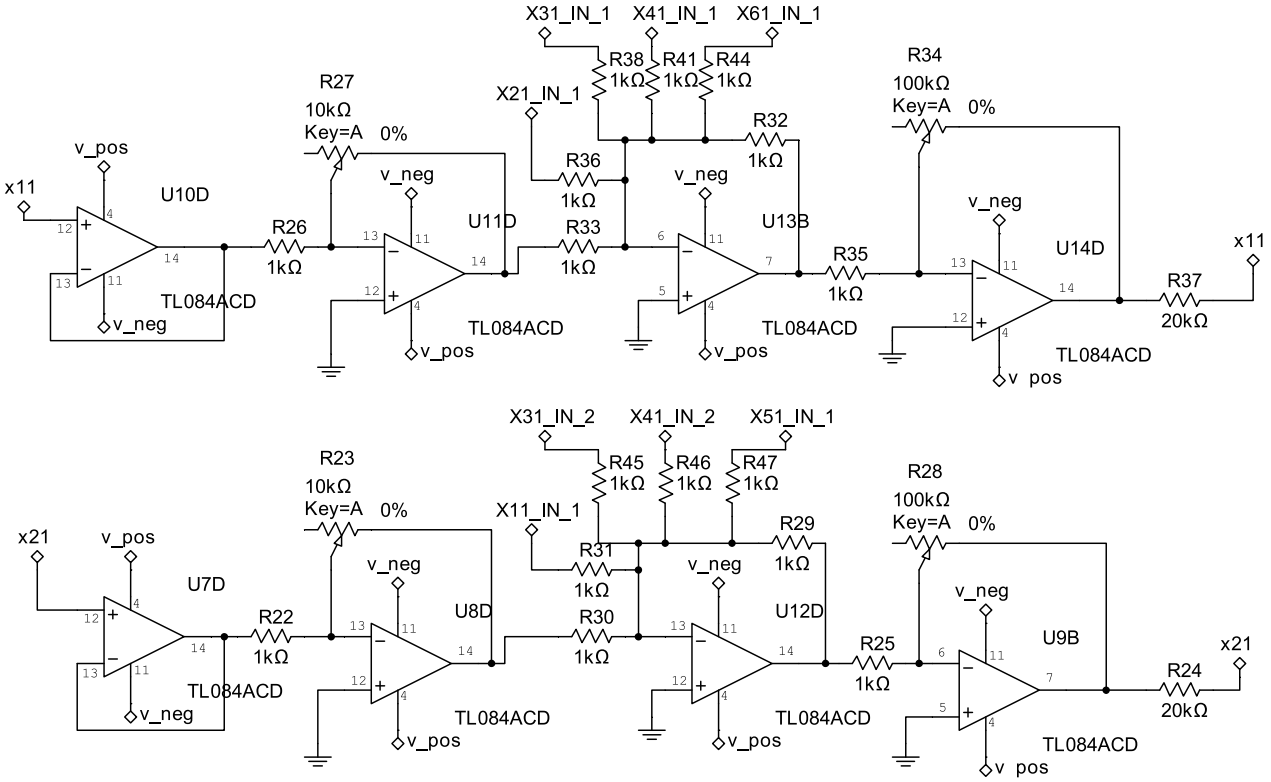

Figure 6. Electrical diagram of the controllers u_1 and u_2.

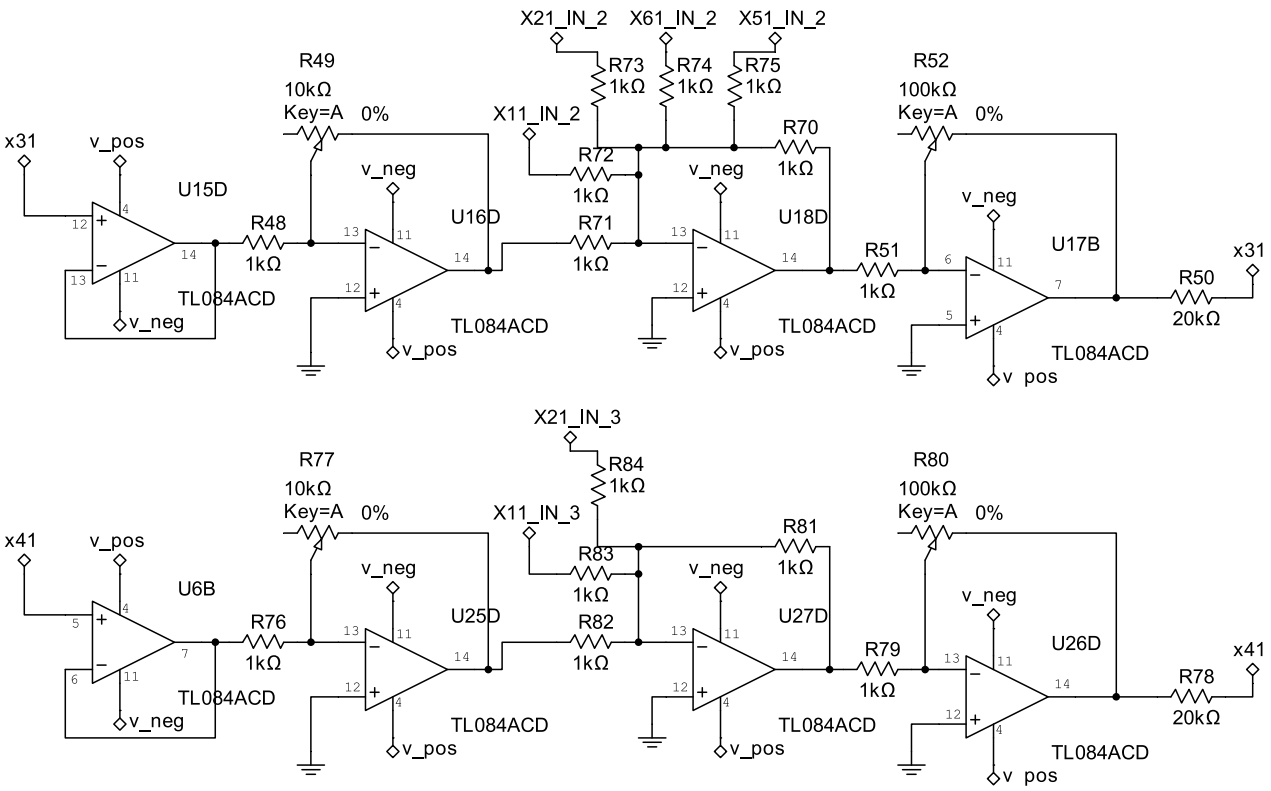

Figure 7. Electrical diagram of the controllers u_3 and u_4.

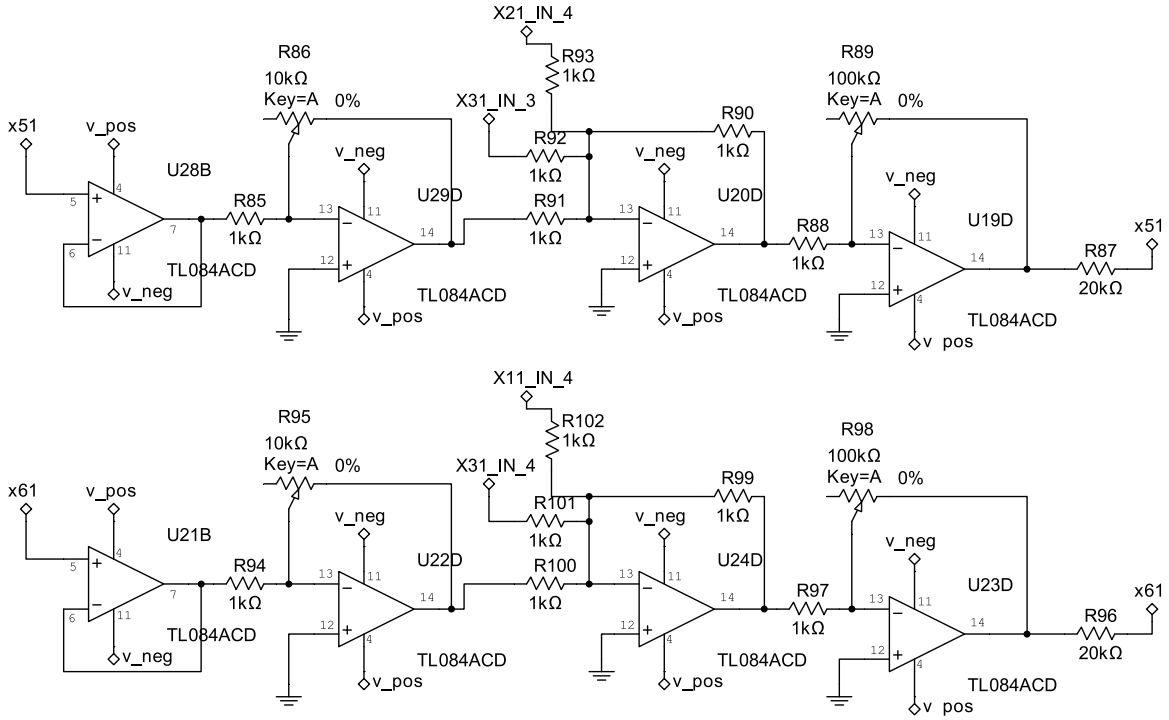

Figure 8. Electrical diagram of the controllers u_5 and u_6.

Figure 9a,b show the phase planes of the states x_{11} versus x_{i1} and x_{12} versus x_{i2} of the chaotic Chua's circuits, with $i = 1, 2, \ldots, 6$, respectively.

(a) (b)

Figure 9. (**a**) Phase portrait of states x_{11} versus x_{i1}, (**b**) phase portrait of states x_{12} versus x_{i2} for 6 chaotic Chua's circuits.

5.1. Experimental Application for analog Encryption in a DSWN

This section presents the chaotic encryption and transmission of information using a DSWN with six Chua's circuits, the encryption is achieved using the network of $N(1)$ previously synchronized. Once the network is synchronized, encrypted analog messages can be transmitted (Tx) from any node in the network and can be received (Rx) and decrypted in any other node that integrates the network. By way of illustration, the following example is presented: the message $m = sin(2\pi ft)$, with $f = 1$ khz, is encrypted in the node $N4$ configured as Tx, and it is recovered in the node $N6$ configured as Rx. The communication scheme consists of adding the chaotic dynamics of the x_{41} state to the message m, therefore the resulting cryptogram is $Z_d = x_{41} + m$, see Figure 10a, then, the Rx node $N6$ uses the chaotic dynamics of the x_{61} state to recover the encrypted message, which results in the recovered message $\bar{m} = Z_d - x_{61}$, see Figure 10b.

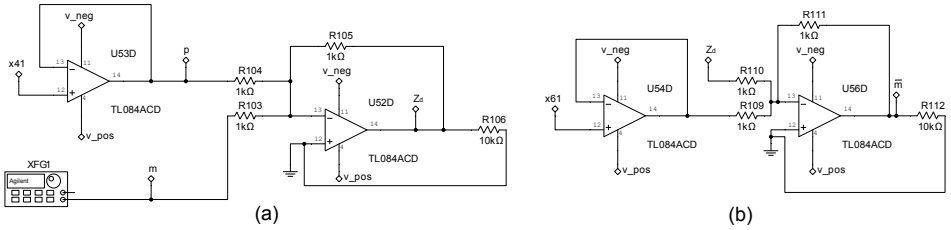

Figure 10. (**a**) Electrical diagram to generate a Z_d cryptogram and send it from node Tx ($N4$), (**b**) electrical diagram to recover the message $\bar{m}$ in the node Rx ($N6$).

In Figure 11a, the cryptogram $Z_d = x_{41} + m$ is presented in the frequency domain, whereas Figure 11b shows the original message $m = sin(2\pi ft)$ (green line) and the decrypted message $\bar{m} = Z_d - x_{61}$ (purple line). From Figure 11a, we can establish that the signal $m = sin(2\pi ft)$ is hidden in the chaotic carrier.

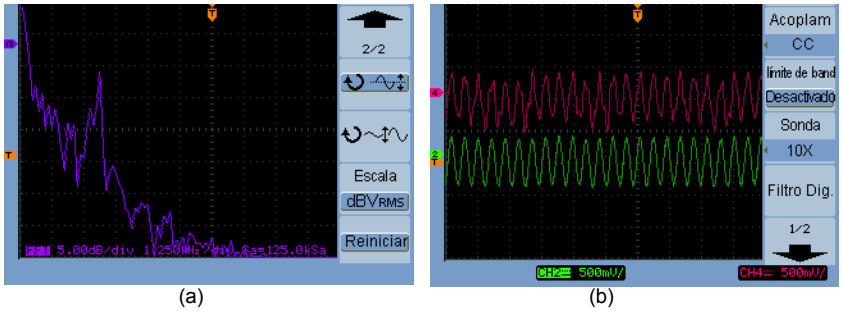

Figure 11. (**a**) Cryptogram in the frequency domain $Z_d = x_{41} + m$, (**b**) original message m (green line) in $N4$ and decrypted message $\bar{m}$ (purple line) in node $N6$.

5.2. Experimental Application for Bit Encryption in a DSWN

In this section, we conducted the encryption of a digitized image using the experimental implementation of the Chua's circuit. Figure 12 shows the electronic circuit for the encryption process by varying the resistance $R7$ using a microcontroller microchip $P16F84A$, where we chose node $N1$ as a Tx.

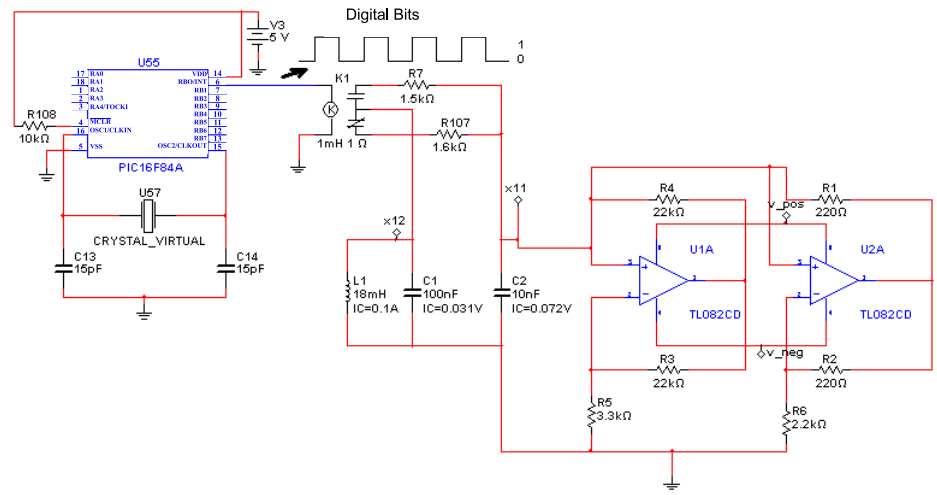

Figure 12. Node $N1$ as a Tx, $N2$ to $N6$ nodes remain unchanged.

The binary information of the scanned image was taken from [20]. Only unidirectional bits can be sent in this application, this is because the information flows from the Tx node $N1$ to the Rx nodes N_i, $i = 2, \ldots, 6$, where this is achieved by adding the electronic circuit of Figure 12 in the node that is selected as the Tx; the Rx nodes remain without modifications.

Figure 13a shows the message to be sent in green color (3 bytes) and the synchronization error between nodes $N1$ and $N5$ in (purple line), where a 1 binary represents synchrony between systems and a 0 binary represents no synchronization. In the synchrony error (purple signal), there are quite a few unwanted peaks due to the use of a mechanical relay. The synchrony error signal can be recovered using filters to clean the undesired peaks and comparators to restore the information to appropriate voltage levels, in this case the main idea is to show the digital encryption in a general way. Figure 13b shows the chaotic dynamics of the states x_{11} and x_{51}, it is observed that the dynamics are similar, this is the case when a binary 1 is sent from $N1$ to $N5$.

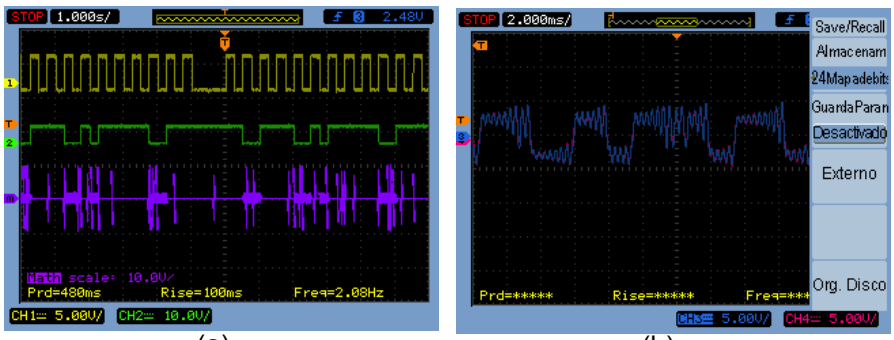

Figure 13. (**a**) Transmission of encrypted digital data using a DSWN: clock (yellow line), data (green line), and synchrony error (purple line); (**b**) chaotic dynamics of the states x_{11} and x_{51} when Tx sends a 1 binary from $N1$ to $N5$.

6. Digital Synchronization and Communication of a DSWN Implemented in FPGA

For the digital implementation, we used Euler's method to approximate the ordinary differential equations (ODEs) and to obtain the model proposed in (21)–(33). Euler's method is used in order to discretize a continuous system that is derived from Taylor's series, when the quadratic and upper order term are truncated [21,22], i.e., if we have the following equation

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}); \;\; \mathbf{x}(0) = \mathbf{x}_0, \;\; \mathbf{x} \in \mathbb{R}^n, \tag{34}$$

then the DV using Euler's method is given by

$$\mathbf{x}_{(k+1)} = \mathbf{x}_{(k)} + \tau \mathbf{f}(\mathbf{x}_{(k)}), \tag{35}$$

where τ is the step size and k is the iteration number that represents the time in discrete version. Euler's numerical algorithm (35) was considered to obtain the DV of the proposed DSWN (21)–(33) as follows:

$$ND1 \begin{cases} x_{11(k+1)} = x_{11(k)} + \tau(\alpha(x_{12(k)} - h(x_{11(k)})) \\ \qquad\qquad +k(-4x_{11(k)} + x_{21(k)} + x_{31(k)} + x_{41(k)} + x_{61(k)}), \\ x_{12(k+1)} = x_{12(k)} + \tau(x_{11(k)} - x_{12(k)} + x_{13(k)}), \\ x_{13(k+1)} = x_{13(k)} + \tau(-\beta x_{12(k)}). \end{cases} \tag{36}$$

$$h(x_{11(k)}) = m_1 x_{11(k)} + \frac{1}{2}(m_0 - m_1)(|x_{11(k)} + 1| - |x_{11(k)} - 1|), \tag{37}$$

$$ND2 \begin{cases} x_{21(k+1)} = x_{21(k)} + \tau(\alpha(x_{22(k)} - h(x_{21(k)})) \\ \qquad\qquad +k(x_{11(k)} - 4x_{21(k)} + x_{31(k)} + x_{41(k)} + x_{51(k)})), \\ x_{22(k+1)} = x_{22(k)} + \tau\Big(x_{21(k)} - x_{22(k)} + x_{23(k)}\Big), \\ x_{23(k+1)} = x_{23(k)} + \tau\Big(-\beta x_{22(k)}\Big). \end{cases} \tag{38}$$

$$h(x_{21(k)}) = m_1 x_{21(k)} + \frac{1}{2}(m_0 - m_1)(|x_{21(k)} + 1| - |x_{21(k)} - 1|), \tag{39}$$

$$ND3\begin{cases} x_{31(k+1)} = x_{31(k)} + \tau(\alpha(x_{32(k)} - h(x_{31(k)})) \\ \qquad\qquad +k(x_{11(k)} - x_{21(k)} - 4x_{31(k)} + x_{51(k)} + x_{61(k)})), \\ x_{32(k+1)} = x_{32(k)} + \tau(x_{21(k)} - x_{32(k)} + x_{33(k)}), \\ x_{33(k+1)} = x_{33(k)} + \tau(-\beta x_{32(k)}). \end{cases} \tag{40}$$

$$h(x_{31(k)}) = m_1 x_{31(k)} + \frac{1}{2}(m_0 - m_1)(|x_{31(k)} + 1| - |x_{31(k)} - 1|), \tag{41}$$

$$ND4\begin{cases} x_{41(k+1)} = x_{41(k)} + \tau(\alpha(x_{42(k)} - h(x_{41(k)})) \\ \qquad\qquad +k(x_{11(k)} + x_{21(k)} - 2x_{41(k)})), \\ x_{42(k+1)} = x_{42(k)} + \tau(x_{41(k)} - x_{42(k)} + x_{43(k)}), \\ x_{43(k+1)} = x_{43(k)} + \tau(-\beta x_{42(k)}). \end{cases} \tag{42}$$

$$h(x_{41(k)}) = m_1 x_{41(k)} + \frac{1}{2}(m_0 - m_1)(|x_{41(k)} + 1| - |x_{41(k)} - 1|), \tag{43}$$

$$ND5\begin{cases} x_{51(k+1)} = x_{51(k)} + \tau(\alpha(x_{52(k)} - h(x_{51(k)})) \\ \qquad\qquad +k(x_{21(k)} + x_{31(k)} - 2x_{51(k)})), \\ x_{52(k+1)} = x_{52(k)} + \tau(x_{51(k)} - x_{52(k)} + x_{53(k)}), \\ x_{53(k+1)} = x_{53(k)} + \tau(-\beta x_{52(k)}). \end{cases} \tag{44}$$

$$h(x_{51(k)}) = m_1 x_{51(k)} + \frac{1}{2}(m_0 - m_1)(|x_{51(k)} + 1| - |x_{51(k)} - 1|), \tag{45}$$

$$ND6\begin{cases} x_{61(k+1)} = x_{61(k)} + \tau(\alpha(x_{62(k)} - h(x_{61(k)})) \\ +k(x_{11(k)} + x_{31(k)} - 2x_{61(k)})), \\ x_{62(k+1)} = x_{62(k)} + \tau(x_{51(k)} - x_{62(k)} + x_{63(k)}), \\ x_{63(k+1)} = x_{63(k)} + \tau(-\beta x_{62(k)}). \end{cases} \tag{46}$$

$$h(x_{61(k)}) = m_1 x_{61(k)} + \frac{1}{2}(m_0 - m_1)(|x_{61(k)} + 1| - |x_{61(k)} - 1|), \tag{47}$$

$$\begin{cases} x_{1prom(k)} = \frac{1}{6}(x_{11(k)} + x_{21(k)} + x_{31(k)} + x_{41(k)} + x_{51(k)} + x_{61(k)}), \\ x_{2prom(k)} = \frac{1}{6}(x_{12(k)} + x_{22(k)} + x_{32(k)} + x_{42(k)} + x_{52(k)} + x_{62(k)}), \\ x_{3prom(k)} = \frac{1}{6}(x_{13(k)} + x_{23(k)} + x_{33(k)} + x_{43(k)} + x_{53(k)} + x_{63(k)}). \end{cases} \tag{48}$$

We used the FPGA Cyclone IV DEi-150 Altera-Intel main-board to design the hardware of the embedded system (ES) to implement the DSWN (36)–(47), which has a general purpose input/output (GPIO) that is configured to connect six external digital-to-analog converters (DACs); all the hardware of the ES is described in Figure 14.

To build the algorithm for the digital circuit implementation of the ES, we used the Quartus II version 12 software, which offers the Qsys tool to design the hardware and software, specifically, the 32-bit embedded main processor Nios II (fast version) and the serial-peripheral-interface (SPI) protocol were implemented inside of the FPGA [23,24]. Subsequently, the SPI port was configured to create the links that use the GPIO port from the FPGA De-i150 main board, which is setting in MOSI (master-output-slave-input) mode where the 32-bit micro-controller in the FPGA generates control signals such as chip-select and clock to set the external DACs, MISO (master-input slave-output) mode is not used. Figure 15 shows the schematic circuit of the FPGA to implement the DV of the DSWN (36)–(47).

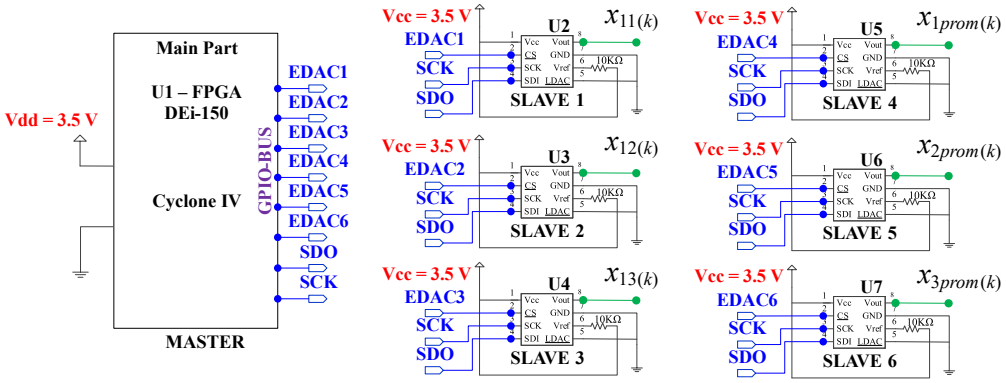

Figure 14. Hardware implementation of the embedded system using the GPIO bus to implement the DSWN (36)–(47).

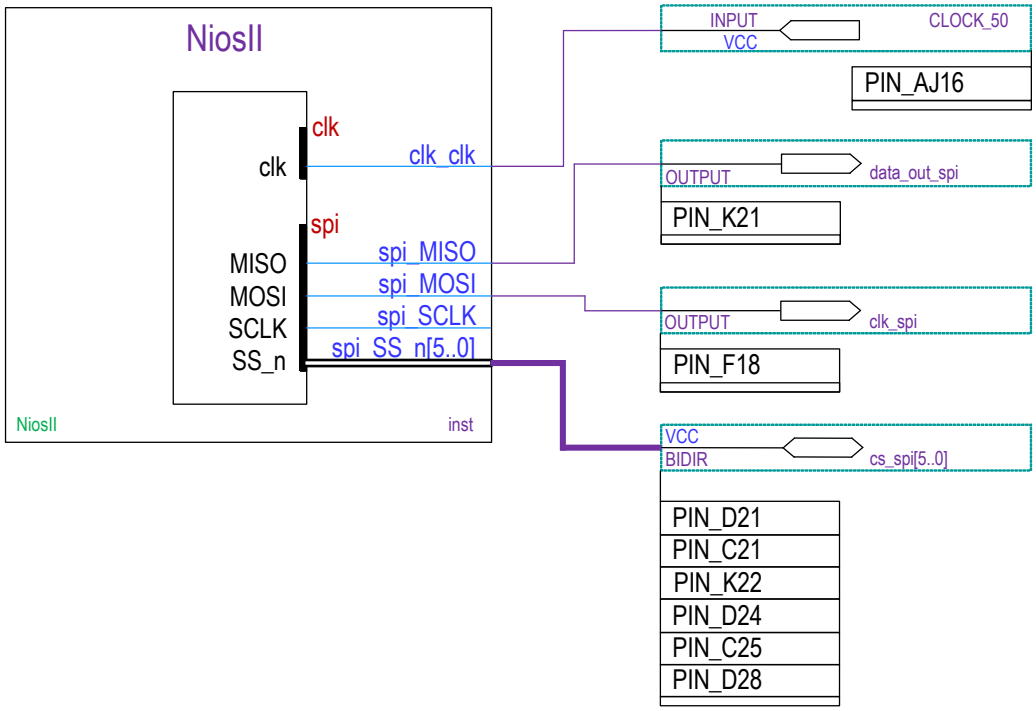

Figure 15. Schematic diagram to implement the processor Nios II fast version within FPGA Cyclone-IV U1 and the pins distribution to set the SPI protocol.

The FPGA Cyclone IV DEi-150 was configured in master mode and the GPIO pins were used to reproduce the SPI control signals: SCK, SDO, and SS1-SS6 for each DAC1-DAC6 as slaves, in order to represent the state variables, respectively. The experimental results showed good performance, presenting a time complexity of $t = 664$ µs using a clock of 50 MHz. According to the value of the parameter k, we proposed to analyze two cases for systems (36)–(47), these are $k = 0$, i.e., the nodes are decoupled, and $k = 10$, i.e., the discretized nodes are coupled.

6.1. Uncoupled Nodes

In Figure 16, for $k = 0$, the phase planes of node $ND1$ are presented corresponding to the discretized network (36) and (37) versus the representation of the average states of the six nodes of the expression (48).

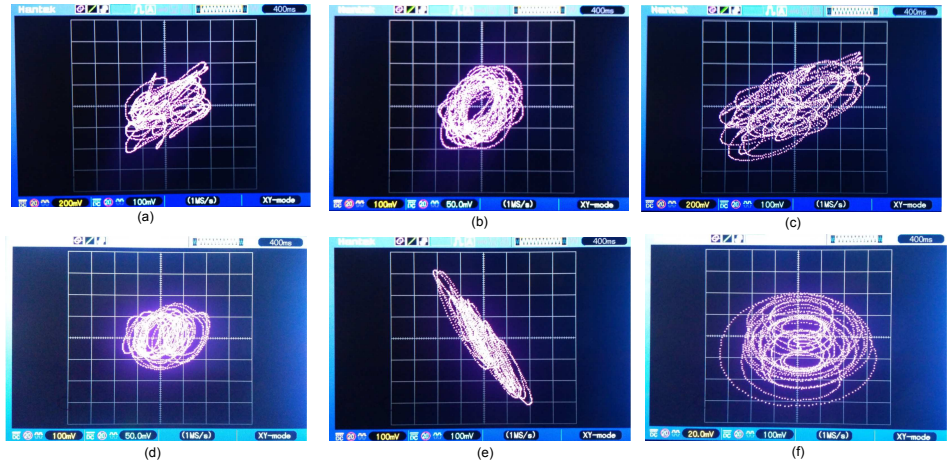

Figure 16. Comparison of the phase planes of the discretized network (36) and (37) and the average states of the network (48) for $k = 0$: **(a)** $x_{11(k)}$ vs. $x_{1prom(k)}$, **(b)** $x_{12(k)}$ vs. $x_{2prom(k)}$, **(c)** $x_{13(k)}$ vs. $x_{3prom(k)}$, **(d)** $x_{1prom(k)}$ vs. $x_{2prom(k)}$, **(e)** $x_{1prom(k)}$ vs. $x_{3prom(k)}$, and **(f)** $x_{2prom(k)}$ vs $x_{3prom(k)}$.

Figure 17 shows the time evolution of the node $ND1$ corresponding to the system (36) and (37).

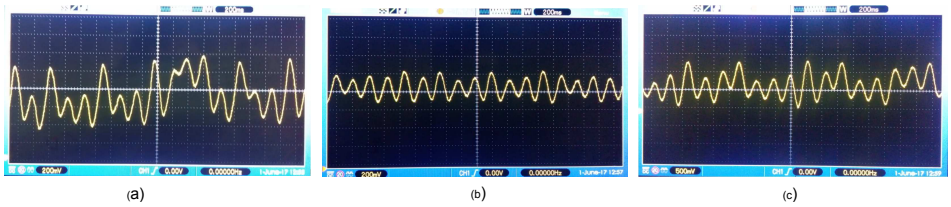

Figure 17. Time evolution of (36) and (37) for $k = 0$: **(a)** $x_{11(k)}$, **(b)** $x_{12(k)}$, and **(c)** $x_{13(k)}$.

6.2. Coupled Nodes

In Figure 18, the phase planes of the node $ND1$ corresponding to the system (36) and (37) versus the representation of the average states of the six coupled nodes of the system (48) are presented, where for this case we use $k = 10$.

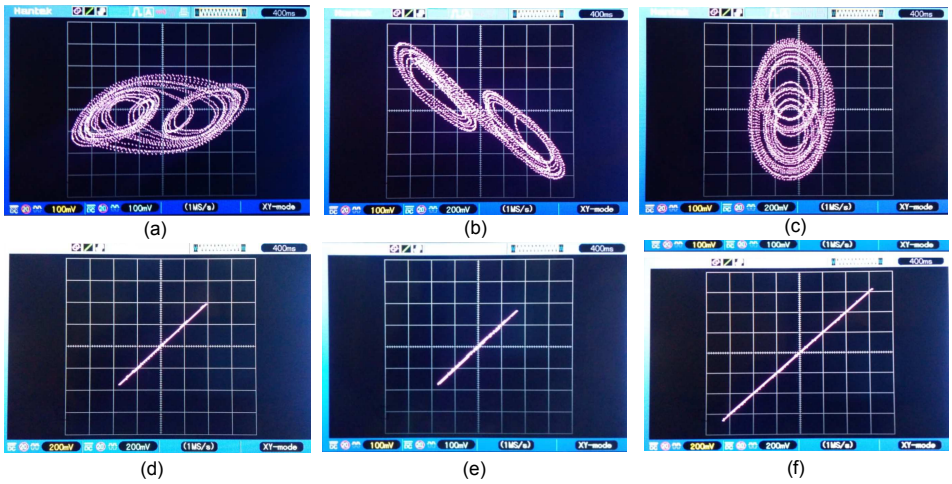

Figure 18. Comparison of the phase planes of system (36) and (37) and the average states of the network (48) using $k = 10$: **(a)** $x_{11(k)}$ vs. $x_{1prom(k)}$, **(b)** $x_{12(k)}$ vs. $x_{2prom(k)}$, **(c)** $x_{13(k)}$ vs. $x_{3prom(k)}$, **(d)** $x_{1prom(k)}$ vs. $x_{2prom(k)}$, **(e)** $x_{1prom(k)}$ vs. $x_{3prom(k)}$, and **(f)** $x_{2prom(k)}$ vs. $x_{3prom(k)}$.

6.3. Digital Application in Communications Using FPGA in a DSWN

We consider an experimental implementation to encrypt a signal $m_p(t)$ using the digital circuit with FPGAs, the signal $m_p(t)$ is described as follows:

$$m_p(t) = 0.042 \sin(\frac{\pi}{180}) + V_{ref} \tag{49}$$

Figure 19 shows the signal of the chaotic carrier x_{14} used in the node $ND4$ to encrypt the signal $m_p(t)$. The message $m_p(t)$ was received successfully in the node $ND6$.

Figure 19. Yellow line represents chaotic carrier x_{41} in the node $ND4$, blue line represents cryptogram $Z = x_{41} + m_p(t)$, and the white line represents the message recovered $\hat{m} = Z - x_{61}$ in the node $ND6$.

7. Conclusions

We have proposed the synchronization and encrypted communication transmissions of analog and digital messages in a DSWN using Chua's circuit as chaotic node. Analytical, numerical, and experimental studies to confirm the obtained results were conducted. We have presented a numerical method to build DSWNs starting with an iteration $l = 0$ with $N = 3$ nodes until iteration $l = 3$ conformed by $N = 24$ nodes. We have proposed the electronic implementation of DSWNs for a continuous version and also the digital implementation in a novel digital FPGA-tool Nios II embedded processor. One of the main disadvantages in the presented algorithm is that it does not have flexibility with respect to the modification of the DSWN topologies obtained at each iteration l, i.e., there is a fixed topology obtained at each iteration l. On the other hand, we believe that this work can motivate some possible future works. For example, we can build DSWNs using different chaotic nodes (or even fractional order chaotic nodes). Additionally, outwardly coupled DSWNs can be implemented in order to achieve outer synchronization. Furthermore, different components in the analog and digital implementations (OA or FPGA, respectively) can be applied, among other potential future works.

Author Contributions: Conceptualization, D.R.-D.l.C. and C.C.-H.; methodology, D.R.-D.l.C. and C.C.-H.; software, D.R.-D.l.C. and A.A.-D.; validation, D.R.-D.l.C., R.M.-R., A.A.-D. and C.C.-H.; formal analysis, D.R.-D.l.C.; investigation, D.R.-D.l.C. and C.C.-H.; resources, C.C.-H.; writing—original draft preparation, D.R.-D.l.C., R.M.-R., A.A.-D. and C.C.-H.; writing—review and editing, D.R.-D.l.C., R.M.-R., A.A.-D. and C.C.-H.; visualization, D.R.-D.l.C. and R.M.-R.; supervision, C.C.-H.; project administration, C.C.-H.; funding acquisition, C.C.-H. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Council for Research and Technology (CONACyT), Mexico, under research grant 166654 (A1-S-31628).

Institutional Review Board Statement: Not applicable.

Data Availability Statement: The data used to support the findings of this study are included within the article.

Acknowledgments: This research was funded by the National Council for Research and Technology (CONACyT), Mexico, under research grant 166654 (A1-S-31628). Adrian Arellano-Delgado is a

CONACYT research fellow commissioned to the Universidad Autónoma de Baja California (Project no. 3059).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Watts, D.J.; Strogatz, S.H. Collective dynamics of small-world networks. *Nature* **1998**, *393*, 440–442. [CrossRef] [PubMed]
2. Uzun, R.; Yilmaz, E.; Ozer, M. Effects of autapse and ion channel block on the collective firing activity of Newman–Watts small-world neuronal networks. *Phys. A Stat. Mech. Its Appl.* **2017**, *486*, 386–396. [CrossRef]
3. Ismail, A.A.O.O.; Amouzandeh, G.; Grant, S.C. Structural connectivity within neural ganglia: A default small-world network. *Neuroscience* **2016**, *337*, 276–284. [CrossRef] [PubMed]
4. Arellano-Delgado, A.; Cruz-Hernández, C.; López-Gutierrez, R.M.; Posadas-Castillo, C. Outer synchronization of nearest-neighbor and small-world chaotic networks. *Ifac. Papers Online* **2015**, *48*, 227–232. [CrossRef]
5. Ferreira, D.S.; Papa, A.R.; Menezes, R. Small world picture of worldwide seismic events. *Phys. A Stat. Mech. Its Appl.* **2014**, *408*, 170–180. [CrossRef]
6. Liao, X.; Vasilakos, A.V.; He, Y. Small-world human brain networks: Perspectives and challenges. *Neurosci. Biobehav. Rev.* **2017**, *77*, 286–300. [CrossRef] [PubMed]
7. Ruan, Y.; Li, A. A new small-world network created by Cellular Automata. *Phys. A Stat. Mech. Its Appl.* **2016**, *456*, 106–111. [CrossRef]
8. Comellas, F.; Ozon, J.; Peters, J.G. Deterministic small-world communication networks. *Inf. Process. Lett.* **2000**, *76*, 83–90. [CrossRef]
9. Comellas, F.; Sampels, M. Deterministic small-world networks. *Phys. A Stat. Mech. Its Appl.* **2002**, *309*, 231–235. [CrossRef]
10. Zhang, Z.; Rong, L.; Guo, C. A deterministic small-world network created by edge iterations. *Phys. A* **2006**, *363*, 567–572. [CrossRef]
11. Zhang, Y.; Zhang, Z.; Zhou, S.; Guan, J. Deterministic weighted scale-free small-world networks. *Phys. A Stat. Mech. Its Appl.* **2010**, *389*, 3316–3324. [CrossRef]
12. Cruz-Hernández, C. Synchronization of time-delay Chua's oscillator with application to secure communication. *Nonlinear Dyn. Syst. Theory* **2004**, *4*, 1–13.
13. Posadas-Castillo, C.; López-Gutiérrez, R.M.; Cruz-Hernández, C. Synchronization of chaotic solid-state Nd:YAG lasers: Application to secure communication. *Commun. Nonlinear Sci. Numer. Simul.* **2008**, *13*, 1655–1667. [CrossRef]
14. Gámez-Guzmán, L.; Cruz-Hernéz, C.; López-Gutiérrez, R.M.; García-Guerrero, E.E. Synchronization of Chua's circuits with multi-scroll attractors: Application to communication. *Commun. Nonlinear Sci. Numer. Simul.* **2009**, *14*, 2765–2775. [CrossRef]
15. Cruz-Hernández, C.; Romero-Haros, N. Communicating via synchronized time-delay Chua's circuits. *Commun. Nonlinear Sci. Numer. Simul.* **2008**, *13*, 645–659. [CrossRef]
16. Wang, X.F.; Chen, G. Synchronization in small-world dynamical networks. *Int. J. Bifurc. Chaos* **2002**, *12*, 187–192. [CrossRef]
17. Wang, X.F. Complex networks: Topology, dynamics and synchronization. *Int. J. Bifurc. Chaos* **2002**, *12*, 885–916. [CrossRef]
18. Reyes-De la Cruz, D.; Cruz-Hernández, C.; Posadas-Castillo, C.; Martínez-Clark, R. Encriptado caótico en una red determinista de mundo pequeño. In Proceedings of the Congreso Latinoamericano de Control Automático 2014, Cancún Quintana Roo, Mexico, 14–17 October 2014.
19. Rabinder, M. (Ed.) *Chua's Circuit: A Paradigm for Chaos*; World Scientific: Singapore , 1993.
20. Arellano-Delgado, A.; López-Gutiérrez, R.M.; Cruz-Hernández, C.; Posadas-Castillo, C. Experimental network synhronization via plastic optical fiber. *Opt. Fiber Technol.* **2013**, *19*, 93–108. [CrossRef]
21. Méndez-Ramírez, R.; Arellano-Delgado, A.; Cruz-Hernández, C.; Abundiz-Pxexrez, F.; Martxixnez-Clark, R. Chaotic digital cryptosystem using serial peripheral interface protocol and its dsPIC implementation. *Front. Inf. Technol. Electron. Eng.* **2018**, *19*, 165–179. [CrossRef]
22. Méndez-Ramírez, R.; Cruz-Hernández, C.; Arellano-Delgado, A.; López-Gutixexrrez, R.M. Degradation Analysis of Generalized Chua's Circuit Generator of Multi-Scroll Chaotic Attractors and its Implementation on PIC32. In Proceedings of the Future Technologies Conference 2016, San Francisco, CA, USA, 6–7 December 2016.
23. Cyclone IV Device Handbook Home Page. Available online: https://www.intel.com/content/www/us/en/content-details/653974/cyclone-iv-device-handbook.html?wapkw=cyclone%20iv (accessed on 16 February 2023).
24. Intel® Quartus® II Web Edition Design Software Version 13.1 for Windows Home Page. Available online: https://www.intel.com/content/www/us/en/software-kit/666221/intel-quartus-ii-web-edition-design-software-version-13-1-for-windows.html (accessed on 16 February 2023).