

Article

Lattice Patch Structure for Fixed-Frequency Transmon Quantum Computer with High-Fidelity CNOT Gates

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Abstract

Superconducting transmon processors represent a leading platform for large-scale quantum computing due to their high gate fidelities and scalability. However, conventional qubit–coupler–qubit (QCQ) architectures face critical physical and structural bottlenecks, notably frequency crowding [spectator qubit collisions] during system scaling and inefficient mapping onto the standard surface code. To overcome these limitations, we propose a novel lattice-patch architecture that couples four fixed-frequency transmons to a single fixed-frequency coupler. This design enhances qubit connectivity and maps directly onto the surface-code lattice unit [plaquette], thereby minimizing the compilation overhead associated with logical qubit implementation. Furthermore, utilizing an entirely fixed-frequency design intrinsically eliminates susceptibility to external flux noise, ensuring robust operational stability. Multi-level numerical simulations demonstrate CNOT gate fidelities exceeding 0.98 across all six connectivity directions within the patch. Nevertheless, the complex interaction network of the four-qubit architecture induces unintended residual phase accumulation during cross-resonance driving. This parasitic effect necessitates precise calibration, achievable via virtual R_z gates [software phase updates]. Ultimately, our results establish the lattice-patch architecture as an efficient, robust building block for future fault-tolerant quantum computers.

Keywords: superconducting qubit; fixed-frequency transmon; quantum error correction; surface code; cross-resonance gate; lattice-patch architecture

1. Introduction

A variety of quantum computing algorithms, including Shor’s algorithm and Grover’s algorithm, have demonstrated both the necessity and the feasibility of implementing quantum computers. In particular, the potential of quantum computing to surpass the limits of classical computation has driven its rapid adoption across diverse industrial and research fields [1–5]. Among the various physical platforms for qubit implementation, superconducting systems are prominent candidates due to their rapid gate operation times and robust scalability [6–11]. Transitioning from the Noisy Intermediate-Scale Quantum (NISQ) era to practical quantum computation necessitates large-scale Quantum Error Correction (QEC) [12].

Surface codes, which implement logical qubits on a lattice structure, are central to QEC and are the subject of intense research within superconducting hardware development [13–20]. To date, superconducting architectures have primarily diverged into grid-based layouts (Google) and heavy-hexagon structures (IBM). While Google’s grid



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architecture—incorporating individual couplers between qubit pairs—allows for direct surface-code mapping, the escalating number of couplers in larger systems triggers performance degradation through unwanted interactions and crosstalk [21]. Conversely, IBM’s heavy-hexagon structure suppresses these interactions by reducing connectivity [22], yet it incurs mapping inefficiencies, such as the requirement for additional SWAP gate overhead. Furthermore, many current platforms utilize tunable couplers for gate control [23,24], which require dedicated flux-bias lines and expose the system to decoherence from flux noise [25].

To address these structural bottlenecks, research has shifted toward alternative hardware architectures. Recent proposals have explored coupling three fixed-frequency qubits to a single fixed-frequency coupler [26], demonstrating high gate fidelities via microwave-based control [27–29]. However, these configurations still face structural constraints when aligning with surface-code lattice units, necessitating complex mapping procedures for large-scale expansion.

In this work, we propose a “lattice-patch” architecture that integrates four fixed-frequency transmon qubits with a single fixed-frequency coupler. This design achieves topological alignment with the surface code, overcoming the mapping limitations of previous structures. By employing an entirely fixed-frequency configuration, we minimize sensitivity to flux noise and maximize physical stability. Through numerical simulations, we demonstrate CNOT gates across six distinct directions within the patch, establishing this architecture as an efficient and stable building block for next-generation fault-tolerant quantum computers.

2. System Configuration

The proposed architecture integrates four fixed-frequency transmon qubits with a single fixed-frequency coupler, a configuration we define as the Lattice-Transmon system.

2.1. Comparison of Hardware Architecture and Connectivity

Figure 1 illustrates the structural advantages of the Lattice-Transmon system relative to representative superconducting quantum computing architectures.

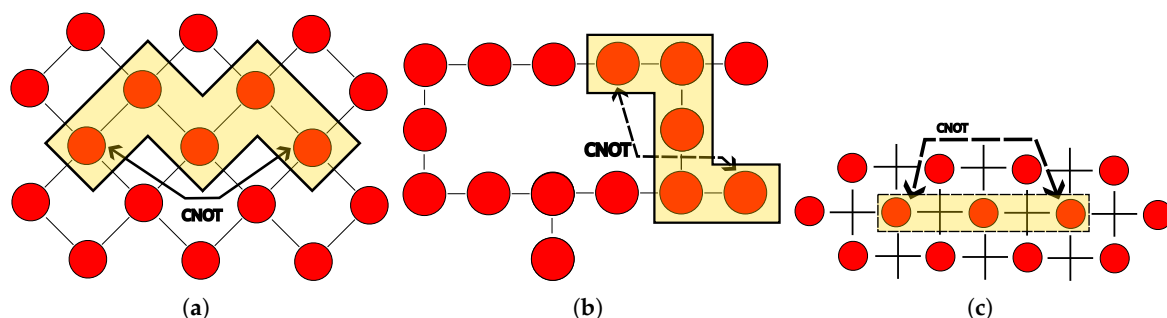


Figure 1. Comparison of prominent superconducting quantum computing architectures. Red dots denote physical qubits in the actual superconducting hardware, and black lines represent the connectivity between adjacent qubits. The yellow shaded regions and dashed arrows indicate the physical qubits and couplers involved in executing a CNOT gate between two specific qubits. (a) Google’s grid architecture utilizes individual couplers between adjacent qubits, enabling direct surface-code mapping; however, the high coupler density in scaled systems leads to performance degradation from parasitic interactions and crosstalk. (b) IBM’s heavy-hexagon structure suppresses these interactions by reducing qubit connectivity, yet it lacks direct surface-code mapping, resulting in reduced mapping efficiency and significant SWAP gate overhead. (c) The proposed lattice-patch architecture couples four fixed-frequency transmons to a single fixed-frequency coupler, facilitating direct topological correspondence with surface-code lattice units [plaquettes] while providing high connectivity without additional hardware overhead.

Conventional designs, such as Google’s grid architecture (Figure 1a) and IBM’s heavy-hexagon layout (Figure 1b), deploy individual couplers between every adjacent qubit pair to mediate direct interactions [8,9]. As systems scale, this approach leads to a prohibitive increase in the number of couplers and control lines. Moreover, during CNOT operations on a target qubit pair, these architectures are highly susceptible to parasitic interactions from the dense surrounding network of couplers and qubits [21]. In contrast, our proposed architecture (Figure 1c) utilizes a patch-based geometry where four qubits are locally coupled through a single central mediator. By minimizing the number of physical components involved in gate operations, this design significantly reduces hardware complexity and mitigates operational overhead [30].

2.2. Physical Model and Energy Level Design

The detailed architecture and circuit model of the proposed system are illustrated in Figure 2. The central fixed-frequency coupler is designed as an LC resonator, to which four transmon qubits are capacitively coupled with strengths G_i (Figure 2a,b).

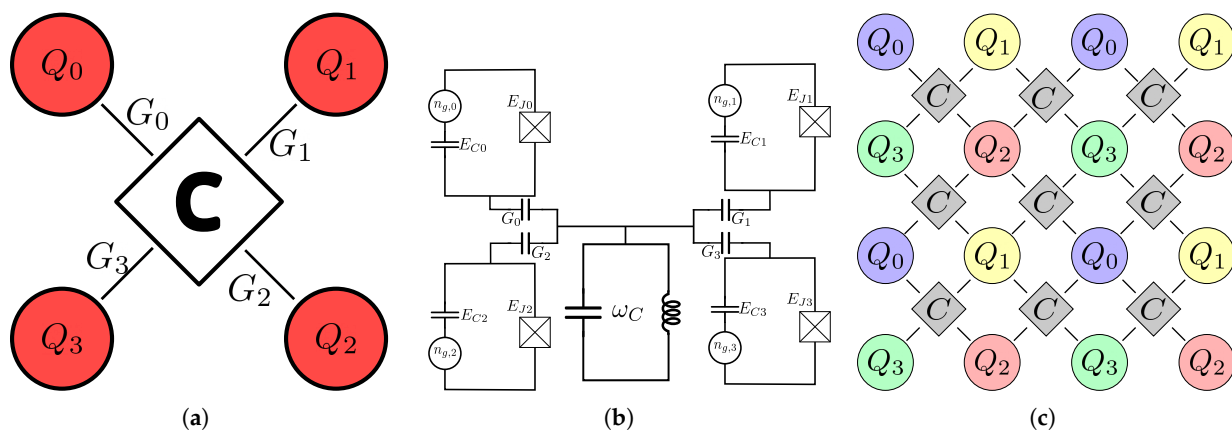


Figure 2. Detailed architecture and circuit model of the lattice-patch structure. (a) Schematic of the 1-coupler-4-qubit system. The Lattice-Transmon architecture consists of four fixed-frequency transmon qubits (Q_0 – Q_3) coupled to a single fixed-frequency central mediator (C). Each qubit is locally connected via coupling strengths G_i , a configuration designed to minimize gate operation overhead. (b) Lumped-element circuit model. The central coupler is implemented as an LC resonator with resonance frequency ω_C . Each transmon is defined by its Josephson energy ($E_{J,i}$) and charging energy ($E_{C,i}$). External microwave drive voltages ($n_{g,i}$) facilitate qubit control, while capacitive coupling mediates interactions between the qubits and the central resonator. (c) Scalability of the lattice patch. The periodic tiling of the patch unit drastically reduces the total coupler count compared to standard architectures and enables direct mapping onto the surface-code lattice.

By utilizing entirely fixed-frequency components, we ensure the system is intrinsically robust against $1/f$ flux noise—a primary decoherence mechanism in superconducting qubits. To prevent frequency crowding, the operating frequencies of the qubits (ω_i) are designed with substantial detunings on the order of several hundred MHz. Furthermore, the coupler frequency is positioned approximately 2 GHz above the qubit frequency band. This high-frequency placement suppresses direct energy exchange between qubits and the coupler, allowing the latter to serve as a stable, dispersive mediator.

2.3. Definition of the System Hamiltonian

We formulate the system Hamiltonian $\hat{H}$ using a lumped-element circuit model. For computational convenience, we set $\hbar = 1$. The total Hamiltonian is defined as the sum of the resonator ($\hat{H}_R$), transmon ($\hat{H}_T$), and interaction ($\hat{H}_I$) terms:

$$\hat{H} = \hat{H}_R + \sum_{i=0}^3 \hat{H}_{T,i}(t) + \hat{H}_I, \quad (1)$$

First, the coupler, implemented as an LC circuit, is modeled as a quantum harmonic oscillator. The Hamiltonian for the resonance frequency ω_C is given by:

$$\hat{H}_R = \omega_C \hat{a}^\dagger \hat{a}, \quad (2)$$

where $\hat{a}^\dagger$ and $\hat{a}$ denote the creation and annihilation operators, respectively.

Second, the Hamiltonian for each transmon qubit, $\hat{H}_{T,i}$, is defined by its charging energy ($E_{C,i}$) and Josephson energy ($E_{J,i}$) [31,32]:

$$\hat{H}_{T,i}(t) = 4E_{C,i}(\hat{n}_i - n_{g,i}(t))^2 - E_{J,i} \cos \hat{\phi}_i, \quad (3)$$

where $\hat{n}_i$ is the Cooper-pair number operator, $\hat{\phi}_i$ is the phase operator, and $n_{g,i}(t)$ represents the external microwave voltage pulses applied for qubit control. The system is designed in the transmon regime ($E_J \gg E_C$) to ensure insensitivity to charge noise.

Third, the interaction between the coupler and qubits follows the Jaynes–Cummings model and is expressed as [33]:

$$\hat{H}_I = \sum_{i=0}^3 G_i (\hat{a} + \hat{a}^\dagger) \hat{n}_i. \quad (4)$$

where G_i represents the coupling strength between the coupler and the i -th qubit.

Given the reliance on fixed-frequency elements, minimizing the residual ZZ interaction during the idle state is critical [34]. By optimizing qubit detunings within the dispersive regime, we suppress unintended parasitic phase accumulation in the computational basis. This design strategy serves as a foundation for mitigating crosstalk in large-scale lattice expansions.

2.4. Numerical Simulation and Multi-Level Considerations

To accurately simulate gate dynamics within a realistic hardware environment, we model the transmons as multi-level systems rather than simple two-level systems. This approach enables a rigorous analysis of leakage errors into non-computational states during gate execution [35]. The total Hilbert space of the system is defined by the tensor product of the resonator's Fock states and the eigenbasis of each transmon:

$$\mathcal{S} = |k\rangle_R \otimes \bigotimes_{i=0}^3 |m_i\rangle, \quad (k, m_i \in 0, 1, 2). \quad (5)$$

To balance computational efficiency with numerical accuracy, we include the three lowest energy levels ($|0\rangle, |1\rangle, |2\rangle$) for each component. By monitoring state transitions out of the computational basis $\{|0\rangle, |1\rangle\}$, we identified the optimal parameters required for achieving high-fidelity gate performance.

3. Pulse Protocol and Quantum Gate Optimization

In this section, we discuss the pulse design strategies and numerical optimization procedures required to implement high-fidelity two-qubit gates within the constrained lattice-patch architecture. Our control protocol utilizes a cross-resonance (CR) pulse-based framework, which has been previously validated in a system coupling three fixed-frequency qubits to a single fixed-frequency coupler [36]. By adapting and expanding this estab-

lished approach to our proposed architecture, we aim to demonstrate that structural scalability and operational consistency can be maintained even under a more complex interaction environment.

3.1. Control Strategy and Scalability

Compared to the previous researching structure coupling three qubits to a single fixed-frequency coupler, the proposed architecture introduces a more pronounced frequency crowding problem, which inherently exacerbates parasitic crosstalk. Despite these physical challenges, we retain the exact pulse framework established in previous literature to verify the physical viability and operational feasibility of our proposed hardware. Maintaining this identical pulse framework ensures its universal applicability within the local patch, thereby offering significant architectural advantages for scaling up large-scale quantum processors.

3.2. Parameter Optimization

Optimizing pulse parameters in superconducting qubit systems not only demonstrates hardware viability but also elucidates the potential limitations and future scalability of the proposed system. To implement the system, we employ two primary pulse types: a CR pulse to induce conditional interactions between the control and target qubits, and a DRAG-based Gaussian flat-top pulse to finalize the CNOT gate implementation. Optimizing the gates using each pulse type serves as a critical metric for evaluating the performance of the proposed system, making the optimization process a key technical challenge. To optimize these pulse parameters, we performed a grid search via a comprehensive parameter sweep.

In this simulation, to demonstrate that CNOT gates can be implemented across all connectivity directions, we realized a total of twelve gates: six forward CNOT gates ($CNOT_{01}, CNOT_{02}, CNOT_{03}, CNOT_{12}, CNOT_{13}, CNOT_{23}$) and six reverse CNOT gates ($CNOT_{10}, CNOT_{20}, CNOT_{21}, CNOT_{30}, CNOT_{31}, CNOT_{32}$). For the reverse gates, we leveraged the pulses already developed for the forward operations and applied an additional Gaussian pulse to achieve the reverse implementation. Specifically, the pulse used for the reverse operations was configured by additionally applying the same Gaussian flat-top gate sequence used in the forward CNOT gate framework. Consequently, to optimize the reverse CNOT gates, it is also necessary to optimize the auxiliary parameters introduced by these additional pulses.

3.3. Pulse Parameter Initialization and Pulse Composition

To implement the CNOT gate, the cross-resonance (CR) pulse is characterized by five parameters, $(f_1, T_S, \Omega_S, \rho, \gamma_1)$, while the Gaussian pulse relies on four parameters, $(f_2, T_X, \Omega_X, \gamma_2)$. Consistent with the approach used in the 1-coupler-3-qubit system, the initial values for the CR pulse parameters were set to $(f_1, T_S, \Omega_S, \rho, \gamma_1) = (f_{\text{target qubit}}, 150, 0.05, 0.1, 0)$. A grid search was subsequently conducted via parameter sweeps with step sizes or ranges of $[0.01, 5, 0.01, 5, 0]$ for each respective parameter.

For the Gaussian pulse, the four parameters $(f_2, T_X, \Omega_X, \gamma_2)$ were initialized to $(f_2, T_X, \Omega_X, \gamma_2) = (f_{\text{target qubit}}, 10, 0.01, 0)$, following the same methodology as the 1-coupler-3-qubit system. This was also optimized using a grid search via parameter sweeps within the bounds of $[0.01, 1, 0.005, 0.01\pi]$. In particular, the phase parameter for the Gaussian pulse was meticulously scanned across the range of $[-\pi, \pi]$ with a fine interval of 0.01.

It is worth noting that in demonstrating the reverse gate fidelities in this study, the pulses for single-qubit gates and their associated physical errors were not explicitly modeled. This is because the single-qubit error rate in current superconducting transmon processor platforms is remarkably low ($\sim 10^{-4}$), making it negligible compared to that of two-qubit gates like the CNOT gate. Furthermore, the primary objective of this work is to introduce and validate a novel architecture where four qubits are coupled to a single

mediator. Specifically, the implementation of the reverse gate aims to confirm that a bidirectional CNOT gate can be successfully achieved not by driving the conventional control qubit, but rather by applying the CR pulse to the target qubit.

The applied microwave drive pulses $n_{g,i}(t)$ conform to the assumed physical model and are designed to interact with the four-qubit energy spectrum via the pre-configured driving Hamiltonian. Figure 3a illustrates the pulse sequence for the forward CNOT gate, while Figure 3b displays the pulse sequence for the reverse CNOT gate.

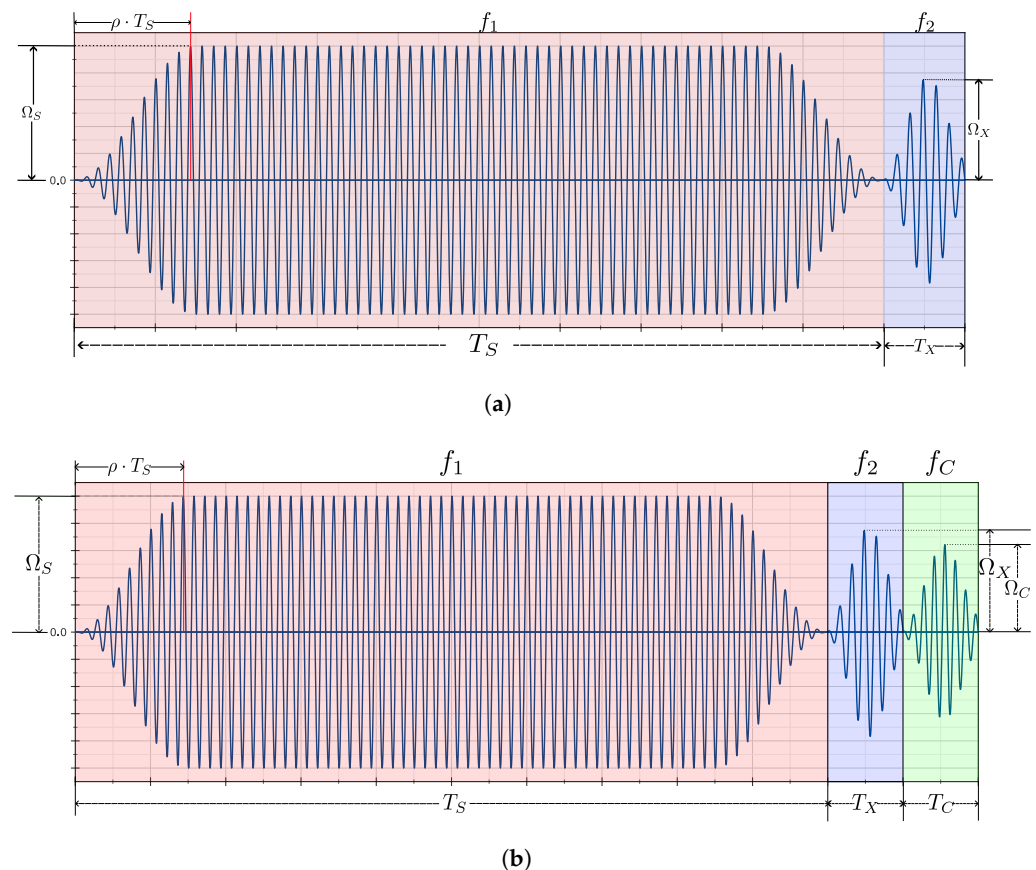


Figure 3. Pulse waveforms for gate implementation. **(a)** Pulse sequences for the forward CNOT gate. The red and blue regions represent the drives applied to the control and target qubits, respectively. The control qubit is driven by a cross-resonance (CR) pulse, where T_S , f_1 , Ω_S , γ , and ρ denote the pulse duration, frequency, amplitude, initial phase, and ramp ratio, respectively; the ramp ratio is scaled relative to the total pulse duration. The target qubit drive consists of a Gaussian pulse with DRAG [Derivative Removal by Adiabatic Gate] correction, characterized by duration T_X , frequency f_2 , amplitude Ω_X , and initial phase γ . **(b)** Pulse sequences for the reverse CNOT gate. The red and blue regions follow the same implementation as the forward gate, while the green region denotes an auxiliary drive applied to the control qubit specifically to enhance the fidelity of the reverse operation.

The pulse sequence employed here is identical to the framework used in the conventional 1-coupler-3-qubit system, and its detailed description is as follows:

1. **Simple Cross-Resonance Pulse Design:** We utilized the most foundational, simple CR pulse scheme to validate the structural feasibility of our 1-coupler-4-qubit architecture. By employing this basic CR drive, our primary objective was to demonstrate that conditional dynamics between two qubits can be successfully realized even within this expanded hardware topology.

2. Leakage Suppression via DRAG: To mitigate frequency crowding and prevent leakage into higher energy levels, we apply the Derivative Removal by Adiabatic Gate (DRAG) technique to all Gaussian pulse envelopes:

$$n_{g,i}(t) = \Omega_G(t) \cos(2\pi f_i t - \gamma_i) + \beta_i \dot{\Omega}_G \sin(2\pi f_i t - \gamma_i). \quad (6)$$

where the scaling parameter β_i is set to $0.5/E_C$ to effectively suppress charge-noise sensitivity and transitions to higher-order levels.

3.4. Flexibility in Reverse-Directional Gate Implementation

Despite the reliance on fixed-frequency components, our architecture enables the efficient implementation of bidirectional CNOT gates through pulse-level calibration (Figure 3b). Rather than wrapping a forward-direction gate with virtual Hadamard transformations, we ensure gate robustness by physically optimizing auxiliary pulses. This optimization explicitly accounts for the hardware-specific coupling strengths (G_i) and frequency detunings, allowing for high-performance operations in both directions.

3.5. Numerical Optimization and Validation Methodology

To evaluate the impact of the designed pulses on the system Hamiltonian and derive the final unitary operator $\hat{\mathcal{U}}$, we perform numerical optimization based on the time-dependent Schrödinger equation. The system Hamiltonian is formulated as the sum of a static term ($\hat{H}_0$) and a pulse-controlled driving term ($\hat{H}_1(t)$):

$$\hat{H}(t) = \hat{H}_0 + \hat{H}_1(t). \quad (7)$$

We calculate the time evolution over the total pulse duration T using a Dyson series expansion. For enhanced numerical precision, we employ a Suzuki-Trotter decomposition [37,38]:

$$\exp(-i\tau\hat{H}(\tilde{t})) \simeq \exp(-i\tau\hat{H}_0/2)V\exp(-i\tau\hat{\Lambda}(\tilde{t}_n))V^\dagger\exp(-i\tau\hat{H}_0/2). \quad (8)$$

where $\hat{\Lambda}(\tilde{t}_n) = V^\dagger\hat{H}_1(\tilde{t}_n)V$, and V denotes the transformation matrix composed of the eigenvectors corresponding to the transmon qubit states. The time step τ is chosen to guarantee numerical convergence and satisfy the required error bounds. In this study, we adopt a fine interval of $\tau = 0.001$ ns to minimize higher-order truncation errors and ensure the reliability of the calculated gate fidelities.

When performing the time evolution of the aforementioned Hamiltonian, the high-frequency oscillations intrinsic to the qubits impose physical and numerical limitations on interpreting the qubit system. To circumvent this challenge, it is necessary to transition from the current laboratory (Lab) frame to a rotating frame. Since this frame transformation must be applied universally across the Hamiltonian terms partitioned via the Suzuki-Trotter decomposition, the frame transition is executed by incorporating additional gauge-like operational terms into the Hamiltonian. The corresponding governing equation can be expressed as follows:

$$\begin{aligned} \exp(-i\tau\hat{H}_0/2) &\rightarrow \exp(-i\tau(\hat{H}_0 + i\dot{R}R^\dagger/2)), \\ \hat{U}_{\text{final}} &= \exp(-i\tau(\hat{H}_0 + i\dot{R}R^\dagger/2))RV\exp(-i\tau\hat{\Lambda}(\tilde{t}_n))V^\dagger R^\dagger \exp(-i\tau(\hat{H}_0 + i\dot{R}R^\dagger/2)). \end{aligned} \quad (9)$$

where R and $\dot{R}$ are defined as follows:

$$R(t) = \begin{bmatrix} 0 & 0 & 0 \\ 0 & e^{i\omega t} & 0 \\ 0 & 0 & e^{2i\omega t} \end{bmatrix}, \quad \dot{R} = \frac{d}{dt}R(t) = \begin{bmatrix} 0 & 0 & 0 \\ 0 & i\omega e^{i\omega t} & 0 \\ 0 & 0 & 2i\omega e^{2i\omega t} \end{bmatrix} \quad (10)$$

By incorporating these frame-transformation terms, we perform numerical simulations that effectively account for the high-frequency dynamics within the Hamiltonian evaluation.

Furthermore, we apply virtual-Z gate techniques to compensate for residual phase errors post-pulse application, yielding the final unitary matrix $\hat{\mathcal{U}}_{\text{total}}$ [39]:

$$\hat{R}_z^{(\text{v})}(\theta) = \bigotimes_{i=0}^3 R_z^{(i)}(\theta_i), \quad \hat{\mathcal{U}}_{\text{total}} = \hat{R}_z^{(\text{v})}\hat{\mathcal{U}}. \quad (11)$$

Gate performance is quantified by the average gate fidelity (F_{avg}), calculated via numerical Monte Carlo integration over $M = 10^4$ samples:

$$F_{\text{avg}} = \frac{1}{M} \sum_{j=1}^M |\langle \psi_j | \hat{\mathcal{U}}_{\text{opt}}^\dagger \hat{\mathcal{U}}_{\text{total}} | \psi_j \rangle|^2. \quad (12)$$

Since the final unitary gate incorporated with the virtual-Z (VZ) gates may not yet represent a fully optimized pulse configuration, an additional fine-tuning optimization process is conducted. Based on the approximate parameter regions identified via the initial grid search sweep, these discovered points are set as the initial coordinates. Subsequently, the derivative-free Nelder–Mead simplex algorithm is executed to further enhance the fidelity and performance of the implemented gate. The comprehensive optimization protocol for the final unitary operator $\mathcal{U}_{\text{final}}$ is structured as follows:

1. Initial Point Setup:

The parameters swept during the primary CR and Gaussian pulse calibrations are utilized to construct the initial points within the proximity of the optimal region. Starting the derivative-free Nelder–Mead algorithm from these pre-localized coordinates is crucial to prevent the optimizer from getting trapped in unfavorable local minima.

2. Loss Function Setup:

To drive the optimization process, we define a loss function $\mathcal{L}$. This loss is formulated using the average gate fidelity F_{avg} calculated from the implemented unitary operator $\mathcal{U}_{\text{total}}$ evaluated over random states $|\psi\rangle$ spanning the computational basis. The loss function $\mathcal{L}$ is computed as follows:

$$\mathcal{L} = 1 - F_{\text{avg}}. \quad (13)$$

3. Convergence Criteria:

The optimization process is terminated and deemed converged when either the variation in the simplex size Δx within the parameter space or the fractional change in the loss function $\Delta \mathcal{L}$ drops below a predefined threshold of 10^{-4} , indicating that no further numerical improvement is achievable.

This rigorous validation framework demonstrates that the proposed lattice-patch architecture achieves high operational reliability within a complex four-qubit network while maintaining the control simplicity of previous microwave-only schemes.

4. Setting Parameters of the Lattice-Transmon System

In this section, we present the hardware specifications and optimized gate parameters to demonstrate the physical viability of the proposed Lattice-Transmon system. We further validate the architectural effectiveness through numerical simulations, analyzing the resulting success probabilities and gate fidelities.

4.1. Hardware Specifications and Frequency Allocation

The hardware parameters for the proposed system are detailed in Table 1. This study extends a previously validated model to a four-qubit architecture, with qubit operating frequencies ranging from $\omega_0/2\pi = 5.03260$ GHz to $\omega_3/2\pi = 4.67259$ GHz. These frequencies are designed to coincide with the eigenfrequencies of the system Hamiltonian in the absence of external driving pulses.

Table 1. Hardware specifications.

	C	Q_0	Q_1	Q_2	Q_3
$\omega/2\pi$	7.0	5.03260	4.91339	4.79421	4.67259
$E_{C,i}/2\pi$	—	0.33	0.32	0.31	0.3
$E_{J,i}/2\pi$	—	11.0	10.8	10.6	10.4
$G_i/2\pi$	—	0.06	0.05	0.03	0.06

To mitigate frequency crowding—a common bottleneck in large-scale processors—we maintained inter-qubit detunings between 100 and 300 MHz. Furthermore, by assigning distinct qubit–coupler coupling strengths (G_i), we analyzed how variations in coupling affect gate implementation and overall performance. To quantify the crosstalk in our system, the residual ZZ interaction strength ζ_{ij} between qubits i and j is defined as follows:

$$\zeta_{ij} = E_{|1,1\rangle} - E_{|1,0\rangle} - E_{|0,1\rangle} + E_{|0,0\rangle}. \quad (14)$$

Moreover, to evaluate the multi-body crosstalk across the entire four-qubit system, we investigate the fourth-order residual ZZ interaction ζ_{1111} , which is expressed as:

$$\begin{aligned} \zeta_{1111} = & E_{|1110\rangle} - (E_{|1101\rangle} + E_{|1011\rangle} + E_{|0111\rangle}) \\ & + (E_{|1100\rangle} + E_{|1010\rangle} + E_{|1001\rangle} + E_{|0110\rangle} + E_{|0101\rangle} + E_{|0011\rangle}) \\ & - (E_{|0001\rangle} + E_{|0010\rangle} + E_{|0100\rangle} + E_{|1000\rangle}) + E_{|1111\rangle} \end{aligned} \quad (15)$$

The resulting residual ZZ interactions for the system are summarized in Table 2.

Table 2. Residual ZZ Interactions (MHz).

ζ_{01}	ζ_{02}	ζ_{03}	ζ_{12}	ζ_{13}	ζ_{23}	ζ_{1111}
0.02339	0.01164	0.16352	0.00536	0.03352	0.00811	0.23288

4.2. Optimization of CNOT Gate Pulse Parameters

Table 3 lists the optimized pulse parameters for the six forward-direction CNOT gates implemented in this architecture. Each gate protocol was optimized by applying a Cross-Resonance (CR) drive at the target qubit frequency (f_2), integrated with Gaussian auxiliary pulses to cancel parasitic interactions. To maximize gate fidelity, we performed fine-frequency sweeps within a ± 10 MHz range and optimized the ramp parameter (ρ) to refine the pulse rise and fall times, thereby minimizing leakage into higher-order energy levels.

Table 3. Forward CNOT gate parameters.

Gate	f_1 [GHz]	f_2 [GHz]	T_S [ns]	T_X [ns]	Ω_S	Ω_X	ρ	γ_1	γ_2
CNOT ₀₁	4.91339	4.91339	220	9	0.05	0.01	0.178	0	0.776
CNOT ₀₂	4.79396	4.79421	295	10	0.07	0.01	0.12	0	0.5
CNOT ₀₃	4.67257	4.67259	200	10	0.06	0.025	0.3	0	−0.05
CNOT ₁₂	4.79398	4.79421	440	10	0.05	0.017	0.1	0	0.03
CNOT ₂₃	4.67298	4.67259	400	10	0.075	0.003	0.1	0	0.87

Note that the amplitude parameters Ω_S and Ω_X are expressed as dimensionless scaling factors incorporated into the driving Hamiltonian, effectively corresponding to the normalized Rabi frequencies. For the implementation of reverse CNOT gates, we utilized a protocol where virtual Hadamard gates were applied to the control and target qubits based on the forward unitary.

The auxiliary drives used for these reverse operations share the same Gaussian flat-top envelope configuration as the forward gates. Specifically, the optimized pulse parameters are specified by the tuple (f, T, Ω, γ) , which represent the target qubit frequency, total pulse duration, dimensionless pulse amplitude, and initial phase, respectively. Detailed parameters for each reverse CNOT gate configuration are provided in Tables 4 and 5.

Table 4. Reverse CNOT gates parameters.

Gate	f [GHz]	T [ns]	Ω	γ
CNOT ₁₀	4.91339	16	0.03	−0.78
CNOT ₂₀	4.79421	45	0.04	0.5
CNOT ₃₀	4.67259	42	0.01	−0.15
CNOT ₂₁	4.99421	41	0.032	−0.9
CNOT ₃₂	4.67259	10	0.015	0.6

Table 5. CNOT₁₃, CNOT₃₁ pulse parameter.

Gate	f_1 [GHz]	f_2 [GHz]	T_S [ns]	T_X [ns]	Ω_S	Ω_X	ρ	γ_1	γ_2
CNOT ₁₃	4.67259	4.91339	210	10	0.085	0.02	0.17	0	0.75398
CNOT ₃₁	4.91369	4.67259	430	20	0.09	0.0227	0.1	0	−1.13097

However, the CNOT₃₁ gate exhibited a trend where fidelity failed to improve despite the application of ideal Hadamard gates and subsequent pulse optimization. Consequently, we configured the CNOT₃₁ gate using a direct forward-drive pulse sequence rather than the reverse-wrapping method, as detailed in Table 5.

This observation suggests that increasing the qubit-to-coupler ratio narrows the frequency gaps between qubits, exacerbating frequency crowding. These results underscore the critical importance of frequency allocation strategies in large-scale systems, highlighting the need for sophisticated frequency-placement and dynamic tuning techniques in future research.

4.3. Analysis of Gate Fidelity and Success Probability

The final unitary operator is implemented by sequentially applying the virtual-Z (VZ) gates immediately following the primary pulse operations. Table 6 lists the precise rotation angles (θ) applied to each individual qubit to calibrate the pulse-induced unitary operator.

Table 6. Apply correcting VZ gate.

Gate	θ_0	θ_1	θ_2	θ_3	Gate	θ_0	θ_1	θ_2	θ_3
CNOT ₀₁	−0.5966	−0.0314	0	0.3142	CNOT ₁₀	0.0942	−0.0314	0	0
CNOT ₀₂	0.4712	0	0	0	CNOT ₂₀	0	0.0628	0	0
CNOT ₀₃	−0.2512	0	0	0.3142	CNOT ₃₀	0.0314	0.0314	0.0314	0.0628
CNOT ₁₂	0.1884	1.4727	0.2826	0.2198	CNOT ₂₁	0.0314	0.1256	−0.0314	−0.0314
CNOT ₁₃	0.0942	0.942	0	−0.3768	CNOT ₃₁	0.0942	0	0.0314	0.0942
CNOT ₂₃	0.1727	0.0942	−0.0628	0.1099	CNOT ₃₂	0.1256	0.0942	0.157	0.1256

To evaluate the performance of the implemented gates, we performed unitary operations on prepared computational basis states and calculated the resulting success probabilities. As shown in Table 7, the forward CNOT gates (CNOT₀₁ through CNOT₂₃) exhibit high success probabilities exceeding 0.98. High success rates were maintained across varying coupling strengths, albeit with longer gate durations, suggesting that the proposed lattice-patch architecture possesses high robustness against physical parameter fluctuations.

Table 7. Lattice-Transmon system results.

Gate	Max Success Probability	Average Fidelity	Gate	Max Success Probability	Average Fidelity
CNOT ₀₁	0.9912	0.98265	CNOT ₁₀	0.9878	0.98152
CNOT ₀₂	0.9991	0.95864	CNOT ₂₀	0.9657	0.94496
CNOT ₀₃	0.9985	0.97833	CNOT ₃₀	0.9688	0.94266
CNOT ₁₂	0.9982	0.91509	CNOT ₂₁	0.9081	0.89566
CNOT ₁₃	0.9949	0.83292	CNOT ₃₁	0.9644	0.85239
CNOT ₂₃	0.9745	0.91256	CNOT ₃₂	0.9956	0.95000

The final average gate fidelities, calculated after virtual-Z phase corrections, are summarized in Table 7. The calibrated unitary gates achieved the target performance metrics across all connectivity directions. These numerical results demonstrate that our 1-coupler-4-qubit architecture can serve as an efficient building block for next-generation, large-scale quantum processors.

Here, the maximum success probability serves as a metric to evaluate how closely the implemented operator aligns with the ideal gate, evaluated across all computational basis states of the four-qubit system. Because this specific indicator is calculated by discarding phase errors, it inherently yields relatively higher numerical values. In contrast, the average gate fidelity represents the comprehensive mean value obtained only after executing the additional virtual-Z (VZ) gate calibrations. Crucially, because it encapsulates both state-flip errors and phase errors simultaneously, the average fidelity more accurately and rigorously reflects the actual gate performance from a physical hardware perspective.

Particularly, in superconducting qubit platforms, VZ gates are executed entirely through digital frame rotations without applying any physical microwave drive pulses; thus, they introduce zero additional gate overhead or physical error in actual experimental implementations. Furthermore, the auxiliary calibration pulses employed for the reverse CNOT gate implementations were fully integrated into the time-evolution calculations of the total system Hamiltonian during the numerical simulations. Consequently, any potential physical errors induced by these secondary drives, such as parasitic crosstalk or leakage to higher energy levels, are strictly and comprehensively reflected within the final average fidelity values.

4.4. Leakage Error and Error Budget

Because the current numerical simulations explicitly incorporate energy levels higher than the computational basis, the formulated system Hamiltonian naturally includes these higher-dimensional terms. Consequently, by applying the implemented unitary operator to the computational basis, we can quantitatively assess the leakage error. This can be formalized by projecting the final state ρ_{final} , which evolves from an arbitrary initial computational state $|\psi\rangle$ under the action of $\hat{U}_{\text{final}}$, onto the respective Pauli operators σ_x , σ_y , and σ_z :

$$x = \text{Tr}(\sigma_x \rho_{\text{final}}), \quad y = \text{Tr}(\sigma_y \rho_{\text{final}}), \quad z = \text{Tr}(\sigma_z \rho_{\text{final}}). \quad (16)$$

where the density matrix ρ_{final} is defined as follows:

$$\rho_{\text{final}} = \hat{U}_{\text{final}} |\psi\rangle \langle \psi| \hat{U}_{\text{final}}^\dagger. \quad (17)$$

Through this procedure, the final state evolving within the higher-dimensional Hilbert space can be effectively projected back onto the two-dimensional computational subspace. Using these calculated expectation values (x, y, z) , the leakage out of the computational subspace can be quantitatively measured. The resulting leakage error ε_L is expressed by the following equation:

$$\varepsilon_L = 1 - (x^2 + y^2 + z^2). \quad (18)$$

The calculated average leakage errors for the implemented CNOT gates across the various computational basis states are summarized in the following Table 8.

Table 8. Final CNOT gate leakage error.

	CNOT ₀₁	CNOT ₀₂	CNOT ₀₃	CNOT ₁₀	CNOT ₁₂	CNOT ₁₃	CNOT ₂₀	CNOT ₂₁	CNOT ₂₃
ε_L	0.0251	0.0252	0.0238	0.0242	0.0239	0.0228	0.0244	0.0252	0.0218

Furthermore, the physical simulations of the proposed hardware were conducted utilizing a three-level energy system ($|0\rangle$, $|1\rangle$, $|2\rangle$). This explicitly incorporates states higher than the standard two-level computational basis commonly defined in quantum computing architectures. Crucially, as the simulated energy dimension per qubit increases, the overall computational complexity of the proposed system scales as $\mathcal{O}(N^5)$. Although the first excited state outside the computational basis (the second energy level) represents the primary channel where leakage directly occurs, higher-order leakage into even more elevated states remains a physical possibility. To investigate this phenomenon quantitatively, we tracked the specific leakage errors distributed across the higher energy levels 2, 3, and 4 during the execution of the CNOT₀₁ gate, the results of which are compiled in the following Table 9.

Table 9. Energy Level Error Budget.

Energy Level	2	3	4
ε_L	0.9941	0.9748	0.9739

On the other hand, the Hadamard gates ($X_{\pi/2}$ gate) implemented for the current reverse CNOT gates were initially modeled as ideal gates. However, in actual hardware implementations, while single-qubit gates generally exhibit lower error rates compared to CNOT gates, even a minor error rate can significantly impact the overall system performance, making a detailed analysis of single-qubit gates highly critical. These single-qubit gates can be implemented using the same Gaussian pulses previously employed for the

CNOT gate configuration, and the pulse parameters optimized for executing the Hadamard gates on each qubit are summarized in Table 10.

Table 10. Pulse parameters for the implemented $X_{\pi/2}$ gates.

Gate	f [GHz]	T [ns]	Ω	γ	Fidelity
$X_{\pi/2,0}$	5.10260	10	0.023	1.5707	0.998
$X_{\pi/2,1}$	4.91339	10	0.0185	0.3141	0.999
$X_{\pi/2,2}$	4.71721	10	0.024	−0.6283	0.993
$X_{\pi/2,3}$	4.47259	10	0.025	0.3141	0.993

Accounting for these single-qubit operations, the effective fidelity of the reverse CNOT gate incorporating the physical Hadamard transformations is calculated as:

$$F_{\text{eff}} \approx F_{ij} \times (1 - \varepsilon_i)(1 - \varepsilon_j) \quad (19)$$

where F_{ij} denotes the maximum success probability achieved by the reverse CNOT gate under idealized conditions, and $\varepsilon_i = 1 - F_{X_{\pi/2,i}}$ represents the error rate of each respective Hadamard gate. Based on this formulation, the total effective fidelities for the reverse CNOT gates are evaluated as follows in Table 11.

Table 11. Effective fidelities of the reverse CNOT gates.

Gate	CNOT ₁₀	CNOT ₂₀	CNOT ₂₁	CNOT ₃₀	CNOT ₃₂
F_{eff}	0.9848	0.9364	0.9008	0.9600	0.9817

These comprehensive results demonstrate the profound impact of single-qubit errors originating from actual physical pulse sequences compared to idealized 2-qubit operations that only incorporate virtual phase corrections. Consequently, this analysis highlights that evaluating the full operation sequence is indispensable, thereby providing a rigorous and clear benchmark for assessing the practical lower bound of physical hardware performance.

4.5. Scalability and Structural Advantages

From a hardware implementation perspective, the 1:4 lattice-patch structure drastically reduces the total coupler count compared to conventional 1:1 or 1:2 coupling schemes, thereby mitigating control-line complexity. Furthermore, each patch functions as a unit cell [plaquette] for the surface code, and periodic tiling of these patches can form a global square lattice. This structural advantage addresses frequency crowding in fixed-frequency systems while providing an efficient physical-layer foundation for fault-tolerant quantum computing.

5. Discussion

The single-coupler 4-qubit lattice-patch architecture proposed in this study presents a novel framework for overcoming the physical and structural constraints inherent in conventional fixed-frequency transmon systems. Our numerical simulations demonstrate the successful implementation of six independent forward CNOT gates mediated by a single LC resonator, with the flexibility to extend these operations to bidirectional gates. Despite the increased qubit density, the system achieves an average gate fidelity (F_{avg}) exceeding 0.98—comparable to the performance of previous 1:3 qubit configurations. These results confirm that individual qubit controllability and coherence can be maintained within a more complex, multi-qubit coupled environment.

The primary advantage of this architecture lies in its structural scalability. Conventional 1:2 coupling schemes, such as Google's Sycamore, face an inevitable and prohibitive surge in wiring complexity and coupler count as the system scales. Furthermore, previously studied 1:3 coupling systems suffer from structural limitations that require complex encoding or significant SWAP gate overhead to implement the surface code.

In contrast, our 4-qubit unit functions as a fundamental unit cell (plaquette), enabling direct topological mapping onto the surface code without additional compilation overhead. This offers a significant paradigm shift for hardware design in fault-tolerant quantum computing. However, challenges such as frequency crowding and residual interactions intensify as qubit density increases.

The primary objective of the pulse configuration implemented in the current hardware model is to validate the structural feasibility and foundational viability of the proposed architecture using a simple CR pulse scheme. As cross-resonance pulse engineering matures, advanced variations—such as echoed CR or active-cancellation CR techniques—have emerged. Incorporating these sophisticated protocols into future physical simulations is highly expected to yield substantial further improvements in gate fidelities.

Furthermore, it should be noted that the current numerical simulations were evaluated within a closed quantum system that excludes dissipative environments and auxiliary coupling elements. In practical hardware implementations, shifting away from a closed-system idealization to account for open-system dynamics—such as energy relaxation (T_1), dephasing (T_2) mediated by the Lindblad master equation, and interactions with readout Purcell filters—is of paramount importance. Nevertheless, the core focus of this study remains squarely on the architectural paradigm of coupling four or more fixed-frequency qubits to a single, localized fixed-frequency coupler. Introducing these additional physical components will naturally alter the overall system Hamiltonian and consequently perturb the pulse parameters, which will necessitate subsequent parameter recalibration in future engineering stages.

The relatively low fidelities (ranging from 0.83 to 0.91) observed in certain gate directions in Table 7 stem from frequency crowding and residual crosstalk. These phenomena are inherently induced by the tight structural layout where four multi-level qubits are densely coupled within a narrow bandwidth spanning [4.67–5.03] GHz via a single fixed mediator. Crucially, rather than arbitrarily tuning or individually optimizing the hardware specifications to favor specific gate directions, this numerical simulation strictly applied a single, uncompromised set of global hardware parameters to validate all twelve bidirectional CNOT gates simultaneously. Consequently, the physical control limits became apparent along certain vulnerable gate paths depending on the localized frequency detunings and coupling strengths (G_i).

While the resulting non-uniformity highlights the intrinsic trade-offs embedded in fixed-frequency architectures, it does not imply an absolute or permanent performance ceiling for the proposed topology. In physical device fabrication and blueprint design phases, these bottlenecks can be effectively mitigated by meticulously engineering the native qubit-to-coupler frequency allocations, optimizing inter-qubit detunings, and adopting advanced pulse-shaping technologies. If adjacent qubit frequency crowding can be systematically suppressed in subsequent works, the currently degraded gate fidelities can comfortably surpass the rigorous fault-tolerant thresholds required for surface-code error correction.

In conclusion, the core scholarly value of this study transcends the mere localized fine-tuning of specific gate parameters; rather, it represents the first successful proof-of-concept demonstrating that a 1-coupler-4-qubit architecture can be numerically controlled and physically realized under strict quantum dynamics. By introducing a novel hardware topology that fundamentally circumvents the exponential surge in coupler count and

control-line complexity—traditionally the most critical bottleneck in scaling large-scale quantum processors—this architecture holds distinct academic significance. It establishes a primary foundational milestone toward achieving scalable quantum error correction (QEC) schemes. Therefore, granular optimization of hardware specifications, quantitative sensitivity analyses against parameter fluctuations, and advanced pulse engineering will serve as clear and highly valuable directions for follow-up research built upon the architectural foundation established in this work.

6. Conclusions

In this work, we proposed and validated a lattice-patch architecture designed to resolve the scalability bottlenecks of fixed-frequency transmon processors. Our primary findings are summarized as follows:

First, we achieved structural optimization by coupling four fixed-frequency qubits to a single central resonator. This configuration reduces hardware complexity and enhances control-line efficiency. Second, we demonstrated high-fidelity gate operations; by utilizing optimized CR pulses and DRAG techniques, we achieved CNOT gate fidelities exceeding 0.98 and confirmed the robust implementation of bidirectional gates. Finally, we verified that this structure allows for direct correspondence with surface-code lattice units, significantly reducing the computational overhead typically associated with logical qubit implementation.

In conclusion, the lattice-patch architecture offers a promising path toward scalable superconducting quantum processors and is expected to serve as a standard building block for future large-scale, fault-tolerant systems. Future research will explore the integration of active coupling control [tunable couplers] to shorten gate durations and further enhance the system's robustness against external noise.

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