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Fractional-Order Reactive Power Control for Electro-Thermal-Constrained Fault Ride-Through of Grid-Forming Converters

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Abstract

Grid-forming converters are essential for low-inertia power systems. However, their semiconductor current and junction-temperature limits make them vulnerable to protection-triggered blocking and thermal overstress during severe voltage sags. Existing control methods still struggle to suppress fault-instant current surges and the associated transient thermal stress induced by rapid overcurrent, which restricts the continuous operation of grid-forming converters during fault ride-through. This paper proposes a two-stage coordinated electro-thermal control strategy centered on fractional-order reactive power regulation. First, a fractional-order operator is embedded into the reactive-power loop of the virtual synchronous generator to smooth the transient response of the internal electromotive force and directly suppress the amplitude of fault-induced inrush current. By introducing a continuously tunable order, the proposed controller enhances transient damping, mitigates the waterbed effect trade-off associated with integer-order control, and reduces the initial junction-temperature shock at the fault instant. A constraint-based feasible-region identification procedure is then developed, in which a full-range parameter sweep is performed to screen fractional orders under stability, current, and thermal constraints. Second, generalized discontinuous pulse-width modulation and switching-frequency reduction are jointly applied to mitigate post-transient thermal accumulation. Electro-thermal co-simulation results indicate that, under the specified voltage-sag condition, the proposed strategy reduces transient overcurrent and thermal stress and improves the simulated fault-ride-through performance of grid-forming converters without additional hardware thermal margins.

Keywords: fractional-order control; fractional-order operator; grid-forming converter; virtual synchronous generator; fault ride-through; inrush current suppression; electro-thermal coupling



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1. Introduction

With the increasing penetration of renewable energy sources, modern power systems are becoming increasingly dominated by power electronic converters [1]. In low-inertia grids, grid-forming (GFM) converters are required to provide voltage support, frequency

regulation, and synthetic inertia, making them key interfaces for renewable-energy integration and grid stability enhancement [2–4]. However, unlike conventional synchronous generators, GFM converters are constrained by the current and thermal limits of power semiconductor devices. Under large grid disturbances, such as grid voltage sags, severe transient current surges may occur [5,6]. These surges can trigger overcurrent protection or gate-pulse blocking, and can also increase power device losses and peak junction temperature at the initial fault stage. During the subsequent fault-ride-through interval, sustained fault current further causes thermal accumulation. Therefore, the fault-ride-through capability of GFM converters depends on the coordinated suppression of current surges and the resulting electro-thermal stress [7–10].

Existing studies have proposed several methods to enhance the overcurrent withstand capability of GFM converters. Virtual impedance methods can increase the equivalent output impedance and limit the fault current [11,12]. Current-limiting control strategies can also restrict the converter current within a predefined range [13]. However, these methods may affect terminal-voltage support, power synchronization, or the original voltage-source characteristics of GFM converters under large disturbances. In conventional virtual synchronous generator (VSG) control, the reactive-power loop usually adopts a fixed integer-order integral operator. This structure has limited dynamic freedom in regulating the internal voltage amplitude. As a result, fast voltage support and transient current surge suppression are difficult to achieve simultaneously [14–16].

Fractional calculus has been increasingly applied to power electronic and renewable-energy control because it provides additional tuning freedom beyond integer-order controllers [17–19]. In DC–DC converters, fractional-order controllers have been used for output-voltage regulation and robustness improvement under load and input-voltage variations. In photovoltaic systems, fractional-order maximum power point tracking (MPPT) and fractional-order PI/PID controllers have been applied to improve tracking dynamics under irradiation changes and partial shading. In grid-connected converters, fractional-order control has been used for LCL-filtered inverter regulation and harmonic disturbance rejection. In microgrids and renewable-energy-integrated power systems, fractional-order PID, fuzzy, and cascaded controllers have been employed for load-frequency control, automatic generation control, and frequency stabilization. These studies show that fractional-order operators are suitable for systems with nonlinear dynamics, parameter uncertainty, and multi-time-scale responses.

Recent studies have further introduced fractional-order control into VSGs and GFM converters. Fractional-order VSG methods have been used to improve power damping and inertial response by replacing fixed integer-order dynamics with non-integer-order control terms [20]. Fractional-order PI droop control has also been investigated for GFM converters to improve transient response and stability [21]. Related fractional-order fault-ride-through controllers have been applied to converter-side or dc-link regulation to mitigate fault-induced current and voltage disturbances [22]. Nevertheless, most existing fractional-order studies focus on frequency regulation, virtual inertia emulation, power-oscillation damping, or droop-loop enhancement [23,24]. Meanwhile, existing current-limiting and fault-ride-through strategies for GFM converters generally rely on virtual-impedance adjustment, current-reference modification, or dedicated current-limiting loops [25,26].

In contrast, less attention has been paid to the use of fractional-order operators in suppressing the fault-instant transient current surge through the internal voltage-regulation mechanism of GFM converters. For a VSG-based GFM converter, the reactive-power loop directly determines the internal voltage amplitude. During a grid fault, the transient mismatch between the internal voltage and the grid voltage is the main source of the inrush current [27,28]. Therefore, the proposed method embeds a fractional-order operator into

the reactive-power loop to reshape the transient internal-voltage response and reduce the voltage mismatch that drives the fault current. Moreover, the fractional order is selected by jointly considering the phase margin, transient current peak, and junction-temperature peak. This electro-thermal-constrained order-selection mechanism distinguishes the proposed method from existing fractional-order controllers and current-limiting strategies designed mainly according to electrical dynamic performance.

The selection of the fractional order is also a key issue. A larger fractional order can enhance the attenuation of fault-induced high-frequency disturbances. However, it also introduces additional phase lag and may reduce the stability margin. In addition, the electrical and thermal effects of the fractional order are coupled [29]. A lower peak current does not necessarily correspond to a lower junction-temperature peak because the thermal response also depends on the duration and energy distribution of the fault current. Therefore, the fractional order should be selected under the combined constraints of closed-loop stability, transient current limitation, and junction-temperature safety [30].

After the initial current surge is suppressed, the converter may still experience post-transient thermal accumulation during the remaining fault-ride-through interval. Passive thermal design can improve hardware thermal margins, but it increases system volume and cost. Active thermal control provides another solution by adjusting modulation and switching variables without changing the hardware. In this paper, generalized discontinuous pulse-width modulation (GDPWM) and switching-frequency reduction are simultaneously introduced as post-transient thermal regulation measures to mitigate sustained thermal accumulation. This combined regulation layer complements the fractional-order current-suppression strategy.

To address the above issues, this paper proposes a fractional-order VSG control strategy with electro-thermal constraints for GFM converters. The main contributions are summarized as follows:

- (1) A fractional-order reactive-power loop is designed for the VSG-based GFM converter. The fractional-order operator introduces an additional tuning degree of freedom into the reactive-power loop. This flexibility helps suppress the transient current surge at fault inception and the associated initial junction-temperature rise.
- (2) A constraint-based feasible-region identification procedure is developed for fractional-order selection. A full-range parameter sweep is performed, and the candidate orders are screened according to the stability margin, transient current limitation, and junction-temperature constraints. This provides a systematic alternative to empirical order tuning without formulating an additional optimization objective.
- (3) A full-order electro-thermal co-simulation model is established in PLECS. The simulation results demonstrate the effects of fractional-order current suppression, feasible-region-based order selection, and coordinated post-transient thermal regulation.

The remainder of this paper is organized as follows. Section 2 establishes the GFM converter model and analyzes the electro-thermal coupling mechanism caused by fault-induced overcurrent, which provides the physical basis for the fractional-order control design. Section 3 presents the fractional-order reactive power control strategy and determines the feasible region of the fractional order under stability, current, and junction-temperature constraints. Section 4 introduces a complementary post-transient thermal regulation strategy to support the fractional-order current suppression during the remaining fault-ride-through interval. Section 5 verifies the proposed fractional-order control framework through electro-thermal co-simulations. Section 6 concludes the paper.

2. Fundamentals of GFM Converters and Electro-Thermal Coupling Mechanisms Under Overcurrent Scenarios

This section establishes the fundamental electro-thermal model of GFM converters under fault overcurrent scenarios. By analyzing the voltage-source characteristics and transient circuit behavior of GFM converters, the formation mechanism of transient inrush current under severe grid disturbances is clarified. Then, an electro-thermal loss model of the semiconductor devices is developed to quantify the relationship between fault-current stress, power loss, and junction-temperature rise. This modeling framework provides the physical basis for the subsequent fractional-order control design, whose objective is to suppress fault-induced current surges and the associated initial thermal shock.

2.1. Voltage-Source Characteristics and Control Principles of GFM Converters

Unlike PLL-dependent grid-following converters, GFM converters operate as controlled ac voltage sources. They establish the voltage and frequency at the point of common coupling and provide synthetic inertia and voltage support. A typical converter employs an LC or LCL filter and a cascaded control architecture comprising an outer power loop and inner voltage and current loops.

As shown in Figure 1, the GFM converter consists of a dc voltage source, a three-phase IGBT full-bridge, an LC filter, and an ideal grid voltage source. The lumped inductance L_{eq} represents the total series coupling inductance between the converter and the grid in the benchmark model. The active power loop emulates the rotor motion equation to generate the reference frequency and phase, while the reactive-power loop emulates the excitation regulator to determine the reference voltage amplitude. Their time-domain mathematical models are expressed as follows:

$$\begin{cases} J \frac{d\omega}{dt} = \frac{P_{ref} - P_0}{\omega_{ref}} + D_p(\omega_{ref} - \omega) \\ E = \frac{1}{K} \int [D_q(U_n - U_0) + (Q_{ref} - Q_0)] dt \\ \theta_g = \int \omega dt \end{cases} \quad (1)$$

where J is the virtual moment of inertia of the system; D_p and D_q are the active-frequency damping coefficient and the reactive-voltage droop coefficient, respectively; K denotes the integral inertia coefficient for voltage regulation; P_{ref} and Q_{ref} are the active and reactive power reference commands; P_0 and Q_0 are the actual active and reactive power output by the converter; ω_{ref} and ω are the rated angular frequency of the grid and the actual output angular frequency of the converter, respectively; U_n and U_0 are the rated terminal voltage amplitude and the observed actual terminal voltage amplitude. The phase angle θ_g and the internal EMF amplitude E , generated by the above equations, jointly constitute the internal voltage reference, which is then fed into the inner loops for rapid dynamic tracking. Ultimately, the output of the inner loops is sent to the PWM module to generate the gate signals S_g for driving the power IGBTs within the converter. The control block diagram of the outer power loop is illustrated in Figure 2.

Although the GFM converter exhibits favorable steady-state voltage-source characteristics, its reactive power regulation in the conventional VSG framework relies on a fixed integer-order integral operator. During severe grid voltage sags, this fixed-order operator provides limited dynamic degrees of freedom for balancing voltage support and overcurrent suppression. Consequently, the transient response of the internal voltage amplitude may aggravate the voltage difference between the converter and the sagged grid, leading to severe fault-current surges. This limitation motivates the fractional-order modification of the reactive-power loop in the following section.

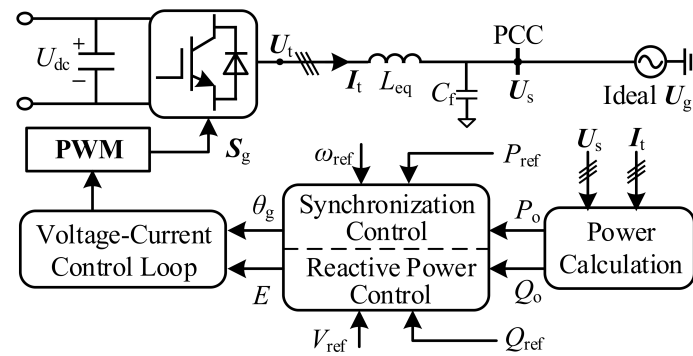


Figure 1. System configuration and control block diagram of the GFM converter.

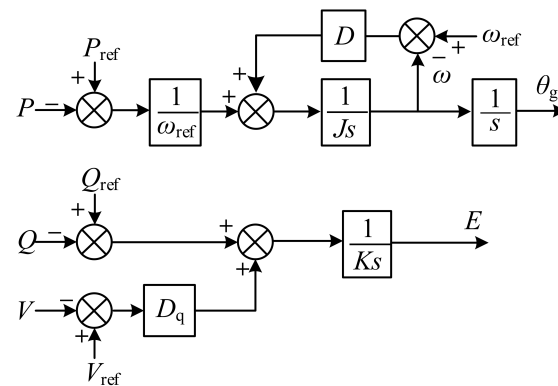


Figure 2. Active and reactive power control loop of the VSG.

2.2. Transient Inrush Current Mechanism

Under grid sags, the inherent low-impedance characteristics and limited integer-order control bandwidth of GFM converters inevitably excite severe transient inrush currents. To quantitatively elucidate this mechanism, a dynamic fault model is established. By combining phasor space analysis with time-domain equivalent circuits, the transient current response at the fault instant is rigorously derived.

Figure 3 illustrates the voltage-current phasor relationship during a transient fault. When the grid voltage U_g sags, the internal electromotive force E cannot change abruptly due to the VSG virtual inertia J and control delays. This sharply widens the potential difference, triggering a transient overcurrent. As the sag deepens, this potential difference becomes amplitude-dominated rather than phase-dominated. Given the small inductive equivalent output impedance Z_{eq} , the phase lag of the current vector i_c progressively increases, approaching 90° .

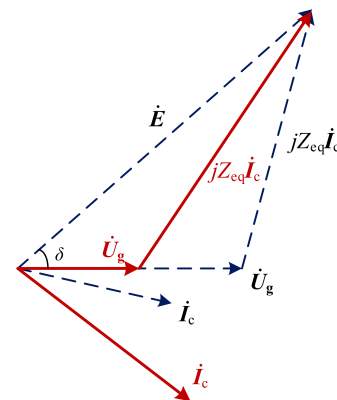


Figure 3. Phasor diagram of the converter under grid fault conditions.

To quantitatively analyze these phasor dynamics in the time domain, a transient equivalent circuit is established. In this circuit, the converter operates as a constant controlled-voltage source, and the sharply widened potential difference acts directly on the low-damping filter branch. Applying Kirchhoff's voltage law, the differential equation for the transient current $i_c(t)$ is expressed as:

$$\begin{cases} L_{eq} \frac{di_c(t)}{dt} + R_{eq} i_c(t) = e(t) - pu_g(t) \\ e(t) = E \cos(\omega_0 t + \theta_g) \\ u_g(t) = \cos(\omega_0 t) \\ Z_{eq} = R_{eq} + jL_{eq} \end{cases} \quad (2)$$

where $e(t)$ is the time-domain expression of the internal electromotive force of the converter; $u_g(t)$ is the normal grid voltage before the sag; p denotes the retained-voltage coefficient during the voltage sag; L_{eq} and R_{eq} are the total equivalent inductance and physical equivalent resistance of the loop, respectively. By solving this first-order non-homogeneous linear differential equation, the fully analytical expression of the converter's output transient current can be obtained. This current $i_c(t)$ is strictly composed of the superposition of the forced-response steady-state AC component $i_{ac}(t)$ and the zero-input-response naturally decaying DC bias component $i_{dc}(t)$.

The above analysis indicates that the fault current surge is essentially driven by the sudden mismatch between the converter internal voltage and the sagged grid voltage. Therefore, suppressing the transient current peak requires not only current limiting at the output stage but also appropriate regulation of the internal voltage dynamics. This provides the direct physical basis for introducing a fractional-order operator into the reactive-power loop, where the additional order freedom can be used to reshape the transient current trajectory.

2.3. Electro-Thermal Loss Modeling of Power Devices

The transient inrush current discussed above not only causes electrical overcurrent stress but also leads to rapid thermal stress in the semiconductor devices. Therefore, an electro-thermal model is required to evaluate the junction-temperature response of the IGBT module during fault ride-through (FRT). During converter operation, the total power loss of the IGBT can be expressed as:

$$P_{loss} = P_{sw} + P_{cond} \quad (3)$$

where P_{cond} is the conduction loss of the IGBT, and P_{sw} is the switching loss of the IGBT. The switching loss of the IGBT can be further divided into the turn-on loss, P_{sw-on} , and the turn-off loss, P_{sw-off} . The conduction loss of the IGBT can be expressed as:

$$P_{con} = V_{ce} \cdot I_c \cdot D(t) \quad (4)$$

where V_{ce} is the on-state voltage drop of the IGBT; I_c is the current flowing through the IGBT; $D(t)$ denotes the duty cycle at the moment the IGBT is conducting; the on-state voltage drop V_{ce} is affected by the IGBT junction temperature T_j , and can be expressed as:

$$P_{cond} = R_T \cdot I_c^2 + V_{ce0} \cdot I_c = f(I_c, T_j) \quad (5)$$

where R_T and V_{ce0} denote the on-state slope resistance and threshold-voltage intercept of the IGBT, respectively, both of which are affected by temperature. It can be seen that the conduction loss of the IGBT is a function of temperature, and the conduction loss

also causes changes in the junction temperature. This dependence forms a bidirectional electro-thermal coupling between the device losses and junction temperature.

The switching loss is determined by the turn-on and turn-off energy losses within each switching period:

$$P_{sw} = (E_{on} + E_{off}) \cdot f_{sw} \quad (6)$$

where E_{on} is the energy loss of the IGBT during the turn-on process within one switching cycle; E_{off} is the energy loss of the IGBT during the turn-off process within one switching cycle; f_{sw} is the switching frequency. E_{on} and E_{off} are related to the IGBT on-state voltage drop V_{ce} , the junction temperature T_j , and the current I_c , and can be written as:

$$\begin{cases} E_{on} = f(T, I_c) \cdot \left(\frac{V_{ce}}{V_{ref}}\right)^{K_{on}} \\ E_{off} = g(T, I_c) \cdot \left(\frac{V_{ce}}{V_{ref}}\right)^{K_{off}} \end{cases} \quad (7)$$

where K_{on} and K_{off} are the correction coefficients provided by the manufacturer, and V_{ref} is the reference voltage in the datasheet. Equations (3)–(7) show that the fault current directly increases the conduction loss and also affects the switching loss through current- and temperature-dependent energy characteristics.

To calculate the transient junction temperature, the Foster thermal network shown in Figure 4 is adopted. In the electro-thermal analogy, power loss is regarded as a heat source, thermal resistance corresponds to electrical resistance, and thermal capacitance corresponds to electrical capacitance. Compared with the Cauer model, the Foster model is more convenient for engineering implementation because its parameters can be obtained from the transient thermal impedance curves provided by the manufacturer.

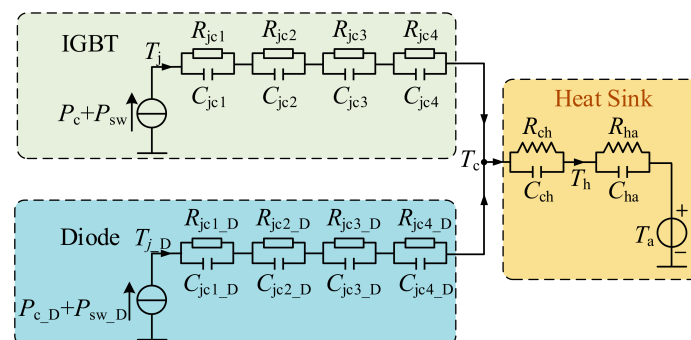


Figure 4. Foster equivalent thermal network model of the IGBT and diode.

For the fourth-order Foster thermal network, the junction temperatures of the IGBT and the anti-parallel diode are calculated as:

$$\begin{cases} T_j = T_c + (P_c + P_{sw}) \sum_{i=1}^4 \frac{R_{jci}}{1 + R_{jci}C_{jci}s} \\ T_{j_D} = T_c + (P_{c_D} + P_{sw_D}) \sum_{i=1}^4 \frac{R_{jci_D}}{1 + R_{jci_D}C_{jci_D}s} \\ T_c = T_a + (P_c + P_{sw} + P_{c_D} + P_{sw_D}) \left(\frac{R_{ch}}{1 + R_{ch}C_{ch}s} + \frac{R_{ha}}{1 + R_{ha}C_{ha}s} \right) \end{cases} \quad (8)$$

where T_j and T_{j_D} are the junction temperatures of the IGBT and diode, respectively; T_c and T_a are the case temperature and ambient temperature; P_c , P_{sw} , P_{c_D} , and P_{sw_D} are the conduction and switching losses of the IGBT and diode; and R_{jc} , C_{jc} , R_{ch} , C_{ch} , R_{ha} , and C_{ha} are the corresponding thermal parameters. The parameters of the fourth-order Foster

model are listed in Table 1. The thermal capacitance of each Foster branch is calculated from the corresponding thermal time constant as:

$$C_j = \frac{\tau_j}{R_j} \quad (9)$$

Table 1. Parameters of the fourth-order Foster model.

Parameter	1	2	3	4
R_{jc} (K/W)	0.0318	0.1749	0.1696	0.1537
τ_{jc} (s)	0.01	0.02	0.05	0.1
R_{jc_D} (K/W)	0.0504	0.2772	0.2688	0.2436
τ_{jc_D} (s)	0.01	0.02	0.05	0.1

The electro-thermal model above establishes the mapping from fault current to junction-temperature response. At the fault instant, the transient current surge rapidly increases device losses and produces an initial junction-temperature shock. During the subsequent FRT interval, sustained overcurrent further causes thermal accumulation. Therefore, transient inrush current suppression and post-transient thermal-stress mitigation should be considered together. In this paper, the former is mainly addressed by the fractional-order reactive power control, while the latter is further supported by the coordinated active thermal regulation strategy.

3. Fractional-Order Reactive Power Control for Transient Inrush Current Suppression

3.1. Design of the Fractional-Order Reactive-Power Loop

In the VSG-based control architecture of GFM converters, the reactive-power loop emulates the excitation regulation of a synchronous generator and determines the internal voltage amplitude E . As analyzed in Section 2, under severe grid voltage sags, the mismatch between the converter internal voltage and the sagged grid voltage is the direct source of the transient inrush current. Therefore, the dynamic response of the reactive-power loop is critical for suppressing the fault-current surge at the initial fault stage.

For the conventional integer-order VSG control, the reactive power regulation equation in the complex-frequency domain can be written as:

$$E(s) = \frac{1}{Ks} [D_q(U_n - U_b(s)) + Q_{ref} - Q_0(s)] \quad (10)$$

where U_n and U_0 are the rated and observed terminal voltage amplitudes, respectively; Q_{ref} and Q_0 represent the reactive power reference command and the actual reactive power output; D_q is the reactive-power-voltage droop coefficient; K denotes the integral inertia coefficient for voltage regulation; and s denotes the complex-frequency variable in the Laplace domain.

Equation (10) shows that the conventional reactive-power loop relies on a first-order integral operator $1/s$. This operator has a fixed-magnitude slope of -20 dB/dec and a fixed phase lag of -90° . During severe voltage sags, the reactive-voltage error contains wideband transient components. A smaller K may accelerate voltage regulation but can amplify the transient variation in E , thereby increasing the voltage difference applied to the equivalent impedance. Conversely, a larger K improves the attenuation of fast disturbances but slows down voltage recovery. This reflects the inherent trade-off of the integer-order integral structure between dynamic response speed and transient overcurrent suppression.

To introduce an additional degree of freedom into the reactive power dynamics, the integer-order integral operator is replaced by a fractional-order integral operator $s^{-\alpha}$. The reconstructed fractional-order reactive-power loop is shown in Figure 5, and its control equation is expressed as:

$$E(s) = \frac{1}{Ks^\alpha} [D_q(U_n - U_0(s)) + Q_{ref} - Q_0(s)] \quad (11)$$

where $\alpha > 0$ denotes the fractional integration order. Under zero initial conditions, the operator $s^{-\alpha}$ used in Equation (11) is interpreted as the Laplace-domain representation of the Riemann–Liouville fractional integral. For a causal input $x(t)$, it is defined as:

$$\begin{cases} {}_0I_t^\alpha x(t) = \frac{1}{\Gamma(\alpha)} \int_0^t (t - \xi)^{\alpha-1} x(\xi) d\xi \\ \mathcal{L}\{{}_0I_t^\alpha x(t)\} = s^{-\alpha} X(s) \end{cases} \quad (12)$$

where $\Gamma(\cdot)$ denotes the Gamma function. When $\alpha = 1$, Equation (11) reduces to the conventional integer-order reactive-power controller. When $\alpha > 1$, the magnitude attenuation slope of the fractional integral becomes -20α dB/dec, and its phase lag becomes $-90\alpha^\circ$. Therefore, the fractional order provides an additional degree of freedom for shaping the transient response of the internal voltage amplitude E .

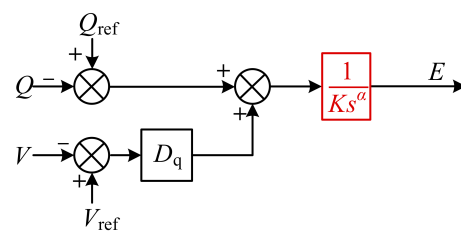


Figure 5. Control block diagram of the reactive-power loop with fractional-order control.

It should be noted that α is not varied or scheduled online in the proposed controller. It is determined offline through the feasible-region analysis presented in Section 3.2 and remains fixed during converter operation. Therefore, the proposed strategy does not introduce additional transients associated with online order switching.

The short-time behavior of the fractional integral can be further interpreted using a dimensionless normalized time variable. To ensure a dimensionally consistent comparison with the conventional first-order integral, the reference-time-normalized operator $T_r^{1-\alpha} s^{-\alpha}$ is considered, where $T_r = 1$ s is introduced only as a normalization reference rather than a sampling period. The constant factor $T_r^{1-\alpha}$ is included in the controller coefficient K in Equation (11). Defining:

$$\vartheta = \frac{t}{T_r} \quad (13)$$

the normalized unit-step responses of the fractional-order and conventional first-order integrals can be written as:

$$\begin{cases} \bar{y}_\alpha(\vartheta) = \frac{\vartheta^\alpha}{\Gamma(\alpha+1)} \\ \bar{y}_1(\vartheta) = \vartheta \end{cases} \quad (14)$$

For $1 < \alpha \leq 2$ and $0 < \vartheta < 1$, the following relation holds:

$$\frac{\vartheta^\alpha}{\Gamma(\alpha+1)} < \vartheta \quad (15)$$

Since the fault-induced inrush-current peak generally occurs within the first several tens of milliseconds, the corresponding normalized time satisfies $\vartheta \ll 1$. Therefore, the

fractional-order integral exhibits a slower normalized initial growth than the conventional first-order integral. This characteristic smooths the short-time variation in the internal voltage amplitude E and reduces the voltage-driving term of the fault current.

As a result, the fault-induced current trajectory can be reshaped at the source, suppressing the first current peak and the associated initial junction-temperature shock. However, increasing α also introduces additional phase lag and may reduce the stability margin of the reactive-power loop. Therefore, the fractional order cannot be selected arbitrarily. Its feasible range must be determined under stability, current-limiting, and thermal constraints, as discussed in the following subsection.

3.2. Constraint-Based Feasible-Region Identification for the Fractional Order

Although increasing the fractional order α can improve the attenuation of fault-induced high-frequency disturbances, α cannot be selected arbitrarily. A larger α also introduces additional phase lag and may reduce the damping margin of the reactive-power loop. Moreover, the electrical and thermal effects of α are not strictly monotonic: a lower peak current does not necessarily correspond to a lower junction-temperature peak because the thermal response also depends on the duration and energy accumulation of the fault current. Therefore, the admissible fractional orders should be identified within a feasible region constrained by closed-loop stability, transient current limitation, and junction-temperature safety.

3.2.1. System Stability Boundary Constraint

Using a standard power-system analysis approach, the VSG is linearized around a steady-state operating point. The equivalent power transmission model shown in Figure 6 can be obtained by taking the grid phase angle as the reference and calculating the equivalent impedance between the VSG and the grid.

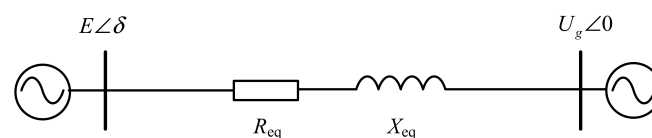


Figure 6. Equivalent circuit of the grid-connected converter system.

As illustrated in Figure 6, E denotes the internal electromotive force of the VSG, U_g represents the grid voltage, and δ indicates the phase angle difference between the VSG and the grid, also known as the power angle. R_{eq} and X_{eq} are the equivalent resistance and equivalent reactance between the VSG and the grid, respectively.

The three-phase complex power at the grid side can be expressed as:

$$S = P + jQ = 3U_g I^* \quad (16)$$

where I is the current injected into the grid by the VSG and can be expressed as:

$$I = \frac{E\angle\delta - U_g\angle 0}{R_{eq} + jX_{eq}} \quad (17)$$

where the superscript $*$ denotes the complex conjugate operation. Substituting the line current expression into the complex power equation yields the power transmission equation:

$$\begin{cases} P = 3 \frac{REU_g \cos \delta - RU_g^2 + XEU_g \sin \delta}{R^2 + X^2} \\ Q = 3 \frac{XEU_g \cos \delta - XU_g^2 - REU_g \sin \delta}{R^2 + X^2} \end{cases} \quad (18)$$

For the ideal-grid benchmark considered in this study, no separate grid-side impedance is introduced. The series coupling between the converter and the grid is represented by L_{eq} . Therefore, the equivalent impedance is predominantly inductive, with:

$$\begin{cases} R_{eq} \approx 0 \\ X_{eq} = \omega_0 L_{eq} \end{cases} \quad (19)$$

Under this inductive-coupling approximation, Equation (18) can be simplified as follows:

$$\begin{cases} P = \frac{3EU_g}{X_{eq}} \sin \delta \\ Q = \frac{3U_g}{X_{eq}} (E \cos \delta - U_g) \end{cases} \quad (20)$$

Linearizing Equation (20) around the steady-state operating point (E_0, δ_0) yields:

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \frac{3U_g}{X_{eq}} \begin{bmatrix} \sin \delta_0 & E_0 \cos \delta_0 \\ \cos \delta_0 & -E_0 \sin \delta_0 \end{bmatrix} \begin{bmatrix} \Delta E \\ \Delta \delta \end{bmatrix} \quad (21)$$

which indicates that the active and reactive power channels are generally coupled at a nonzero operating power angle. According to Equation (21), the incremental synchronizing coefficient between the active power and the power angle can be expressed as:

$$K_s = \left. \frac{\partial P}{\partial \delta} \right|_{(E_0, \delta_0)} = \frac{3E_0 U_g}{X_{eq}} \cos \delta_0 \quad (22)$$

when the converter operates around the nominal low-power-angle condition, namely $\delta_0 \approx 0$, $\sin \delta_0 \approx 0$, and $\cos \delta_0 \approx 1$, the synchronizing coefficient remains finite, and Equation (21) reduces to:

$$\begin{cases} \Delta P \approx \frac{3E_0 U_g}{X_{eq}} \Delta \delta \\ \Delta Q \approx \frac{3U_g}{X_{eq}} \Delta E \end{cases} \quad (23)$$

Accordingly, the P - δ and Q - E channels can be approximately decoupled in the vicinity of the nominal low-power-angle operating point. Under the condition $|\delta_0| \ll 1$, the steady-state active power remains small, whereas the incremental synchronizing coefficient defined in Equation (22) remains finite. Hence, Equation (23) characterizes the local small-signal sensitivity of active power to power-angle perturbations rather than the steady-state active-power level.

Based on this local operating condition and the VSG modeling procedure in reference [31], the open-loop transfer function of the fractional-order reactive-power loop is expressed as:

$$G_{qe}(s) = \frac{2.121(2E - U_g)}{KXs^\alpha + D_q X_{eq}} \quad (24)$$

To ensure consistency between the stability analysis and the practically implementable controller, the ideal fractional-order operator was replaced by the finite-dimensional Oustaloup rational approximation described in Section 3.3. For each value of α , the corresponding rational open-loop transfer function was constructed using the numerator and denominator coefficients generated in MATLAB 2024B. The Bode diagrams and phase margins shown in Figure 7 were calculated directly from these approximated open-loop transfer functions rather than from the ideal operator $s^{-\alpha}$. Therefore, the phase-margin results already include the phase characteristics introduced by the finite-band Oustaloup approximation. In the analysis, α was varied from 1 to 2 with an interval of 0.1.

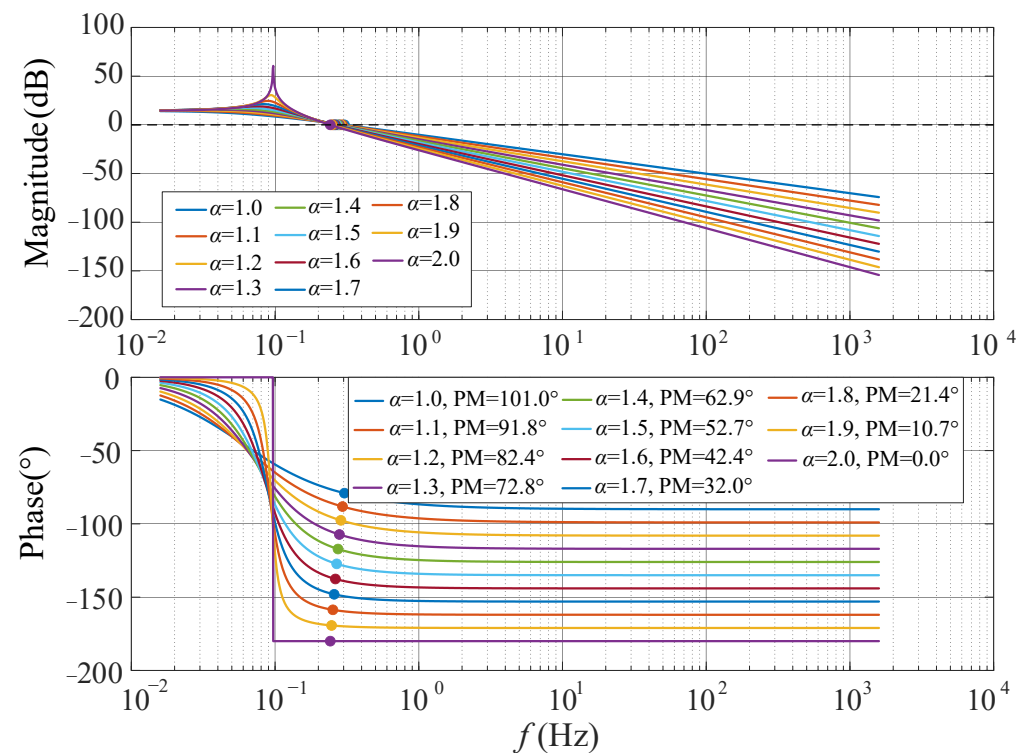


Figure 7. Open-loop Bode diagrams and phase margins based on the Oustaloup-approximated fractional-order controllers.

As indicated by the open-loop Bode plot, increasing α progressively degrades the phase margin, theoretically destabilizing the system at $\alpha = 2$. In practice, inherent factors such as low-pass filters and sampling delays introduce additional phase lag, causing premature instability well before α reaches 2. Furthermore, while a larger α enhances high-frequency attenuation, it simultaneously induces a low-frequency resonance peak, indicating diminished low-frequency damping. Consequently, configuring α necessitates a rigorous trade-off: an excessive value triggers instability and degrades low-frequency damping, whereas an insufficient value weakens high-frequency attenuation. The feasible parameter region satisfying these stability constraints is denoted by S_{stab} .

It should be noted that the stability region S_{stab} shown in Figure 7 is obtained around the nominal low-power-angle operating point. When the power angle changes abruptly, the operating point shifts, and the coupling between the active- and reactive-power loops becomes stronger. As the power angle increases, the synchronizing capability gradually weakens, while the cross-coupling between the power-angle and reactive-power channels becomes more pronounced. Therefore, fractional orders close to the upper stability boundary are more sensitive to power-angle disturbances, computational delays, and other unmodeled dynamics.

To maintain an adequate stability margin, the fractional order should be selected from the interior of the feasible region rather than near its upper boundary. As shown in Figure 7, the phase margin is 82.4° for $\alpha = 1.2$, but decreases to 21.4° and 0° for $\alpha = 1.8$ and $\alpha = 2.0$, respectively. Therefore, $\alpha = 1.2$ retains a substantial stability margin and can be regarded as an interior candidate for the subsequent electrical and thermal evaluations. Nevertheless, the stability analysis presented here is based on local small-signal characteristics and does not guarantee stable operation under arbitrarily large power-angle excursions. When the power angle approaches the power-transfer limit, the synchronizing capability decreases significantly, and the large-signal stability is mainly determined by the active-power synchronization loop.

The phase margin required for stable operation depends on the converter parameters, operating point, and nonlinear time-domain dynamics. Therefore, a universal fixed phase-margin threshold is not imposed in this study. Instead, a case-specific critical phase margin, denoted by PM_{lim} , is identified by comparing the frequency-domain phase margins with the corresponding time-domain responses of the scanned candidate orders. The stability constraint set is defined as:

$$S_{stab} = \{\alpha_k \in S_{scan} \mid PM(\alpha_k) \geq PM_{lim}\} \quad (25)$$

The numerical value of PM_{lim} is determined from the transition between the last stable candidate and the first unstable candidate under the specified test condition.

3.2.2. Electrical Safety Constraint for Transient Inrush Current Suppression

Beyond maintaining steady-state stability, the fractional-order control primarily aims to suppress extreme transient currents at the fault instant. The conventional integer-order controller, corresponding to $\alpha = 1$, is used as the electrical reference. Let $I_{peak}(\alpha)$ denote the maximum three-phase current envelope during the specified fault interval. A candidate satisfies the electrical constraint when its current peak does not exceed the integer-order baseline. As illustrated in Figure 8, varying the fractional order changes both the initial current peak and the subsequent transient-current trajectory. Although the current envelopes are not strictly ordered at every instant, the maximum absolute current extracted for each candidate order provides a quantitative indicator for evaluating the electrical safety constraint.

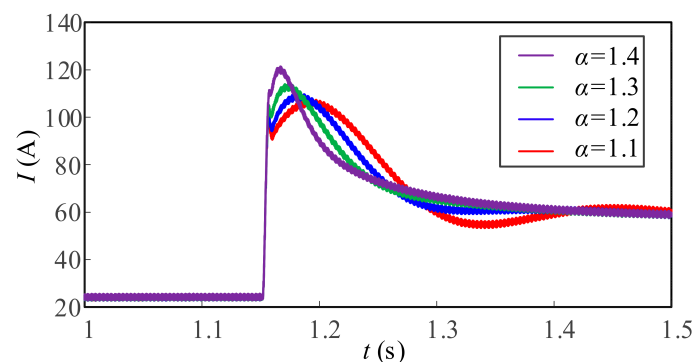


Figure 8. Transient-current envelopes under representative fractional orders.

For the specified voltage-sag case, the conventional integer-order controller corresponding to $\alpha = 1$ is adopted as the electrical reference. Let $I_{peak}(\alpha)$ denote the maximum three-phase current envelope during the fault interval. The current-constrained set is defined as:

$$S_{trad_max} = \{\alpha \in S_{scan} \mid I_{peak}(\alpha) \leq I_{peak}(1)\} \quad (26)$$

For the case study considered in this paper, the conventional integer-order current peak is $I_{peak}(1) = 136.64$ A. Therefore, a candidate order is accepted by the electrical constraint when its current peak does not exceed this baseline value. This numerical threshold is specific to the converter parameters and voltage-sag condition considered in this study.

3.2.3. Junction-Temperature Constraint

A lower transient current peak does not necessarily lead to a lower peak junction temperature. The thermal response depends on both the magnitude and duration of the

semiconductor losses. Based on the Foster thermal network, the junction-temperature response can be expressed as follows:

$$T_j(t) = T_c + \sum_{i=1}^n \int_0^t P_{loss}(\tau) \frac{R_{th,i}}{\tau_{th,i}} e^{-\frac{t-\tau}{\tau_{th,i}}} d\tau \quad (27)$$

where T_c is the heat sink baseplate case temperature; $R_{th,i}$ and $\tau_{th,i}$ are the thermal resistance and thermal time constant of the i -th order Foster branch, respectively.

Conventional integer-order control produces a larger but shorter-duration inrush current, whereas the long-memory behavior of the fractional-order operator can extend the transient-current tail. Although the peak current is reduced, the longer loss duration may increase thermal-energy accumulation and, consequently, the peak junction temperature. A comparison diagram is shown in Figure 9.

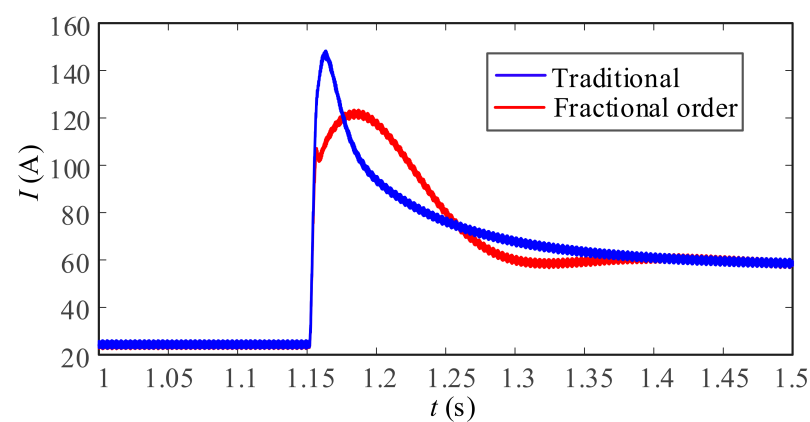


Figure 9. Comparison of upper envelopes of transient inrush currents between fractional-order control and traditional integral control.

For the thermal constraint, a junction-temperature limit of 125 °C is adopted for the present case study. This limit retains a 25 °C design margin relative to the rated maximum junction temperature of the selected semiconductor module. The margin is introduced to account for model uncertainty and transient thermal variation. The thermal constraint set is defined as

$$\begin{cases} S_{temp} = \left\{ \alpha_k \in S_{stab} \mid T_{j,peak}(\alpha_k) \leq T_{j,lim} \right\} \\ T_{j,lim} = 125 \end{cases} \quad (28)$$

This criterion excludes candidate orders that cause excessive thermal accumulation during the specified voltage-sag interval. The resulting set is denoted by S_{temp} .

3.2.4. Full-Range Parameter Sweep and Feasible-Region Identification

To establish a practical configuration standard, the independent constraints concerning system stability, transient current limiting, and thermal accumulation must be integrated. Consequently, the ultimate feasible domain $S_{feasible}$ for the fractional order α is strictly defined as the intersection of these three subdomains.

As illustrated in Figure 10, only the parameters located within the shaded intersection can simultaneously satisfy the requirements of grid-connected stability, inrush-current suppression, and thermal safety.

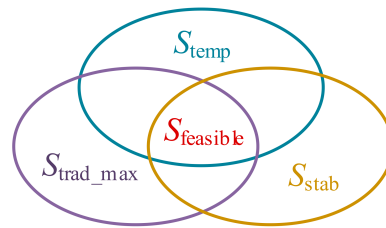


Figure 10. Schematic diagram of feasible region coupling.

To determine the numerical boundaries of the three constraint sets, a uniform parameter sweep is conducted over:

$$\alpha_k = 1.0 + 0.1k, \quad k = 0, 1, \dots, 10 \quad (29)$$

thus, the scan range is $[1.0, 2.0]$, and the resolution is $\Delta\alpha = 0.1$. The lower bound is set to $\alpha = 1.0$ because preliminary simulations under the specified voltage-sag condition show that orders below 1.0 produce current peaks higher than the integer-order baseline $I_{\text{peak}}(1)$ and therefore fail the electrical constraint. The point $\alpha = 1.0$ is retained as the conventional integer-order baseline. The points from $\alpha = 1.1$ to $\alpha = 2.0$ are evaluated as fractional-order candidates.

All candidates are tested under the same operating condition. The grid voltage decreases from 1.0 pu to 0.7 pu at $t = 1.13$ s, and the voltage sag lasts for 0.5 s. The circuit parameters, control gains, initial operating point, semiconductor model, and thermal network remain unchanged during the sweep.

For each candidate order, the phase margin, maximum three-phase current, and maximum IGBT junction temperature are recorded. The candidate is accepted only when the following three conditions are satisfied:

$$\begin{cases} PM(\alpha) \geq PM_{\text{lim}} \\ I_{\text{peak}}(\alpha) \leq I_{\text{peak}}(1) \\ T_{j,\text{peak}}(\alpha) \leq 125 \end{cases} \quad (30)$$

The three constraint sets are denoted by S_{stab} , $S_{\text{trad_max}}$, and S_{temp} , respectively. The final feasible set is obtained from:

$$S_{\text{feasible}} = S_{\text{stab}} \cap S_{\text{trad_max}} \cap S_{\text{temp}} \quad (31)$$

The identified numerical boundaries apply only to the specified case study. They may change with the converter rating, grid impedance, voltage-sag depth, fault duration, controller parameters, and semiconductor thermal characteristics.

The above procedure defines the numerical screening process for the fractional order, the complete flowchart is shown in Figure 11. The phase margin, current peak, and junction-temperature peak of each candidate order are obtained from the small-signal model and the PLECS electro-thermal simulation. The complete numerical results are presented in Section 5.3. It should be noted that the resulting boundaries are specific to the converter parameters and voltage-sag condition considered in this paper. They are used to illustrate the proposed constraint-based screening method and should not be interpreted as universal fractional-order limits.

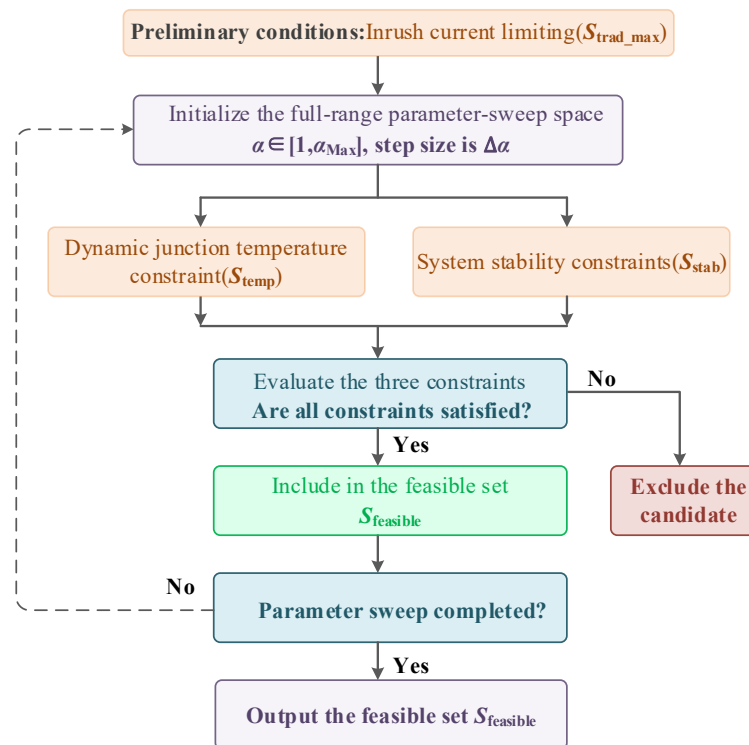


Figure 11. Flowchart of the full-range parameter sweep and constraint-based feasible-region identification.

3.3. Oustaloup Approximation of the Fractional-Order Operator

With the theoretical framework and feasible region established, the physical implementation of the fractional-order operator must be addressed. Given its infinite-dimensional nature, the ideal operator cannot be directly implemented in industrial electro-thermal coupled simulation software. Consequently, a high-order integer-order rational transfer function is employed to approximate it continuously within the core operational frequency band.

This paper adopts a continuous approximation strategy based on the Oustaloup recursive filtering algorithm. The core concept of this algorithm is to decompose the target fractional order α into a linear combination of a rounded-down integer part n and a pure fractional part γ :

$$\alpha = n + \gamma \quad (32)$$

Targeting this pure fractional part, the algorithm configures alternately distributed poles and zeros with logarithmic equal spacing between the specified lower frequency limit ω_b and upper frequency limit ω_h of the control system, thus precisely constructing a rational polynomial transfer function $G_\gamma(s)$ with a fitting order of $2N + 1$:

$$s^{-\gamma} \approx G_\gamma(s) = K \prod_{k=-N}^N \frac{s + \omega_{z,k}}{s + \omega_{p,k}} \quad (33)$$

where K is selected to match the magnitude response at the center frequency. The pole and zero frequencies are determined by the frequency-band boundaries and the fractional order as follows:

$$\begin{cases} \omega_{z,k} = \omega_b \left(\frac{\omega_h}{\omega_b} \right)^{\frac{k+N+0.5+0.5\gamma}{2N+1}} \\ \omega_{p,k} = \omega_b \left(\frac{\omega_h}{\omega_b} \right)^{\frac{k+N+0.5-0.5\gamma}{2N+1}} \end{cases} \quad (34)$$

The complete approximation is obtained by cascading the integer-order and fractional components:

$$G_{total}(s) = \frac{1}{s^n} G_\gamma(s) \quad (35)$$

To implement the above approximation in the electro-thermal simulation model, a MATLAB-based coefficient-generation program was developed. For each specified fractional order α , the program first decomposes it into the integer part $n = \lfloor \alpha \rfloor$ and the pure fractional part $\gamma = \alpha - n$. The fractional component $s^{-\gamma}$ is then approximated using the Oustaloup recursive filter, while the integer component s^{-n} is represented by conventional integral elements.

In this study, the approximation-order parameter was set to $N = 4$, yielding a ninth-order rational approximation for the pure fractional component. The frequency band of interest was selected as $[\omega_{\min}, \omega_{\max}] = [10, 10^5]$ rad/s, while the pole-zero distribution interval was extended to $[\omega_b, \omega_h] = [0.1, 10^7]$ rad/s to reduce the approximation errors near the frequency boundaries. The approximation gain was normalized at the logarithmic center frequency $\omega_m = 10^3$ rad/s, ensuring that the approximated and ideal fractional-order operators have the same magnitude at ω_m .

To quantitatively evaluate the accuracy of the rational approximation, the maximum magnitude and phase errors over the frequency band of interest are defined as:

$$\begin{cases} \varepsilon_M = \max_{\omega \in [\omega_{\min}, \omega_{\max}]} \left| 20 \log_{10} |G_\gamma(j\omega)| - 20 \log_{10} |(j\omega)^{-\gamma}| \right| \\ \varepsilon_\phi = \max_{\omega \in [\omega_{\min}, \omega_{\max}]} \left| \angle G_\gamma(j\omega) + 90\gamma^\circ \right| \end{cases} \quad (36)$$

For the selected order $\alpha = 1.2$, corresponding to $\gamma = 0.2$, the maximum magnitude and phase errors over the frequency band $[10, 10^5]$ rad/s were evaluated using the MATLAB-generated rational transfer function. The resulting errors were approximately 0.082 dB and 0.56° , respectively, indicating that the ninth-order approximation accurately reproduces the ideal fractional-order characteristics within the frequency band of interest.

The resulting numerator and denominator coefficients were directly assigned to a continuous-time transfer-function block in PLECS. Therefore, the Oustaloup rational approximation was implemented in continuous time and was not discretized in the present electro-thermal simulation. Consequently, no independent controller sampling period or discrete transformation method was introduced for this fractional-order block. The discrete-time realization and the corresponding sampling-period selection will be considered in future real-time digital implementation.

4. Coordinated GDPWM and Switching-Frequency Reduction for Post-Transient Thermal Regulation

The fractional-order reactive power control developed in Section 3 is mainly responsible for suppressing the current surge at fault inception and the associated initial junction-temperature shock. However, after the first transient peak is reduced, the converter may still experience sustained thermal accumulation during the remaining fault-ride-through interval. This section therefore introduces a complementary active thermal regulation layer based on GDPWM and switching-frequency reduction. The objective is to reduce post-transient thermal stress without changing the main fractional-order current-suppression mechanism.

4.1. GDPWM-Based Thermal Regulation

GDPWM is introduced as one of the post-transient thermal-regulation measures because it reduces switching actions during high-current intervals without changing the

nominal switching frequency. Its basic principle is to inject an appropriate zero-sequence voltage into the three-phase modulation references, so that one bridge leg is clamped during selected intervals. When the clamping interval is aligned with the phase-current peak, switching losses can be reduced in the high-current region, thereby lowering the junction-temperature rise.

Let u_a , u_b , and u_c denote the three-phase reference voltages. The maximum and minimum reference values are first extracted as:

$$\begin{cases} v_{\max} = \max(u_a, u_b, u_c) \\ v_{\min} = \min(u_a, u_b, u_c) \end{cases} \quad (37)$$

The clamping offset angle is denoted by φ_α . After the Clarke transformation, the fundamental phase angle θ is obtained. The control angle θ_{ctrl} and the sector index k are calculated as:

$$\begin{cases} \theta_{\text{ctrl}} = (\theta + \varphi_\alpha) \bmod 360^\circ \\ k = \left\lfloor \frac{\theta_{\text{ctrl}} + 30^\circ}{60^\circ} \right\rfloor \bmod 6 \end{cases} \quad (38)$$

where $k \in \{0, 1, 2, 3, 4, 5\}$. Even sectors correspond to positive half-cycle peak regions, whereas odd sectors correspond to negative half-cycle peak regions. The injected zero-sequence component is then defined as:

$$u_z = \begin{cases} 1 - v_{\max}, k \in \{0, 2, 4\} \\ -1 - v_{\min}, k \in \{1, 3, 5\} \end{cases} \quad (39)$$

The final modulation references are obtained by adding u_z to the original three-phase references and comparing them with the triangular carrier, as shown in Figure 12. GDPWM reduces switching actions near the phase-current peaks while retaining the nominal switching frequency.

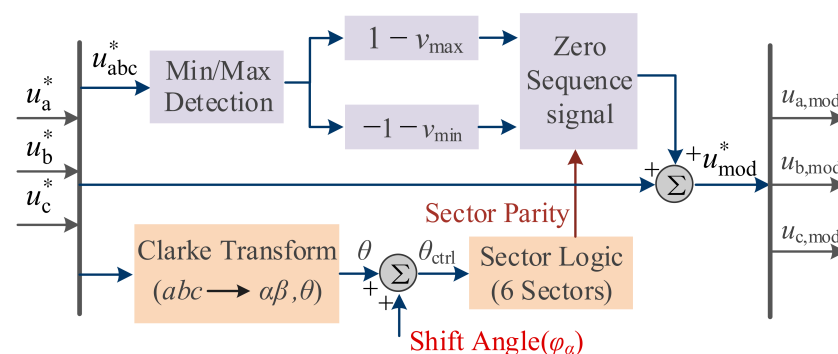


Figure 12. GDPWM control block diagram.

4.2. Switching-Frequency Reduction for Thermal Regulation

Switching-frequency reduction is applied together with GDPWM to further reduce average switching losses under severe thermal stress. According to the switching-loss model in Section 2.3, the switching loss is approximately proportional to the switching frequency. Therefore, decreasing f_{sw} can reduce the average switching loss and slow down the junction-temperature rise. However, this method also increases the harmonic current. The RMS value of the phase-current harmonic can be expressed as:

$$I_x = \sqrt{\left(\frac{U_{dc}}{24L_s f_{\text{sw}}}\right)^2 \cdot HDF} \quad (40)$$

where x denotes phase a , b , or c ; U_{dc} is the DC-link voltage; L_s is the total inductance of the harmonic-current path; f_{sw} is the switching frequency; and HDF is the harmonic distortion function determined by the modulation strategy.

Equation (40) shows that the harmonic current is inversely related to f_{sw} . Therefore, excessive switching-frequency reduction may degrade current quality and affect the grid-connected performance of the converter. In the proposed coordinated scheme, switching-frequency reduction is applied together with GDPWM during the post-transient fault interval. This measure further reduces the cumulative switching energy, while GDPWM redistributes the switching actions away from high-current intervals.

4.3. Coordinated Implementation of GDPWM and Switching-Frequency Reduction

During the post-transient fault interval, GDPWM and switching-frequency reduction are activated simultaneously. GDPWM shifts switching actions away from the phase-current peaks, while the reduced switching frequency decreases the total number of switching events. Their coordinated action reduces both high-current switching losses and cumulative switching energy, thereby mitigating the junction-temperature rise without requiring an additional thermal activation threshold.

5. Electro-Thermal Simulation Results and Analysis

5.1. Simulation Platform and Test Conditions

To verify the proposed fractional-order control strategy, a full-order electro-thermal model of the GFM converter was built in PLECS. The model was used to evaluate the electrical transient response and the junction-temperature variation under severe grid voltage sags. Since destructive tests under extreme grid faults may involve high hardware cost and equipment risk, the simulation platform provides a safe and repeatable basis for quantitative analysis.

The simulated system consists of a GFM converter connected to an ideal grid-voltage source through a lumped-equivalent coupling inductance. No separate grid-side resistance or inductance is introduced in the PLECS model. The parameter L_{eq} represents the total series inductive effect between the converter and the grid in this benchmark configuration. The main circuit consists of a dc voltage source, a three-phase full-bridge inverter, an LC filter, and an ideal three-phase grid voltage source. The conventional integer-order reactive-power loop is replaced by the proposed fractional-order structure, while the other VSG control loops remain unchanged.

In Table 2, T_a is the ambient temperature; U_{dc} is the dc-link voltage; U_g is the peak value of the grid phase voltage; f_0 and f_{sw} are the rated grid frequency and nominal switching frequency, respectively; and L_{eq} is the total series coupling inductance between the converter and the grid in this benchmark model. P_{ref} and Q_{ref} are the active- and reactive-power references. J is the virtual moment of inertia, D_p is the active-power-frequency damping coefficient, D_q is the reactive-power-voltage droop coefficient, and K is the integral coefficient of the voltage-amplitude regulation loop. $K_{p,V}$ and $K_{i,V}$ are the proportional and integral gains of the inner voltage loop, whereas $K_{p,I}$ and $K_{i,I}$ are the corresponding gains of the inner current loop.

The manufacturer-provided PLECS electro-thermal model of the FF50R12RT4 module was directly employed. Its temperature- and current-dependent conduction characteristics, switching-energy characteristics, antiparallel-diode losses, and transient thermal impedance were used to calculate the semiconductor losses and junction-temperature response. The Foster thermal-network parameters are listed in Table 1, while the main circuit and control parameters are summarized in Table 2. All initial operating points were

set within the rated operating range to ensure stable grid-connected operation before the voltage sag was applied.

Table 2. PLECS Simulation Parameter Settings.

Parameter	Value	Parameter	Value
T_a	25 °C	U_{dc}	800 V
U_g	311 V	f_0	50 Hz
f_{sw}	10 kHz	L_{eq}	2.5 mH
P_{ref}	10 kW	Q_{ref}	0 kvar
J	0.02	D_p	50
D_q	200	K	540
$K_{p,V}$	5	$K_{i,V}$	50
$K_{p,I}$	0.5	$K_{i,I}$	5

Note: The grid is modeled as an ideal voltage source. No separate grid-side resistance or inductance is introduced. The total series coupling inductance is represented by L_{eq} .

Although the above PLECS model includes the semiconductor loss characteristics and the Foster thermal network, the present validation remains model-based. It cannot fully reproduce all nonideal factors of a physical converter. These factors include sensing noise, sampling and computational delays, PWM dead time, parasitic parameters, device-parameter dispersion, and thermal-interface uncertainty. Therefore, the results mainly verify the proposed control mechanism and the relative electro-thermal response trends under the specified conditions. They should not be interpreted as complete experimental validation. Real-time hardware-in-the-loop and laboratory prototype tests are still required to evaluate controller discretization, implementation delay, protection interaction, and parameter uncertainty.

5.2. Verification of Fractional-Order Inrush Current Suppression

To verify the transient current suppression capability of the proposed fractional-order VSG control, a symmetrical three-phase voltage sag is applied at 1.13 s. As shown in Figure 13c, the grid voltage amplitude decreases from 1.0 pu to 0.7 pu and remains at this level for 0.5 s.

Under the conventional integer-order VSG control, the fixed first-order integral operator in the reactive-power loop provides limited freedom for shaping the internal voltage response during the fault transient. As shown in Figure 13a, the converter terminal current exhibits a pronounced transient peak at the fault instant. The maximum three-phase current reaches 136.64 A, which may increase the risk of overcurrent protection and gate-pulse blocking.

For comparison, Figure 13b shows the response under the proposed fractional-order VSG control with $\alpha = 1.3$. This order is adopted here as an additional representative fractional-order case to present the transient-current waveform under a different fractional order and to avoid repeating the $\alpha = 1.2$ waveform analyzed in the subsequent feasible-region validation. It should be noted that $\alpha = 1.3$ is used only for this illustrative comparison, whereas $\alpha = 1.2$ is identified as the preferred feasible value through the combined stability, transient-current, and junction-temperature constraints. With $\alpha = 1.3$, the peak transient current is reduced to 118.85 A. Compared with the conventional integer-order controller, the current peak is reduced by approximately 13.02%.

The improvement is consistent with the analysis in Section 3. The fractional-order integral operator provides an additional degree of freedom and enhances the attenuation of fault-induced high-frequency components. As a result, the transient variation in the internal voltage amplitude is smoothed, and the voltage-driving term of the fault current is reduced.

The lower current peak also helps reduce the initial loss stress of the semiconductor devices, which provides the basis for the subsequent electro-thermal evaluation. This result indicates that the fractional-order operator can effectively reshape the fault-current trajectory by modifying the transient response of the reactive-power loop.

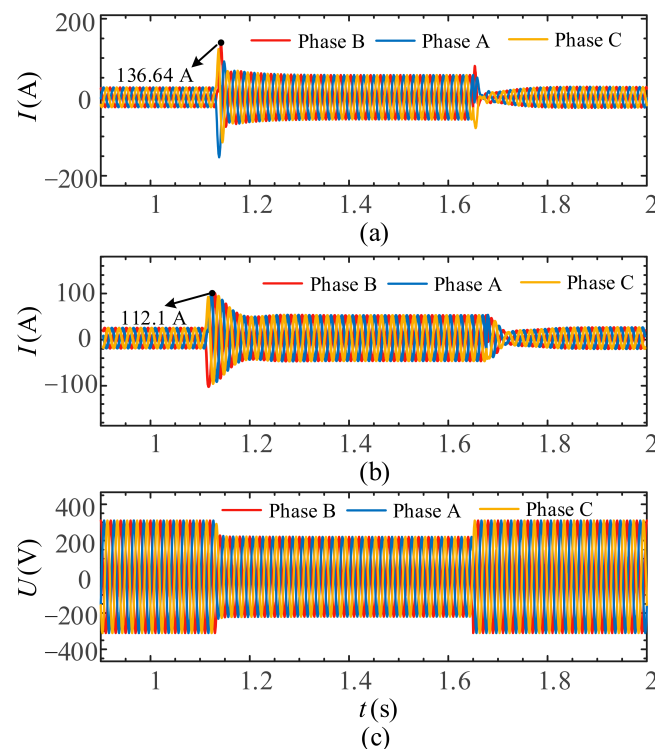


Figure 13. Comparison of operational waveforms with and without fractional-order control: (a) conventional integer-order control, (b) fractional-order control, (c) grid-voltage waveforms.

To place the above result in the context of existing fault-current suppression strategies, the proposed method is further compared with representative virtual-impedance and dedicated current-limiting methods.

As discussed in the Introduction, virtual impedance limits the fault current by increasing the equivalent output impedance of the converter. This method has a simple structure, but its performance depends on the selected impedance parameters. A large virtual impedance may also weaken terminal-voltage support during severe faults. Dedicated current-limiting methods directly modify or clamp the current or voltage reference to impose an explicit current bound. However, the associated control-mode transition may affect the voltage-source characteristics, synchronization dynamics, and fault-recovery process of the GFM converter.

The proposed method follows a different control principle. It reshapes the transient response of the internal voltage amplitude through the fractional-order reactive-power loop. Its main purpose is to reduce the current surge at fault inception rather than to impose a hard current limit. Therefore, it should be regarded as a complementary fault-current suppression method rather than a universal replacement for virtual impedance or dedicated current limiters. It can also be coordinated with these methods as an auxiliary control layer. By reducing the initial current stress, the proposed method may lessen the subsequent intervention burden on the main current-limiting or protection mechanism. A concise method-level comparison is provided in Table 3.

Table 3. Qualitative comparison of representative fault-current suppression methods.

Method	Control Mechanism	Main Advantage	Main Limitation
Virtual impedance	Increase equivalent output impedance	Simple structure	Parameter sensitivity; reduced voltage support
Dedicated current limiting	Modify or clamp current/voltage reference	Explicit current bound	Mode transition; synchronization impact
Proposed method	Reshape internal-voltage transient	Initial-surge suppression; electro-thermal screening	Case-specific order selection; simulation-based validation

The above comparison clarifies the control role of the proposed method. The numerical feasibility of the fractional-order selection is further evaluated in the following subsection.

5.3. Numerical Validation of the Case-Specific Feasible Region

To validate the feasible-region identification procedure presented in Section 3.2.4, all candidate orders from $\alpha = 1.0$ to $\alpha = 2.0$ were evaluated with a resolution of $\Delta\alpha = 0.1$. The same circuit parameters, control gains, initial operating point, semiconductor model, and voltage-sag condition were used for all candidates. For each order, the phase margin, maximum current, and maximum IGBT junction temperature were recorded. The complete numerical screening results are summarized in Table 4.

Table 4. Complete numerical screening results under the specified voltage-sag condition.

α	PM (°)	I_{peak} (A)	$T_{j,\text{peak}}$ (°C)	S_{stab}	$S_{\text{trad_max}}$	S_{temp}	S_{feasible}
1.0	101.0	136.64	135.0	✓	Baseline	×	×
1.1	91.8	127.8	128.6	✓	✓	×	×
1.2	82.4	118.9	122.5	✓	✓	✓	✓
1.3	72.8	112.1	126.4	✓	✓	×	×
1.4	62.9	109.2	128.9	✓	✓	×	×
1.5	52.7	106.9	131.3	✓	✓	×	×
1.6	42.4	N/A	N/A	×	×	×	×
1.7	32.0	N/A	N/A	×	×	×	×
1.8	21.4	N/A	N/A	×	×	×	×
1.9	10.7	N/A	N/A	×	×	×	×
2.0	0.0	N/A	N/A	×	×	×	×

The results in Table 4 represent a numerical example under the operating condition considered in this paper. The identified boundaries may change with the converter rating, grid impedance, voltage-sag depth, fault duration, controller parameters, and semiconductor thermal characteristics.

Table 4 provides the complete numerical basis for the feasible-region identification under the specified voltage-sag condition. The system remains stable at $\alpha = 1.5$, where the phase margin is 52.7° , but becomes unstable at $\alpha = 1.6$, where the phase margin decreases to 42.4° . Therefore, the case-specific critical phase margin satisfies:

$$42.4^\circ < PM_{\text{lim}} \leq 52.7^\circ \quad (41)$$

The final feasible set is therefore:

$$\begin{cases} S_{\text{stab}} = \{1.0, 1.1, 1.2, 1.3, 1.4, 1.5\} \\ S_{\text{trad_max}} = \{1.0, 1.1, 1.2, 1.3, 1.4, 1.5\} \\ S_{\text{temp}} = \{1.2\} \\ S_{\text{feasible}} = S_{\text{stab}} \cap S_{\text{trad_max}} \cap S_{\text{temp}} = \{1.2\} \end{cases} \quad (42)$$

This result applies only to the system parameters and fault condition considered in this study. Other converter ratings, grid conditions, and thermal models may result in different numerical boundaries.

To further illustrate the dynamic characteristics of different constraint regions, several representative orders were selected for waveform comparison. The values $\alpha = 0.8, 1.2, 1.4$, and 1.8 represent the sub-unity region, the preferred feasible region, the thermally constrained region, and the unstable region, respectively.

When $\alpha = 0.8$, the fractional order is lower than the integer-order baseline. As shown in Figure 14, the converter presents a high transient current peak at the fault instant. The maximum current reaches 181.4 A, and the peak junction temperature reaches 135.5 °C. This result indicates that $\alpha < 1$ weakens the attenuation capability of the reactive-power loop and is not suitable for transient current suppression under severe voltage sags.

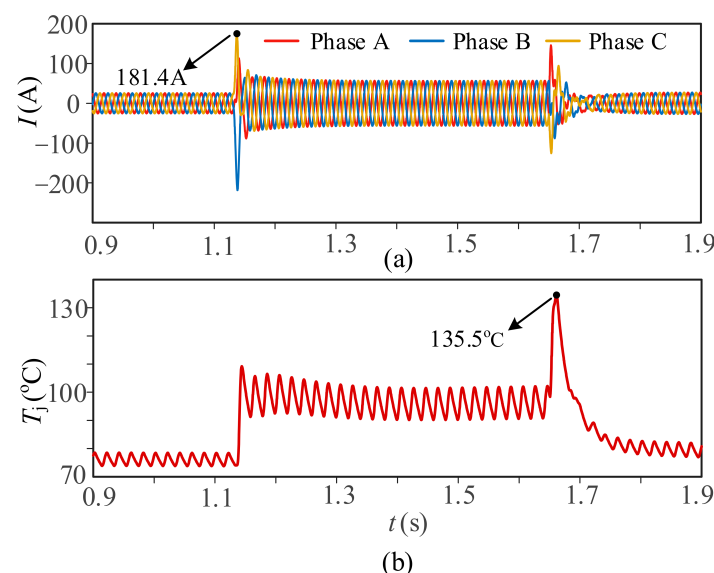


Figure 14. Waveforms under fractional-order control with $\alpha = 0.8$: (a) current waveforms, (b) junction temperature waveforms.

When α is increased to 1.2, the operating point enters the feasible region. As shown in Figure 15, the transient current peak is reduced to 118.9 A. The peak junction temperature is also reduced to 122.5 °C. Compared with the $\alpha = 0.8$ case, both electrical stress and thermal stress are reduced. This result is consistent with the mechanism analyzed in Section 3. A fractional order greater than one provides stronger high-frequency attenuation and smooths the transient response of the reactive-power loop.

When α is further increased to 1.4, the transient current peak is reduced to 109.2 A, as shown in Figure 16. However, the peak junction temperature increases to 128.9 °C. This result shows that current suppression and thermal response are not strictly monotonic with respect to α . Although a larger fractional order can further reduce the current peak, it may also change the duration and waveform of the transient current. The accumulated semiconductor loss may therefore increase. This confirms that the fractional order should not be selected only according to the minimum current peak.

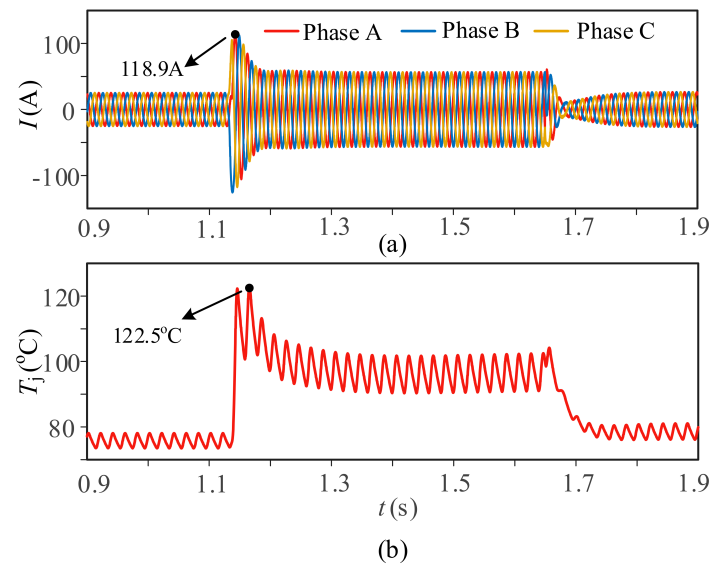


Figure 15. Waveforms under fractional-order control with $\alpha = 1.2$: (a) current waveforms, (b) junction temperature waveforms.

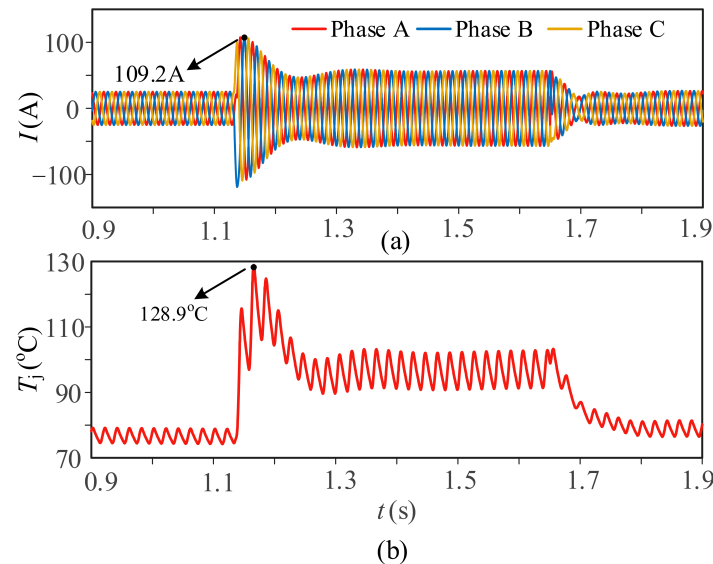


Figure 16. Waveforms under fractional-order control with $\alpha = 1.4$: (a) current waveforms, (b) junction temperature waveforms.

When $\alpha = 1.8$, the closed-loop system becomes unstable, as shown in Figure 17. The three-phase current loses its regular waveform and increases rapidly, indicating that this fractional order lies outside the admissible stability region. Figure 17b retains the thermal-model output directly calculated by PLECS after the onset of electrical instability. However, once the electrical subsystem becomes unstable, the calculated semiconductor losses no longer correspond to a physically valid converter operating condition. Therefore, the rapidly increasing thermal-model output should be interpreted only as a numerical consequence of the unstable electrical response rather than as a physically meaningful junction-temperature waveform. Consequently, no reliable current peak or junction-temperature peak is reported for this case, and $\alpha = 1.8$ is excluded from the feasible region.

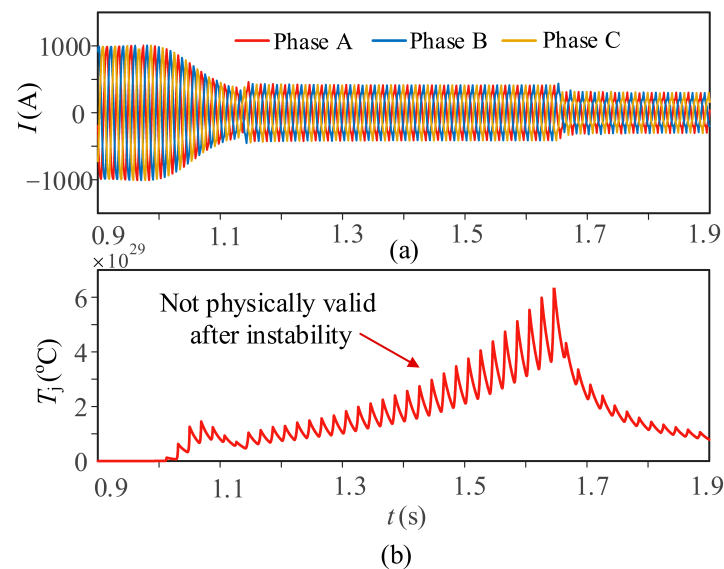


Figure 17. Responses under fractional-order control with $\alpha = 1.8$: (a) unstable three-phase current response; (b) PLECS-calculated thermal-model output after electrical instability.

The above results support the feasible-region analysis presented in Section 3. Although $\alpha = 1.4$ reduces the current peak from 118.9 A to 109.2 A compared with $\alpha = 1.2$, its junction-temperature peak increases from 122.5 °C to 128.9 °C. This is because the larger fractional order suppresses the initial current peak but prolongs the subsequent current and loss responses. The slower branches of the Foster thermal network, with time constants of 0.05 and 0.1 s, continue to accumulate the losses associated with this extended transient tail. Therefore, a lower current peak does not necessarily result in a lower junction-temperature peak. Among the tested cases, $\alpha = 1.2$ provides the preferred feasible compromise among current suppression, junction-temperature limitation, and stability margin. It should also be emphasized that $\alpha = 1.2$ is fixed throughout the subsequent simulations and is located well inside the stable region rather than close to its upper boundary. It is therefore selected as a conservative feasible value rather than a mathematically optimized solution. This conservative selection reduces the sensitivity of the controller to power-angle excursions and additional phase delays that are not fully represented by the nominal small-signal model.

5.4. Evaluation of Post-Transient Thermal Regulation

Based on the identified feasible region and the comparative results in Table 4, $\alpha = 1.2$ was selected as the preferred feasible value for the subsequent post-transient thermal evaluation. Under this setting, a three-phase voltage sag with a depth of 0.3 pu was applied at 1.13 s and lasted for 0.5 s. The junction-temperature responses under different modulation measures are shown in Figure 18.

With only the fractional-order VSG control, the transient current peak was suppressed, but heat accumulation still occurred during the remaining fault interval. The peak junction temperature reached 122.47 °C, and the average junction temperature during the fault was 98.01 °C. This result shows that the fractional-order controller mainly addresses the current surge at fault inception, while the post-transient thermal response still depends on the switching-loss distribution.

GDPWM reduces the peak junction temperature from 122.47 °C to 108.6 °C by reducing switching actions near the phase-current peaks. When GDPWM is combined with switching-frequency reduction, the peak junction temperature is further reduced to 104.6 °C. These results indicate that the two measures provide complementary reductions in post-transient thermal accumulation under the simulated condition.

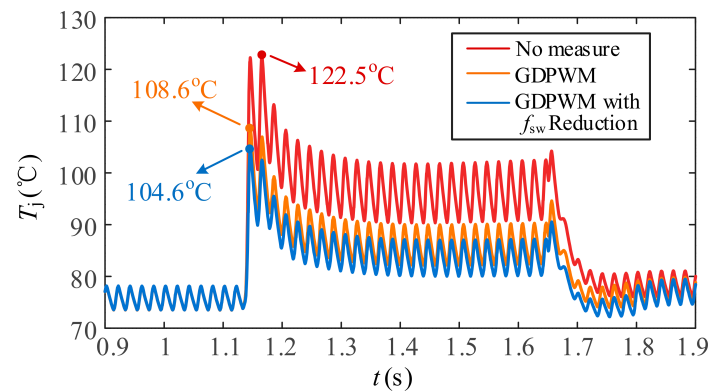


Figure 18. Junction temperature waveforms under different thermal control measures.

6. Conclusions

This paper proposed a fractional-order electro-thermal coordinated control strategy for improving the fault-ride-through capability of GFM converters under grid fault conditions. The main focus was placed on the fractional-order reconstruction of the reactive-power loop by reshaping the internal-voltage dynamics that drive the fault current. The main conclusions are as follows.

- (1) A fractional-order operator was introduced into the reactive power control loop of the VSG-based GFM converter. Compared with the conventional integer-order controller, the proposed fractional-order loop provides an additional order degree of freedom for shaping the transient response of the internal voltage amplitude. This helps reduce the voltage mismatch between the converter and the sagged grid during the initial fault stage, thereby suppressing the transient inrush current and the associated initial junction-temperature shock. In addition, the feasible region of the fractional order was identified through a full-range parameter sweep under stability-margin, current-limitation, and junction-temperature constraints, providing a systematic alternative to empirical order selection.
- (2) A complementary post-transient thermal regulation strategy was introduced to mitigate the thermal accumulation that remains after the initial current surge is suppressed. GDPWM and switching-frequency reduction are applied simultaneously and operate in coordination to reduce switching losses and cumulative thermal stress during the sustained fault period. Their combined action reduces the simulated junction-temperature rise and increases the available thermal margin.
- (3) Electro-thermal co-simulation provided model-based validation of the proposed framework under the specified voltage-sag condition. The fractional-order reactive-power loop reduced the transient current peak relative to the integer-order baseline. The constraint-based screening procedure provided a numerical basis for selecting the fractional order. The coordinated thermal-regulation measures further reduced post-transient thermal accumulation. These results support the feasibility of the proposed mechanism, but they do not replace real-time or experimental validation.

Future work will implement the fractional-order controller on a real-time digital platform. Hardware-in-the-loop and laboratory-scale converter tests will be conducted under different voltage-sag depths, fault durations, grid strengths, and fault types. Quantitative comparisons with virtual-impedance and dedicated current-limiting methods will also be performed under identical hardware and fault conditions.

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