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Simple Scheme for the Implementation of Low Voltage Fully Differential Amplifiers without Output Common-Mode Feedback Network

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Abstract: A simple scheme to implement class AB low-voltage fully differential amplifiers that do not require an output common-mode feedback network (CMFN) is introduced. It has a rail to rail output signal swing and high rejection of common-mode input signals. It operates in strong inversion with ±300 mV supplies in a 180 nm CMOS process. It uses an auxiliary amplifier that minimizes supply requirements by setting the op-amp input terminals very close to one of the rails and also serves as a common-mode feedback network to generate complementary output signals. The scheme is verified with simulation results of an amplifier that consumes 25 µW, has a gain-bandwidth product (GBW) of 16.1 MHz, slew rate (SR) of 8.4 V/µs, the small signal figure of merit (FOM_{SS}) of 6.49 MHz*pF/µW, the large signal figure of merit (FOM_{LS}) of 3.39 V/µs*pF/µW, and current efficiency (CE) of 2.03 in strong inversion, with a 10 pF load capacitance.

Keywords: low voltage amplifiers; class AB operational amplifiers; analog integrated circuits

1. Introduction

As CMOS technologies scale down, supply voltage requirements have been reduced. The need for transistor size and power supply scaling has been motivated by the rapid increase in the market of portable devices (i.e., for Internet of Things and biomedical applications) and their need for low-voltage, low-power circuitry to increase battery time [1]. Analog circuits, contrary to their digital counterpart, have not easily adapted to the rapid supply voltage downscaling, mostly due to the fact that the threshold voltages have been reduced at a much lower rate than the supply voltage and currently represent a significant fraction of the nominal supply voltage in current deep sub-micrometer CMOS technologies [2]. The minimum supply voltage of circuits with operational amplifiers is determined by the headroom HR_{DP} of the differential input stage. Signals in conventional op-amp topologies usually have a mid-supply common-mode component to allow for maximum and symmetrical peak-peak signal swing close to the supply voltage. This requires a minimum supply $V_{supplyMIN} = 2HR_{DP}$ in conventional architectures. With the current values of supply and threshold voltages, this biasing no longer allows transistors to operate in strong inversion in conventional amplifiers.

Several techniques have been proposed to solve this problem. Bulk driven (BD) amplifiers [3–7] can operate with reduced supply voltages; however, the bulk-to-source transconductance g_{mb} of MOS transistors is significantly lower than their gate-to-source transconductance g_m (by approximately a factor 5). An additional degradation factor of BD circuits comes from the fact that PMOS differential pairs are commonly used in the input stage of BD amplifiers. PMOS transistors have an additional factor 3–5 lower transconductance gain than NMOS transistors with the same bias current and dimensions.

This degrades the performance of bulk driven circuits in terms of bandwidth, noise, DC offset and causes their figure of merit $FOM = GBWCL/P_{diss}$ and power efficiency to be lower than that of their gate driven (GD) counterparts for similar bias currents (P_{diss} is the static power dissipation, and CL is the load capacitance). An additional disadvantage of BD circuits is that their input swing is severely limited in order to prevent forward biasing of the MOS transistor substrate-source and substrate-drain PN junctions that can lead to destructive latch-up. This constrains BD circuits to operate in subthreshold with supply voltages lower than 0.6 V and with small gain-bandwidth products (GBWs, typically lower than 50 kHz). Circuits with floating gates input differential pairs have been reported for the implementation of gate driven low supply circuits with transistors in saturation [8]. Since they are based on capacitive voltage dividers at the input terminals of the op-amp, they are also subject to GBW, noise, and offset degradation. Circuits with quasi-floating gate transistors overcome these problems and can operate with low supply voltages, but they require a DC offset cancellation circuit to prevent saturation of the output nodes [9]. Two non-conventional techniques of digital-based (DB) operational transconductance amplifiers (OTAs) have been proposed for the implementation of low supply voltage systems. One of them is based on "time signal processing" and is characterized by relatively small and large signal FOM [10]. The other one is based on the digital implementation of differential pairs using inverters [11]. This technique has large FOMs and has been refined to introduce digital calibration [12], but it is characterized by relatively low CMRR and open-loop gain, and their voltage gain accuracy (when implementing amplifiers) does not depend on component ratios.

Two families of gate driven low voltage techniques with transistors in saturation are based on DC level shifting techniques, which cause the op-amp input terminals to operate very close to a supply rail. This provides headroom HR_{DP} for the op-amp NMOS differential input stage, which is close to the total supply voltage $HR_{DP} \cong V_{supply} = |V_{DD} - V_{SS}|$ and allows reduction by almost a factor 2 of the minimum supply voltage $V_{supplyMIN}$. One of the families is based on *voltage-mode techniques* and uses floating DC voltage sources [13]. This technique inserts floating DC voltage sources (see Figure 1) with value $V_{DDP} = V_{DD} - V_{DSsat} \cong V_{DD} - 0.1V$ inserted in series with the op-amp input terminals (an NMOS input differential pair is assumed). The floating DC sources are implemented, as shown in Figure 1, with a resistor R_{bat} and matches sinking and sourcing current sources I_{bat} that satisfy $V_{DDP} = I_{bat}R_{bat}$. They allow signal nodes Z, Z' to operate at the mid-supply voltage and maintain at the same time the op-amp input terminals at a voltage V_{DDP} (close to V_{DD}), which reduces the minimum supply requirements by close to a factor two $\left(V_{DDsupplyMIN} \sim HR_{DP}\right)$. A drawback of this approach is the additional noise introduced by the resistors R_{bat}. A *current-mode family* of low voltage amplifiers is based on current source DC level shifting techniques. They apply common-mode level shifting currents I_{CM} at the op-amp input terminals. These currents pull the voltage level at the input terminals of the op-amp to a voltage V_{DDP} close to the upper rail. The injected currents I_{CM} must satisfy the condition $I_{CM} = V_{DDP}/(R1 \| R2) - \left(V_{CMinp}/R_1 + V_{refCM}/R_2\right)$, where $V_{CMinp} = \left(V_{inp}^{+} + V_{inp}^{-}\right)/2$ is the common-mode voltage of the input signals V_{inp}^{+} and V_{inp}^{-}, and V_{refCM} is the reference common-mode output voltage.

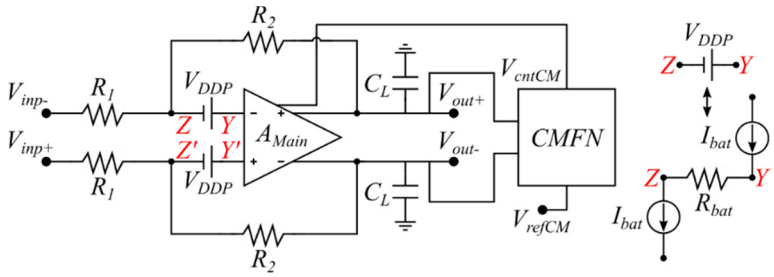


Figure 1. Voltage-mode technique using floating batteries.

In the implementation of Figure 2 [14,15], pull-up resistors R_{PU} with fixed value $R_{PU} = (V_{DD}/V_{DDP} - 1)(R_1 \| R_2)$ are used to generate constant currents $I_{CM}' = V_{DDP}/(R_1 \| R_2)$, which assume a constant input common-mode component (usually $V_{refCM} = 0$) and constant supply V_{DD}. Due to the fixed value of R_{PU}, the scheme is not functional if common-mode input signals are present or if there are variations in the supply voltage V_{DD}. Another drawback is that for V_{DD} close to V_{DDP}, the pull-up resistors R_{PU} are required to have values $R_{PU} \ll R_1 \| R_2$; this leads to significant degradation of the amplifier's bandwidth and offset since R_{PU} is an integral part of the amplifier's feedback network β, and R_{PU} decreases the value of the feedback factor β. This degrades the bandwidth (BW) given by $BW = \beta(GBW)$. It can also significantly increase the output DC offset voltage and noise. Figure 2 illustrates another implementation of the current source level shifting scheme reported in [16]. In this implementation level, shifting currents I_{CM}, which include a component dependent on the common-mode input signal V_{CMinp}, are injected at the op-amp input terminal. The common-mode input voltage $V_{CMi} = \left(V_i^+ + V_i^-\right)/2$ of the op-amp input terminals is sensed using resistors R_{CMi} in the main amplifier. An auxiliary amplifier A_{AUX} drives transistors M1, M1'; this generates matched currents I_{CM}, which leads to $V_{CMi} = V_{DDP}$. This scheme is functional with variable supply voltage and variable common-mode input voltage V_{CMinp}, but the common-mode sensing resistors R_{CMi} also lead to bandwidth and offset degradation. This is to a much lower degree than the scheme of Figure 2 since no condition is placed on the value of R_{CMi}, which can take values $R_{CMi} \gg R_1$ to minimize BW and offset degradation. The three fully differential low-voltage amplifier schemes of Figures 1 and 2 require a relatively complex output common-mode feedback network that can also operate with a low supply voltage.

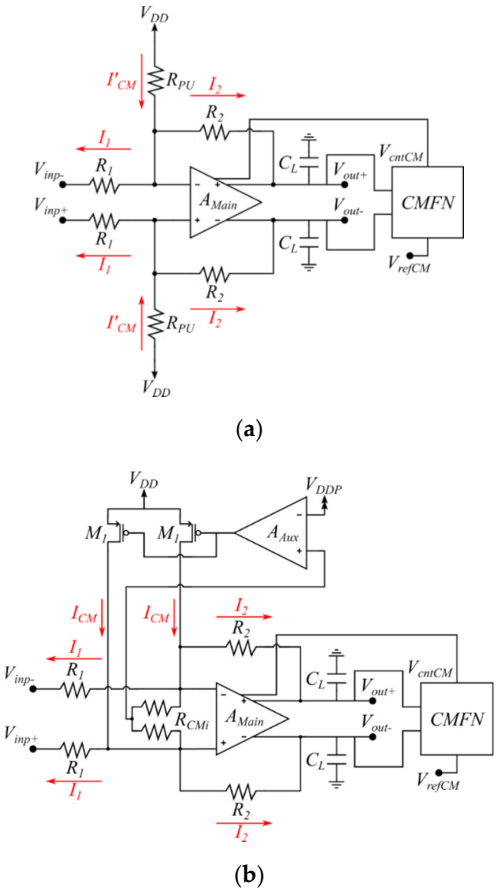


Figure 2. (**a**) Current mode low voltage technique I: pull up resistor level shifting technique. (**b**) Current mode technique II: current source level shifting technique.

In this paper, a current-mode DC level shifting technique for the implementation of fully differential low supply voltage amplifiers and transistors operating in saturated mode is proposed, which overcomes the problems listed above. It is functional with variable supply voltages. It has high common-mode input signal rejection, high open-loop gain, and high small signal and large signal FOMs. Its main advantage is that it does not require a low-voltage output common-mode feedback network, and it does not include additional resistors in the main amplifier feedback network that degrades BW, DC offset, and noise. The proposed circuit is described in the next Section 2.

2. Circuit Description of the Implementation of Proposed Current Mode Low Voltage Technique

We assume in the following discussion, without loss of generality, fully differential Miller op-amps operating from dual symmetrical supplies $V_{DD} = -V_{SS} = V_{supply}/2$, with NMOS input differential stages and with input/output signals having quiescent common-mode voltages that correspond to the mid-supply value $V_{CMinpQ} = V_{CMoutQ} = (V_{DD} - V_{SS})/2 = 0$. Operation at low voltage is achieved in the proposed circuit by shifting also the common-mode voltage of the amplifier input terminals $V_{CMi} = \left(V_i^+ + V_i^-\right)/2$ to a voltage V_{DDP} close to the upper rail V_{DD} . This is done by injecting level shifting currents sources I_{CM} at the op-amp input terminals (nodes Z, Z'). Figure 3 shows the scheme of the proposed amplifier that includes, besides the main amplifier, also an auxiliary amplifier A_{AUX}. The transistor-level implementation of the fully differential op-amp and the auxiliary amplifier are shown in Figure 4a,b, respectively.

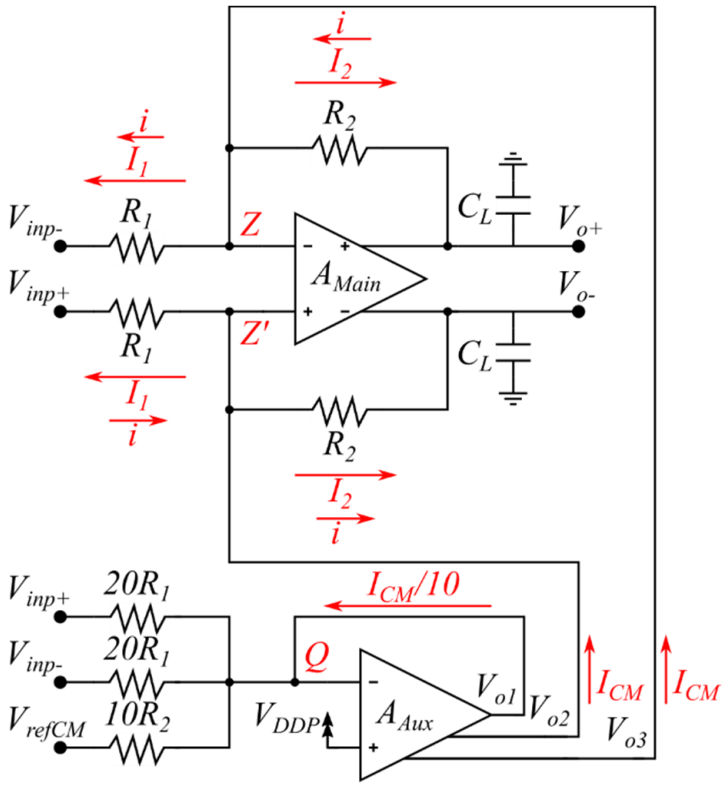


Figure 3. Proposed current source level shifting technique.

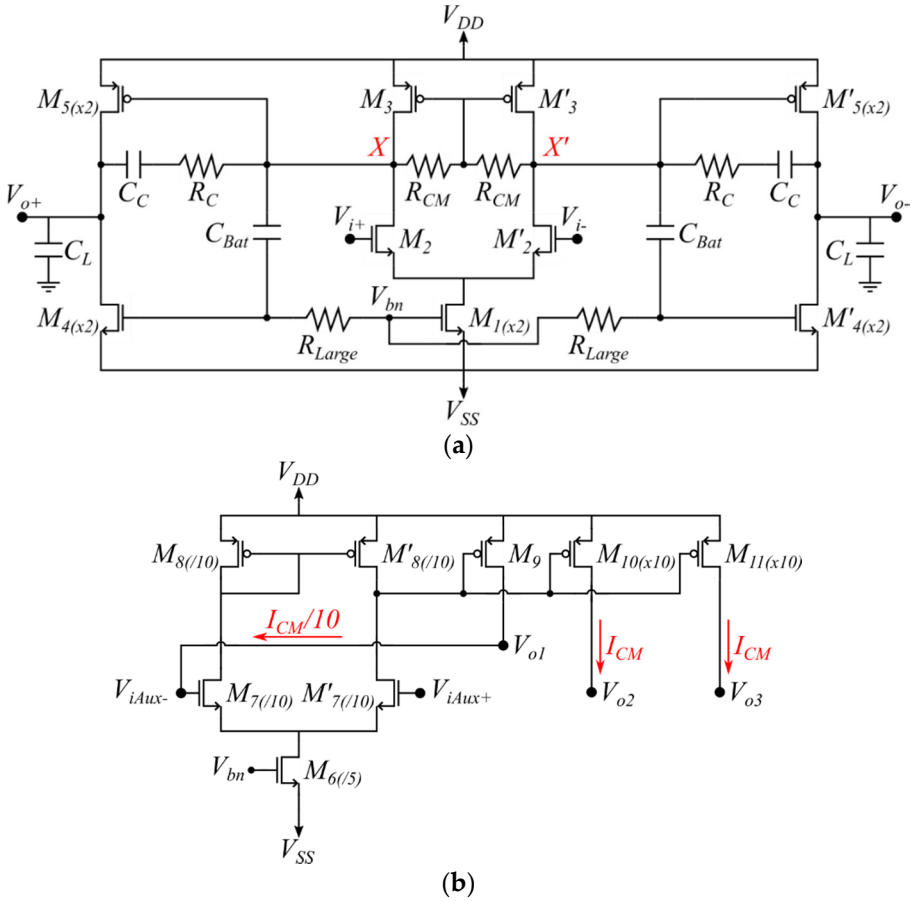


Figure 4. (**a**) Free class AB two-stage (Miller) amplifier. (**b**) Auxiliary amplifier.

The level shifting common-mode current sources have a value $I_{CM} = I_1 + I_2 = (V_{DDP} - V_{CMinp})/R_1 + (V_{DDP} - V_{refCM})/R_2$, where $V_{CMinp} = (V^+_{inp} + V^-_{inp})/2$ is the common-mode voltage of V^+_{inp} and V^-_{inp} that might include common-mode signals, and V_{refCM} is the reference nominal common-mode output voltage (usually to maximize and obtain symmetrical output signal swing $V_{refCM} = 0$, but it can take a different value). These currents are generated by the single-ended auxiliary amplifier A_{AUX}. This amplifier has its positive input terminal connected to V_{DDP} and has three outputs, two of them with factor 10 current scaling/replication. The output V_{o1} is connected to the negative input terminal of A_{AUX} at node Q. This node is also connected to two resistors with values $20R_1$ and to a resistor with value $10R_2$. The main amplifier input signals V^+_{inp}, V^-_{inp} are applied to one of the terminals of the resistors with value $20R_1$, and the output common-mode reference voltage V_{refCM} is applied to one terminal of the resistor $10R_2$. Due to negative feedback, the current delivered by the output terminal V_{o1} to node Q has a value $I_{CM}/10 = (I_1 + I_2)/10$. Outputs V_{o2} and V_{o3} of the auxiliary amplifier deliver accurate scaled-up replicas (by factor 10) with value I_{CM} to nodes Z, Z′ of the main amplifier. Besides pulling up the op-amp common-mode input voltage V_{CMi} to a value $V_{CMi} = V_{DDP}$, at the same time, currents I_{CM} lead to complementary output signals with a common-mode voltage V_{refCM}. It can be seen that the auxiliary amplifier performs simultaneously as a common-mode sensor for V^+_{inp}, V^-_{inp}, as a DC level shifter for the op-amp input terminals, and as a replacement for the output common-mode feedback network. Besides working as a level shifter with input common-mode rejection, it generates complementary output signals with an output common-mode voltage V_{refCM}. Scaling down by factor 10 the current delivered by V_{o1} with resistors $20R_1$ and $10R_2$ in the auxiliary amplifier is done with the purpose of reducing power dissipation (and increasing power efficiency of the proposed scheme) since in this case, the output of the auxiliary amplifier has a current $I_{CM}/10$. Transistors M6-M8 in A_{AUX} of Figure 4b are also scaled down by a factor 10 with the same purpose.

The main op-amp is designed as a fully differential two-stage AB (Miller) op-amp. Resistors R_{CM} in the input stage of Figure 4a implement a resistive local common-mode feedback network [17]. They set the DC operating point at nodes X, X′ to value $V_X = V'_X = V_{DD} - V_{SGM6}$ and provide complementary signals at these nodes. This is required since the op-amp does not have an output common-mode feedback network (CMFN). The output stage is a high power-efficient "free class AB amplifier" [18] that provides approximately symmetrical positive and negative slew rates not limited by the quiescent current of the output stage. R_{large} and C_{bat} are used to set the quiescent output current and to provide dynamic class AB operation to the output stage. R_C and C_C are conventional Miller compensation elements.

3. Results

The proposed low voltage amplifier of Figure 2 is simulated using cadence design framework with ±300 mV dual supplies, in a commercial 180 nm technology that has a nominal supply voltage $V_{supplynom} = 1.8$ V using $V_{DDP} = 200$ mV and $I_{bias} = 5$ μA in three different cases: (a) Applying common-mode input signals $V^+_{inp} = V^-_{inp} = V_s$; (b) Applying a single-ended input $V^+_{inp} = V_s$, $V^-_{inp} = 0$; (c) Applying complementary input signals with zero common-mode input voltage $V^+_{inp} = V_s/2$, $V^-_{inp} = -V_s/2$. The input test signal V_s is a 100 kHz sinusoidal signal with a 20 mV peak amplitude. Resistors R_1 and R_2 are set for a nominal gain $G = R2/R1 = 10\ V/V$. Figure 5a shows the differential output voltage V_{output} and the single-ended complementary outputs V^+_o and V^-_o for the last two cases, while Figure 5b shows the differential output V_{output} and single-ended outputs V^+_o and V^-_o for common-mode inputs. Notice that the results are the same for the last two cases. This verifies the high rejection of common-mode input signals with the generation of complementary output signals at mid-supply in the proposed scheme. It also shows operation with a total supply $V_{DD} - V_{SS} = 600$ mV.

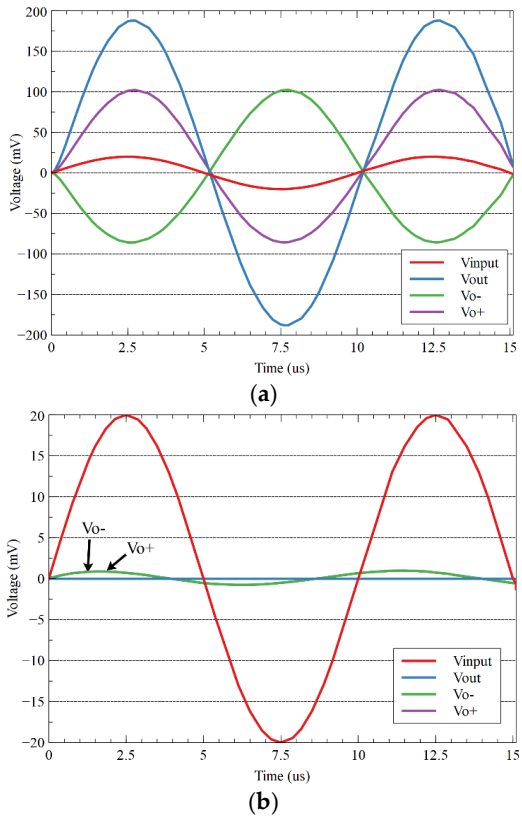


Figure 5. Transient response of the proposed amplifier with nominal gain G = 10. (**a**) Vout, Vo+, and Vo− waveforms (same) with complementary and single-ended input signals. (**b**) Vout, Vo+, and Vo− waveforms with common-mode input signals.

Figure 6 shows the simulated frequency response of the amplifier for nominal gains: 1, 2, 10, 20, 50, 100, and open loop. The DC open-loop gain is found to be 42.2 dB. The unity gain frequency of the open-loop response is 10 MHz. The slew rate of 8.4 V/µs is calculated from the pulse response of Figure 7, with a 500 kHz, 1 *Vpp* differential input pulse, and in this case, the gain of the amplifier is set to 1. Figure 8 shows the transient simulation of V_{output} at different gains for a 100 kHz, 20 mV peak sinusoidal differential input signal.

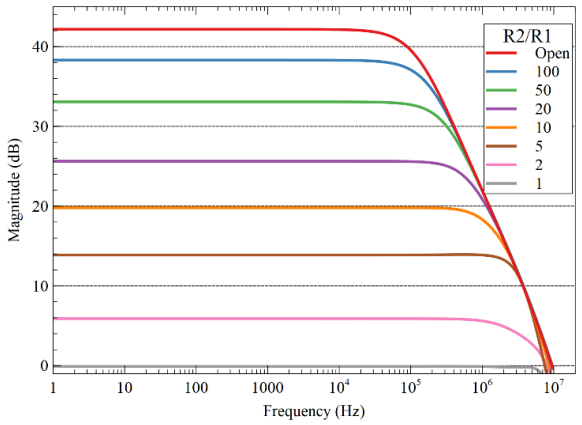


Figure 6. Frequency response for various gain values.

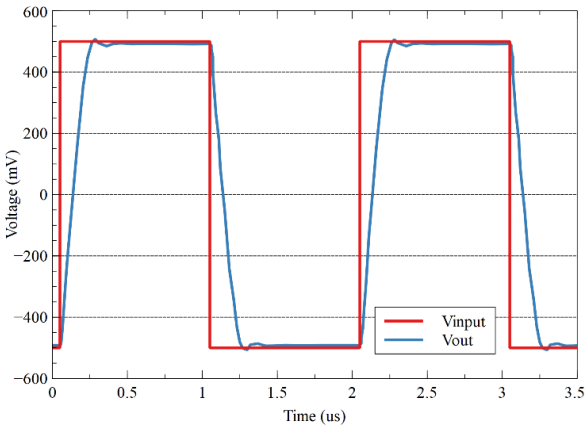


Figure 7. Pulse response at unity gain for slew rate (SR) characterization.

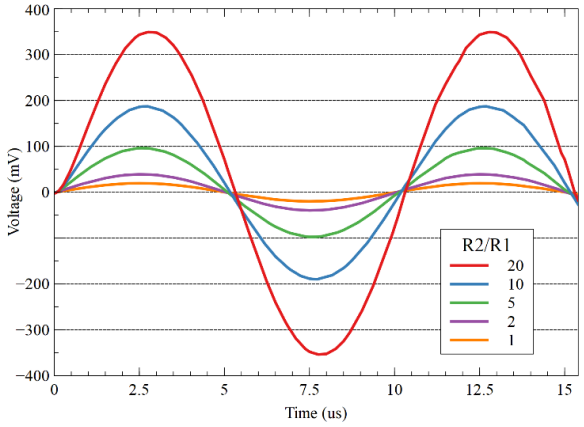


Figure 8. Transient response differential output V_{output} with 100 kHz, 20 mV peak sinusoidal input.

The proposed circuit is fabricated in a TSMC 180 nm CMOS process for a fixed gain of 10 with resistors $R2 = 500$ kΩ and $R1 = 50$ kΩ. Functionality with a gain of 9.87 V/V is verified with dual supplies ±300 mV and $V_{DDP} = 180$ mV and with 5 µA bias current. An input offset of 1.9 mV is

measured. Figure 9 shows the chip microphotograph and circuit layout design. Table 1 shows the design parameters of the proposed circuit.

Table 1. Design Parameters.

	Parameters
Ibias (μA)	5
NMOS W/L (μm)	30/0.5
PMOS W/L (μm)	75/0.5
Rlarge (kΩ)	100
Rcm (MΩ)	1
Rc (kΩ)	20
Cc (pF)	0.8
Cbat (pF)	2
R2 (kΩ)	140
R1 (kΩ)	14

Table 2 shows the parameters obtained from the characterization in the cadence of the circuit with 5 μA bias current. This table also contains the comparison with other gate driven and bulk driven low voltage amplifiers. Corner analysis of the performance parameters of the proposed amplifier at three temperatures is included in Table 3.

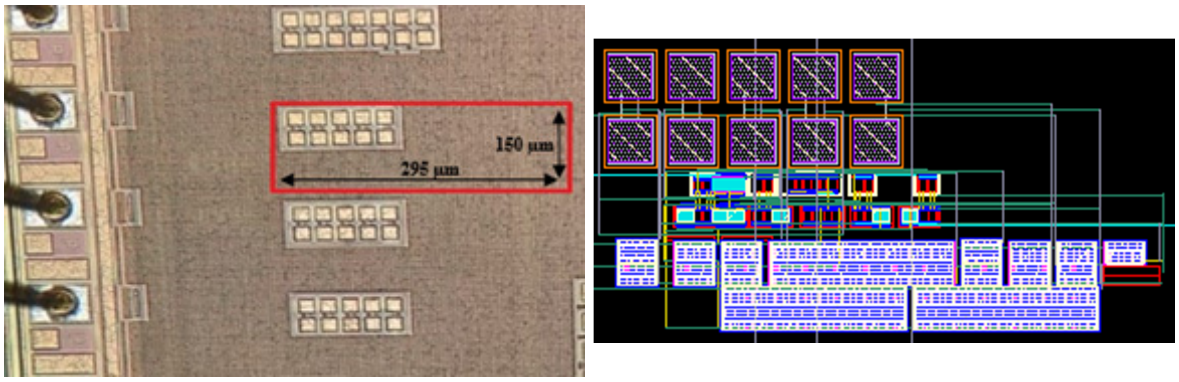
Table 2. Performance parameters and comparison.

	This Work	**[3] 2020**	**[4] 2018**	**[5] 2016**	**[14] 2005**	**[16] 2000**
Technology (nm)	180	180	180	180	180	1200
Topology *	FD, GD	SE, BD	SE, BD	SE, BD	FD, GD	FD, GD
Ibias (μA)	5	5	5	-	-	70
Supply voltages (mV)	±300	600	600	700	500	1 V
SR^+ (V/μs)	8.4	1.61	3	1.8	2	0.3
SR^- (V/μs)	8.4	2.2	2.94	3.8	-	-
GBW (MHz)	16.1	2.1	2.34	3	10	9
PM	54°	59	85	60	-	-
DC gain (dB)	42.2	57.9	56	57.5	62	60
C_L (pF)	10	30	20	20	20	20
Input noise (nV/√Hz) at 1 MHz	69	90	90	100	70	-
CMRR (dB)	85.12	75	60	19	74.5	-
PSRR+ (dB)	53.25	69.2	24	52.1	81.4	-
PSRR − (dB)	56.89	-	-	66.4	-	-
Pdiss (μW)	24.8	44	120	25.4	75	250
FOM_{SS}	6.49	1.43	0.6	2.4	2.7	0.72
FOM_{LS}	3.39	1.09	0.77	2.2	0.54	0.024
CE **	2.03	0.44	0.4	3.1	0.53	0.05

* Topology: FD: fully differential, SE: single-ended, GD: gate driven, BD: bulk driven. ** Current efficiency $CE = I_{outmax}/I_{TotalQ}$.

Table 3. Corner analysis.

	T = 27 °C						**T = 0 °C**						**T = 100 °C**					
Corner	**tt**	**ff**	**fs**	**sf**	**ss**	**SD**	**tt**	**ff**	**fs**	**sf**	**ss**	**SD**	**tt**	**ff**	**fs**	**sf**	**ss**	**SD**
I_{TotalQ} (μA)	82.7	85.6	83.9	83.7	83.3	1.09	83.8	85	82.9	82.9	82.3	1.05	84.7	85.8	85.5	85.1	83.6	0.86
GBW (MHz)	16.1	16.8	11.3	15.4	14.1	2.17	16.4	17.6	11	13.7	10.1	3.27	13.7	14	11	13.8	13.4	1.24
PM	54	53	54	54	55	0.71	54	53	54	55	61	3.21	54	54	53	54	54	0.45
Gain (dB)	42.2	42.3	41.5	42.4	41.5	0.44	42.1	42.3	41.4	42.1	34	3.58	41.9	41.9	41.4	42.1	41.9	0.26
SR^+ (V/μs)	8.4	8.8	7.4	8.6	7.7	0.6	8.3	8.8	7.2	8.5	7.1	0.78	8.4	8.6	7.6	8.6	8.1	0.42
SR^- (V/μs)	8.4	8.8	7.4	8.6	7.7	0.6	8.3	8.8	7.2	8.5	7.1	0.78	8.4	8.6	7.6	8.6	8.1	0.42
CMRR (dB)	85.1	89.3	80.5	92.3	90.7	4.8	90.1	89.9	79.8	94.6	91.2	5.5	86.8	86.5	82.1	88.3	87.3	2.4
PSRR + (dB)	53.3	62.2	34.7	70.5	61	13.5	61	62.5	33	72.8	65	15.2	59	60.7	38.4	66.5	57.4	10.6
PSRR − (dB)	56.9	78.5	50.2	79.2	91	16.7	84.9	79	49.7	71.3	63.6	13.8	75.8	78.2	53.3	84.7	74.7	11.9
P_{diss}	24.8	25.7	25.2	25.1	25	0.33	25.1	25.5	24.9	24.9	24.7	0.32	25.4	25.7	25.7	25.5	25.1	0.26
FOM_{SS}	6.49	6.54	4.49	6.13	5.64	0.85	6.52	6.9	4.42	5.51	4.09	1.24	5.39	5.44	4.29	5.41	5.34	0.5
FOM_{LS}	3.39	3.43	2.94	3.42	3.08	0.23	3.3	3.45	2.9	3.42	2.88	0.28	3.31	3.34	2.96	3.37	3.23	0.16



(**a**) (**b**)

Figure 9. (**a**) Test chip microphotograph with a proposed circuit highlighted in red, (**b**) Layout design of the proposed circuit.

4. Conclusions

A simple, power-efficient technique to implement low voltage gate driven amplifiers based on a current source level shifting technique is presented and verified in 180 nm CMOS technology with ±300 mV supplies. This corresponds to a 66.6% reduction of the nominal 1.8 V supply voltage. It does not lead to BW and offset degradation and has a high rejection of common-mode input signals. An important advantage over previous voltage and current mode schemes is that it does not require a low voltage output common-mode feedback network but, still, has the high rejection of common-mode signals.

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