



Article

A Tunable CMOS Sine Waveform Generator for On-Chip Impedance Spectroscopy

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Abstract

This paper presents a low-power fully integrated sine signal generator for on-chip bioimpedance spectroscopy applications. The circuit is based on a relaxation oscillator, which generates a triangular signal, followed by a sixth-order Gm-C bandpass filter (BPF) that linearizes the waveform. Both blocks, designed in a 0.18 μm CMOS process with 1.8 V supply, make use of a current division technique to generate low-frequency signals without requiring high-valued passive components. The relaxation oscillator features an extended frequency tuning range from 300 Hz to 300 kHz, controlled via a tuning current and a digital capacitor bank. The sine output waveform spans from 1 kHz to 50 kHz, and exhibits a -48.8 dB total harmonic distortion at 10 kHz with 18 mV amplitude. The overall system area is 0.7 mm^2 and the power consumption is lower than 30 μW .

Keywords: signal generator; impedance spectroscopy; relaxation oscillator; Gm-C bandpass filter; low power

1. Introduction

Bioimpedance spectroscopy (BIS) is a noninvasive, cost-effective, and versatile technique in biomedical applications, such as body composition estimation, tissue characterization, and early lymphedema detection, among others [1–8], which relies on acquiring the bioimpedance (BioZ) spectrum by sweeping the excitation signal across a range of frequencies. In order to foster major advancements in portable point-of-care (POC) devices, there is a growing demand for high-performance, compact, and energy-efficient integrated circuit solutions capable of driving precise BIS instrumentation. While wide-band signal excitation offers faster measurement times by simultaneously characterizing multiple frequencies, single-tone excitation provides a higher signal-to-noise ratio and better measurement sensitivity [9–11], which are critical specifications for these applications. Figure 1 illustrates the block diagram of a BioZ measurement front-end. The sine-wave generator serves as a precise voltage reference and drives a dedicated, high-input-impedance current driver (e.g., a V-I converter), which injects the excitation current $i_{exc}(t)$ into the target biological tissue (Z_{DUT}). The resulting voltage response $v_z(t)$ is acquired by the readout stage. The sine-wave generator operates under light loading conditions, ensuring low distortion, a well-defined operating frequency, and the tunability range required by the application, while the current driver maintains operation strictly within safety bounds for biomedical sensing.



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This work focuses exclusively on the sine-wave generator block, which can be either digitally implemented or based on analog oscillator topologies. Digital architectures, such as Direct Digital Synthesis (DDS) and generators based on Digital-to-Analog Converters (DACs), are highly linear. However, they rely on high-speed clocks and high-resolution DACs, which may result in high power and silicon area consumption [11–13]. In order to achieve low-power sine-wave generation, the Wien-bridge oscillator is often used in the literature [14–16], but it requires an automatic gain control circuit to reduce the third-harmonic, and digitally programmable resistors in the feedback network for frequency tuning. Furthermore, as the feedback resistors must be matched to prevent frequency instability, multiple resistor banks are needed, significantly increasing the area of the circuit [16]. Finally, large-sized passive components are required to generate low-frequency signals, which in some cases leads to the use of off-chip components [15]. Alternatively, Gm-C sinusoidal generators avoid the area overhead of integrated resistors, but their inherent linearity is limited [17]. As for sine synthesizers based on wave-shaping techniques, they rely on the non-linear characteristics of transistors in the sub-threshold region to generate the sine wave, resulting in high harmonic distortion due to their strong dependence on bias conditions [18].

This paper presents a tunable sine waveform generator based on a relaxation oscillator and a sixth-order Gm-C bandpass filter. A current division technique is applied to both subcircuits in order to achieve low-frequency operation without requiring high-value passive components. Additionally, multiple frequency control mechanisms are incorporated to extend the achievable operating frequency range while preserving low-power operation. The remainder of the paper is organized as follows: Section 2 describes the design and characteristics of the proposed tunable relaxation oscillator, and Section 3 presents the design of the sixth-order Gm-C bandpass filter, based on low-Gm operational transconductance amplifiers (OTAs). Section 4 shows the post-layout simulation results of the proposed sine waveform generator and compares the design with related works in the literature. Finally, the main conclusions are summarized in Section 5.

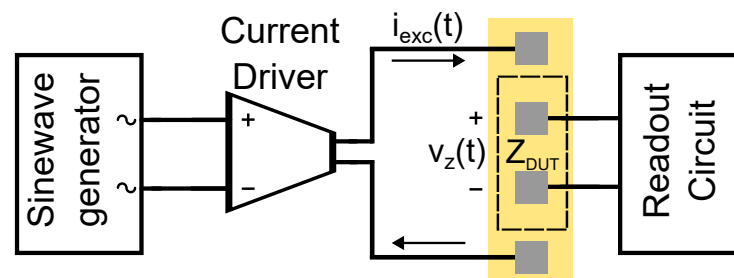


Figure 1. Block diagram of a BioZ measurement front-end.

2. Relaxation Oscillator

The proposed relaxation oscillator, shown in Figure 2, consists of three main subcircuits: a voltage-to-current (V-I) converter, a switchable capacitor bank, and the threshold and switching logic, referred to here as the slope control circuit (SCC). A reference input voltage $V_{ref1} - V_{ref2}$ is converted into an output current I_{out} in order to charge/discharge the capacitors, thus producing a voltage ramp with alternating positive and negative slopes. The transition between current injection and extraction is regulated by the SCC, which monitors the voltages across the capacitors and compares them with the threshold voltages V_L and V_H , in order to determine when the polarity of the slope must change to form the triangular shape. The oscillator thus generates two differential signals: a triangular waveform with predefined frequency and amplitude at the capacitor terminals, and a square waveform, synchronized at the same frequency, at the output of the SCC.

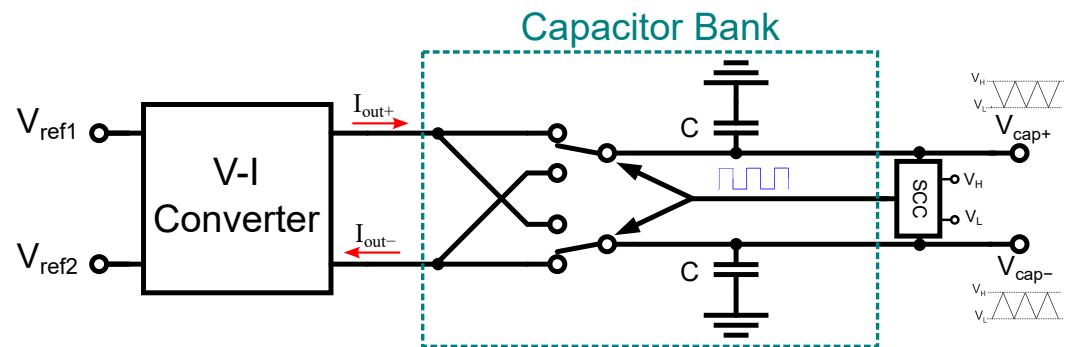


Figure 2. Block diagram of the proposed relaxation oscillator.

The oscillation frequency is determined by the following equation:

$$f = \frac{I_{out}}{2C(V_H - V_L)} = \frac{V_{ref1} - V_{ref2}}{2RC(V_H - V_L)} \quad (1)$$

where $1/R$ is the transconductance value of the V-I converter, and C is the capacitance value. The oscillation frequency is thus directly proportional to the output current of the V-I converter, which sets a trade-off between power consumption and the maximum achievable frequency. Additionally, since the frequency is directly proportional to the transconductance $1/R$ and inversely proportional to the capacitance C , a trade-off arises between silicon area and the minimum achievable frequency. To prevent an increase in current consumption, the V-I converter was designed with a constant resistance value R_1 , and a tunable current mirror configuration to scale up or down the current delivered to the capacitors, i.e., to scale up or down the equivalent transconductance $1/R$. Furthermore, a capacitor bank is used to provide coarse frequency control, thus extending the tuning range. Finally, overlapping among the three available frequency intervals is ensured by adjusting the value of V_{ref2} . All these frequency control mechanisms will be explained next.

2.1. V-I Converter

The schematic of the V-I converter is shown in Figure 3. As illustrated, it consists of two negative-feedback amplifiers that set the voltage across the terminals of resistor R_1 . If the same reference voltage $V_{ref1} = V_{ref2}$ is applied to both non-inverting inputs, the effective voltage drop across R_1 is minimized and the current I_{R1} is established in the nanoampere range. This current is subsequently replicated into additional branches via current mirrors in order to generate two output currents I_{out+} and I_{out-} , with opposite polarity and equal magnitude. The $1:\alpha$ block sets the copy factor of the current mirror $M_{a1} - M_{a2}$. The α value depends on the distribution of the bias current I_{BT} between the input transistors of a PMOS differential pair, as proposed in Ref. [19] and shown in Figure 4, where I_{TUN} represents the tuning current. As transistors $M_{a1,2}$ and $M_{C1,2}$ operate in weak inversion and saturation, it can be shown that the copy factor is given by:

$$\alpha = \frac{I_{TUN}}{I_{BT} - I_{TUN}} = \frac{\beta}{1 - \beta} \quad (2)$$

with $\beta = I_{TUN}/I_{BT}$. Therefore, the output currents of the V-I converter are given by:

$$I_{out\pm} = \frac{2\beta - 1}{1 - \beta} I_{R1} = \frac{2\beta - 1}{1 - \beta} \frac{(V_{ref1} - V_{ref2})}{R_1} \quad (3)$$

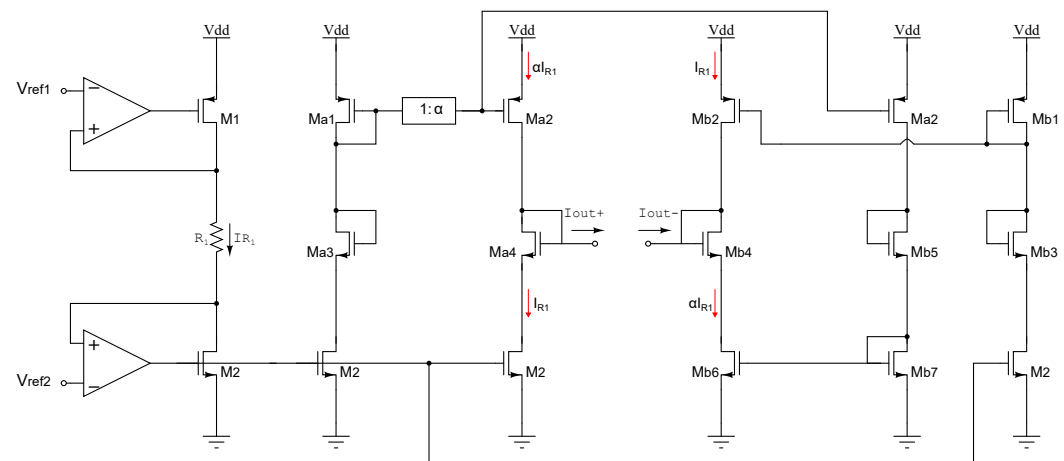


Figure 3. Schematic of the V-I converter.

Note that β always remains between 0 and 1. If $\beta=0.5$ ($I_{TUN} = I_{BT}/2$), I_{out} ideally becomes zero because $\alpha = 1$, causing the currents through the output branches of the V-I converter to cancel out. When $\beta < 0.5$ ($I_{TUN} < I_{BT}/2$), I_{out} reverses its polarity with respect to the orientation illustrated in Figure 3, and its maximum magnitude is limited by I_{R1} ($0 < I_{out} < I_{R1}$), since the tunable current mirror $M_{a1,2}$ attenuates the αI_{R1} current. In contrast, when $\beta > 0.5$, the polarity matches that shown in Figure 3, and I_{out} can become arbitrarily high as β approaches unity. Figure 5 shows the output currents of the V-I converter with $V_{ref2} = 900$ mV, $R_1 = 100$ k Ω , $I_{R1} = 84$ nA, $I_{BT} = 50$ nA, as β is swept from 0 to 1. The absolute differential error between the two output currents, which is lower than 55 nA across the entire range, is also plotted (blue dashed line). To achieve the widest frequency tuning range and avoid potential current polarity reversal caused by device mismatch, β must be chosen higher than 0.5. Furthermore, β should be kept below 1 to limit the maximum power consumption. For this reason, in the proposed design, the tuning parameter is restricted to the range of $0.52 < \beta < 0.92$, which corresponds to a current sweep of 26 nA $< I_{TUN} < 46$ nA. Finally, it is worth noting that the input voltage $V_{ref1} - V_{ref2}$ of the V-I converter can be increased to obtain higher I_{out} values, thus resulting in higher operation frequencies. This additional degree of freedom will also be exploited in Section 2.4 by adjusting V_{ref2} to extend the complete frequency range.

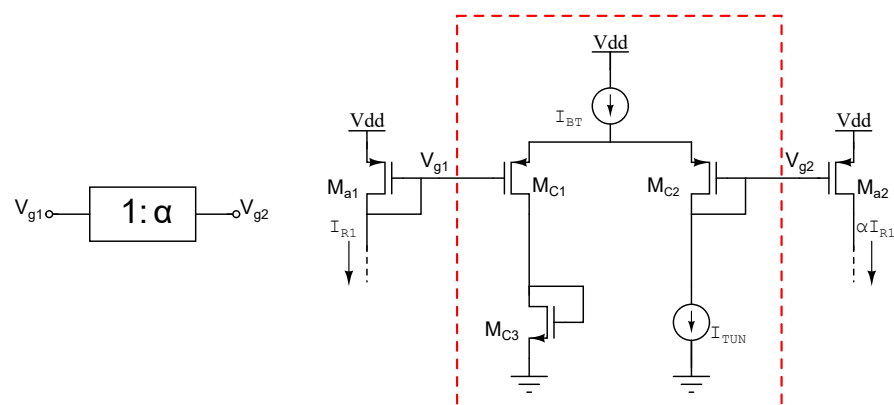


Figure 4. Continuously tunable current mirror.

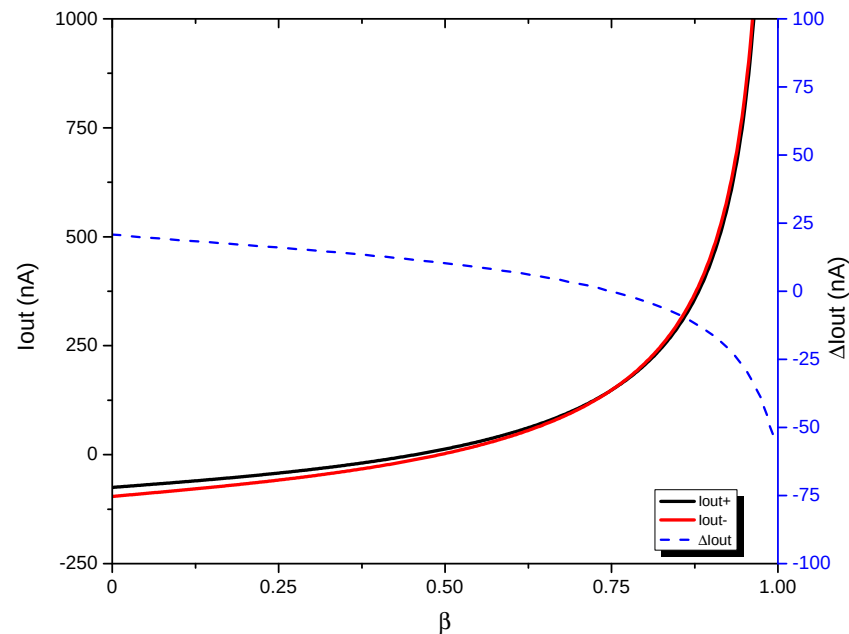


Figure 5. Output currents of the V-I converter as a function of $\beta = I_{TUN}/I_{BT}$.

2.2. Capacitor Bank

A capacitor bank was designed to achieve a wide oscillation frequency range. It consists of an array of switches and capacitors, as shown in Figure 6. Transistors $M_{sw1} - M_{sw4}$ are used to reverse the slope of the triangular waveform, and are therefore controlled by the outputs of the SCC. Transistors M_{sw5} and M_{sw6} are controlled by a bit a_0 to establish the equivalent capacitance value, given by $C = C_n + a_0 C_0$. When $a_0 = 0$, the circuit operates with the nominal capacitance $C_n = 1.5$ pF. Conversely, when $a_0 = 1$, the capacitor $C_0 = 43.5$ pF is connected in parallel, resulting in a total capacitance of $C = 45$ pF. This capacitance variation significantly extends the achievable frequency tuning range.

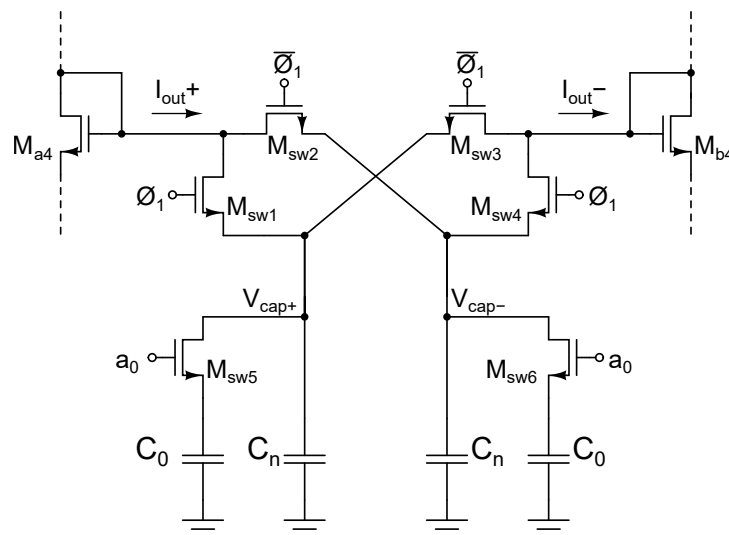


Figure 6. Switchable capacitor bank.

2.3. Slope Control Circuit (SCC)

This circuit relies on four custom-designed comparators, whose inputs are connected to the capacitor terminals V_{cap+} and V_{cap-} , and to the threshold voltages V_H and V_L , as shown in Figure 7. The comparator outputs are connected to a combination of NAND

gates followed by an asynchronous SR latch, whose outputs generate the control voltages required to drive the switching transistors M_{sw1} to M_{sw4} in Figure 6. Additionally, these outputs are differential square-wave signals synchronized in frequency with the triangular waveforms.

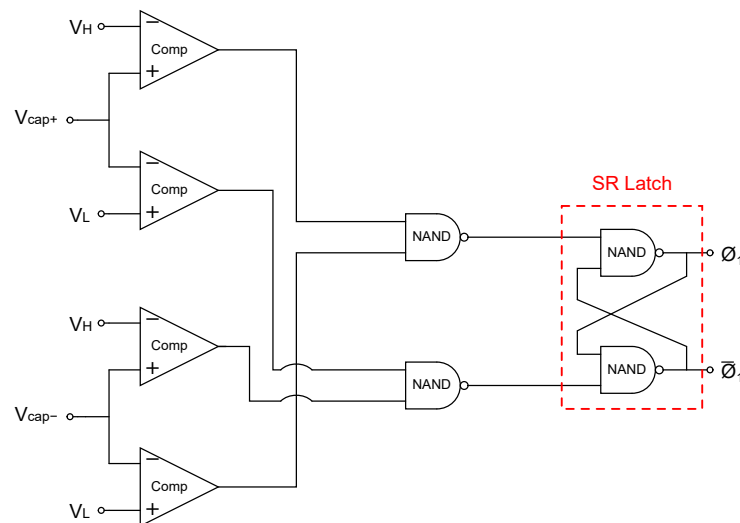


Figure 7. Schematic of the slope control circuit (SCC).

2.4. Relaxation Oscillator Simulation Results

The proposed relaxation oscillator was implemented in a 0.18 μm CMOS process with a 1.8 V supply voltage. Considering all the incorporated frequency control mechanisms, the oscillation frequency is given by:

$$f = \frac{2\beta - 1}{1 - \beta} \frac{V_{ref1} - V_{ref2}}{2R_1(C_n + a_0C_0)(V_H - V_L)} \quad (4)$$

Continuous fine frequency tuning is achieved through the current ratio β , with $I_{BT} = 50$ nA, whereas coarse tuning is performed via the digital bit a_0 . Although the adjustment of the differential voltage $V_{ref1} - V_{ref2}$ could also function as an additional fine-tuning mechanism, in this specific design, V_{ref2} was restricted to two discrete voltage levels to extend frequency operation up to 300 kHz. The key component values and design parameters are summarized in Table 1, and Table 2 shows the different frequency range configurations. To verify the circuit operation, post-layout simulations were performed. The oscillator occupies an area of 0.19 mm^2 and consumes 10.7 μW in the worst case, i.e., at maximum frequency. Figure 8 shows the steady-state differential output waveforms under two extreme conditions: for a tuning current $I_{TUN} = 26$ nA ($\beta = 0.52$), with $V_{ref2} = 900$ mV and $a_0 = 1$, which results in the minimum frequency $f = 300$ Hz; and for a tuning current $I_{TUN} = 46$ nA ($\beta = 0.92$), with $V_{ref2} = 850$ mV and $a_0 = 0$, which results in the maximum frequency of $f = 300$ kHz. The average peak-to-peak output voltage is 1.02 V. Table 3 summarizes the main characteristics of the relaxation oscillator.

Table 1. Component values and design parameters.

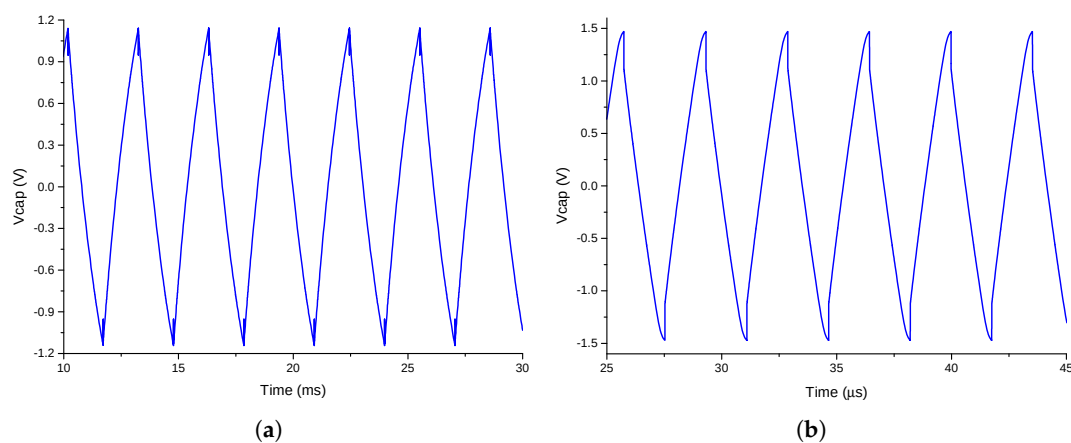
Element	Value
C_n	1.5 pF
C_0	43.5 pF
R_1	100 k Ω
I_{BT}	50 nA
$V_H - V_L$	1.4–0.35 V
V_{ref1}	900 mV

Table 2. Frequency tuning range configurations.

Frequency Range [kHz]	β	a_0	V_{ref2} [mV]
0.3–10	0.52–0.92	1	900
8.5–245	0.52–0.92	0	900
60–300	0.52–0.86	0	850

Table 3. Characteristics of the relaxation oscillator.

Parameter	Value
CMOS Process	0.18 μm
Supply Voltage	1.8 V
Tuning current I_{TUN}	26–46 nA
Frequency range	300 Hz–300 kHz
Average amplitude	1.02 V _{pp}
C_{TOT}	90 pF
Area consumption	0.19 mm ²
Max. Power	10.7 μW

**Figure 8.** Triangular wave generated at (a) 300 Hz and (b) 300 kHz.

To validate robustness, a 200-run Monte Carlo simulation was performed at 1 and 50 kHz, and the results are shown in Figure 9. As observed, the amplitude of the differential triangular waveform remains almost constant at both operating frequencies. At 1 kHz, the mean amplitude is 1 V with a standard deviation of 31 mV, while at 50 kHz, the same mean value of 1 V is maintained with a slightly lower standard deviation of 25 mV. Regarding frequency, the mean values are 1.02 kHz and 50.4 kHz, with standard deviations of 124 Hz and 6.4 kHz, respectively. In both cases, the mean frequency remains close to the intended operating value, although the circuit exhibits frequency dispersion due to process and mismatch variations. However, this frequency deviation can be readjusted after fabrication via the tuning current I_{TUN} .

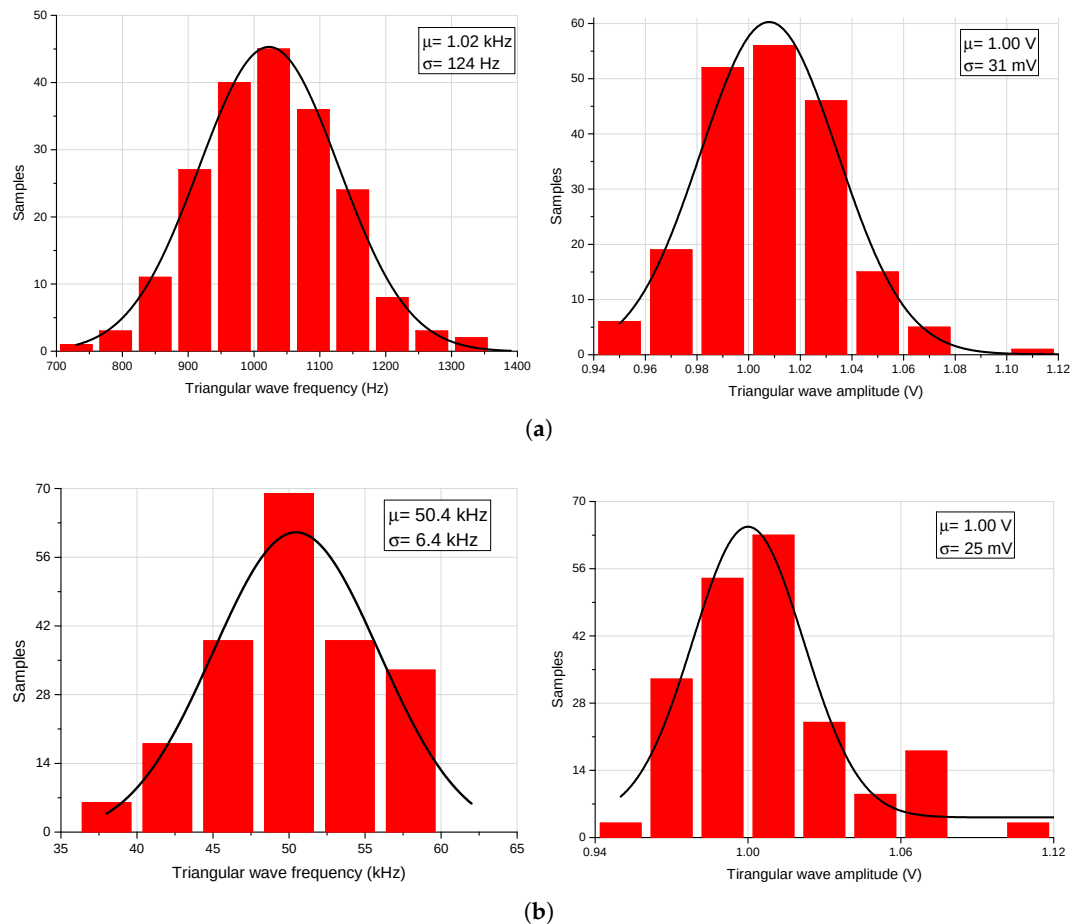


Figure 9. Monte Carlo simulations for frequency and amplitude of the triangular wave at (a) 1 kHz and (b) 50 kHz.

3. Tunable Sixth-Order Gm-C BPF

The linearization stage of the proposed sine waveform generator is a sixth-order bandpass filter based on the fully differential Tow–Thomas biquad shown in Figure 10. Each biquadratic section consists of four fully differential low-Gm OTAs and a programmable NMOS capacitor bank that selects the operation frequency range through a control bit b_0 . For $b_0 = 1$, $C_1 = 3$ pF and $C_2 = 1.5$ pF, providing a center-frequency tuning range from 10 to 50 kHz. When $b_0 = 0$, the capacitances are increased to $C_1 = 20$ pF and $C_2 = 10$ pF, allowing the center frequency to be tuned from 1 to 10 kHz. Figure 11 shows the capacitance–voltage characteristics of C_1 and C_2 for both states of the digital control bit b_0 . The dimensions of these NMOS capacitors are $W_{C1}/L_{C1} = 50 \mu\text{m}/49 \mu\text{m}$ and $W_{C2}/L_{C2} = 24.8 \mu\text{m}/49 \mu\text{m}$.

The transfer function of the biquad is given by:

$$\frac{V_{outb}}{V_{in}} = \frac{s \frac{G_{m1}}{C_1}}{s^2 + s \frac{G_{m2}}{C_1} + \frac{G_{m3}G_{m4}}{C_1C_2}} \quad (5)$$

The gain is determined by the ratio G_{m1}/G_{m2} , while the quality factor Q and the center frequency f_c are given by:

$$Q = \sqrt{\frac{C_1 G_{m3} G_{m4}}{C_2 G_{m2}^2}} \quad (6)$$

$$f_c = \frac{1}{2\pi} \sqrt{\frac{G_{m3}G_{m4}}{C_1C_2}} \quad (7)$$

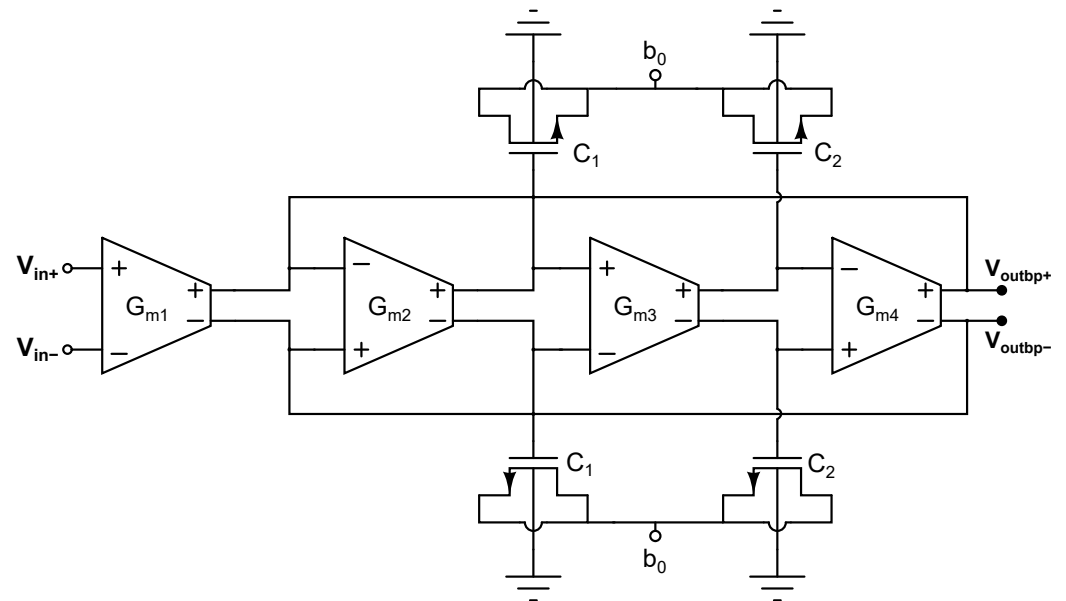


Figure 10. Fully differential Tow–Thomas Gm-C biquad.

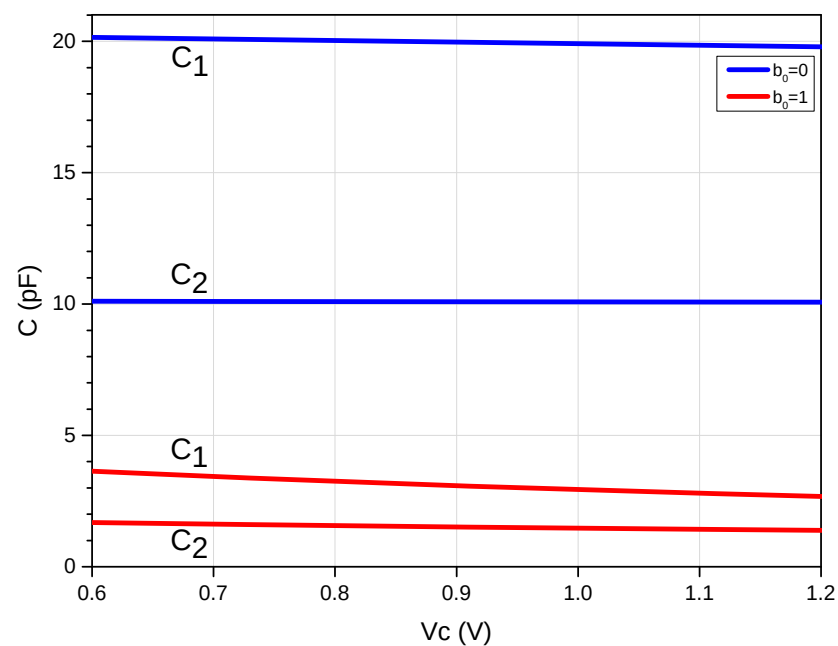


Figure 11. Capacitance–voltage characteristics of C_1 and C_2 .

Synchronous tuning is used across all three biquads to achieve a steep roll-off characteristic, which is essential for effectively suppressing the undesired frequency components generated by the relaxation oscillator. Furthermore, all transconductance values are set to the same G_m value, so the filter gain is unity, and Q and f_c are given by:

$$Q = \sqrt{\frac{C_1}{C_2}} \quad (8)$$

$$f_c = \frac{G_m}{2\pi} \sqrt{\frac{1}{C_1C_2}} \quad (9)$$

In this design, frequency tuning relies solely on the OTA transconductance. By choosing $C_1 = 2C_2$, the quality factor was set to $Q = \sqrt{2}$. The relatively low Q value makes the system tolerant to small frequency alignment errors between the signal frequency f and the center frequency f_c . For instance, from the transfer function of the sixth-order filter, it can be shown that a $\pm 5\%$ misalignment results in a gain drop of less than 0.3 dB, i.e., in an amplitude attenuation of about 3%. Meanwhile, the sixth-order roll-off of the cascaded bi-quadratic stages ensures, as already mentioned, the filtering of high-order harmonics. Note that triangular waveforms contain exclusively odd harmonics, so the closest non-desired frequency component of the input signal is at $3f$, which will be suppressed by the BPF stopband, as shown in the next Section.

The low-Gm OTA is a fully differential version of the architecture proposed in Ref. [20], as shown in Figure 12. It employs current cancellation by splitting the differential output current of a transconductor into four paths and subtracting the resulting currents at the outputs. This technique results in transconductance values ranging from a few units to several hundreds of nS. A transconductance control circuit (TCC) generates the bias voltages V_B and V'_B through the ratio m between a control current I_C and a bias current I_B . The equivalent transconductance of the OTA is given by:

$$G_m = \frac{i_{out,d}}{v_{in,d}} = \left(\frac{m-1}{m+1} \right) K \frac{2}{R_S} \quad (10)$$

where $v_{in,d} = v_{in+} - v_{in-}$ is the differential input voltage, K is the gain of the current mirrors $M_{3,4} - M_{3k,4k}$, R_S is the equivalent resistance of the degeneration transistors M_S , and $m = I_C / I_B$ is the current ratio.

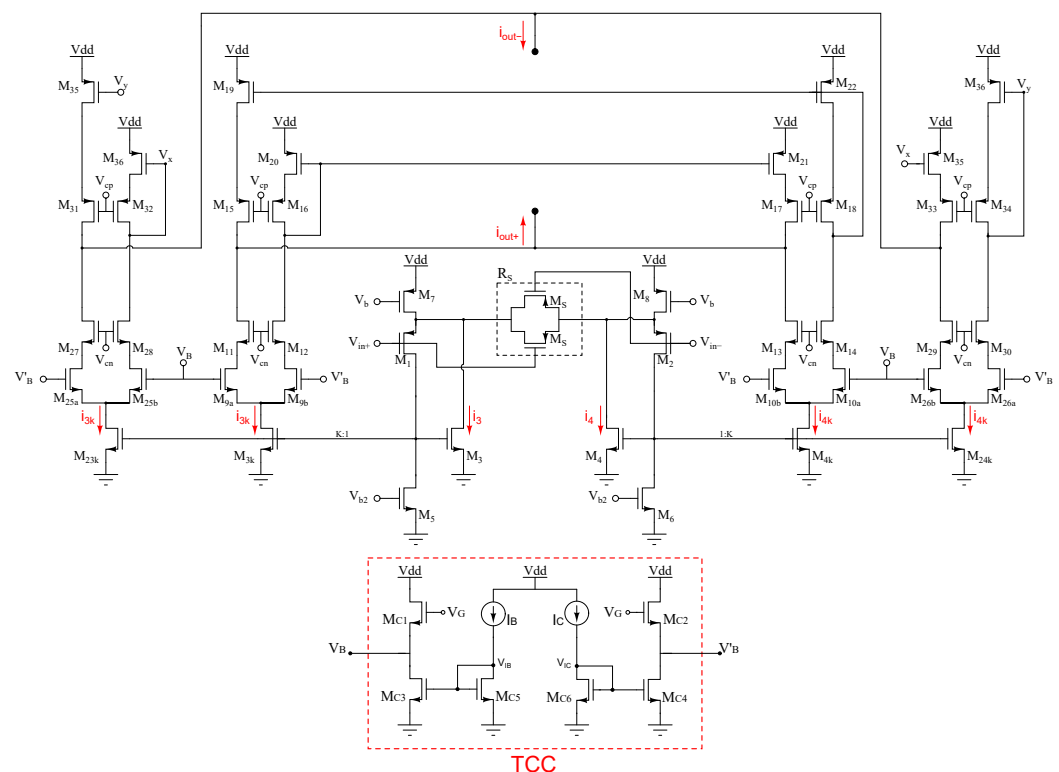


Figure 12. Fully differential low-Gm transconductor.

I_B was set to 25 nA and I_C varies from 28 nA to 2 μ A ($1.12 < m < 80$), so the transconductance of each OTA in the BPF is tuned from 23 to 775 nS. In this way, the center frequency of the filter can be tuned from 1 to 50 kHz. Figure 13 shows the frequency response of the filter at 1, 10, and 50 kHz. The frequency range configurations are shown in

Table 4, while Table 5 summarizes the main BPF characteristics. The power consumption remains under 16 μW across the entire frequency tuning range. Note that the use of low-Gm OTAs to accommodate the low-frequency requirements of the system without demanding large on-chip capacitors also limits the maximum achievable center frequency.

Table 4. Frequency tuning range configurations of the BPF.

Frequency Range [kHz]	m	b_0
1–17.3	1.12–80	0
6.6–50	1.12–4.8	1

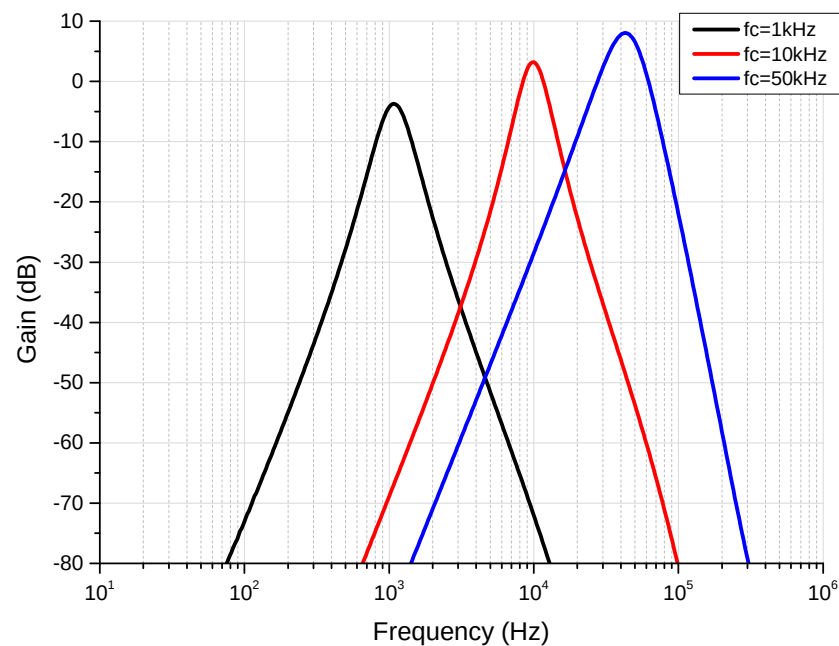


Figure 13. Frequency response of the BPF.

Table 5. Characteristics of the BPF.

Parameter	Value
CMOS Process	0.18 μm
Supply voltage	1.8 V
Control current I_C	28 nA–2 μA
f_c tuning range	1–50 kHz
Q	$\sqrt{2}$
Max. Power	15.6 μW

4. Proposed CMOS Sine Waveform Generator

The CMOS sine waveform generator was implemented by cascading the relaxation oscillator and the sixth-order Gm-C bandpass filter, which serves as the linearization stage. As shown in Figure 14, a voltage scaling stage, which consists of a capacitive attenuator and a low-power buffer, was placed at the output of the oscillator, thus avoiding saturation of the BPF and non-linear effects, which would otherwise compromise the linearization process. The complete circuit layout, designed in 0.18 μm CMOS technology, is shown in Figure 15. It occupies a total area of 0.7 mm^2 and consumes 29.3 μW from a 1.8 V supply voltage. The power and area breakdown are shown in Figure 16. The relaxation oscillator only demands a 37% share for both metrics while providing a triangular output with a wide three-decade frequency tuning range. The power and area consumption are dominated by

the sixth-order BPF, due to the circuit complexity of high-order active filters. As already mentioned, the maximum center frequency is limited by the low-power, low-Gm OTAs used for low-frequency operation. In this prototype, no tuning mechanism was integrated to adjust the passive components in the relaxation oscillator, specifically R_1 , which is a high-resistivity polysilicon resistor. While process variations in these components shift the available tuning range of the triangular wave after fabrication, they do not restrict the tuning range of the whole sine waveform generator. To carry out post-layout simulations, the frequency sub-range was first set by the control bits (a_0, b_0): (1, 0) from 1 to 10 kHz, and (0, 1) from 10 to 50 kHz. Next, the target output frequency was set by sweeping the tuning current I_{TUN} of the relaxation oscillator. Once the target frequency was established, the BPF center frequency was aligned by adjusting its bias current I_C until reaching a maximum output amplitude voltage. Table 6 shows the frequency range configurations of the sine waveform generator. The reference voltage V_{ref2} was kept constant at 900 mV. In order to show how the calibration process can be automated in future implementations, a digitally controlled tuning scheme is conceptually proposed in Appendix A.

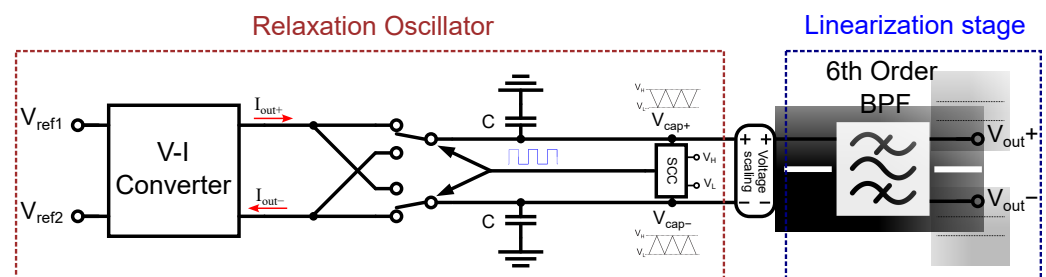


Figure 14. Sine waveform generator block diagram.

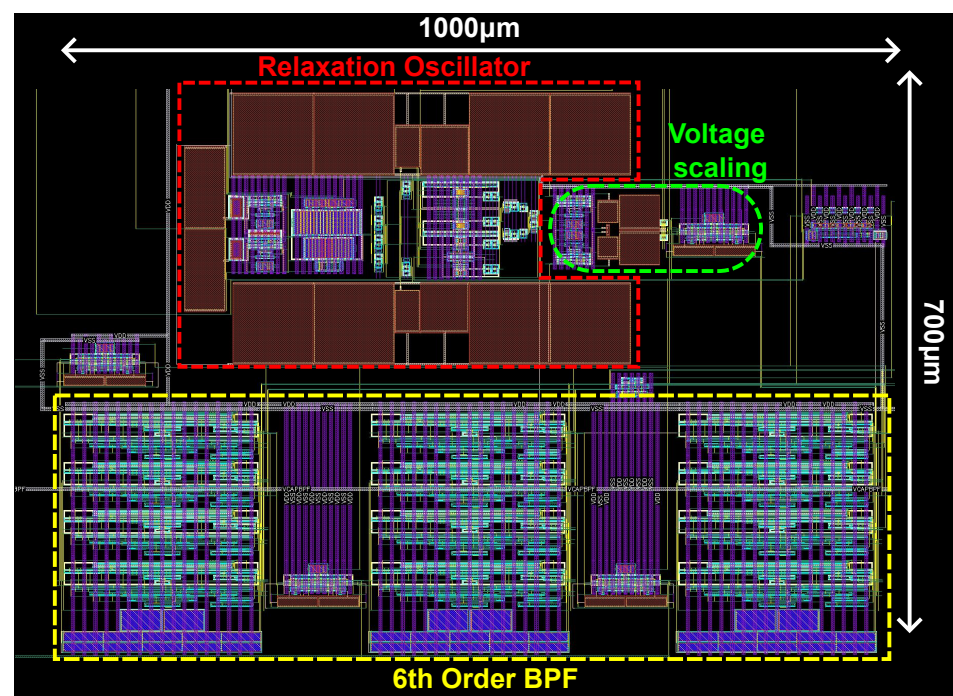


Figure 15. Layout of the proposed sine waveform generator.

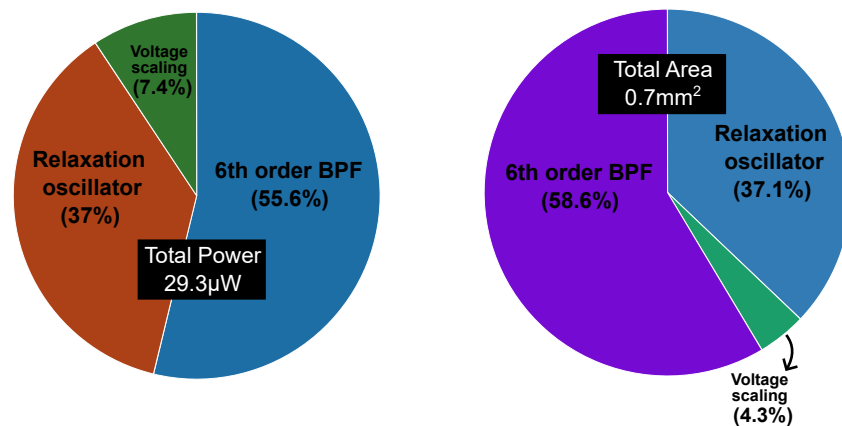


Figure 16. Power and area breakdown of the proposed sine waveform generator.

Table 6. Frequency tuning range configurations of the sine waveform generator.

Frequency Range [kHz]	(a_0, b_0)	$\beta = \frac{I_{TUN}}{I_{BT}}$	$m = \frac{I_C}{I_B}$
1–10	(1, 0)	0.64–0.92	1.24–10
8.5–50	(0, 1)	0.52–0.84	1.4–4.8

Figure 17 shows the steady-state differential output signal of the generator at 1 and 50 kHz, confirming the correct sine waveform generation. In order to demonstrate the linearity improvement achieved by the BPF, Figure 18 compares the frequency spectra of the triangular and sinusoidal signals at several frequency settings. As shown, the third harmonic is reduced by more than 30 dB by the linearization stage. Note that, due to the fully differential architecture, even harmonics are virtually eliminated. The worst-case THD is -48.8 dB at 10 kHz with 32 mV_{pp}, whereas the lowest THD of -55 dB is achieved at 1 kHz with 12 mV_{pp} output voltage. Alternative filter design techniques can be explored in the future to extend the operation frequency of the sine waveform generator without compromising the silicon area or power efficiency. In such a scenario, R_1 in the relaxation oscillator should be replaced by a digitally programmable resistor bank to compensate for process variations across the extended frequency range.

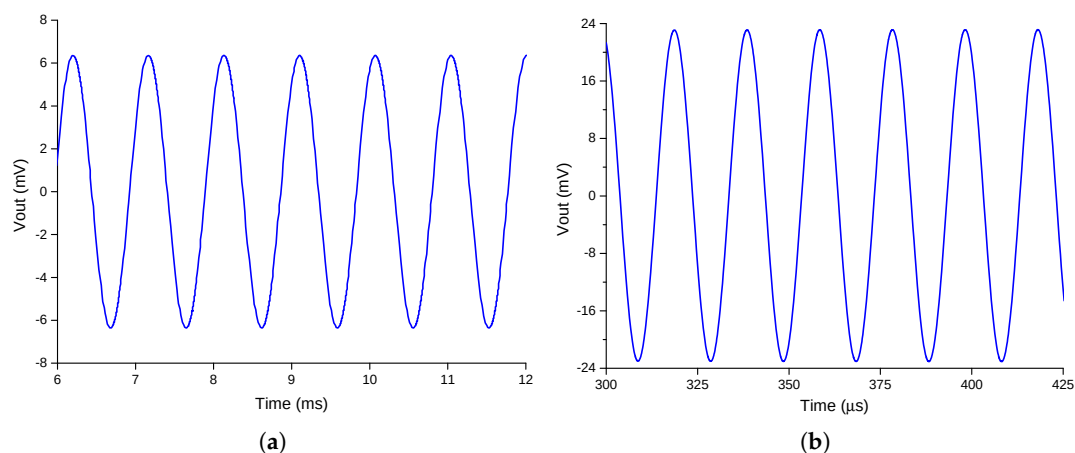


Figure 17. Time response of the sine waveform generator at (a) 1 kHz and (b) 50 kHz.

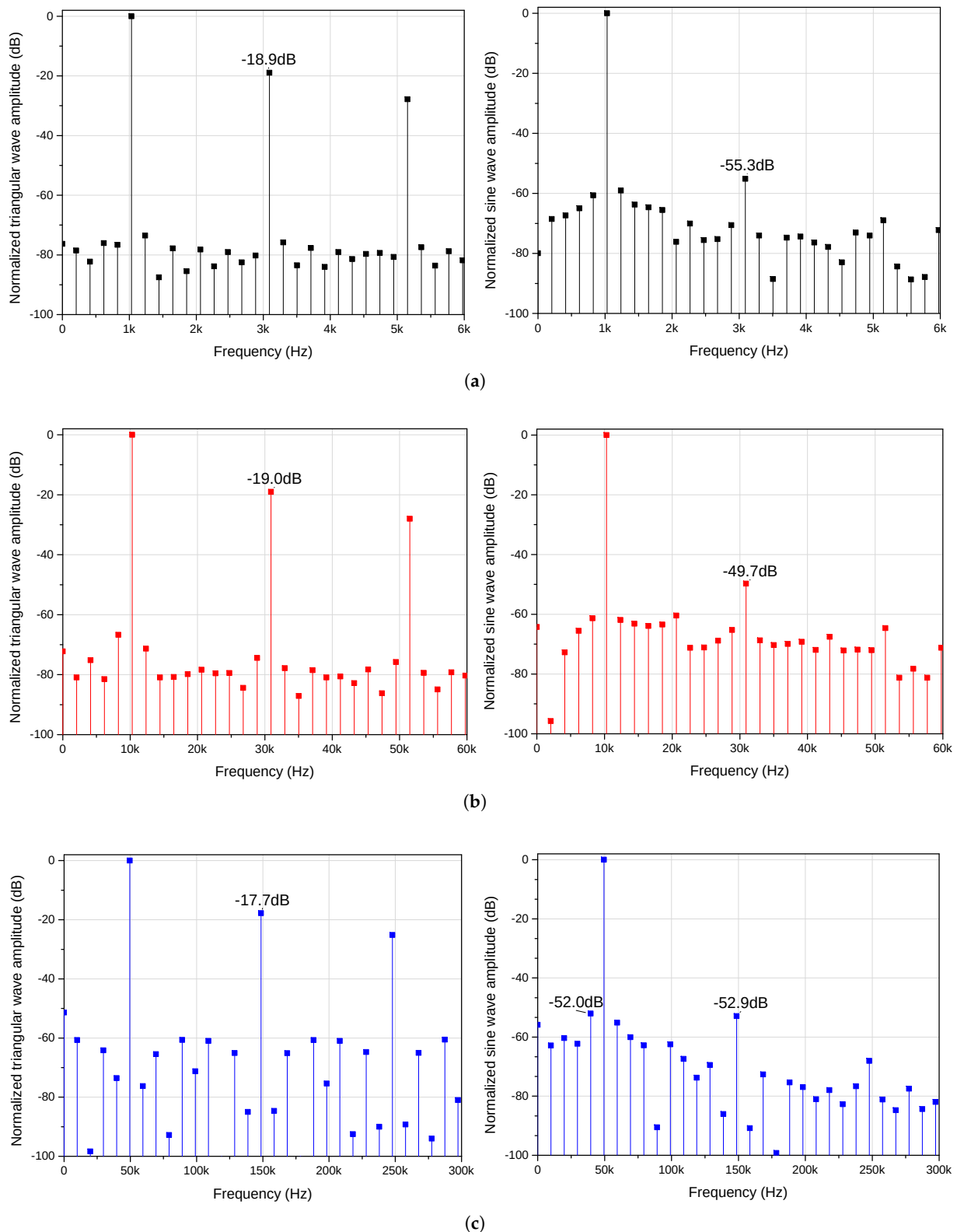


Figure 18. Frequency spectrum of the triangular wave and the output sine wave at (a) 1 kHz, (b) 10 kHz and (c) 50 kHz.

The output amplitude, THD, and power consumption of the sine waveform generator as a function of the operating frequency are shown in Figure 19. The output amplitude ranges from 12 to 50 mV_{pp}, with a THD lower than −48 dB throughout the whole frequency

range. Although power consumption slightly increases with frequency, it remains below $29.3 \mu\text{W}$ in all cases.

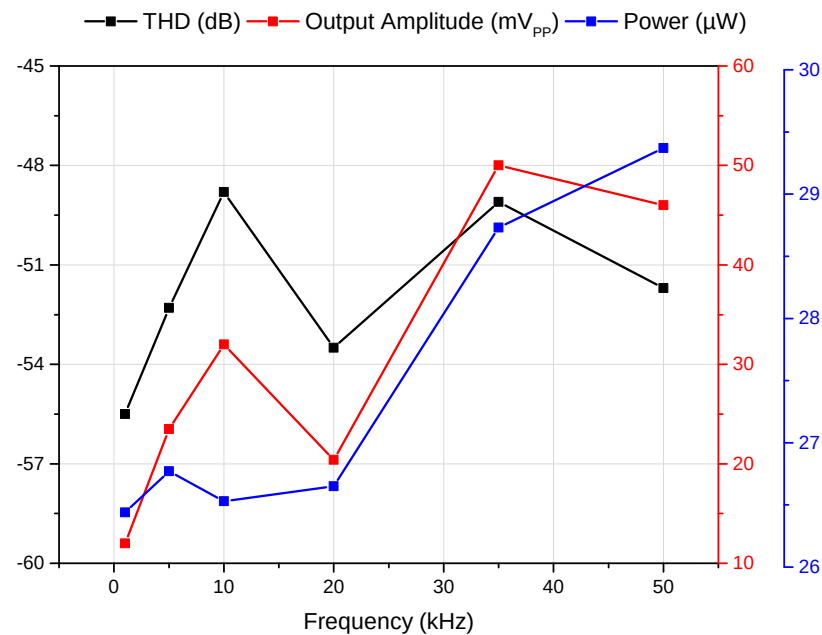


Figure 19. THD, output amplitude and power consumption vs. frequency.

To evaluate the dynamic response between adjacent frequency steps during spectroscopy, Figure 20 illustrates the settling behavior for a 1 to 2 kHz step. This transition represents the most critical scenario in terms of absolute settling time, as lower-frequency signals inherently require longer time intervals to complete the necessary cycles for amplitude stabilization. After the change in the control signals, the differential sinusoidal output achieves steady-state operation within approximately 1.6 ms, which corresponds to about three signal cycles, enabling step-by-step impedance spectroscopy with minimal delay between measurement points.

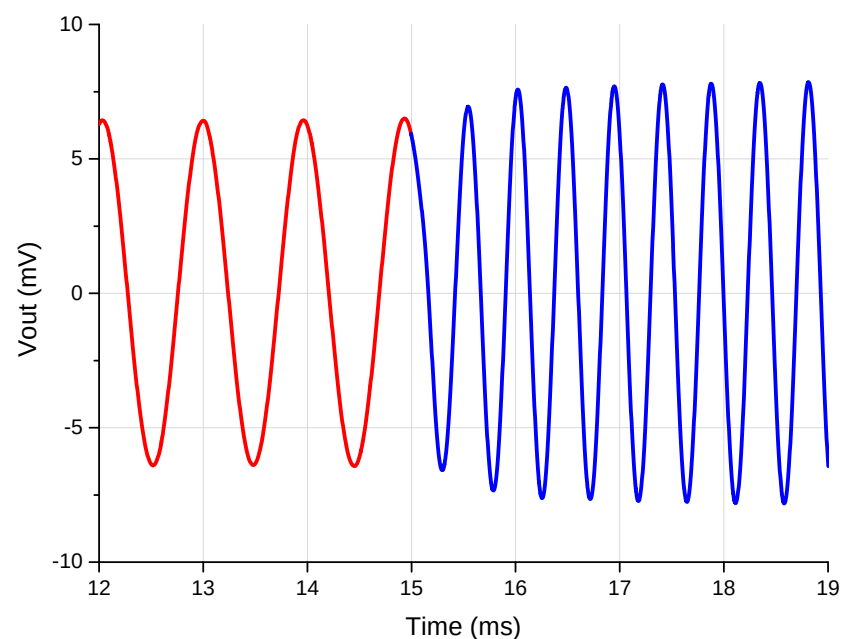


Figure 20. Dynamic settling response for a frequency step from 1 to 2 kHz.

In order to validate the robustness of the sine waveform generator, a 200-run Monte Carlo simulation was performed at 1 and 50 kHz. The results are shown in Figure 21. At 1 kHz, the sinusoidal amplitude has a mean value of 7.3 mV with a standard deviation of 5.9 mV, whereas at 50 kHz the mean value increases to 41 mV with a standard deviation of 9.4 mV. While this amplitude variation could be corrected after fabrication by adjusting the G_{m1}/G_{m2} ratio of the BPF, such calibration is not incorporated in the current design and should be addressed in future implementations. The mean THD remains below 0.3%, decreasing from 0.28% at 1 kHz to 0.24% at 50 kHz, with a standard deviation of 0.11% and 0.27%, respectively. Finally, the frequency distribution of the sine waveform generator is determined by the frequency distribution of the relaxation oscillator, so the mean and standard deviation values are the same as those obtained for the triangular waveform in Section 2: a mean value of 1.02 kHz with 124 Hz standard deviation at 1 kHz, and a mean value of 50.4 kHz with 6.4 kHz standard deviation at 50 kHz. The frequency tuning mechanism provided by the tuning current I_{TUN} of the relaxation oscillator enables precise post-fabrication adjustment to compensate for this dispersion.

Regarding PVT, the proposed low-power sine waveform generator is designed for energy-constrained applications and is intended to operate from a regulated supply voltage to mitigate the impact of supply fluctuations. As for global process and temperature variations, evaluating the generator under fixed open-loop control parameters does not reflect actual operation, since the induced frequency drift is dynamically compensated once integrated into a closed-loop system. The block-level architecture of the master-slave automatic tuning scheme proposed in Appendix A illustrates how this dynamic compensation can be integrated in the final application. However, as this tuning loop is a high-level conceptual proposal, full PVT validation of the closed-loop system is beyond the scope of the present post-layout simulation study. A comparison between the proposed design and recent state-of-the-art sine waveform generators is summarized in Table 7. For Refs. [17,21], which also integrate an output current driver, the silicon area and power consumption of the signal generator were estimated separately to enable a fair comparison. The analog solutions presented in Refs. [17,22] provide a wider frequency tuning range than the proposed generator, at the cost of higher power consumption. In particular, the design in Ref. [17] exhibits higher distortion and consumes approximately 5.5 times more power, while the implementation in Ref. [22] achieves low distortion at a significantly higher output amplitude but consumes several orders of magnitude more power. Furthermore, the design in Ref. [22], which also relies on a relaxation oscillator, requires a massive external capacitor to reach low frequencies, which heavily penalizes the system's portability. Digital approaches, such as the DDS in Ref. [23] or the Delta-Sigma Modulated Look-Up Table ($\Delta\Sigma$ -LUT) architectures in Refs. [21,24], generally exhibit lower distortion figures. The generator in Ref. [21] offers a linearity comparable to our proposal, but features a narrower frequency tuning range (1:5 vs. 1:50). Although the linearity in Ref. [24] stands out, and its power consumption is also slightly lower, its operation is limited to a single 20 kHz frequency. Finally, the design in Ref. [23] provides a wider frequency tuning range and superior linearity at a high output amplitude, but at the cost of a power consumption increase of more than one order of magnitude with respect to this work. In summary, the proposed sine waveform generator shows a good trade-off between frequency programmability, linearity, and power consumption, and is therefore highly suitable for energy-constrained portable medical applications within the kilohertz range.

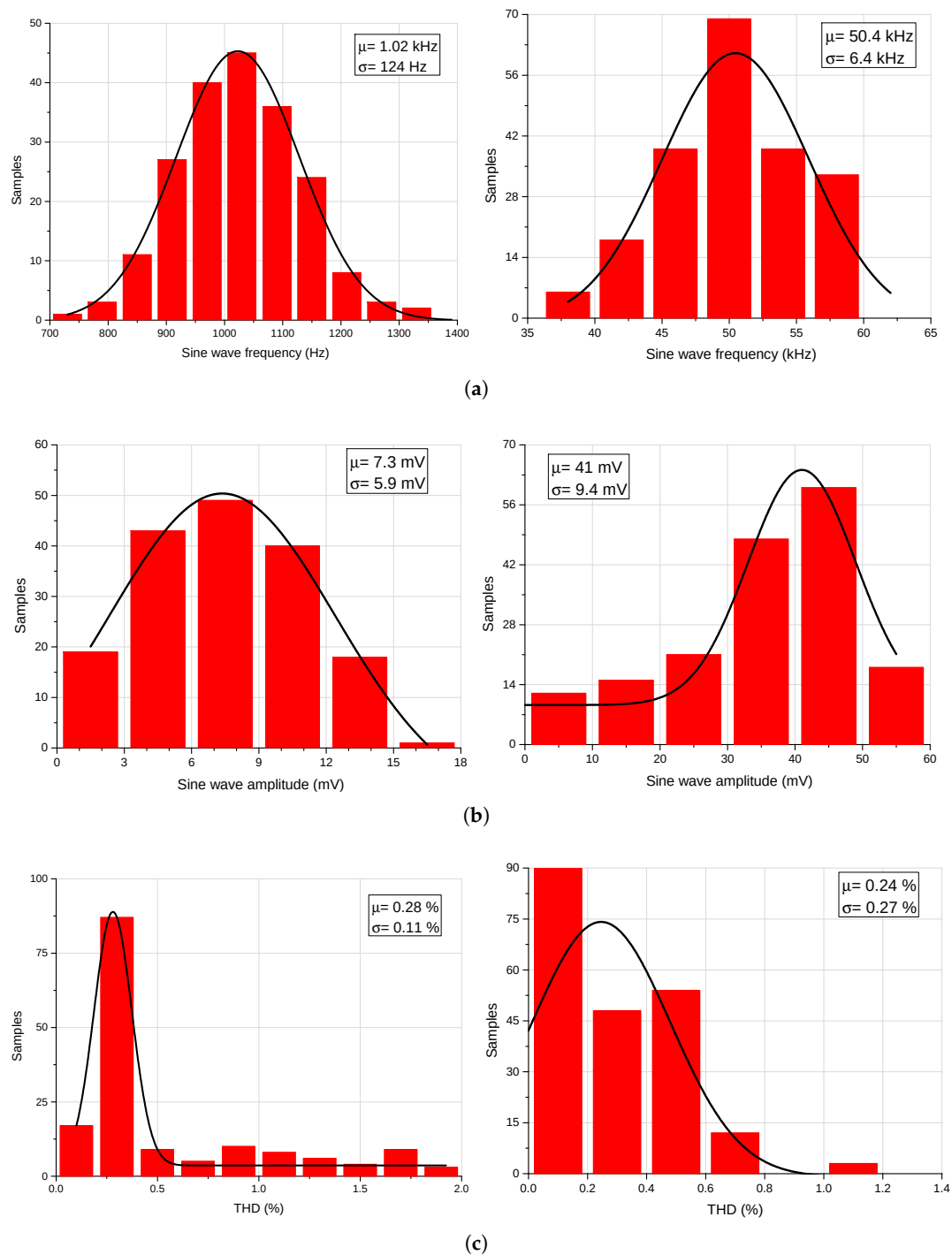


Figure 21. Monte Carlo simulations for the sine wave at 1 kHz and 50 kHz of (a) frequency, (b) amplitude and (c) THD.

Table 7. Performance comparison of sine waveform generators.

Characteristic	This Work	[17]’25	[22]’25	[24]’23	[23]’26	[21]’26
CMOS Process [μm]	0.18	0.18	0.18	0.18	0.18	0.18
V_{DD} [V]	1.8	1.8	5	1.8	3.3	1.8
Frequency Range	1–50 kHz	1 kHz–1 MHz	50 mHz–185 kHz	20 kHz	100 Hz–300 kHz	20–100 kHz

Table 7. Cont.

Characteristic	This Work	[17]’25	[22]’25	[24]’23	[23]’26	[21]’26
Output Amplitude	12 mV _{pp}	38.6 mV _{pp}	360 mV _{pp}	—	700 mV _{pp}	50 μ A _{pp} $\diamond$
THD [%]	0.36	1	0.5	0.07	0.22	0.35
Area [mm ²]	0.7	0.068 [†]	0.49 & $C_{ext} = 200 \mu\text{F}$	0.0072	0.17	0.095 [†]
Power [μ W]	29.3	162.5 [†]	140×10^3	24.8	430	20.3 [†]
Signal generation	Relaxation Oscillator	Gm-C Oscillator	Relaxation Oscillator	$\Delta\Sigma$ -LUT	DDS	$\Delta\Sigma$ -LUT
Validation	Post-layout	Experimental	Post-layout	Experimental	Experimental	Experimental

[†] Estimated from the paper. $\diamond$ Driver output. The wave generator output voltage is not provided.

5. Conclusions

In this paper, a fully integrated CMOS sine waveform generator based on a relaxation oscillator and a sixth-order Gm-C band-pass filter was presented. The proposed circuit was designed in a 0.18 μm CMOS process and operates from a 1.8 V supply voltage. Post-layout simulation results show that the relaxation oscillator generates a differential triangular waveform with a wide frequency tuning range from 300 Hz to 300 kHz, achieved through the combined adjustment of a control current, a reference voltage, and a switchable capacitor bank. The sixth-order Gm-C bandpass filter converts the triangular waveform into a sinusoidal signal with a frequency tuning range from 1 to 50 kHz and a THD lower than 0.36%. Although the maximum center frequency of the BPF is constrained by the low-Gm OTAs designed for low-frequency operation, the use of large on-chip capacitors is avoided, and power consumption is kept to a minimum. The complete sine waveform generator consumes less than 30 μW power, making it suitable for portable BioZ spectroscopy applications within the kilohertz range, such as impedance pneumography-based respiratory monitoring, tissue composition characterization, or cellular health assessment.

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Conflicts of Interest: The authors declare no conflicts of interest.

Appendix A. Automatic Tuning Scheme

To enable continuous frequency sweeping for spectroscopy applications, a high-level master–slave automatic tuning architecture with a digital control circuit (DCC) is conceptually proposed, as shown in Figure A1. The DCC provides the reference clock signal V_{ref} that sets the frequency of the whole circuit. Internally, the DCC features a digital step-counter to sweep the frequency of the clock reference, and a magnitude comparator continuously

evaluates this counter to automatically set the sub-band selection bits (a_0, b_0) according to the corresponding frequency range: (1, 0) from 1 to 10 kHz, and (0, 1) from 10 to 50 kHz. Consequently, the DCC manages both the fine-tuning steps and the coarse sub-band selection. The relaxation oscillator acts as the master block, while the BPF functions as the slave, dynamically tracking the master's frequency.

The master loop is based on an analog phase-locked loop (PLL) to establish the oscillation frequency of the triangular signal. The differential square-wave output provided by the relaxation oscillator (ϕ_1 and $\bar{\phi}_1$ in Figure 7), which is synchronized with the triangular signal, is converted via a limiter into a single-ended digital clock with clean, rail-to-rail transitions, and is then fed into the PFD and compared with V_{ref} . A charge pump (CP) at the output of the PFD provides the analog control voltage required to adjust I_{TUN} , forcing the triangular wave to precisely lock onto V_{ref} .

As for the slave loop, the fully differential output of the BPF is first processed by a differential-to-single-ended (D2S) converter followed by a peak detector (PD) to extract its amplitude envelope (V_{peak}). A dual sample-and-hold network operates in an alternating configuration: one capacitor tracks and stores the current peak voltage, while the second capacitor holds the voltage from the previous state. An analog comparator evaluates both nodes and delivers a binary decision to the digital control logic. Following a successive-approximation register (SAR) algorithm, the digital logic adjusts a digital-to-analog converter (DAC) to tune the BPF. By locking the DAC code at the point of maximum output amplitude, the system guarantees synchronization between the triangular signal and the BPF across the entire frequency sweep.

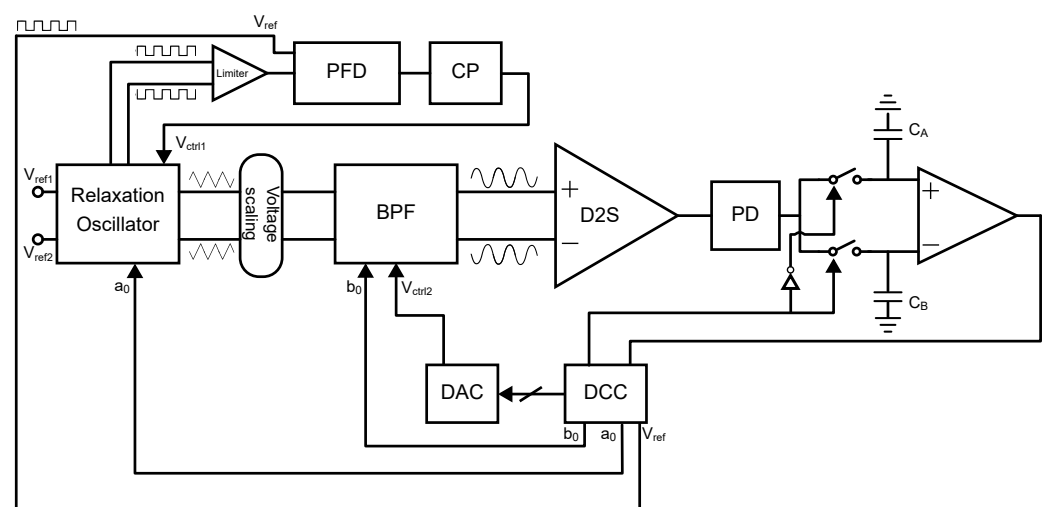


Figure A1. Master–slave automatic tuning architecture.

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