

Article

Underwater Power Conversion and Junction Technology for Underwater Wireless Power Transfer Stations

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Abstract: Underwater wireless power transfer (UWPT) systems are appropriate for battery charging of compact, submerged devices without a complicated and expensive sealing structure or human contact because the power source and load are not physically connected. For the shore-based power supply situation, the underwater power conversion and junction technology should be required to drop down shore-based voltage to the target voltage for the underwater energy supply of the UWPT system. This paper proposes a lightweight, high efficiency and power density underwater power conversion connector system for the UWPT system, in which the LLC resonant converter is constructed with SiC transistors. The full load range zero-voltage switching (ZVS) and load adaptive characteristics have been achieved. The optimized RC level shift driver is adopted to highly reduce the switching loss of SiC transistors. Shore-based voltage of 1000 V was converted to the target voltage of 375 V for the UWPT system. The highest measured efficiency is over 98% at a load power level of 1500 W underwater conditions.



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Keywords: underwater wireless power transfer; underwater power conversion connector; LLC resonant converter; SiC MOSFETs; RC level shift driver

1. Introduction

The maritime observation network has contributed to the improvement of fisheries management, climate projections, and weather forecasts in the past 30 years. It carries out real-time monitoring of ocean dynamics [1–3]. Given the scientific and social requirements of long-term, wide-area, and real-time observation, the marine observation network has acted as an important tool for marine research disaster prevention and early warning [4].

For the marine observation network, the compact, submerged devices, such as unmanned underwater vehicles (UUVs) and autonomous underwater vehicles (AUVs) are playing more and more important roles in survey and monitoring tasks [5]. However, the insufficient battery capacity of UUVs or AUVs is one of the primary causes of restricted mobility. There are different power supply methods, including salvage power replacement and wet plug charging [6], which have the disadvantages of costly, laborious, and complicated maintenance. The underwater wireless power transfer (UWPT) technology has been proposed for charging small, submerged devices, such as AUVs [7,8]. The inductive wireless power transfer (IPT) system's operation is examined in [9] from the standpoint of the distribution of electromagnetic fields. The IPT system's mutual inductance model is simplified and approximated with the electromagnetic field model. Paper [10] figures

out that the diversity and flexibility of devices carried by the ROVs could be increased by the wireless power transfer (WPT) system. It achieves a convenient and safe battery power supply. To increase the rotational and axial misalignment tolerance for AUVs, a novel magnetic coupler in a free-rotation WPT system is given in [11]. For swarm AUVs, a new multi-directional magnetic coupler-based simultaneous wireless power and data transfer system is given in [12]. Other papers [13–15] discuss the high frequency alternating magnetic field resonance compensation network and the coupling structure of the underwater wireless power transmission system. For the underwater power supply application, the capacitive wireless power transmission method has also been presented [16,17]. With the attention of different countries and the large-scale application of underwater vehicles, the underwater wireless power supply technology will develop rapidly.

The above research work improves the charging efficiency and charging stability of AUVs and other devices by optimizing the compensation network or coupling mechanism of the UWPT system. However, paper [18] claims that DC voltage fluctuation widely exists in HVDC systems. This study is concentrated on the power conversion and distribution module to prevent the effect of voltage fluctuations on the stability of the system. The stable voltage conversion from the shore-based high voltage to the expected input voltage of the UWPT system is realized. The parameters of voltage conversion are based on small offshore submarine observation networks, such as the South China Sea Submarine Observation Network and Canada's VENUS Observation Network. Therefore, the connection box needs to achieve 1 kV/375 V voltage conversion. The target power level of a single node is 1.5 kW [19]. To improve the power conversion efficiency and reduce heat losses, there are different topologies that have been proposed, as shown in Table 1, such as the half-bridge LLC resonant circuit, LCL-T resonant DC-DC circuit, parallel resonant DC-DC circuit and dual active bridge (DAB) circuit [20–25]. Most topologies have a switching frequency exceeding 100 kHz to decrease the system size and improve the power density. Additionally, the configuration of zero-voltage switching (ZVS) significantly reduces these topologies' switching losses.

Table 1. Comparison of different underwater power conversion junction topologies.

Reference	Type of Topology	Power Level	Output Voltage	Soft Switching	Switching Frequency	Efficiency
[20]	LLC resonant	/	380 V	Nope	106 kHz	/
[21]	Parallel resonant	450 W	120 V	ZVS	250 kHz	/
[22]	LCL-T resonant	500 W	150 V	ZVS	250 kHz	96.0%
[23]	Parallel resonant	500 W	50~250 V	ZVS	250 kHz	94.0%
[24]	DAB	500 W	150 V	ZVS	250 kHz	95.0%
[25]	LLC resonant	200 W	60 V	ZVS/ZCS	100 kHz	93.2%
This Work	LLC resonant	1500 W	375 V	ZVS/ZCS	100 kHz	98.0%

To extend the application range with high efficiency and high power density, this paper presents a 1500 W power level undersea DC-DC converter with the LLC resonant circuit topology for the UWPT system. It could provide the load adaptive feature operating with the variable load resistance. The resonant frequency of the converter is set as 100 kHz with the SiC transistors. The power conversion efficiency at the rated power level is 98% with the shore-based power supply. What is more, corrosion-protection, pressure-resistant, and low-cost hull designs are adopted.

The sections of this paper are organized as follows. Section 2 provides the design of the underwater power conversion connector system and the principle of ZVS. This section proposes a dead zone time calculation method based on critical ZVS. The design of the gate driver structure of the wide-bandgap device is shown in Section 3. Section 4 shows the flow of the parameter design. Simulation and experiments in the water environment are carried out in Section 5. Conclusions and discussions are presented in Section 6.

2. Operation Analysis of the Power Conversion System

2.1. Frequency Domain Analysis of LLC Circuits

The topology and the equivalent circuit of the underwater power conversion connector system are shown in Figures 1 and 2. According to the output current and voltage relationship based on the equivalent circuit model, the load resistance of the LLC resonant converter could be converted to the primary equivalent resistance of the transformer [26]. The equivalent resistance R_{eq} and the equivalent input voltage V_{ab} are derived as follows:

$$V_{ab} = \frac{2\sqrt{2}}{\pi} V_{in}, \quad R_{eq} = \frac{8N^2}{\pi^2} R_o \quad (1)$$

where N is the transformer turns ratio, V_{in} is the input voltage, and R_o is the load resistance.

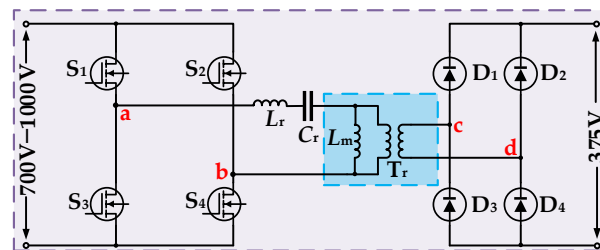


Figure 1. Topology of the underwater power conversion connector system.

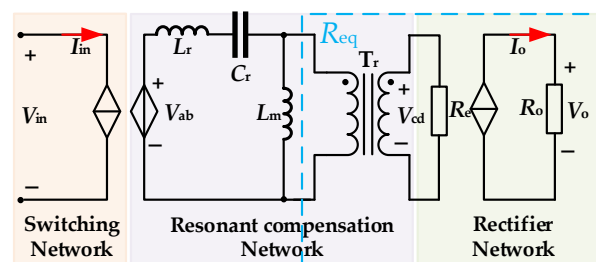


Figure 2. Equivalent circuit of the underwater power conversion connector system.

According to Figure 2, the system transfer function is calculated as follows:

$$H(j\omega) = \frac{V_o}{V_{ab}} = \frac{j\omega L_m R_{eq}}{\frac{L_m}{C_r} + \frac{R_{eq}}{j\omega C_r} + j\omega L_r R_{eq} + j\omega L_m R_{eq} - \omega^2 L_m L_r} \quad (2)$$

where L_r is the resonant inductor, L_m is the magnetic inductor, C_r is the resonant capacitor, and ω is the switching angular frequency.

In the paper, K can be defined as the ratio between magnetic inductance L_m and the resonant inductance L_r , F is the ratio between switching frequency f_s and the resonant frequency f_{r1} , and Q is the quality factor of the resonance circuit.

$$K = \frac{L_m}{L_r}, \quad F = \frac{f_s}{f_{r1}}, \quad Q = \frac{1}{R_{eq}} \sqrt{\frac{L_r}{C_r}} \quad (3)$$

Therefore, the normalized gain can be obtained as follows:

$$M = \left| \frac{V_o}{V_{ab}} \right| = \frac{1}{\sqrt{\left[1 + \frac{1}{K} \left(1 - \frac{1}{F^2}\right)\right]^2 + Q^2 \left(F - \frac{1}{F}\right)^2}} \quad (4)$$

According to the relationship between the switching frequency f_s and the first and second resonant frequencies f_{r1} and f_{r2} , the LLC resonant converter is divided into three

operating intervals: $f_s > f_{r1}$, $f_s = f_{r1}$, and $f_{r2} < f_s < f_{r1}$. The LLC resonant converter ensures the ZVS of the SiC transistors of the primary side full-bridge circuit. When the phase of the output voltage of transistors is ahead of the phase of the current flowing through the transistors at the beginning of the conversion process, the switching frequency $f_s > f_{r2}$. The resonant cavity will be equivalent to the inductive impedance. When the switching frequency $f_s > f_{r1}$, the primary side network still maintains the characteristics of ZVS [27]. The resonant frequency f_{r1} and f_{r2} can, respectively, be expressed as follows:

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}}, \quad f_{r2} = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \quad (5)$$

Based on Equation (5), when the switching frequency f_{r1} is equal to the second resonant frequency f_{r2} , the system is considered as the resistive load. The zero-phase angle (ZPA) output character will be achieved. According to paper [27], when the switching frequency is $f_{r2} < f_s < f_{r1}$ or $f_s = f_{r1}$, the operating state of the converter is the same. When the inductance characteristic of the circuit rather than the resistance characteristic is maintained, the ZVS character of the MOSFETs is achieved. Therefore, when the controller of the system is designed, the frequency fluctuation should be kept in the range of $f_{r2} < f_s \leq f_{r1}$. At the rated operating point of the system, the switching frequency should be maintained as f_{r1} .

By substituting Equations (1) and (3) into (5), the resonant inductors L_r and the resonant capacitors C_r and the magnetic inductors L_m can be expressed as follows:

$$C_r = \frac{1}{2\pi Q f_{r1} \cdot R_{eq}}, \quad L_r = \frac{1}{(2\pi f_{r1})^2 \cdot C_r}, \quad L_m = K \cdot L_r \quad (6)$$

2.2. Time Domain Analysis of LLC Circuits

During the circuit design, the efficiency of the system and the stress of the components must be evaluated. Paper [28] proves that the loss of the LLC converter mainly comes from the transformer and resonant inductor L_r . The transformer loss includes the iron loss and the copper loss. Therefore, the total loss of the system can be expressed as follows:

$$P_{loss} = I_{r,rms}^2 R_r + I_{m,rms}^2 R_m + K_f B_m^2 f_s^2 V_T^2 \quad (7)$$

where R_r is the equivalent resistance of the resonant inductor, R_m is the equivalent resistance of the transformer, $I_{r,rms}$ is the effective value of the resonant current, $I_{m,rms}$ is the effective value of the excitation current, K_f is the loss coefficient, B_m is the flux density, and V_T is the volume of the magnetic core.

In paper [29], the law of the conservation of energy is well applied. The resonant current $I_{r,rms}$ and secondary side current of transformer $I_{s,rms}$ can be written as follows:

$$\begin{cases} I_{r,rms} = \frac{\sqrt{4\pi^2 P_o^2 L_m^2 f_{r1}^2 + V_{in}^4}}{4\sqrt{2} V_{in} L_m f_{r1}} \\ I_{s,rms} = \frac{V_{in} \cdot \sqrt{5\pi^2 N^4 R_o^2 - 48N^4 R_o^2 + 12\pi^4 L_m^2 f_{r1}^2}}{4\sqrt{6} N L_m f_{r1} R_o^2} \end{cases} \quad (8)$$

where P_o is the ideal output power.

The effective value of excitation current $I_{m,rms}$ can be expressed as follows:

$$I_{m,rms} = I_{r,rms} - \frac{I_{s,rms}}{N} \quad (9)$$

Furthermore, by substituting Equation (3) into Equation (6), L_m will be obtained as follows:

$$L_m = \frac{kQ \cdot R_{eq}}{2\pi f_{r1}} \quad (10)$$

Therefore, the parameters of the system can be expressed as:

$$\begin{cases} v_{ab} = \frac{2\sqrt{2}}{\pi} \sin(\omega t) \\ i_r = \sqrt{2} I_{r,rms} \sin(\omega t + \alpha) \\ v_{L_r} = \sqrt{2} I_{r,rms} \cdot \omega L_r \cos(\omega t + \alpha) \\ v_{C_r} = -\frac{\sqrt{2} I_{r,rms}}{\omega C_r} \cos(\omega t + \alpha) \\ \eta = \frac{P_o}{P_o + P_{loss}} \end{cases} \quad (11)$$

where α is the phase difference between resonant current i_r and resonant voltage v_{ab} ($\alpha = -\arcsin \frac{V_{in}}{4\sqrt{2} I_{r,rms} L_m f_{r1}}$), v_{L_r} is the voltage stress of L_r , v_{C_r} is the voltage stress of C_r , and η is the efficiency of the system.

According to Equations (7)–(11), the influence of quality factor Q as well as inductance ratio K on the circuit state can be established. The conclusion is as follows:

- When the system is at the rated operating point, the increases in K value and Q value contribute to the increase of the system efficiency.
- When the system is out of the rated operating point, too large a K value will reduce the adjustment range of the switching frequency. It will not be conducive to the design of the control circuit and will cause the system to lose stability. When Q is too large, the system may enter the capacitive working region during the frequency regulation process. This is not conducive to the implementation of ZVS. What is more, it is difficult to achieve the high voltage gain of the system when the Q is too large.
- K and Q that are too large will also increase the current of the circuit and improve the voltage stress of the resonant element. This is not conducive to the selection of component models.

Based on the above discussions, the circuit parameters are designed in Section 4.

2.3. ZVS Characteristic Analysis

When LLC resonant converters are applied in high-voltage and high-power situations, it is usually necessary to select a larger dead zone time to ensure the safe operation of the system. However, the soft switching characteristic of the converter is affected by dead zone time. The traditional design method mainly considers the influence of switch junction capacitance on soft switching characteristic. It achieves complete discharge of junction capacitance within the dead zone time by reducing excitation inductance to ensure the ZVS [27]. However, the above measurements will increase the turn-off loss. To address the above issues, the dead zone time design method under critical conditions is proposed in this paper.

The mechanism of ZVS is shown in Figure 3a. There is a dead zone between t_1 and t_2 . During this period, all the MOSFETs are turned off and the resonant current is equal to the excitation current. On the one hand, the excitation current discharges the junction capacitors of S_2 and S_3 . On the other hand, the excitation current charges the junction capacitors of S_1 and S_4 until the voltage of the junction capacitors of S_2 and S_3 is 0 V. At the same time, the body diodes of S_2 and S_3 are conducting until t_2 , when the S_2 and S_3 will be turned on. Therefore, the ZVS of S_2 and S_3 can be achieved. S_1 and S_4 are kept at ZVS from t_3 to t_4 .

To ensure the safe operation of each bridge arm switch tube, the dead zone time needs to meet the requirement of the following Equation (12):

$$t_d \geq (t_{off} - t_{on}) + t_p \quad (12)$$

where t_d is the dead zone time, t_{off} is the falling edge time of the drive signal, t_{on} is the rising edge time of the drive signal, and t_p is the delay time of signal transmission.

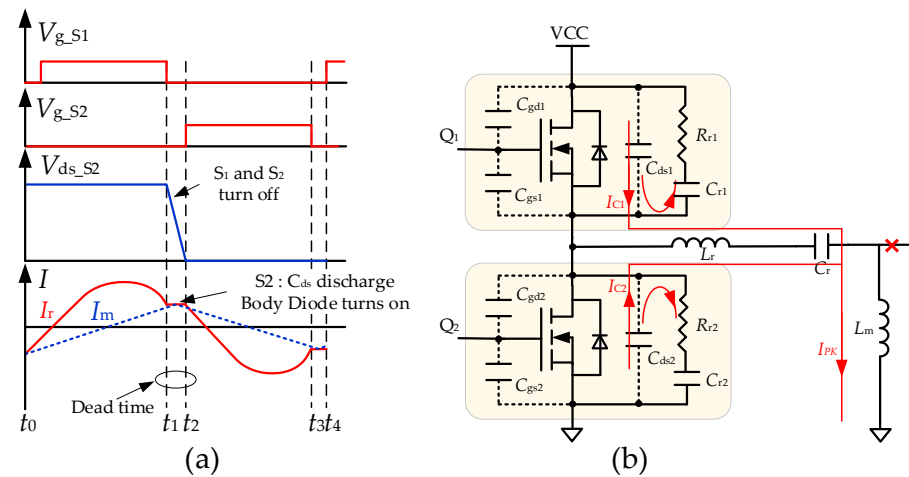


Figure 3. (a) ZVS timing waveform; (b) current path of bridge arm from t_1 to t_2 .

During the commutation period of the primary side MOSFETs, ZVS can be achieved by cycling the excitation current between the upper and lower bridge arm capacitors. Therefore, it should ensure that there is sufficient dead zone time for the body capacitors to complete charging and discharging. According to Figure 3a, the ZVS condition is guaranteed by the peak excitation current I_{PK} . Equation (13) is as follows:

$$I_{PK} = \frac{NV_o}{L_m} \cdot \frac{T_s}{4} \quad (13)$$

where T_s is the switching period of MOSFETs.

To make sure that the energy stored in the body capacitors of the transistor can be fully released into the resonant cavity within the dead zone time, the excitation current from t_1 to t_2 should meet the following requirement:

$$\frac{1}{2}(L_m + L_r)I_{PK}^2 > \frac{1}{2} \cdot C_j V_{in}^2 \quad (14)$$

It is worth noting that the junction capacitance C_j in (14) includes the drain-source capacitance of the MOSFET and the buffer circuit capacitance. C_j is expressed as follows:

$$C_j = C_{ds} + C_s \quad (15)$$

where C_{ds} is the parasitic capacitor of MOSFETs, and C_s is the parallel capacitance of MOSFETs.

Due to the large excitation inductance, it can be assumed that the excitation current is constant. It means that between t_1 and t_2 , the excitation inductance charges or discharges the junction capacitor C_j with a constant current $I_{PK}/2$. Furthermore, the junction capacitor current will also flow into the buffer circuit. This will reduce the time required for discharging. At this point, the current path in the half-bridge circuit is shown in Figure 3b, and the dead zone time can be written as t_d , as follows:

$$\frac{V_{in}C_{ds}}{I_{PK} \cdot \frac{C_s}{C_{ds}+C_s}} \leq t_d \leq \frac{V_{in}C_j}{\frac{I_{PK}}{2}} \quad (16)$$

3. Optimization Design of Driving Circuit

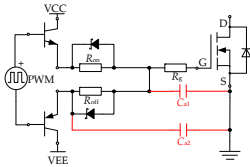
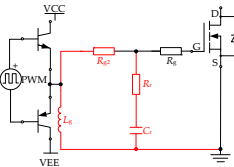
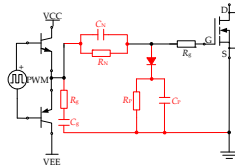
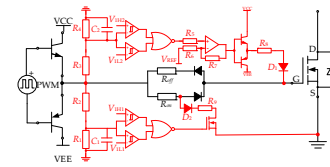
The switching characteristics of SiC MOSFETs are mainly affected by parasitic junction capacitance, in which C_{gd} forms a feedback loop between the input (GS) and output (DS). This will greatly increase the input capacitance and affect the circuit characteristics. The above phenomenon is called the Miller effect. As a result, the C_{gd} is also known as Miller capacitance. The Miller capacitors in a half-bridge are C_{gd1} and C_{gd2} , as seen in Figure 3b.

The main difference between the SiC device and the Si device is the size of the Miller capacitor. The SiC device has a smaller Miller capacitor. Therefore, the drive voltage rise time and the fall time is shorter. The high-frequency characteristics of SiC devices are better than Si devices [30].

However, with the high switching frequency, there will be some challenges, such as the ringing effect and the high-frequency crosstalk effect. These will increase switching loss or cause false turn-on in full-bridge applications, resulting in circuit efficiency reduction or even device burnout [31]. To solve the above problems, the driver circuit needs to be redesigned.

For different issues, different driver structures are proposed in other papers [32–35], as shown in Table 2. In this paper, the output voltage (DS) of MOSFET is 1000 V. The switching frequency is set between 85–150 kHz. Based on [32–35], the RC level shift structure is selected as the gate driving structure. A traditional level shift structure uses resistors and capacitors to form an energy absorption circuit. This helps to eliminate gate oscillation [34]. However, it will generate energy loss during a steady state. The circuit efficiency will be reduced. Therefore, the parallel circuit composed of R_g and C_g is replaced by the magnetic bead. This unique design not only contributes to inhibiting the oscillation of a specific frequency but also reduces the switching loss. At the same time, it will also reduce the voltage spikes. The switching voltages of D_{P1} and D_{P2} are clamped. The R_s and C_s are injected between the source and drain to absorb the inrush current to ensure that the transistors are working within the safety zone. The optimized gate driver structure is shown in Figure 4.

Table 2. Comparisons of different drive structures.

Reference	[32]	[33]	[34]	[35]
Feature	Dual Capacitance	Passive RC Resonant	RCD Level Shift	Active Current Injection
Driver Structure				
Advantages	Low turn-off gate impedance	Small oscillation of drive voltage	Stable turn-on or turn-off state	Small transient drive voltage and current
Disadvantages	Turn-off time delay increased	High drain-source voltage	Causes higher order oscillations	Complex circuit and driving loss is large
Test Conditions	In the 1.1 kW buck converter	Double pulse test	In the 1 kW full-bridge inverter	Double pulse test
Type of Device	C3M0065090X	EPC2015	C3M0065090J	CMF20120D
Frequency	100 kHz	200 kHz	145 kHz	100 kHz
Conclusion	System efficiency is improved by 0.60%	Oscillation amplitude is reduced by 61.00%	Switching loss is improved by 24.9%	The peak of the drain current is reduced by 19.50%

Based on the driving circuit proposed in Figure 4, the on-transient driving current and crosstalk current paths of SiC MOSFETs are analyzed. The equivalent circuit diagram is obtained, as shown in Figure 5. In Figure 5, the blue path represents the direction of the driving current, and the red path represents the direction of energy transfer. Therefore, according to Figure 5, the parameters of the drive circuit can be designed.

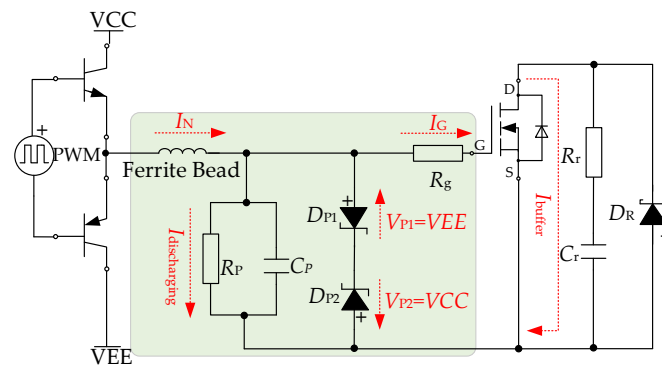


Figure 4. Optimized gate driver structure.

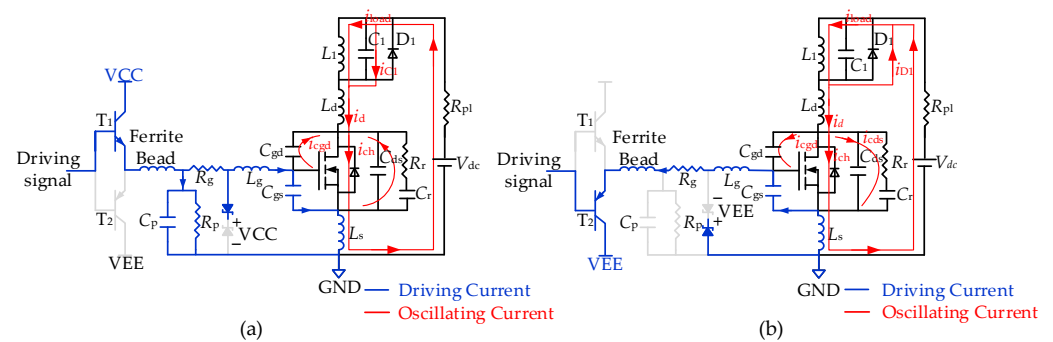


Figure 5. (a) Transient current path of the circuit opening state; (b) transient current path of the circuit off state.

3.1. Gate Circuit Design

In the design of the gate circuit, the appropriate magnetic bead and resistance should be selected properly. Based on Kirchhoff's law, the drive current is analyzed. The following equations can be derived:

$$\begin{cases} i_d = i_{\text{load}} + i_{C1} \\ i_d = i_{\text{ch}} \pm i_{\text{cgd}} \pm i_{\text{cds}} \end{cases} \quad (17)$$

$$(L_d + L_s) \frac{di_d}{dt} + V_{C_1} + R_{pl} i_d = V_{dc} \quad (18)$$

where i_{load} is the conduction current, i_{d} is the drain current of MOSFETs, i_{ch} is the channel current of MOSFETs, i_{cgd} is the current flowing through C_{gd} , i_{cds} is the current flowing through C_{ds} , i_{C1} is the current flowing through C_1 .

Generally, the effect of R_{pl} will be ignored. During the opening phase of MOSFETs, substituting Equation (17) into (18), the following equation can be achieved:

$$(L_d + L_s)C_1 \frac{d^2 i_{C_1}}{dt^2} + i_{C_1} = -C_1 \frac{dV_{ds}}{dt} \quad (19)$$

During the off phase of MOSFETs, Equation (19) can be rewritten as the following Equation (20):

$$(L_d + L_s) \left(C_{gd} + C_{ds} \right) \frac{d^2 V_{ds}}{dt^2} + V_{ds} = V_{dc} - (L_d + L_s) \frac{di_{ch}}{dt} \quad (20)$$

It can be concluded that the on-oscillation is caused by the parasitic inductors L_d and L_s of the main power loop and the parasitic capacitor C_1 of the complementary bridge arm.

The off-oscillation is caused by the parasitic inductors L_d and L_s of the main power loop and the parasitic capacitors C_{gd} and C_{ds} of the off-bridge arm. Equation (21) is as follows:

$$f_{on} = \frac{1}{2\pi} \sqrt{\frac{1}{(L_d + L_s)C_p}}, f_{off} = \frac{1}{2\pi} \sqrt{\frac{1}{(L_d + L_s)(C_{gd} + C_{ds})}} \quad (21)$$

where f_{on} is the frequency of on-oscillation and f_{off} is the frequency of off-oscillation.

Through the above derivation, the model of magnetic bead is determined in this paper. In addition, the selection of gate resistors is the key step to achieving the high performance of the driving circuit. A small resistance value could cause the gate drive voltage to overshoot, while a larger resistance value can bring about oscillation over damping and prolong switching time. The impedance equation of the gate circuit is obtained as follows:

$$Z_{gate} = (R_{DC} + j\omega L_F) || R_g + j\omega L_g \quad (22)$$

where L_F is the ferrite bead equivalent inductance, R_{DC} is the ferrite bead equivalent DC resistance, and R_{AC} is the ferrite bead equivalent AC resistance.

Therefore, the factor quality of the gate circuit Q_{gate} can be expressed as follows:

$$Q_{gate} = \frac{\text{Im}(Z_{gate})}{\text{Re}(Z_{gate})} = \frac{\omega R_{AC} \cdot A - \omega L_F \cdot B}{\omega^2 L_F \cdot A + R_{AC} \cdot B} \quad (23)$$

A and B can, respectively, be written as follows:

$$\begin{cases} A = R_{AC}L_F + R_gL_F + R_{AC}L_g \\ B = R_{AC}R_{DC} + R_{AC}R_g - \omega^2 L_FL_g \end{cases} \quad (24)$$

Based on the above discussion, there is a gate resistor with a quality factor Q_{gate} between 0.5 (critical damping) and 1 (underdamping) that needs to be designed. When the Q_{gate} is determined, an appropriate resistance value will be calculated.

3.2. Shift Circuit Design

According to Figure 4, the parameters of the shift circuit are shown as in the following Equation (25):

$$V_{CP-off} = \frac{R_P}{R_P + R_g} \cdot (-VEE), V_{CP-on} = \frac{R_P}{R_P + R_g} \cdot VCC \quad (25)$$

where V_{CP-on} is the voltage of the shift circuit when the MOSFET is turning on, and V_{CP-off} is the voltage of the shift circuit when the MOSFET is turning off.

At the same time, the gate circuit is described as follows:

$$V_F = VCC - V_{CP} = L_F \frac{di_F}{dt} \quad (26)$$

where V_F is the magnetic bead voltage and i_F is the magnetic bead current. Equation (27) is as follows:

$$i_F = i_g + i_P \quad (27)$$

where i_g is the drive current, and i_P is the shift circuit current.

$$i_P = \frac{V_{CP}}{R_P} + C_P \frac{dV_{CP}}{dt} \quad (28)$$

Therefore, the critical driving current and the relationship between capacitance and resistance in the shift circuit are determined.

3.3. RC Buffer Circuit Design

Paper [35] analyzed the generation mechanism of crosstalk and overvoltage; MOSFETs will generate overvoltage due to their parasitic inductance when it is turned on and off, and the voltage peak is derived as follows:

$$V_{\max} = V_{\text{in}} + V_D + \left(-L_S \frac{di_d}{dt} \right) \quad (29)$$

where V_{in} is the supply voltage, V_D is the diode transient forward voltage drop, L_S is the parasitic inductance of the transistor, and i_d is the drain current of the transistor.

In the driver circuit, the electromagnetic energy stored in the parasitic inductance can be written as follows:

$$W_{L_S} = \int_0^{t_0} U(t)I(t)dt = \frac{1}{2}L_S I_d^2 \quad (30)$$

The energy absorbed by the buffer circuit is as follows:

$$W_{RC} = \frac{1}{2}C_s V_{\max}^2 - \frac{1}{2}C_s V_{\text{in}}^2 \quad (31)$$

Ideally, the energy spilled by the parasitic inductor needs to be fully absorbed by the buffer circuit. As a result, an expression for the buffer capacitance can be derived as:

$$C_s = \frac{L_S i_d^2}{V_{\max}^2 - V_{\text{in}}^2} \quad (32)$$

For the design of the resistance value, the buffer circuit should conduct the energy transfer in one cycle. Furthermore, the resistance should have a certain suppression effect on the oscillation caused by parasitic parameters. Therefore, when the switching signal duty cycle is set to 0.5, R_s can be obtained as follows:

$$\begin{cases} R_s \leq \frac{T_S}{2C_s} \\ R_s \leq \sqrt{\frac{L_d}{C_{ds}}} \end{cases} \quad (33)$$

4. Circuit Design for Underwater Power Conversion Connector System

The design method mentioned in this paper has been applied to the 1.5 kW LLC resonant converter. The subsequent content presents an elaborate design procedure.

- (1) The value of the excitation inductor L_m needs to be calculated. The first resonant frequency of the system is 100 kHz. According to Equation (8), the relationship between the excitation inductor L_m and the system current can be established. As shown in Figure 6a, when the resonant current is less than 5 A, the critical value of the excitation inductor L_m is 384 μH .
- (2) K and Q need to be selected. The effect of K and Q on the system efficiency is shown in Figure 7. When the value of L_m is 384 μH , the relationship between K and Q is shown as the red curve. In addition, to achieve the high efficiency of the system, K and Q should be designed in the area above the blue curve. According to Figure 7b, the critical K and Q values are set as (5.3, 0.6), respectively.
- (3) The parameters of the power circuit that need to be designed. According to Equations (3) and (6), the values of the resonant capacitance C_r and the resonant inductance L_r are determined. In addition, according to Equation (11), the voltage stress of the system is shown in Figure 6b. The maximum voltage stress of the resonant capacitor C_r is 653 V, and the minimum is 480 V. The maximum voltage stress of the resonant inductance L_r is 316 V, and the minimum value is 311 V. Inductors and capacitors need to be connected in parallel or in series to meet the stress requirements.

- (4) The model of MOSFET selected in the paper is SCT20N170. Furthermore, the optical coupler is the ACPL-332J-500E, and it has a maximum propagation delay of 250 ns. According to the datasheet of MOSFET, the parasitic capacitance and the drive parameters are shown in Table 3.
- (5) Based on the driving circuit design theory presented in Section 3, the gate ferrite bead BLM18PG121SN1D is selected to suppress the oscillations during the turn-on and turn-off processes. At the same time, when the input voltage is 1000 V, the expected maximum voltage oscillation is 1200 V. According to Equations (32) and (33), the parameters of the driver circuit and power circuit are shown in Table 4.

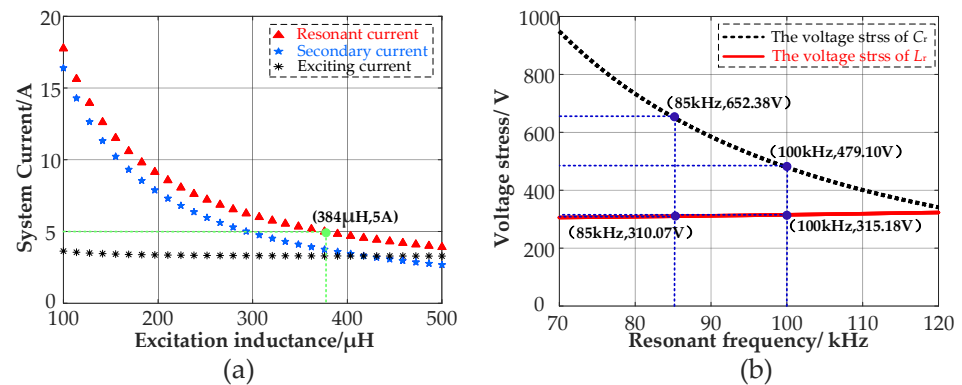


Figure 6. (a) The relationship between excitation inductor L_m and system current; (b) the relationship between resonant frequency f_{r1} and voltage stress.

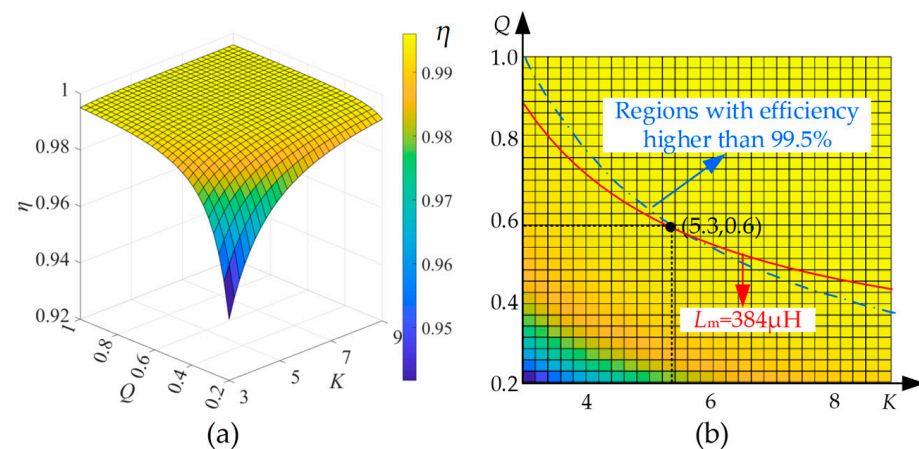


Figure 7. (a) The relationship between K , Q , and system efficiency (3D); (b) relationship between K , Q , and system efficiency (X-Y plane).

Table 3. Parasitic parameters and operating voltage and current of MOSFET.

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1000	V
V_{GS}	Gate-source voltage	−5/+20	V
I_D	Drain current (25 °C to 100 °C)	5	A
C_{iss}	Input capacitance	1568	pF
C_{oss}	Output capacitance	141	pF
C_{rss}	Reverse transfer capacitance	21	pF
t_d	Dead zone time of driving	127–302	ns

Table 4. Parameters of the driving circuit.

Symbol	Parameter	Value	Unit
Drive Circuit Specifications			
R_g	Gate resistance	7.85	Ω
R_p	Shift circuit resistance	4	k Ω
C_p	Shift circuit capacitance	513	nF
R_s	Buffer circuit resistance	83	m Ω
C_s	Buffer circuit capacitance	15	pF
Resonant Circuit Specifications			
n	Turns ratio of the transformer	8/3	
L_r	Resonant inductance	72.45	μ H
C_r	Resonant capacitance	23	nF
L_m	Magnetic inductance	384	μ H

5. Simulated and Experimental Verification

Based on LT-Spice, the switching transient processes of gate-source voltage and drain-source voltage of SiC MOSFETs are simulated. The simulated results are shown in Figure 8. Figure 8a,b are the waveforms before the optimization of the driving circuit. Figure 8c,d show the optimized waveforms of the driving circuit. According to Figure 8, the oscillation period is significantly reduced after the driver circuit is optimized. Substantial energy losses are avoided. Furthermore, the high dv/dt of the drain-source voltage is almost unaffected. This means that the original switching speed can be guaranteed. Compared to the pre-optimized waveform, a more stable state of the MOSFETs when turned on or turned off is guaranteed by the optimized drive structure.

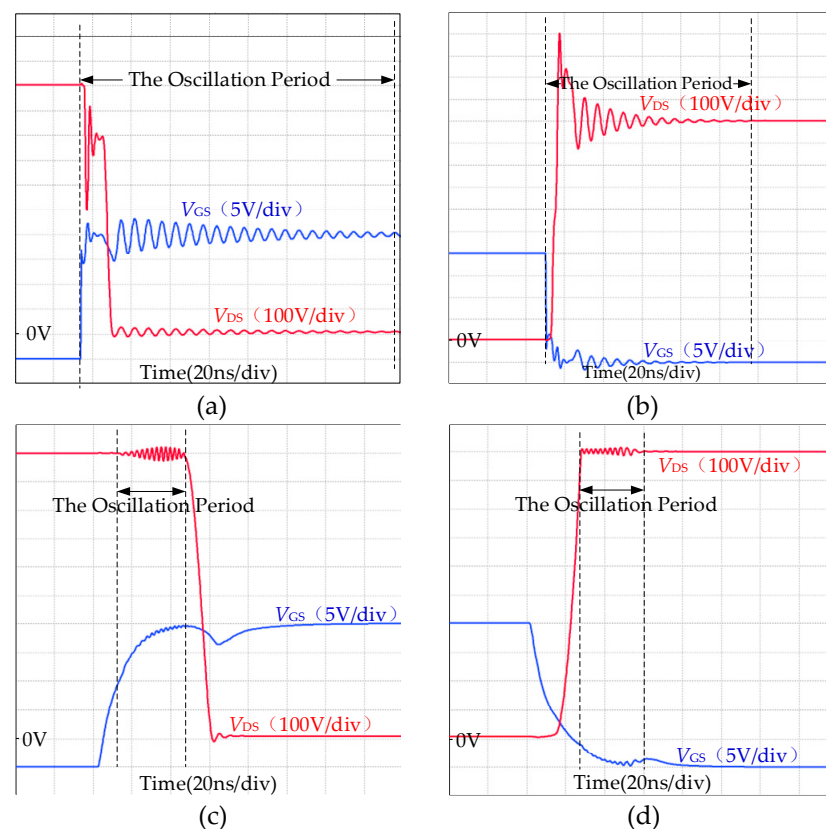


Figure 8. (a) The opening stage of SiC MOSFET before the optimization; (b) the closing stage of SiC MOSFET before the optimization; (c) the opening stage of SiC MOSFET after the optimization; (d) the closing stage of SiC MOSFET after the optimization.

The power circuit design theory is validated with PLECS. The simulated results are shown in Figure 9. The waveform of the current and voltage at the first resonant frequency point is shown in Figure 9a. The ZVS waveform of the primary side MOSFETs can be observed, and the secondary rectifier diode operates in a critical continuous state. When the switching frequency is reduced to less than 100 kHz, the simulation waveform is shown in Figure 9b. The resonant current is not the standard sine wave. At that time, the ZVS of the transistors is realized. What is more, the zero-current switching (ZCS) of the secondary side diodes can be achieved. The simulated results show that large switching losses of MOSFETs are avoided. The efficiency of the system could be further improved. As a result, stable voltage conversion is achieved.

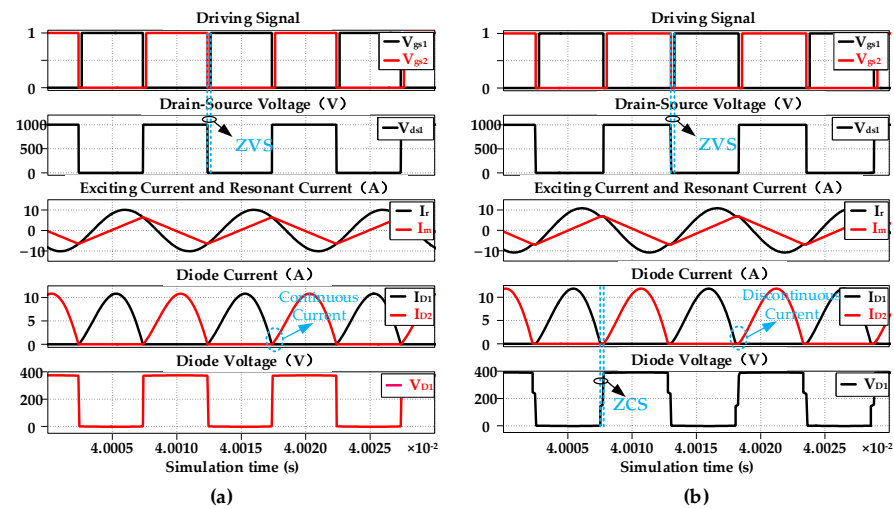


Figure 9. (a) System voltage and current waveform ($f_s = f_{r1}$); (b) system voltage and current waveform ($f_{r2} < f_s < f_{r1}$).

The high power density, high efficiency, and low switching power loss of the LLC resonant converter will be achieved by using SiC transistors to form high-frequency inverters and rectifiers. This is because of the particularity of the working environment of the converter. The high complexity of the undersea environment needs to be considered. A waterproof metal hull design and epoxy coating could effectively protect the power conversion system against seawater corrosion. Aluminum alloy material and a cylindrical structure design ensure that the hull is maintained with strong stability. The internal structure of the underwater power conversion connector system is shown in Figure 10. It adopts a modular design. The LLC resonant converter and the rectifier could be easily placed in the metal hull with good water resistance and heat dissipation performance. The power circuit heat dissipation module is connected to the metal hull. As a result, the generated heat could be delivered to the seawater. Furthermore, when designing the water tightness of the cavity and connector of the underwater connecting box, according to the elasto-plastic failure criterion, the thickness of the underwater connection box is calculated by the medium-diameter formula [36]. Therefore, the converter system can be kept in a normal operation mode in the deeper water.

To test the performance of the underwater power conversion connector system, the presented converter was placed in a water tank, as shown in Figure 11. The power conversion board is housed in a specially designed metal hull. The underwater power conversion connector consists of an LLC resonant converter and a rectifier.

The parameters of the system are shown in Table 4. The input voltage ranges from 700 V to 1000 V, and the resonant frequency is designed to be 100 kHz. The rated power level is set at 1500 W and the output voltage is set at 375 V.

Corresponding to the simulation results in Figure 8, the characteristics of the driving circuit are first tested in this paper. Figure 12 is the comparison of experimental waveforms

before and after the optimization of the drive circuit. Based on Figure 12a, it can be seen that compared with the traditional structure, the optimized driver has a smaller voltage spike and a shorter oscillation time with the same switching speed. In Figure 12b, the oscillation energy is absorbed through the buffer circuit. Therefore, the overvoltage and oscillation time of the system are significantly reduced. The switch status of the transistors is more stable.

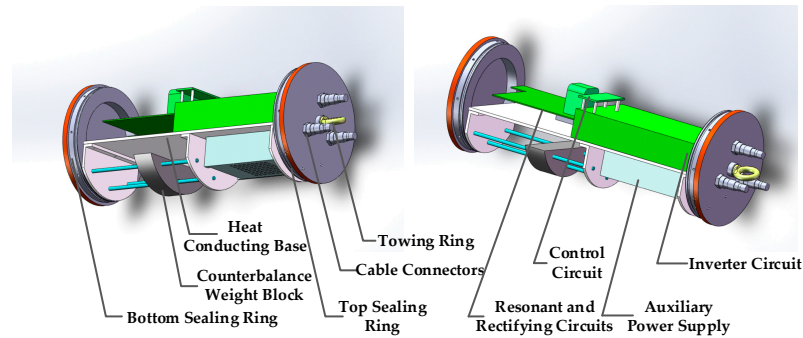


Figure 10. The structure design of the underwater power conversion connector system.

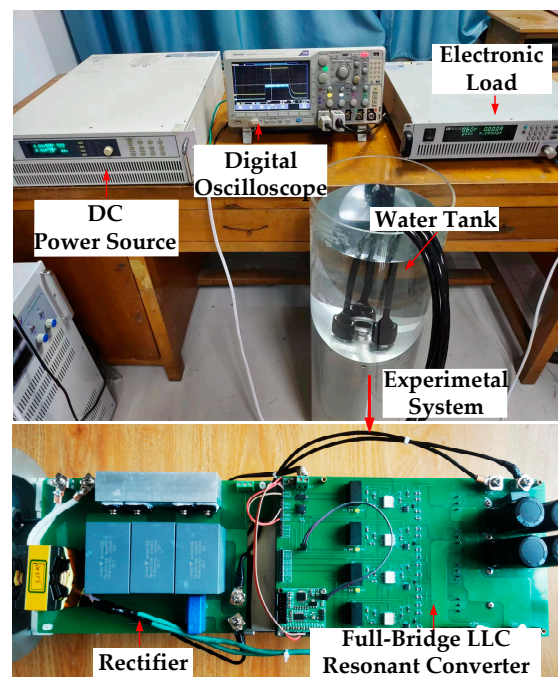


Figure 11. Experiment platform of the underwater energy conversion.

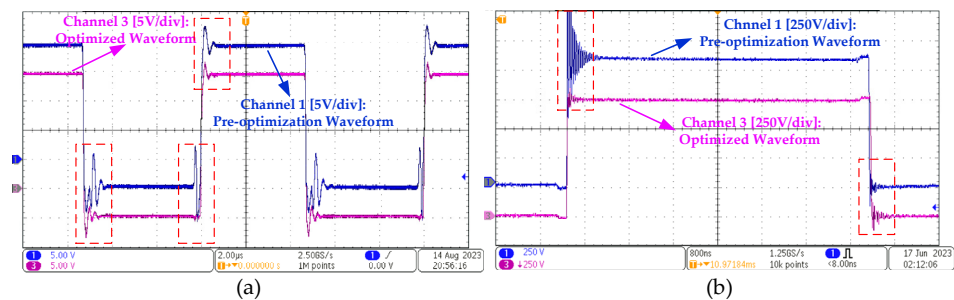


Figure 12. (a) Input voltage (V_{GS}) waveform comparison of MOSFET; (b) output voltage (V_{DS}) waveform comparison of MOSFET.

The optimized RC level conversion driving structure proposed in this paper can not only improve the stability of SiC devices in practical applications, but also ensures the adaptability of the devices in high-frequency scenarios. It is conducive to the application of silicon carbide semiconductor devices.

The experimental results of the power circuit are shown in Figures 13–15. When the resistive load changes, the output voltage and output current waveforms of the LLC resonant converter system are shown in Figure 13. The power conversion system has a fast response speed. Furthermore, with the load resistance increasing or decreasing, the load voltage can be maintained constant with low voltage ripples. This means that the undersea power conversion connector system can satisfy the requirements of different charging scenarios. External interference can be resisted.

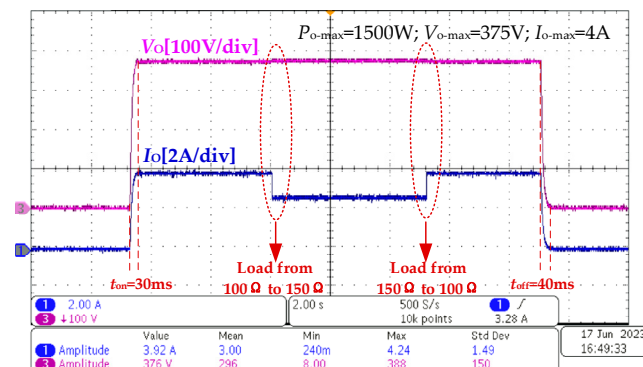


Figure 13. Dynamic response experimental waveform of the underwater power conversion connector system.

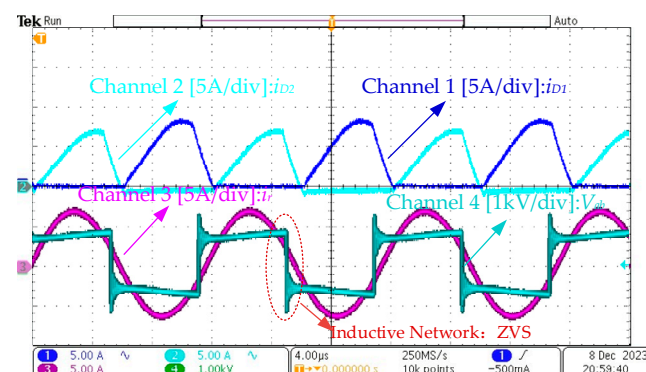


Figure 14. Experimental waveforms of the resonant network and diode current.

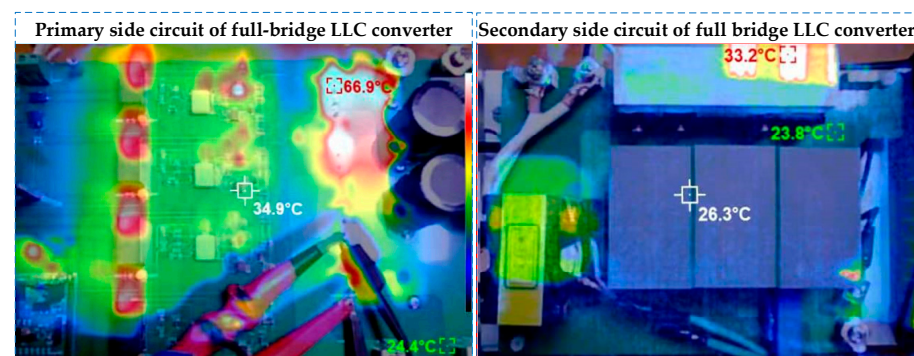


Figure 15. Thermal field analysis of the underwater power conversion connector system with a load power of 1500 W.

In addition, the diode current on the secondary side and the voltage and current of the resonant network on the primary side were also measured, and the results are shown in Figure 14. The waveforms of channel 1 and channel 2 indicate that the diode is in a critical continuous state. The resonant network waveforms of channel 3 and channel 4 indicate that the voltage is ahead of the current. Therefore, the system has enough inductive energy to achieve ZVS. The experimental results are consistent with the simulation results.

The heat losses of the system are also analyzed under the air condition. When the load power is 1500 W, the surface temperature of the element is measured. As shown in Figure 15, the maximum surface temperature of the power conversion board is about 66.4 °C. When the power conversion board is placed in water, with the excellent thermal conductivity of the connector hull, the system will provide lower heat losses and higher efficiency.

The experiment was also conducted in the water environment. Compared with the air environment, the system has better heat dissipation performance when it is placed underwater, and the system efficiency is improved slightly. At the same time, the long-term underwater work shows that the power conversion connector system designed in the paper offers an excellent performance. The high efficiency and stable voltage conversion can be realized. In addition, the efficiency of the system was measured under different input voltages and different load powers, as shown in Figure 16. With the increase of load power, the efficiency of the system is constantly improving. However, when the input voltage is reduced, the efficiency of the system is lower than expected because the transformer is not sufficiently excited. When the input is 700 V, the voltage conversion function can still be achieved. When the input voltage is 1000 V and the load power is 1500 W, the system efficiency is 98.37%. It means that low switching losses and low heat losses were achieved. The underwater power conversion connector system proposed in this paper strengthens the application of silicon carbide transistors in the field of underwater electrical energy conversion.

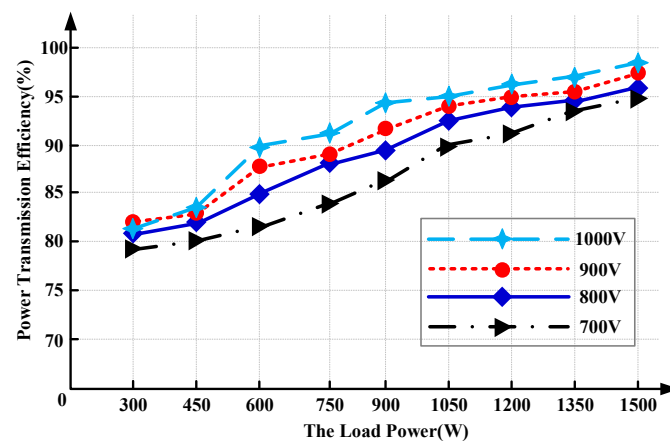


Figure 16. The efficiency of the underwater power conversion connector system under different input voltages and different load power.

Therefore, the efficiency of the circuit and the underwater performance of the system are verified. A wide input voltage range counterbalances the effect of voltage fluctuations in the HVDC cables, which is conducive to the stability and efficiency improvement of the UWPT system. The output power could be adjusted automatically with an adaptive dynamic load function. It is not necessary to set many underwater connection boxes to complete the charging of electrical equipment of different power levels. The underwater power converter presented in the paper will make the marine observation network or the undersea power station more concise and stable. In this work, a cordwood system-type structure is constructed, and the high power level could be achieved with more power units.

6. Conclusions and Discussion

To improve the stability and efficiency of the undersea wireless power transmission (UWPT) system, an underwater power conversion connector is proposed. It can realize the conversion of a high voltage shore-based power source into the hundreds of volts of direct voltage required by the UWPT system. The main conclusions are as follows:

- Combined with fundamental wave analysis and time domain analysis, the parameters designing of the power circuit of the LLC converter are optimized, and the stress of the components is reduced.
- The characteristics of the zero-voltage switching (ZVS) were analyzed, and a dead zone time design based on the critical ZVS was analyzed. The stability and efficiency of the system are guaranteed by an appropriate dead zone time.
- The passive driving structure is proposed. It is conducive to improving the high-frequency performance of transistors. Therefore, a lot of switching losses during switching process could be avoided.
- A 1.5 kW prototype is developed, and an experimental platform is built. The experimental results show that the system structure and parameter configuration method are feasible.

The presented underwater power conversion connector has a good building block design feature. The high power level requirements could be satisfied with more modules for marine environment applications. It will improve the underwater power supply research on the high power density and high voltage conversion ratio system.

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Abbreviations

L_g	Gate parasitic inductance of MOSFET.
L_d	Drain parasitic inductance of MOSFET.
L_s	Source parasitic inductance of MOSFET.
L_1	Load inductance.
R_{pl}	Bus equivalent resistance.
V_{dc}	Bus voltage.
C_{gs}	Grid-source parasitic capacitance of MOSFET.
C_{ds}	Drain-source parasitic capacitance of MOSFET.
C_{gd}	Grid-drain parasitic capacitance of MOSFET.
C_1	Complementary bridge arm parasitic capacitance.

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