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A Delay-Aware Method for Inverter Nonlinearity Compensation in Sensorless PMSM Drives

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Abstract

This paper presents a delay-aware observer-side voltage-source inverter (VSI) nonlinearity compensation chain for medium- and high-speed sensorless control of permanent magnet synchronous motors (PMSMs). The method reduces the observer-model voltage mismatch caused by inverter nonlinearities and is implemented with a continuous boundary-layer adaptive-gain sliding-mode observer (ASMO) and a second-order phase-locked loop (PLL). Two-point linear prediction estimates the phase current when the VSI nonlinear voltage error actually takes effect. A C^1 -continuous cubic zero-crossing weight limits abrupt direction changes near current zero crossings, while a synchronous correlation signal derived from the estimated back electromotive force updates the equivalent distortion-voltage amplitude online. Compensation is applied only to the reconstructed ASMO input voltage, leaving the original current loop and space-vector pulse-width modulation (SVPWM) unchanged. Comparative and ablation simulations show lower characteristic back-EMF harmonics and electrical rotor-position estimation error than conventional compensation. Hardware tests under variable-speed and load-step conditions confirm improved dynamic estimation and disturbance rejection. The intended operating region is medium to high speed, where the back-EMF has sufficient signal-to-noise ratio and a nonsalient machine model is appropriate. The fixed-point realization is reported as implementation-feasibility evidence rather than as the principal contribution.

Keywords: permanent magnet synchronous motor; sensorless control; adaptive-gain sliding-mode observer; inverter nonlinearity; digital delay; current prediction



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1. Introduction

Permanent magnet synchronous motors (PMSMs) combine high efficiency and power density with fast dynamic response, making them common in servo drives, transportation, industrial automation, and compact robotic actuators. These properties are also attractive for lower-limb rehabilitation exoskeletons, whose joint drives must remain compact and reliable while providing accurate motion control. Field-oriented control (FOC) normally obtains rotor position and speed from a mechanical sensor, but the sensor adds cost, occupies installation space, and can be vulnerable to the operating environment. Sensorless control derives the same information from electrical measurements and a machine model, reducing this dependence under suitable operating conditions [1]. High-frequency injection can

cover the low-speed region, although it introduces additional loss, noise, and computation. Back-EMF observers are less intrusive at medium and high speeds [2]. Accordingly, this work focuses on the back-EMF-observable region and assumes negligible motor saliency.

Sliding-mode observers (SMOs) use current-observation error to generate a switching injection and offer robust estimation with modest computational demand [1]. With a fixed gain, however, reachability at high speed and chattering at low speed impose competing requirements. A continuous boundary layer softens the switching action but introduces a phase lag that varies with speed and parameters. The adaptive-gain SMO (ASMO) and phase compensation reported in [3] address this compromise. Other studies have improved convergence or back-EMF quality through high-order, fixed-time, and quasi-super-twisting structures [4–9]. Finite-time observers and modified phase-locked loops (PLLs) have likewise been used to reduce ramp error and reject harmonics [10–13]. These observer developments generally rely on the voltage model receiving a faithful representation of the motor-terminal voltage.

The voltage applied by a practical voltage-source inverter (VSI) differs from its modulation reference because of dead time, switching delay, device voltage drops, and dc-link variation. Observer-based and recursive least-squares (RLS) approaches can estimate this distortion, whereas compensation based on a fixed inverter model remains sensitive to the operating point [14,15]. Current-dependent voltage distortion is dominated by 5th- and 7th-order components, which appear as 6m-order position ripple after synchronous demodulation [4,16–20]. A fixed compensation amplitude cannot follow temperature, dc-link voltage, or device-state changes. Reducing the gain near current zero crossings limits erroneous compensation but leaves the timing mismatch unresolved [21]. RLS and harmonic-state techniques provide adaptation at the cost of covariance updates, iterations, or extra observer states [15,17,19,20,22]. A recent active-flux/MRAS method jointly adapts the position observer and corrects the PWM duty ratio online [23]. Sampling, computation, observer dynamics, and pulse-width modulation (PWM) updating introduce additional digital delay [24–26]. If the phase current reverses between sampling and actuation, its sampled polarity selects the wrong compensation direction, and the magnitude of the resulting compensation-voltage error can reach twice the equivalent distortion-voltage amplitude.

The principal contribution is a delay-aware observer-side compensation chain that coordinates two-point current prediction, C^1 -continuous cubic zero-crossing weighting, and online equivalent-distortion-voltage amplitude correction without modifying the current controller or SVPWM. Its organizing issue is the timing mismatch between current sampling and the actual actuation of the VSI nonlinear voltage error. Deadband, projection, and enabling logic protect the slow update when excitation or operating conditions are unsuitable. Matched comparisons among Schemes A, B, and E assess the overall effect, while the B–E ablations separate the contributions of prediction, cubic weighting, and amplitude updating. Dynamic loading, dead-time adaptation, and execution overhead are evaluated on a laboratory-developed PMSM drive. The ASMO gain law, phase compensation, and second-order PLL follow [3]; they serve as the observer baseline and are not claimed as original contributions.

Table 1 compares the present method with Refs. [4,15,16,23–26] across the five structural features relevant to this work.

Section 2 develops the PMSM and VSI-distortion models. Section 3 presents the proposed compensation method and residual-error bound. Section 4 reports the simulation and hardware results, and Section 5 concludes the paper. The analysis is local and assumes bounded residual distortion, sufficient excitation, and time-scale separation. It does not establish global asymptotic stability under saturation, loss of lock, or full-range operation.

Table 1. Structural comparison with the closely related methods.

Method	Digital Delay	Actuation-Time Polarity	Continuous Zero Crossing	Online Amplitude	Compensation Location
Ref. [4]	No	No	No	Yes	Command side
Ref. [15]	No	No	No	Yes, RLS	Command + observer inputs
Ref. [16]	No	No	No	Yes, RTLS	Command side
Ref. [24]	No; discrete-time model	N/A	N/A	N/A	SMO/PLL
Ref. [25]	Yes	No; current-value prediction	N/A	N/A	Current-feedback/SMO path
Ref. [26]	Yes	Yes, reference-current sign	No, hard sign	No; adapts delay time	PWM timing
Ref. [23]	No	No	No	Yes, MRAS	PWM duty ratio
This work	Yes	Yes	Yes, C^1 cubic weight	Yes	Reconstructed ASMO input

N/A indicates that the feature is not applicable because the cited method does not compensate VSI nonlinearity. Ref. [24] treats low-sampling-ratio discretization rather than sampling-to-actuation delay. Ref. [25] predicts actuation-time current values for delay precompensation but does not use their polarity to select a VSI-nonlinearity compensation direction. Ref. [26] adapts compensation time rather than distortion-voltage amplitude.

2. System Model and Problem Formulation

2.1. Approximate PMSM Model and Sensorless FOC

For medium- and high-speed operation, a surface-mounted PMSM or another machine with negligible saliency can be represented by $L_d \approx L_q = L_s$. Parameter mismatch, weak residual saliency, and unmodeled losses are included in a bounded disturbance. The stator-current model in the stationary $\alpha\beta$ frame is

$$\frac{di_{\alpha\beta}}{dt} = -\frac{R_s}{L_s} \cdot i_{\alpha\beta} + \frac{1}{L_s} \cdot (u_{\alpha\beta} - e_{\alpha\beta}). \quad (1)$$

where R_s and L_s denote the stator resistance and equivalent stator inductance. The vectors $i_{\alpha\beta}$, $u_{\alpha\beta}$, and $e_{\alpha\beta}$ are the stator current, actual equivalent terminal voltage, and back-EMF. Under the sinusoidal back-EMF assumption,

$$e_{\alpha\beta} = \omega_e \psi_f \begin{bmatrix} -\sin \theta_e \\ \cos \theta_e \end{bmatrix}, \quad E = |\omega_e| \psi_f. \quad (2)$$

where θ_e , ω_e , and ψ_f are the electrical angle, electrical angular speed, and permanent-magnet flux linkage, respectively. If θ_m and ω_m denote the corresponding mechanical quantities and p is the number of pole pairs, then $\theta_e = p\theta_m$ and $\omega_e = p\omega_m$. This study uses an amplitude-invariant Clarke transformation. The sign convention of the Park transformation is written explicitly as

$$i_{\alpha\beta} = C i_{abc}, \quad C = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}, \quad (3)$$

$$i_{dq} = P(\hat{\theta}_e) i_{\alpha\beta}, \quad P(\theta) = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix}.$$

FOC sets $i_d^* = 0$, while the outer mechanical-speed loop supplies the q-axis current reference i_q^* . Both the Park and inverse Park transformations use the estimated electrical angle $\hat{\theta}_e$. Only $\hat{\theta}_e$ and $\hat{\omega}_e$ from the ASMO-PLL close the sensorless loop; the magnetic encoder is used solely as offline ground truth. Hereafter, $u_{\alpha\beta}^{\text{ref}}$ is the SVPWM reference

voltage and $u_{\alpha\beta}$ is the actual equivalent motor-terminal voltage. The ASMO input $\hat{u}_{\alpha\beta}$ is reconstructed from the reference voltage and estimated VSI distortion. The complete control structure is shown in Figure 1.

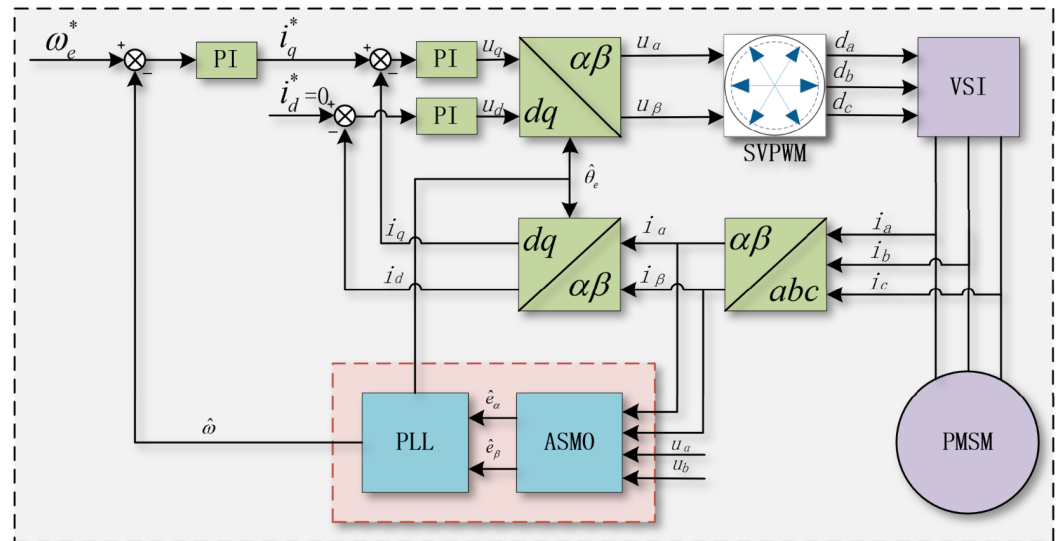


Figure 1. Structure of the sensorless PMSM FOC system.

2.2. Adaptive-Gain SMO and Second-Order PLL

The ASMO gain law, boundary-layer phase compensation, and second-order PLL used in this subsection follow [3]. They are retained as an established observer baseline and are not original contributions of this work. With $\hat{u}_{\alpha\beta}$ as its input, the continuous-boundary-layer ASMO has the current-state equation

$$\frac{d\hat{i}_{\alpha\beta}}{dt} = -\frac{R_s}{L_s} \cdot \hat{i}_{\alpha\beta} + \frac{1}{L_s} \cdot (\hat{u}_{\alpha\beta} - z_{\alpha\beta}). \quad (4)$$

For the current-observation error $e_{i,\alpha\beta} = \hat{i}_{\alpha\beta} - i_{\alpha\beta}$, equality of the observer and terminal voltages, $\hat{u}_{\alpha\beta} = u_{\alpha\beta}$, gives

$$L_s \dot{e}_{i,\alpha\beta} = -R_s e_{i,\alpha\beta} + e_{\alpha\beta} - z_{\alpha\beta}. \quad (5)$$

Following Liu et al. [3], the continuous boundary-layer function is

$$f(x) = \begin{cases} 1, & x \geq a, \\ \frac{x}{a}, & |x| < a, \\ -1, & x \leq -a. \end{cases} \quad (6)$$

where $a > 0$ is the boundary-layer half-width. The adaptive sliding-mode gain is denoted by κ to distinguish it from the discrete sampling index. Its update law, also adopted from [3], is

$$\delta = \|e_{i,\alpha\beta}\|_2 - \sigma\kappa, \quad \kappa = K_{p,\kappa}\delta + K_{i,\kappa} \int_0^t \delta(\tau) d\tau. \quad (7)$$

where σ is a positive proportional coefficient, and $K_{p,\kappa}$ and $K_{i,\kappa}$ are the PI gains for adaptation. The function $f(\cdot)$ acts elementwise on vectors. The sliding-mode injection and reconstructed back-EMF are

$$z_{\alpha\beta} = \kappa f(e_{i,\alpha\beta}), \quad \hat{e}_{\alpha\beta} \approx z_{\alpha\beta}, \quad a \geq \sigma \max(|e_\alpha|, |e_\beta|). \quad (8)$$

The final condition in Equation (8) is taken from [3] and applies under the continuous-time model and parameter assumptions used there. Within the small-error region, the boundary layer behaves as a finite-bandwidth element. The corresponding phase lag and back-EMF vector compensation are

$$\theta_{\text{lag}} = \arctan\left(\frac{L_s \omega_e}{R_s + \kappa/a}\right), \quad \hat{e}_{\alpha\beta}^c = R(\theta_{\text{lag}}) \hat{e}_{\alpha\beta}. \quad (9)$$

PLL-based extraction remains sensitive to back-EMF harmonics and speed ramps. The trade-off between harmonic rejection and dynamic tracking is discussed in recent surveys and generalized or improved QPLL studies [10–13].

The rotation matrix is $R(\theta) = [\cos \theta, -\sin \theta; \sin \theta, \cos \theta]$, with positive rotation defined consistently in the $\alpha\beta$ frame. The compensated vector $\hat{e}_{\alpha\beta}^c$ is provided to the second-order PLL, and the superscript c is omitted below. With $\hat{E} = \sqrt{\hat{e}_\alpha^2 + \hat{e}_\beta^2}$, the phase-detector error and PLL states satisfy

$$\varepsilon_\theta = \frac{-\hat{e}_\alpha \cos \hat{\theta}_e - \hat{e}_\beta \sin \hat{\theta}_e}{\hat{E} + \varepsilon_E}, \quad (10)$$

$$\hat{\omega}_e = K_{p,\theta} \varepsilon_\theta + K_{i,\theta} \int \varepsilon_\theta dt, \quad \hat{\theta}_e = \hat{\omega}_e.$$

Here, $\varepsilon_E > 0$ is an additive regularization constant with units of volts; it prevents the normalized phase-detector denominator from approaching zero when the estimated back-EMF amplitude is small. It should be selected well below the minimum back-EMF amplitude in the enabled operating region, while remaining above the effective numerical and measurement-noise floor. The implemented value is $\varepsilon_E = 0.1$ V. Every comparison scheme uses the same a , $K_{p,\kappa}$, $K_{i,\kappa}$, $K_{p,\theta}$, and $K_{i,\theta}$, so the VSI compensation branch is the only changed element. The stability result of [3] does not extend directly to a complete closed loop with discrete sampling, residual voltage error, and online amplitude updating. Section 3.3 therefore states only a residual compensation-voltage bound and its local conditions. Figure 2 summarizes the ASMO and PLL signal chain.

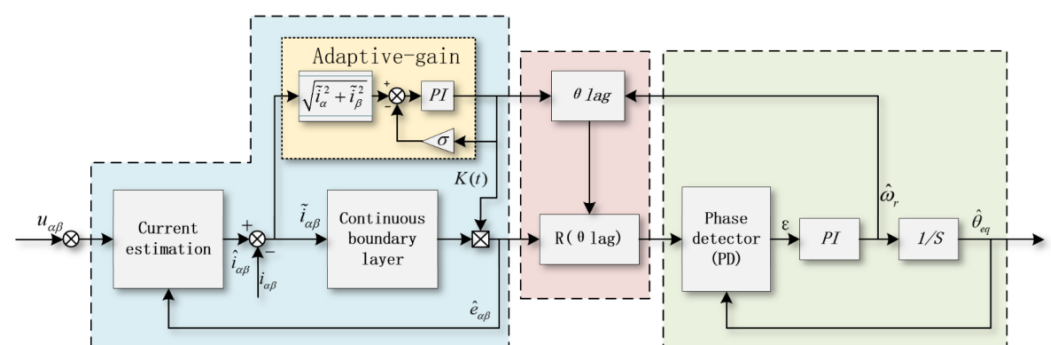


Figure 2. Structure of the continuous-boundary-layer ASMO and second-order PLL.

2.3. VSI Nonlinearity and Error Propagation

The current direction determines the voltage deviation introduced by VSI nonlinearity. The relation between the modulation reference and actual terminal voltage is

$$u_{\alpha\beta} = u_{\alpha\beta}^{\text{ref}} - \Delta u_{\alpha\beta}^{\text{inv}}. \quad (11)$$

where $\Delta u_{\alpha\beta}^{\text{inv}}$ denotes the actual equivalent VSI distortion voltage. For a two-level inverter, its dominant three-phase component is approximated by

$$\Delta u_{abc}^{\text{inv}} = V_{\text{inv}} \begin{bmatrix} \text{sgn}(i_a) \\ \text{sgn}(i_b) \\ \text{sgn}(i_c) \end{bmatrix} + r_{abc}. \quad (12)$$

where V_{inv} is the equivalent distortion-voltage amplitude, while r_{abc} collects dc-link ripple, leg mismatch, and unmodeled transients. Dead time, device delays, and voltage drops provide an initial estimate and physical bounds for this amplitude:

$$V_{\text{inv}} \approx \left(\frac{T_{\text{dead}} + T_{\text{on}} - T_{\text{off}}}{T_{\text{sw}}} \right) V_{\text{dc}} + V_{\text{drop}}(i_x, V_{\text{dc}}, T_j). \quad (13)$$

where T_{sw} is the PWM switching period, T_j is the junction temperature, and V_{drop} represents the device conduction-voltage drop. Observer-based and RLS-assisted compensation schemes have also modeled these nonidealities and their equivalent distortion voltage [14,15]. After removal of the common-mode component, the Clarke transformation gives the distortion in the $\alpha\beta$ frame:

$$\Delta u_{\alpha\beta}^{\text{inv}} = V_{\text{inv}} C \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} + r_{\alpha\beta}, \quad s_x = \text{sgn}(i_x). \quad (14)$$

The balanced three-phase polarity function is six-step periodic. For an individual phase,

$$\text{sgn}(\sin \vartheta) = \frac{4}{\pi} \sum_{\substack{h=1 \\ h \text{ odd}}}^{\infty} \frac{\sin(h\vartheta)}{h}. \quad (15)$$

Phase shifting and the Clarke transformation cancel zero-sequence triplen harmonics, leaving mainly positive- and negative-sequence components of order $6m \pm 1$. For the complex estimated back-EMF $\hat{e}_s = \hat{e}_\alpha + j\hat{e}_\beta$, where $j^2 = -1$, the dominant harmonics can be written as

$$\hat{e}_s = jE_1 e^{j\theta_e} + j \sum_{m=1}^{\infty} \left[E_{6m+1} e^{j(6m+1)\theta_e} + E_{6m-1} e^{-j(6m-1)\theta_e} \right]. \quad (16)$$

If the harmonic amplitudes remain well below the fundamental and the angular error is small, the dominant periodic position-estimation error is approximated by

$$e_\theta \approx \frac{1}{E_1} \sum_{m=1}^{\infty} A_{6m} \sin(6m\theta_e + \varphi_{6m}). \quad (17)$$

Here, $E_1 > 0$ is the fundamental estimated back-EMF amplitude, with units of volts, and $E_{6m\pm 1}$ are complex back-EMF harmonic coefficients containing the corresponding harmonic amplitudes and phases. The quantity A_{6m} denotes the equivalent back-EMF harmonic-voltage coefficient associated with the $6m$ -order electrical-position-error component and therefore has units of volts. Consequently, A_{6m}/E_1 represents the corresponding small-angle electrical-position-error amplitude, which is dimensionless and expressed in radians, whereas φ_{6m} denotes its phase. Thus, 5th- and 7th-order back-EMF harmonics can generate sixth-order position ripple [16–20]. The error e_θ is the estimated electrical angle minus its reference, wrapped into $(-\pi, \pi]$. In contrast to feedforward methods that alter inverter-leg commands, this work uses $\Delta \hat{u}_{\alpha\beta}^{\text{inv}}$ only to reconstruct the ASMO input voltage. It directly reduces observer-model voltage mismatch; any changes in phase-current

harmonics or torque ripple arise indirectly through the closed loop. Figure 3 traces this propagation path.

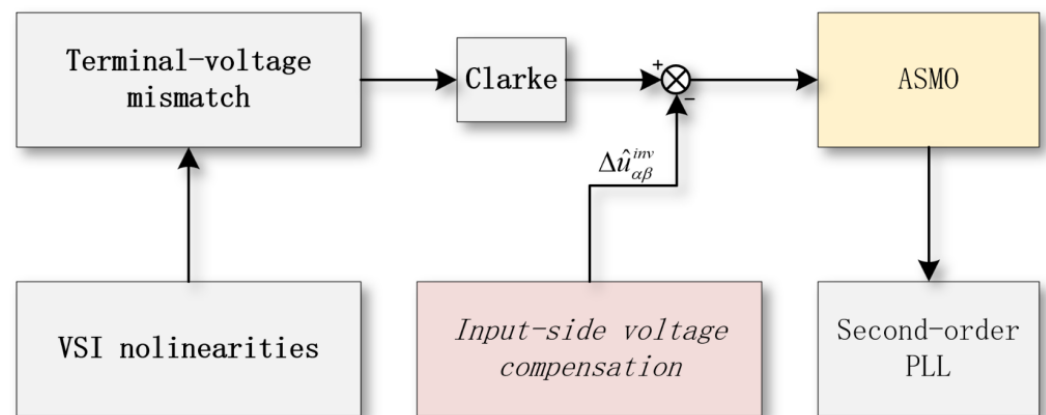


Figure 3. Propagation path from VSI-nonlinearity-induced terminal-voltage mismatch to electrical-position error.

3. Delay-Aware VSI Nonlinearity Compensation Method

3.1. Actuation-Instant Current Prediction and C1-Continuous Cubic Zero-Crossing Weight

The proposed method comprises a fast current-polarity branch and a slow amplitude branch. During each current-control cycle, the fast branch predicts the phase currents at the instant when the VSI nonlinear voltage error takes effect. It then reconstructs the three-phase distortion voltage using a C1-continuous cubic zero-crossing weight. The slow branch updates the amplitude only when the observer is locked and excitation is sufficient. The equivalent digital delay from a valid ADC sample to the effective update of the new PWM duty cycle is defined as

$$T_d = T_{\text{ADC}} + T_{\text{cal}} + T_{\text{upd}}. \quad (18)$$

where T_{ADC} , T_{cal} , and T_{upd} denote the sampling, computation, and PWM-update delays, respectively. Sensorless PMSM studies have reported both observer-delay suppression and overall system-delay compensation [24–26]. These works motivate explicit timing treatment, whereas the present method aligns the current polarity used by the observer-input VSI compensation branch through actuation-instant phase-current prediction. This delay does not mean that the observer compensation is applied directly to the inverter legs. Instead, it aligns the current polarity used for voltage reconstruction with the actual polarity at the instant when the VSI nonlinear voltage error takes effect, $t_k + T_d$. Define the actuation-instant current as $i_{x,d} = i_x(t_k + T_d)$, with $s_{x,d} = \text{sgn}(i_{x,d})$. The conventional polarity decision is $s_{x,0} = \text{sgn}[i_x(t_k)]$, yielding the following single-phase voltage error due to current-polarity misclassification:

$$\begin{aligned} \varepsilon_{u,x}^{\text{dir}} &= V_{\text{inv}}(s_{x,d} - s_{x,0}), \\ |\varepsilon_{u,x}^{\text{dir}}| &= 2V_{\text{inv}}, \quad s_{x,d} = -s_{x,0}, \quad s_{x,d}, s_{x,0} \in \{-1, 1\}. \end{aligned} \quad (19)$$

To reduce the dependence of the fast task on motor parameters, two-point linear prediction with dual saturation is used. Let $i_x[k] \equiv i_x(t_k)$; the predicted current is

$$\begin{aligned} \hat{i}_{x,p}[k] &= \text{sat}\left(i_x[k] + \text{sat}(\lambda_p(i_x[k] - i_x[k-1]); -\Delta I_{\text{max}}, \Delta I_{\text{max}}); -I_{\text{max}}, I_{\text{max}}\right), \\ \lambda_p &= \frac{T_d}{T_s}. \end{aligned} \quad (20)$$

where $x \in \{a, b, c\}$, T_s is the current-sampling period, and $\text{sat}(y; a, b) = \min\{\max(y, a), b\}$. When PWM and sampling are synchronized, $T_s = T_{\text{sw}}$. The measured delay is $T_d = 100 \mu\text{s}$, giving $\lambda_p = 1.0$. When $T_d \approx T_s$ and neither limit is active, Equation (20) reduces to $2i_x[k] - i_x[k-1]$.

The two saturation limits are selected from the normal operating-current range and the maximum admissible current variation during T_d . Let $I_{\text{op,pk}}$ be the maximum normal phase-current peak, I_{OC} the overcurrent threshold, and M_I a design margin. The absolute limit is chosen to satisfy

$$I_{\text{op,pk}} + M_I \leq I_{\text{max}} < I_{\text{OC}}. \quad (21)$$

The increment limit is selected statistically from offline current records rather than from an extreme voltage-model bound. Let Ω denote a representative calibration set that includes speed changes, load steps, and current reversals. Define

$$\begin{aligned} \Delta I_{\text{obs,max}} &= \max_{k, \Omega, \phi \in \{a, b, c\}} |i_\phi[k] - i_\phi[k-1]|, \\ \Delta I_{\text{req}} &= \eta_\Delta \Delta I_{\text{obs,max}} + M_{\Delta I}, \quad \Delta I_{\text{max}} \geq \Delta I_{\text{req}}. \end{aligned} \quad (22)$$

where $\eta_\Delta \geq 1$ is a safety-margin factor and $M_{\Delta I}$ is a current-measurement-noise margin obtained from ADC noise statistics. In the calibration data set Ω , the maximum normal instantaneous phase-current peak was $I_{\text{op,pk}} = 4.4 \text{ A}$. With $M_I = 1.0 \text{ A}$, $I_{\text{max}} = 8 \text{ A}$, and $I_{\text{OC}} = 9.77 \text{ A}$, Equation (21) is satisfied. All current limits in Equations (20)–(22) are expressed as instantaneous phase-current peak values. The offline records give $\Delta I_{\text{obs,max}} = 0.72 \text{ A}$ per sampling period; with $\eta_\Delta = 1.2$ and $M_{\Delta I} = 0.1 \text{ A}$, Equation (22) gives $\Delta I_{\text{req}} = 0.964 \text{ A}$, and the implemented increment limit is rounded upward to $\Delta I_{\text{max}} = 1 \text{ A}$. Thus, I_{max} prevents the predicted current from exceeding the admissible operating range, whereas ΔI_{max} suppresses noise spikes and abnormal extrapolation. The latter is an engineering limiter calibrated from representative records; it is not a strict theoretical upper bound on PMSM current dynamics.

To reduce abrupt polarity changes caused by prediction errors and current noise in the zero-crossing region, define $I_{\text{th}} > 0$ and use the following C1-continuous cubic zero-crossing weight:

$$\xi = \frac{i}{I_{\text{th}}}, \quad \rho(i) = \begin{cases} 1, & \xi \geq 1, \\ \frac{\xi(3 - \xi^2)}{2}, & |\xi| < 1, \\ -1, & \xi \leq -1. \end{cases} \quad (23)$$

Its first derivative is

$$\rho'(i) = \begin{cases} \frac{3}{2I_{\text{th}}} (1 - \xi^2), & |\xi| < 1, \\ 0, & |\xi| \geq 1. \end{cases} \quad (24)$$

Equations (23) and (24) show that $\rho \in C^1(\mathbb{R})$, although second-derivative continuity at the boundaries is not required. We set $I_{\text{th}} = 0.2 \text{ A}$, above the measured current-sampling offset and noise range. The fast task sequentially updates historical samples, performs two-point linear prediction, applies saturation, evaluates ρ , and reconstructs the three-phase voltage. The current sample initializes the history at the first valid acquisition. Under overcurrent, undervoltage, abnormal sampling, or PLL loss of lock, the algorithm retains the latest valid amplitude and bypasses online updating.

3.2. Online Update of the Equivalent Distortion-Voltage Amplitude

The single-phase distortion-voltage estimate generated by the fast branch is

$$\Delta \hat{u}_x^{\text{inv}}[k] = \hat{V}_{\text{inv}}[\ell] \rho(\hat{i}_{x,p}[k]), \quad x \in \{a, b, c\}. \quad (25)$$

where k and ℓ denote the fast-sampling index and slow amplitude-update index, respectively. Let $\ell = \ell(k)$ denote the slow-update interval containing fast sample k . $\hat{V}_{\text{inv}}[\ell]$ is held constant by a zero-order hold between two successive slow updates. If one update occurs every N_a fast samples, then $\ell(k) = \lfloor k/N_a \rfloor$. For conciseness, the discrete indices are omitted in Equations (26), (31) and (33). A fixed $\hat{V}_{\text{inv}}$ cannot accommodate changes in temperature, dc-link voltage, and device voltage drops. Online RLS and parameter-identification mechanisms can track operating-point variations but require additional recursive states [15,22]. The low-bandwidth correlation update developed here instead uses two scalar filtered statistics and a projected deadband update. For a PMSM with negligible saliency and nearly sinusoidal back-EMF, the d-axis component is nearly zero. This approximation holds when the d-axis aligns with the rotor flux and the angular error is small. To avoid confusion with update deadband operator D , φ_d denotes the d-axis projection of the compensation direction:

$$\begin{aligned} \hat{e}_d &= \hat{e}_\alpha \cos \hat{\theta}_e + \hat{e}_\beta \sin \hat{\theta}_e, \\ \varphi_d &= \begin{bmatrix} \cos \hat{\theta}_e & \sin \hat{\theta}_e \end{bmatrix} C \begin{bmatrix} \rho(\hat{i}_{a,p}) \\ \rho(\hat{i}_{b,p}) \\ \rho(\hat{i}_{c,p}) \end{bmatrix}. \end{aligned} \quad (26)$$

Within a local region where $i_d \approx 0$, the PLL is locked, and the angular error is small, $\hat{e}_d \approx (V_{\text{inv}} - \hat{V}_{\text{inv}}) \varphi_d + v_d$. Here, v_d collects parameter mismatch, measurement noise, flux harmonics, the projection of unmodeled distortion r_{abc} , and zero-crossing smoothing bias from $\text{sgn}(i_{x,d}) - \rho(i_{x,d})$. It also includes the residual actuation-instant current-prediction error. The slow task samples only at fast indices k_ℓ , so $\hat{e}_d[\ell] \equiv \hat{e}_d[k_\ell]$ and $\varphi_d[\ell] \equiv \varphi_d[k_\ell]$. It then applies first-order low-pass updates to the correlation and excitation variables:

$$\begin{aligned} \bar{g}[\ell] &= (1 - \lambda_a) \bar{g}[\ell - 1] + \lambda_a \hat{e}_d[\ell] \varphi_d[\ell], \\ \bar{q}[\ell] &= (1 - \lambda_a) \bar{q}[\ell - 1] + \lambda_a \varphi_d^2[\ell]. \end{aligned} \quad (27)$$

where $0 < \lambda_a < 1$.

The online amplitude-update task is executed at 100 Hz, once every 100 current-control cycles, so its update period is 10 ms. In contrast, 1 Hz is the cutoff frequency of the low-pass filter applied to the correlation variables. For the 10 ms update period, the corresponding discrete coefficient is $\lambda_a = 1 - \exp(-2\pi \times 1 \times 0.01) = 0.0609$. Thus, 100 Hz denotes the task execution frequency, whereas 1 Hz denotes the filter bandwidth.

The normalized correlation residual is defined as

$$\varepsilon_V[\ell] = \frac{\bar{g}[\ell]}{\bar{q}[\ell] + \varepsilon_q}. \quad (28)$$

Here $\varepsilon_q > 0$ prevents division by zero under insufficient excitation. A symmetric update deadband is introduced to suppress noise-induced back-and-forth updates:

$$D(\varepsilon; \varepsilon_n) = \begin{cases} 0, & |\varepsilon| \leq \varepsilon_n, \\ \varepsilon - \varepsilon_n \text{sgn}(\varepsilon), & |\varepsilon| > \varepsilon_n. \end{cases} \quad (29)$$

The amplitude update law is written explicitly as

$$\hat{V}_{\text{inv}}[\ell + 1] = \begin{cases} \Pi_{[V_{\min}, V_{\max}]} \{ \hat{V}_{\text{inv}}[\ell] + \gamma_V D(\varepsilon_V[\ell]; \varepsilon_n) \}, & \chi[\ell] = 1, \\ \hat{V}_{\text{inv}}[\ell], & \chi[\ell] = 0. \end{cases} \quad (30)$$

$\Pi_{[V_{\min}, V_{\max}]}$ denotes the projection operator, and $\chi \in \{0, 1\}$ is the online amplitude-update enabling variable. The implemented update uses $\varepsilon_q = 0.005$, $\varepsilon_n = 0.02$ V, $\gamma_V = 0.125$, $V_{\min} = 0$ V, and $V_{\max} = 3$ V. Let $h[\ell] = 1$ when the back-EMF amplitude exceeds 3 V, $\bar{q} > q_{\min} = 0.05$, the PLL is locked, the current and dc-link samples are valid, and neither the PI controller nor SVPWM has been saturated for two consecutive slow updates. Otherwise, $h[\ell] = 0$.

The enabling logic uses the two states INIT/HOLD ($\chi = 0$) and TRACK ($\chi = 1$). At startup, INIT/HOLD is retained for $N_{\text{init}} = 10$ slow updates (0.10 s). A reversal trigger is generated from the sign change of the q -axis current reference:

$$r_{\text{rev}}[\ell] = \begin{cases} 1, & i_q^*[\ell] i_q^*[\ell - 1] < 0, \\ 0, & \text{otherwise.} \end{cases}$$

If $r_{\text{rev}} = 1$ or $h = 0$, the state enters HOLD immediately. A reversal HOLD lasts at least $N_H = 16$ slow updates (0.16 s). TRACK resumes only when this interval has elapsed and $h = 1$, $|i_q| \geq I_{q,\text{rel}} = 0.30$ A, and $\text{sgn}(i_q) = \text{sgn}(i_q^*)$ for $N_{\text{rel}} = 2$ consecutive slow updates. The separation between $I_{\text{th}} = 0.20$ A and $I_{q,\text{rel}} = 0.30$ A provides 0.10-A release hysteresis. Equation (30) leaves the stored amplitude register unchanged whenever $\chi = 0$. Any nonzero displayed difference is limited to readout or plotting quantization. Parameters λ_a and γ_V keep the amplitude-update bandwidth substantially below the current-loop, ASMO, and PLL bandwidths. Thus, $\hat{V}_{\text{inv}}$ follows only slow device-state variations and does not track harmonics within each PWM cycle.

3.3. Compensation Integration and Supporting Analyses

The zero-sequence component is first removed from the three-phase distortion estimate, which is then transformed into the $\alpha\beta$ coordinates:

$$\begin{aligned} \Delta \hat{u}_{abc}^{\text{inv}} &= \hat{V}_{\text{inv}} \begin{bmatrix} \rho(\hat{i}_{a,p}) \\ \rho(\hat{i}_{b,p}) \\ \rho(\hat{i}_{c,p}) \end{bmatrix}, \\ \Delta \hat{u}_{\alpha\beta}^{\text{inv}} &= C \left(\Delta \hat{u}_{abc}^{\text{inv}} - \Delta \hat{u}_0^{\text{inv}} \mathbf{1}_3 \right). \end{aligned} \quad (31)$$

where $\Delta \hat{u}_0^{\text{inv}} = (\Delta \hat{u}_a^{\text{inv}} + \Delta \hat{u}_b^{\text{inv}} + \Delta \hat{u}_c^{\text{inv}})/3$ and $\mathbf{1}_3 = [1, 1, 1]^T$. The reconstructed ASMO input voltage and the general current-error equation are

$$\begin{aligned} \hat{u}_{\alpha\beta} &= u_{\alpha\beta}^{\text{ref}} - \Delta \hat{u}_{\alpha\beta}^{\text{inv}}, \\ L_s \dot{e}_{i,\alpha\beta} &= -R_s e_{i,\alpha\beta} + e_{\alpha\beta} + \Delta \hat{u}_{\alpha\beta}^{\text{inv}} - z_{\alpha\beta}. \end{aligned} \quad (32)$$

where $\Delta \hat{u}_{\alpha\beta}^{\text{inv}} = \Delta u_{\alpha\beta}^{\text{inv}} - \Delta \hat{u}_{\alpha\beta}^{\text{inv}} = \hat{u}_{\alpha\beta} - u_{\alpha\beta}$.

The following propositions are supporting analyses for the engineering compensation method. They characterize a residual-voltage-error bound and a local contraction condition, respectively, and are not a general closed-loop stability theorem.

Proposition 1 (supporting residual voltage-error bound). Let $i_{x,d} = i_x(t_k + T_d)$, $e_{p,x} = \hat{i}_{x,p}[k] - i_{x,d}$, and $\tilde{V}_{\text{inv}} = V_{\text{inv}} - \hat{V}_{\text{inv}}$. If $|r_x| \leq r_{\max}$ and $0 \leq V_{\text{inv}}, \hat{V}_{\text{inv}} \leq V_{\max}$, the single-phase residual satisfies

$$|\Delta u_x^{\text{inv}} - \Delta \hat{u}_x^{\text{inv}}| \leq r_{\max} + V_{\max} b_{p,x} + |\tilde{V}_{\text{inv}}| + \frac{3V_{\max}}{2I_{\text{th}}} |e_{p,x}|. \quad (33)$$

where $b_{p,x} = |\text{sgn}(i_{x,d}) - \rho(i_{x,d})|$.

Proof. Add and subtract $\hat{V}_{\text{inv}}\rho(i_{x,d})$, apply the triangle inequality, and use $|\rho| \leq 1$ together with $|\rho(\hat{i}_{x,p}) - \rho(i_{x,d})| \leq 3|e_{p,x}|/(2I_{\text{th}})$. $\square$

Proposition 2 (supporting local amplitude-error contraction). Assume that the true amplitude is approximately constant between two slow updates, the enabling variable equals 1, and the projection and update deadband are inactive. Under the local linearization that neglects the correlated disturbance term, Equations (27)–(30) give

$$\tilde{V}_{\text{inv}}[\ell + 1] \approx \left(1 - \gamma_V \frac{\bar{q}[\ell]}{\bar{q}[\ell] + \varepsilon_q}\right) \tilde{V}_{\text{inv}}[\ell]. \quad (34)$$

The amplitude error contracts successively in this local scalar model if

$$0 < \gamma_V \frac{\bar{q}[\ell]}{\bar{q}[\ell] + \varepsilon_q} < 2. \quad (35)$$

Proof. The multiplier in Equation (34) has magnitude below one exactly when Equation (35) holds. $\square$

Proposition 1 separates the effects of unmodeled voltage, zero-crossing bias, amplitude-estimation error, and prediction error. Proposition 2 further assumes sufficient excitation, bounded residual input, and time-scale separation between the amplitude update and observer dynamics. It is a local contraction result, not a global stability proof for the complete discrete-time drive.

3.4. Real-Time Implementation

The fixed-point realization on the LCM32F039 is reported only as implementation-feasibility evidence. The fast compensation branch executes synchronously with the 10 kHz current loop, while the amplitude update is evaluated at 100 Hz. $\hat{V}_{\text{inv}}$ is held constant between successive slow-task updates. The resulting real-time implementation is shown in Figure 4.

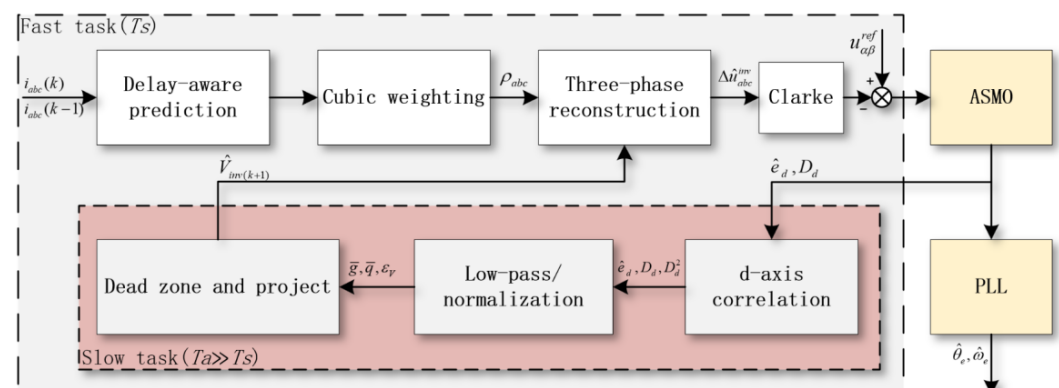


Figure 4. Structure of the proposed delay-aware VSI nonlinearity compensation method.

4. Simulation and Experimental Results

4.1. Simulation Setup, Experimental Platform, and Evaluation Metrics

MATLAB R2025a simulations used a 0.1 ms controller sampling period and the same data-recording interval. An averaged nonlinear VSI model represented dead time through an equivalent voltage error, and a discrete block imposed the digital delay. PMSM parameters, current-loop, ASMO and PLL settings, sampling frequency, and data processing were identical across all schemes. Only the VSI nonlinearity-compensation branch changed between comparisons.

Five progressive schemes were evaluated. Scheme A had no VSI nonlinearity compensation. Scheme B combined currently sampled phase currents, a linear zero-crossing weight, and a fixed equivalent distortion-voltage amplitude. Scheme C changed only the current input of Scheme B to the predicted phase currents. Scheme D retained the fixed amplitude but replaced the linear weight with the C1-continuous cubic weight. Adding online amplitude updating to Scheme D produced the complete Scheme E. The fixed-amplitude setting was identical in Schemes B–D.

Steady-state tests compared Scheme A, conventional Scheme B, and complete Scheme E. Delay sensitivity and module ablation were examined with Schemes B–E. The B-to-C, C-to-D, and D-to-E comparisons isolated prediction, cubic weighting, and online amplitude updating, respectively. The 600 → 1500 → 600 r/min command used linear ramps. Acceleration was 1000 r/min/s with 1 s plateaus, while deceleration was 650 r/min/s with 1.5 s plateaus.

Hardware tests used the in-house PMSM drive platform in Figure 5. It comprised a dc supply, a two-level VSI, an LCM32F039 control board, a 200 W PMSM, a magnetic encoder, and a 1 N · m magnetic powder brake. The brake provided adjustable load torque. The encoder recorded rotor position and speed for offline error evaluation only and was excluded from the sensorless loop. Table 2 lists the principal platform and control parameters.

The permanent-magnet flux linkage in Table 2 was remeasured as $\psi_f = 0.0166$ Wb. Using Equation (2), the corresponding back-EMF amplitudes are 5.22 V at 600 r/min and 13.04 V at 1500 r/min. For the 24 V dc link, the linear-SVPWM phase-voltage limit is $V_{dc}/\sqrt{3} = 13.86$ V; hence, the 1500-r/min point has a back-EMF-only voltage headroom of approximately 0.82 V, corresponding to an ideal modulation ratio of 0.941 before stator and inverter voltage drops are included. All reported hardware tests are confined to the 600–1500 r/min mechanical-speed range, and no operation above 1500 r/min is claimed.

The comparison with Ref. [16] is a module-level controlled benchmark. Its RTLS-based equivalent-distortion-amplitude estimator was transplanted into the common ASMO–PLL platform, while the motor, current and speed controllers, sampling and PWM settings, dead time, effective delay, operating condition, and evaluation windows were kept identical to those of Schemes B and E. Only the VSI nonlinearity-compensation branch was replaced; this benchmark is not presented as a complete reproduction of the sensorless architecture in Ref. [16].

The RTLS forgetting factor was set to $\lambda = 0.998$, with $\mathbf{P}_r = \text{diag}(1, 1000)$, $k_{p,\text{RTLS}} = 1$, $k_{i,\text{RTLS}} = 20$, and an LPF angular cutoff frequency of $\omega_{\text{LPF}} = 461.8$ rad/s. The initial equivalent distortion-voltage amplitude was set to $\hat{V}_{\text{inv}}(0) = 0.60$ V. The RTLS-based benchmark was executed at the same 10 kHz PWM/current-loop frequency used by the other two schemes.

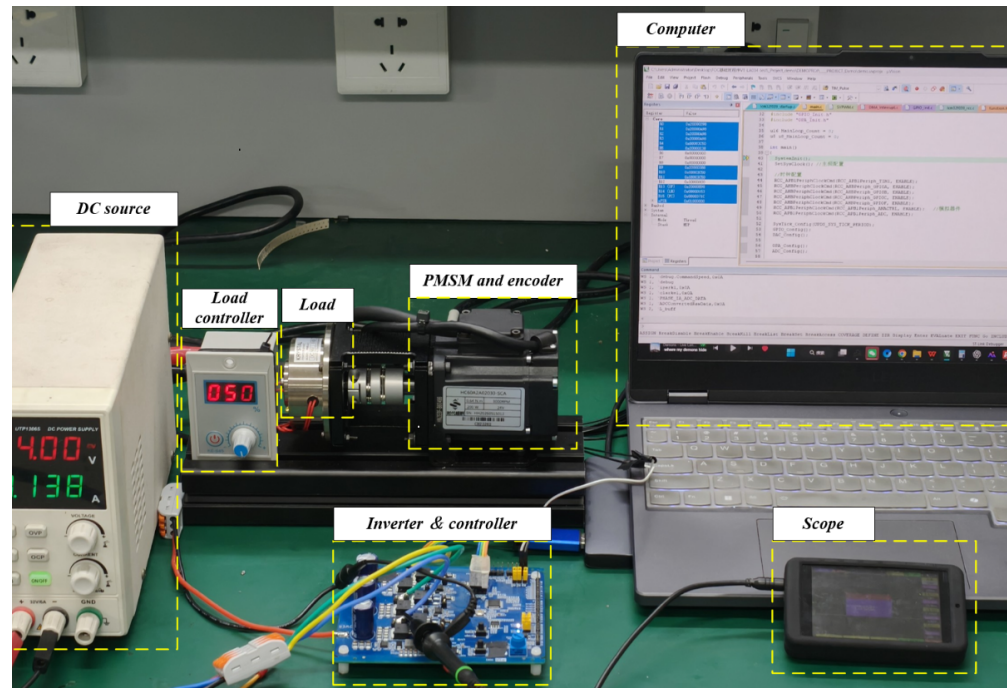


Figure 5. Experimental platform for PMSM sensorless control.

The encoder mechanical angle $\theta_{m,enc}$ was converted to the electrical angle as $\theta_{e,enc}[k] = \text{wrap}_{(-\pi,\pi]}(p\theta_{m,enc}[k])$, where p is the number of pole pairs. The estimated and encoder sequences used a common sampling trigger. The encoder sequence was corrected for a fixed one-sample delay. The mechanical-speed estimation error was defined as $e_n[k] = \hat{n}_m[k] - n_{m,enc}[k]$, and the electrical-position estimation error was $e_\theta[k] = \text{wrap}_{(-\pi,\pi]}(\hat{\theta}_e[k] - \theta_{e,enc}[k])$. The steady-state electrical-position estimation error was characterized by its peak-to-peak value. All position-error angles are reported in electrical degrees, whereas all speeds in r/min are mechanical speeds. Total harmonic distortion (THD) was defined as $\text{THD}_{2:20}(x) = \sqrt{\sum_{h=2}^{20} X_h^2} / X_1 \times 100\%$, where X_h is the h th-harmonic amplitude of signal x . Unless otherwise stated, fast Fourier transform (FFT) analysis was applied to the estimated back-EMF $\hat{e}_\alpha$. A continuous window of 10 electrical periods after steady state was selected. A 1200-point Hann window was used, followed by zero-padding to a 4096-point FFT. The 5th and 7th harmonics were normalized to the fundamental amplitude. The peak value of the sixth-order electrical-position-error component was reported in electrical degrees. Dynamic operating conditions reported the maximum absolute mechanical-speed estimation error and maximum dynamic electrical-position estimation error. Load-step tests reported the maximum mechanical-speed drop, maximum absolute mechanical-speed estimation error, and recovery time. Recovery time was defined as the time required for the response to re-enter $\pm 2\%$ of the reference and remain there continuously for 50 ms. Three load-step records were evaluated for each method. Individual observations and the mean $\pm$ standard deviation (SD) were reported. For visualization, the encoder-speed trajectories were processed using a 45-ms moving-average window, whereas the error trajectories used a 30-ms moving-average window. The summary metrics were calculated separately for each record before aggregation.

Table 2. Main parameters of the PMSM drive experimental platform and control system.

Item	Symbol or Configuration	Value
Motor under test	Type/rated power	PMSM/200 W
Rated electrical parameters	Voltage/current	24 V/8 A
Tested mechanical-speed range	n_m	600–1500 r/min
Number of pole pairs	p	5
Stator resistance	R_s	0.128 Ω
d - and q -axis inductances	L_d / L_q	0.153 mH
Permanent-magnet flux linkage	ψ_f	0.0166 Wb
Loading device	Type/torque capacity	Magnetic powder brake/1 N · m
dc link	V_{dc}	24 V
Controller	MCU/clock frequency	LCM32F039/96 MHz
Sampling period	T_s	100 μ s
Current-control period	—	100 μ s
PWM switching frequency	f_{PWM}	10 kHz
Dead time	T_{dead}	1 μ s (baseline; 1–3 μ s evaluated)
Effective sampling-to-actuation delay	T_d	100 μ s
Current sensing	ADC resolution	12 bit
Position ground truth	Magnetic encoder resolution	13 bit
Numerical implementation	Q format	Q14
Zero-crossing threshold	I_{th}	0.2 A
Correlation-filter coefficient	λ_a	0.0609
Minimum excitation threshold	q_{min}	0.05
Back-EMF update-enable threshold	—	3 V

4.2. Simulation Verification

Schemes A, B, and E were compared at 1000 r/min mechanical speed, 1 μ s dead time, and 10 kHz sampling. Figure 6 presents the three schemes from left to right. With the common FFT window and THD_{2:20} definition, their THD values were 24.29%, 13.60%, and 6.21%, respectively. Relative to conventional Scheme B, complete Scheme E reduced the 5th- and 7th-harmonic amplitudes by 39.72% and 29.27%. The electrical-position-error peak-to-peak value fell from 7.82° to 4.73°, and its sixth-order component decreased by 49.73%. Table 3 collects these metrics. The A–B–E comparison measures the overall change from no compensation to the complete method; the following B–E ablation separates the individual modules. The observed harmonic changes agree with Equations (15)–(17), which link $6m \pm 1$ voltage harmonics to $6m$ -order electrical-position error.

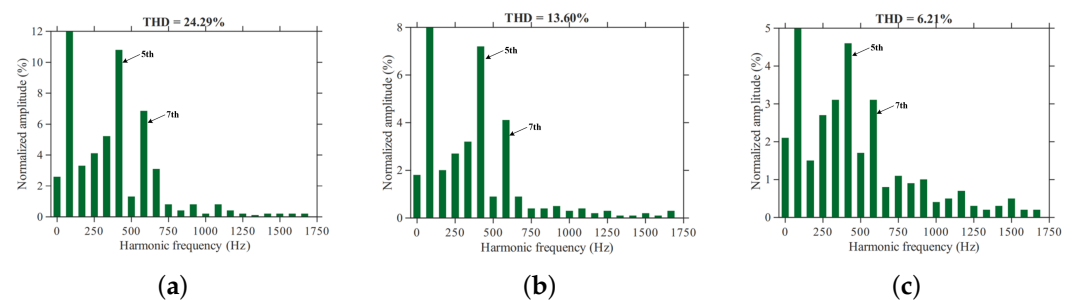


Figure 6. Results of the steady-state comparative evaluation for Schemes A, B, and E: (a) Scheme A without VSI nonlinearity compensation; (b) Scheme B with conventional compensation; and (c) Scheme E with the complete proposed compensation method.

Table 3. Metrics from the steady-state comparative evaluation of Schemes A, B, and E.

Metric	Scheme A	Scheme B	Scheme E	Improvement of Scheme E over Scheme B
H_5/H_1 (%)	10.38	6.32	3.81	39.72%
H_7/H_1 (%)	7.24	4.10	2.90	29.27%
THD _{2:20} ($\hat{e}_\alpha$) (%)	24.29	13.60	6.21	54.33%
RMS of the electrical-position estimation error (°)	3.61	2.14	1.10	48.60%
Peak-to-peak electrical-position estimation error (°)	10.86	7.82	4.73	39.51%
Amplitude of the sixth-order electrical-position-error component (°)	4.630	2.777	1.396	49.73%

Delay-sensitivity and ablation simulations used equivalent digital delays of 0, 1.0, and 1.5 sampling periods. Schemes B and C differed only in the current instant used for compensation direction. The C-to-D change was the zero-crossing weight, and the D-to-E change was online amplitude updating. Schemes B–D shared one fixed amplitude; every other control parameter and data window remained unchanged. Figure 7 includes the error trajectories needed for these comparisons without repeating four complete waveform sets.

At one sampling period of equivalent delay, Scheme B had a 16.22% current-polarity misclassification rate. Actuation-instant prediction lowered this rate to 6.10% in Scheme C. Replacing the linear weight with the C1-continuous cubic weight then reduced the maximum compensation-voltage deviation from 0.339 V to 0.254 V. From Scheme C to D, the electrical-position-error peak-to-peak value and sixth-order component decreased by 13.40% and 16.80%, respectively. Online updating in Scheme E reduced the steady-state amplitude error from 0.116 V to 0.015 V relative to Scheme D. The same comparison reduced the electrical-position-error peak-to-peak value from 4.21° to 3.44°, isolating the amplitude-update contribution. With a delay mismatch of 1.5 sampling periods, Scheme E's dual saturation kept the maximum compensation deviation within 1.941 V. Table 4 summarizes the single-variable comparisons.

Table 4. Delay-sensitivity and module-ablation simulation results for Schemes B–E.

Comparison	Single Modification	Evaluation Metric	Result
B → C	Currently sampled current → predicted current	Current-polarity misclassification rate	16.22% → 6.10%
C → D	Linear zero-crossing weight → C1-continuous cubic zero-crossing weight	Maximum compensation-voltage deviation	0.339 V → 0.254 V
C → D	Linear zero-crossing weight → C1-continuous cubic zero-crossing weight	Peak-to-peak electrical-position error/sixth-order component	Reduced by 13.4%/16.8%
D → E	Fixed equivalent distortion-voltage amplitude → online amplitude update	Equivalent distortion-voltage amplitude error/peak-to-peak electrical-position error	0.116 V → 0.015 V; 4.21° → 3.44°
E, 1.5 T_s	Delay mismatch and dual saturation	Maximum compensation-voltage deviation	≤1.941 V

The sampled phase-*a* current was modeled as $i_{a,m}[k] = i_{a,d}[k] + b_a + n_a[k]$, where $n_a[k] \sim \mathcal{N}(0, \sigma_i^2)$. The direction-proxy RMS error was defined as

$$E_p = \sqrt{\frac{1}{N} \sum_{k=1}^N [\rho(\hat{i}_{a,p}[k]; I_{th}) - \text{sgn}(i_{a,d}[k])]^2}.$$

The injected noise used $\sigma_i = 0.03$ A, and the noise-plus-offset case used $|b_a| = 0.08$ A. At 10 kHz, each threshold used the same 50 realizations generated with the fixed MATLAB R2025a setting `rng(1202,'twister')`. To support the selection of $I_{th} = 0.2$ A, Figure 7b sweeps the threshold from 0.05 to 0.35 A under no-disturbance, noise-only, and noise-plus-offset conditions, with the direction-proxy RMS error reported as the mean $\pm$ standard deviation over 50 runs. A small threshold is favorable without disturbance but is more sensitive to noise and offset, whereas an excessively large threshold widens the smoothed zero-crossing region and increases the error. The noise-offset map in Figure 7c confirms the same trade-off over the tested offset range. The selected value of 0.2 A lies near the low-error region under the disturbed conditions without excessively widening the zero-crossing interval.

The temperature-parameterized simulation in Figure 8 externally schedules temperature from 25 to 125 °C and prescribes an increase in the equivalent VSI distortion-voltage amplitude from 0.60 to 0.75 V to emulate slow device-conduction-drop drift. Scheme D retains a fixed compensation amplitude of approximately 0.59 V, whereas the online estimate in Scheme E follows the imposed amplitude change. Consequently, the reported THD_{2:20} rises from approximately 6.1% to 11.8% for Scheme D but remains between approximately 6.0% and 6.4% for Scheme E. The electrical-position-error peak-to-peak value similarly increases from approximately 4.1° to 7.9° with fixed compensation, while remaining near 4.0–4.3° with the online update. This test evaluates adaptation under a prescribed temperature-dependent drift scenario; it is not an exact electrothermal model of a specific switching device.

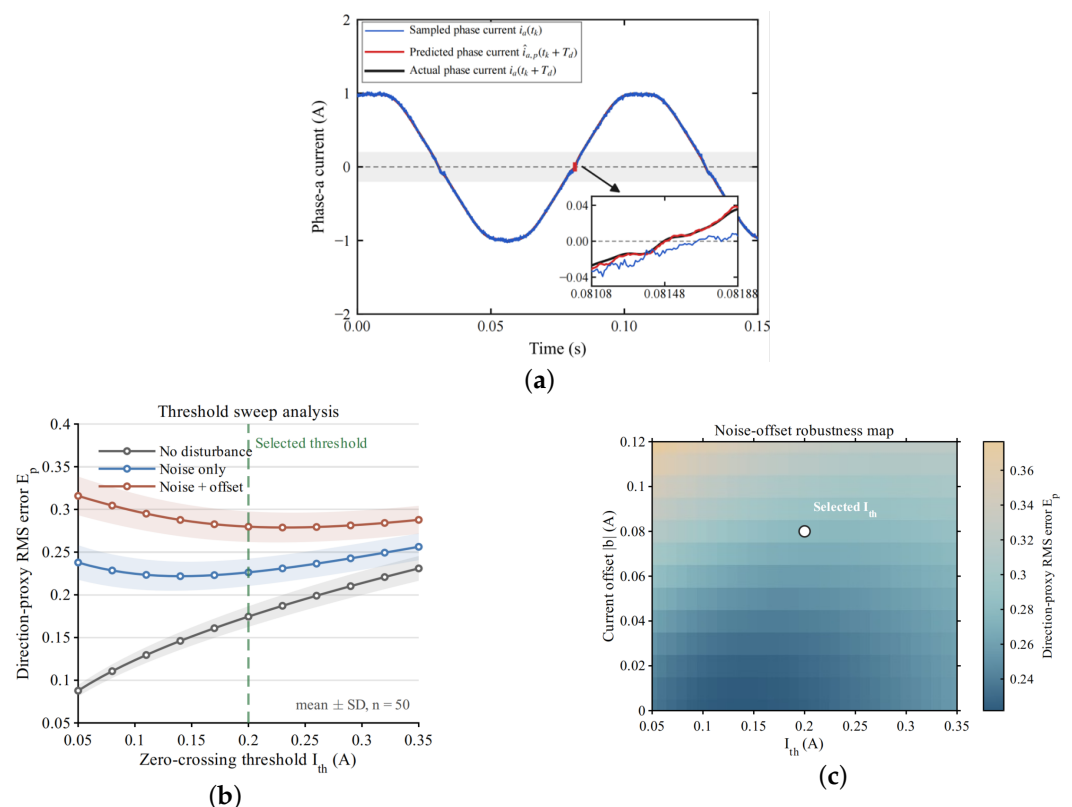


Figure 7. (a) Existing delay-sensitivity and module-ablation simulation; (b) threshold selection analysis of I_{th} ; and (c) robustness analysis with sampling noise and offset.

The factorial ablation in Figure 9 uses four matched groups: Baseline, Prediction only, Cubic only, and Prediction+Cubic. Prediction alone reduces the maximum compensation-voltage deviation from 0.539 to 0.339 V, whereas cubic weighting alone reduces it to 0.453 V. Their combination gives the lowest deviation of 0.254 V. The corresponding electrical-position-error peak-to-peak values are 6.52° , 4.86° , 5.56° , and 4.21° , and the sixth-order components are 1.84° , 1.31° , 1.57° , and 1.09° , respectively. Thus, prediction provides the larger individual reduction under this condition, while cubic weighting gives an additional reduction when combined with prediction. Figure 9 is a separate 2×2 factorial-ablation data set; its Baseline is matched only to the other three groups within that factorial comparison. It is not the Scheme-B record used in the independent A/B/E steady-state comparison of Figure 6 and Table 3. The two data sets and their peak-to-peak values are therefore reported separately and are not cross-combined.

Figure 10 evaluates delay-frequency robustness at switching frequencies of 5, 10, and 20 kHz and delay ratios $T_d/T_s = 0.5, 1$, and 1.5 . Although the polarity-decision, compensation-voltage, and electrical-position errors increase as T_d/T_s increases, Scheme E remains below Scheme B at every tested frequency and delay ratio. The improvement ratio is defined as $\eta = (B - E)/B \times 100\%$ for each metric, and Figure 10d reports their equal-weight mean. The resulting mean improvement remains positive over all nine operating combinations and is approximately 30–55%, supporting robustness to the tested switching-frequency and effective-delay variations.

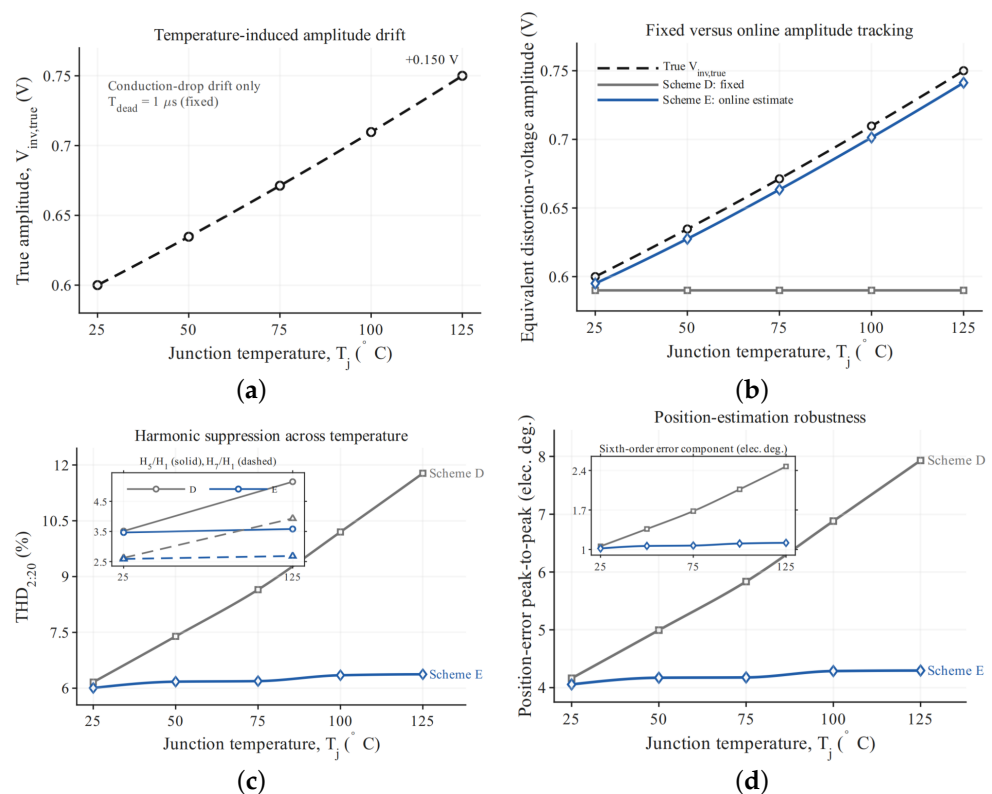


Figure 8. Temperature-parameterized simulation under a prescribed drift of the equivalent VSI distortion voltage: (a) externally scheduled temperature and prescribed amplitude drift; (b) fixed versus online amplitude tracking; (c) harmonic suppression across temperature; and (d) position-estimation robustness.

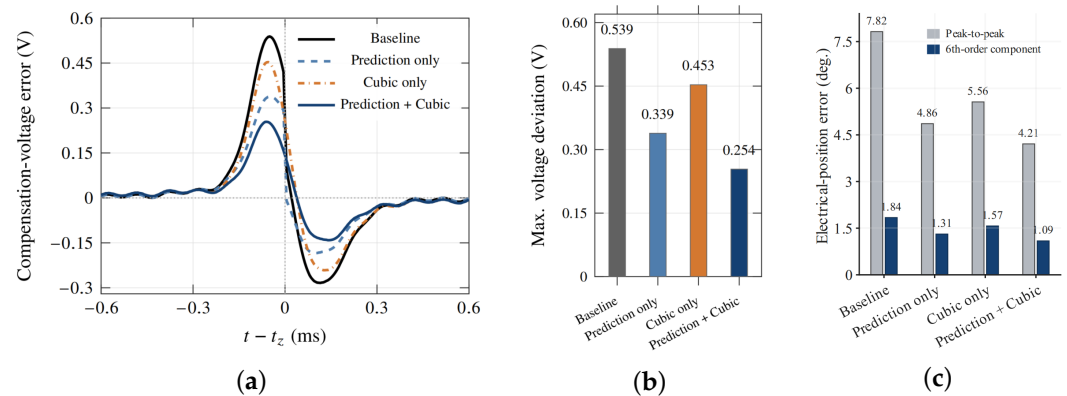


Figure 9. Factorial ablation results of prediction and cubic weighting modules: (a) compensation-voltage error comparison; (b) maximum compensation-voltage deviation; and (c) electrical-position error comparison.

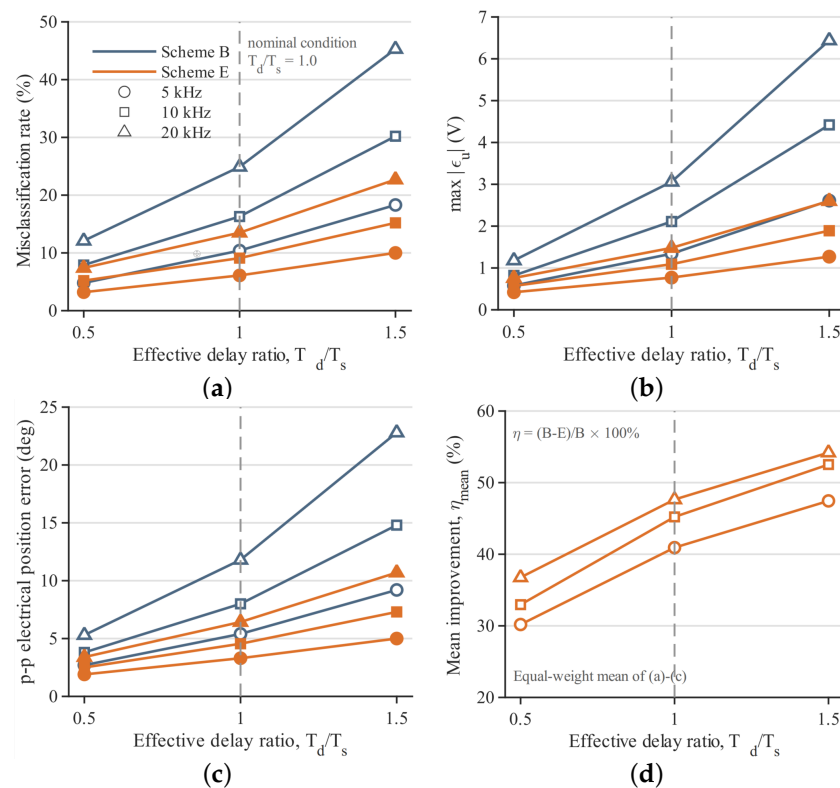


Figure 10. Delay robustness under different switching frequencies and effective delay ratios: (a) polarity decision error; (b) compensation-voltage error; (c) position estimation error; and (d) improvement ratio of Scheme E.

4.3. Experimental Validation

The variable-speed test followed a $600 \rightarrow 1500 \rightarrow 600$ r/min mechanical-speed command. With identical acceleration and deceleration slopes, the maximum absolute mechanical-speed estimation errors were 62.40 r/min for Scheme B and 34.1 r/min for Scheme E. Their corresponding maximum dynamic electrical-position errors were 14.86° and 5.13° . After each speed-plateau transition, Scheme E returned to within $\pm 2\%$ of the reference within 194 ms and remained there for 50 ms. Figures 11 and 12 show the hardware waveforms for Schemes B and E, respectively.

The module-level controlled load-disturbance benchmark in Figure 13 was conducted at 1000 r/min mechanical speed with a $0 \rightarrow 0.5$ N · m load step. It compared Scheme B, the transplanted RTLS compensation module from Ref. [16], and Scheme E under matched plat-

form and controller settings. The maximum mechanical-speed drops (mean $\pm$ SD, $n = 3$) were 55.04 ± 1.43 , 47.51 ± 1.24 , and 42.30 ± 1.10 r/min, respectively. The corresponding recovery times were 1.364 ± 0.079 , 0.867 ± 0.050 , and 0.827 ± 0.048 s. Relative to Scheme B, Scheme E reduced the mean maximum speed drop by 23.15% and the mean recovery time by 39.40%. Relative to the Ref. [16] module, the corresponding reductions were 10.95% and 4.62%. Figure 13a–c show the encoder-measured speed, mechanical-speed estimation error, and electrical-position estimation error. Figure 13d summarizes the maximum speed drop and recovery time across the three records. Scheme E showed the smallest load-induced speed drop and the shortest mean recovery time. These results compare the compensation modules on the common platform and do not imply a full reproduction of Ref. [16].

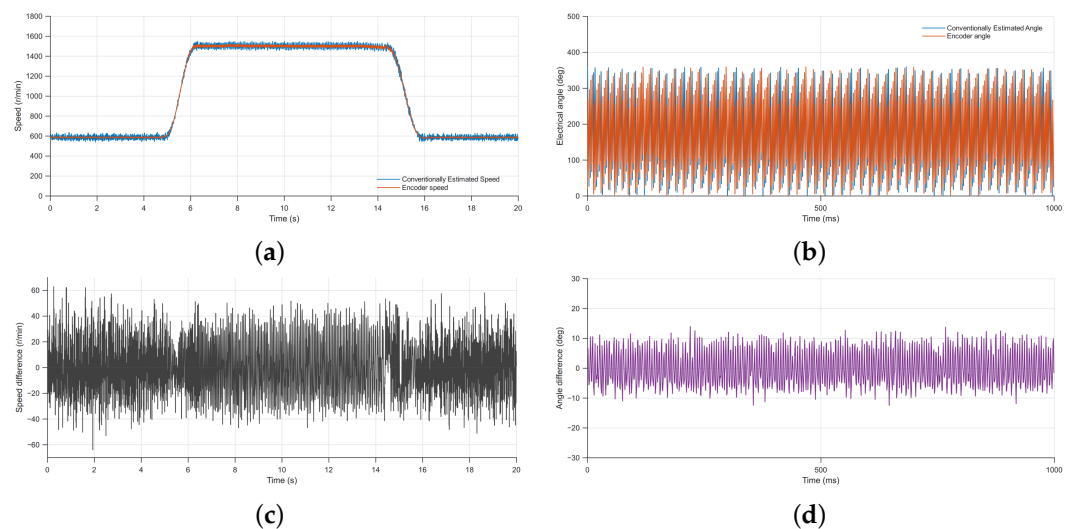


Figure 11. Dynamic speed-tracking results with the conventional compensation scheme: (a) conventionally estimated and encoder-measured mechanical speeds; (b) conventionally estimated and encoder-measured electrical angles; (c) mechanical-speed difference; and (d) electrical-angle difference.

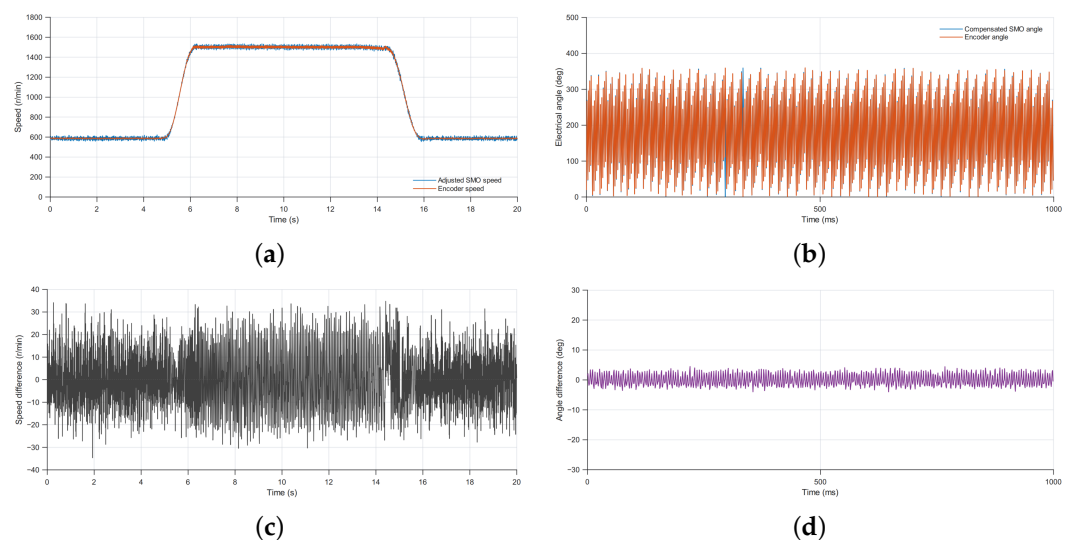


Figure 12. Dynamic speed-tracking results of the proposed scheme: (a) estimated and encoder mechanical speeds; (b) estimated and encoder electrical angles; (c) mechanical-speed difference; and (d) electrical-angle difference.

Figure 14a–c extend the same module-level benchmark with the phase-current waveform, phase-current spectrum, and d - and q -axis current responses. The displayed phase-current THD_{2:20} values are 5.94%, 4.26%, and 3.14% for Scheme B, the Ref. [16] module, and Scheme E, respectively. The corresponding d - q responses show the same ordering: Scheme B has the largest transient i_q overshoot and i_d excursion, the Ref. [16] module is intermediate, and Scheme E has the smallest transient deviation. Because compensation is applied to the observer-side reconstructed voltage, these current-quality differences are interpreted as indirect closed-loop consequences of improved electrical-position estimation rather than as direct current-harmonic or torque control. No torque measurement is claimed.

Dead-time adaptation was tested at 1 μ s, 2 μ s, and 3 μ s. The state machine remains in INIT/HOLD during the first 0.10 s, as shown in Figure 15b. Figure 15a begins when TRACK is enabled, and its time labels include this 0.10 s initialization offset. The amplitude transients in Figure 15a therefore occur only while $\chi = 1$. The steady-state means of $\hat{V}_{inv}$ in Scheme E were 0.58 V, 1.47 V, and 2.20 V, respectively. Figure 15 also reports the electrical-position errors and their steady-state spectra over repeated tests. These measures characterize adaptation across the three dead times.

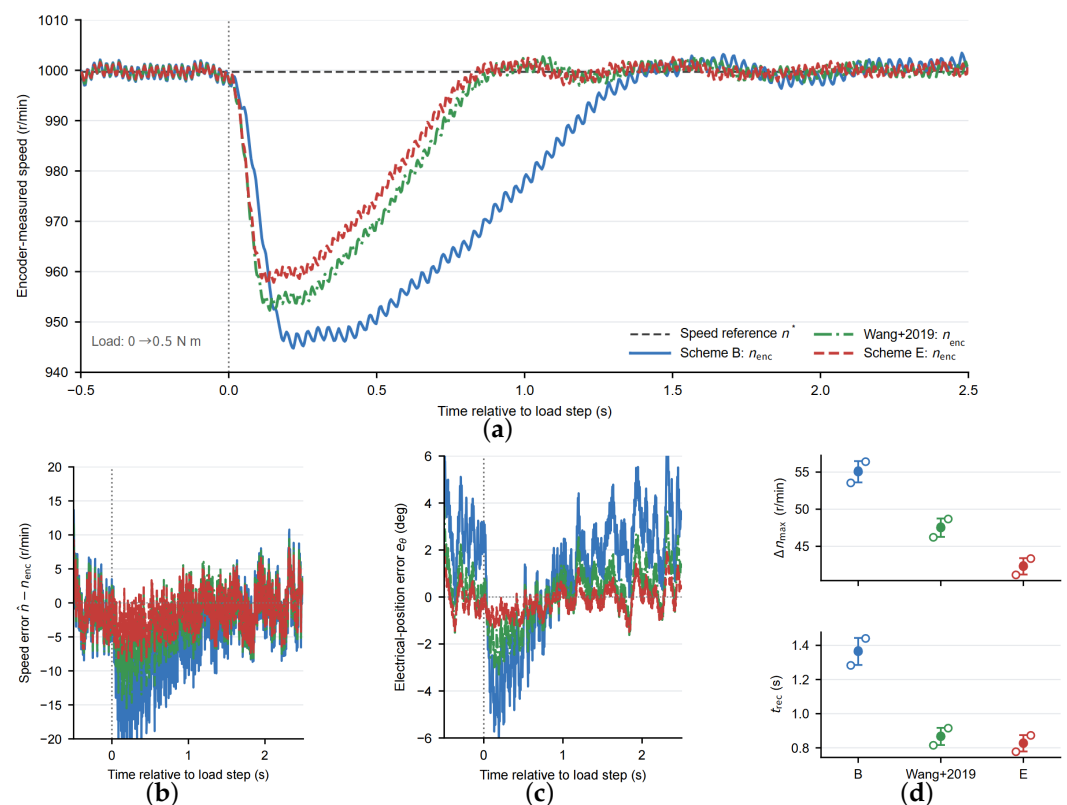


Figure 13. Common-condition load-disturbance comparison of Scheme B, Ref. [16], and Scheme E: (a) encoder-measured mechanical-speed response; (b) mechanical-speed estimation error; (c) electrical-position estimation error; and (d) maximum speed drop and recovery time. In panel (d), open circles show individual records, filled circles show means, and error bars indicate SD ($n = 3$).

The 10-kHz hardware record in Figure 16 uses a $1500 \rightarrow 900 \rightarrow 1500$ r/min mechanical-speed command. During the first deceleration, i_q^* changes from approximately +1.8 to −1.6 A and then returns to its positive level. Its sign change generates the r_{rev} pulse near 0.920 s and latches HOLD, so $\chi = 0$. The measured i_q first crosses zero at approximately 0.934 s. After the 0.16 s minimum HOLD interval, the current-release and health conditions are satisfied at approximately 1.080 s. The state then returns to TRACK, $\chi = 1$, and online updating resumes. During HOLD, $\hat{V}_{inv}$ remains near 0.6143 V, and the displayed maximum sample-to-sample change is 4.0×10^{-5} V. The electrical-position

estimation error remains bounded, with transient extrema of approximately $+4.0^\circ$ and -2.8° . It returns to approximately $\pm 1.0^\circ$ after the reversal. The hardware current-reversal test was repeated three times; Figure 16 shows one representative record.

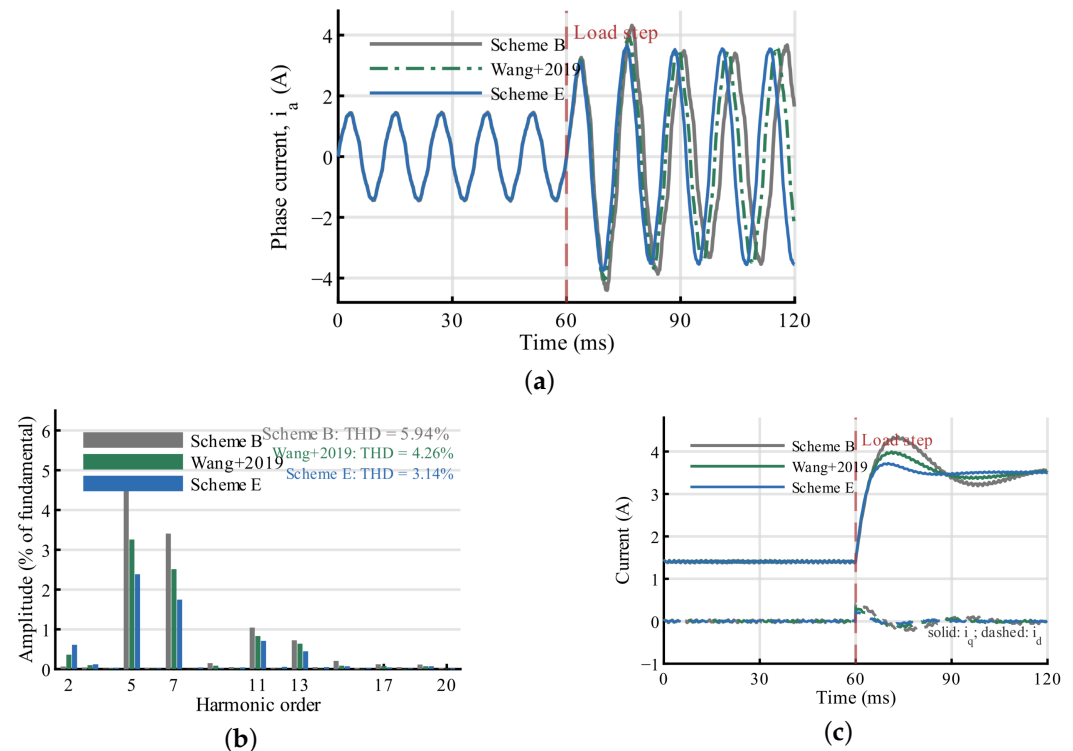


Figure 14. Common-condition current-quality comparison of Scheme B, Ref. [16], and Scheme E: (a) phase-current waveform; (b) phase-current FFT and THD_{2:20}; and (c) d - q -axis current response.

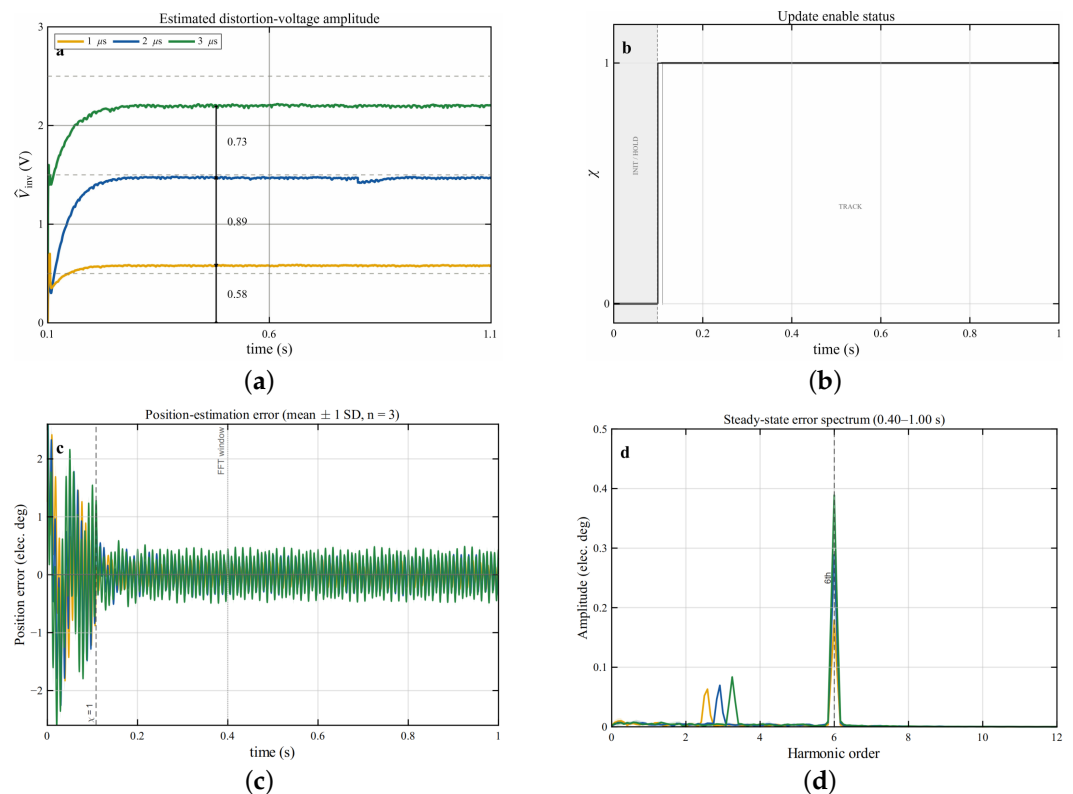


Figure 15. Online equivalent distortion-voltage amplitude update and electrical-position estimation error under different dead times: (a) estimated distortion-voltage amplitude, with the time axis including

the 0.10 s initialization interval; (b) enabling state, with $\chi = 0$ during INIT/HOLD and $\chi = 1$ during TRACK; (c) electrical-position estimation error; and (d) steady-state error spectrum.

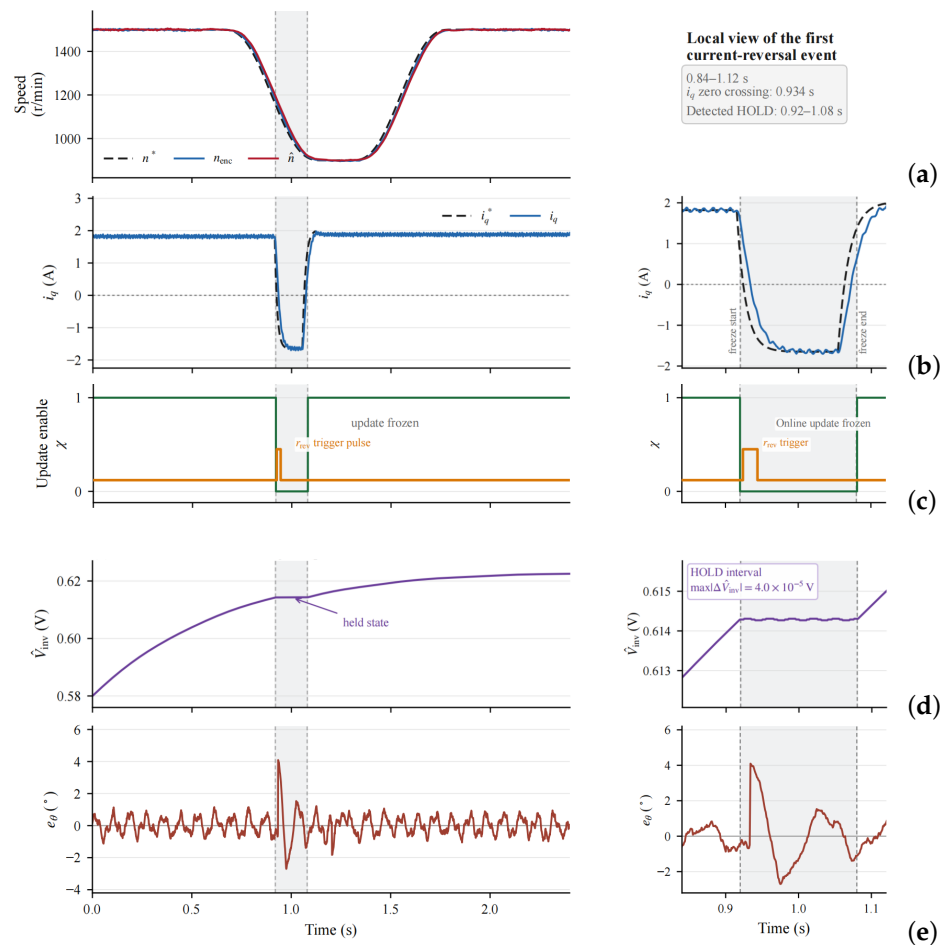


Figure 16. Hardware validation of automatic online-update freezing during q -axis current reversal: (a) speed response; (b) q -axis current reversal; (c) reversal-trigger pulse r_{rev} , vertically offset for visibility, and the latched enabling state χ , with a local view; (d) estimated distortion-voltage amplitude and local HOLD-invariance view; and (e) electrical-position estimation error. The shaded interval denotes the automatically latched HOLD state.

4.4. Discussion

The method acts on the reconstructed ASMO input $\hat{u}_{\alpha\beta}$ rather than the physical VSI terminal voltage. Any reduction in phase-current THD or torque ripple is therefore an indirect closed-loop consequence of improved electrical-position estimation. Unlike RLS-based inverter or motor-parameter identification [15,22] and iterative harmonic optimization [17], the implementation stores no covariance matrix and solves no iterative problem. Ref. [23] jointly changes the active-flux observer and applies MRAS-based correction to the PWM duty ratio, whereas the present chain retains the common ASMO–PLL and PWM command path. The fast branch evaluates three scalar prediction, weighting, and voltage-reconstruction paths followed by zero-sequence removal and one Clarke transformation. The two scalar filters and projected amplitude update execute only at 100 Hz. Its additional worst-case execution time on the LCM32F039 was 6.52 μ s, or 6.52% of the current-control period. Flash and RAM increased by 1536 bytes and 96 bytes, respectively. These implementation results support real-time feasibility but are not presented as the main contribution.

Applicability is limited by back-EMF observability, calibrated effective delay, and synchronous excitation. The local relation in Equation (26) fails at zero or extremely

low speed, during PLL loss of lock, or under sustained VSI saturation. It is also invalid for $\bar{q} \leq q_{\min}$ or rapid current reversal, when the enabling logic freezes the update. Parameter mismatch, saliency, and flux harmonics can also leak into $\hat{e}_d$. The conclusions therefore concern the tested PMSM at medium-to-high speed, where $L_d \approx L_q$ is a reasonable approximation. Zero-speed operation, strongly salient machines, and operation with large uncalibrated delay errors are outside the present scope. In addition, Figure 8 is a temperature-parameterized simulation with an externally prescribed distortion-voltage drift, not a calibrated electrothermal model or a substitute for temperature-controlled hardware validation.

5. Conclusions

This study presents a delay-aware observer-side compensation chain that coordinates two-point current prediction, C^1 -continuous cubic zero-crossing weighting, and online equivalent-distortion-voltage amplitude correction without modifying the current controller or SVPWM. The supporting analyses in Propositions 1 and 2 characterize the residual-voltage-error bound and the local contraction condition of the slow amplitude update under their stated assumptions; they do not constitute a general closed-loop stability theorem.

Against conventional compensation in the A/B/E steady-state simulation, the electrical-position-error peak-to-peak value decreased from 7.82° to 4.73° , a reduction of 39.51%. The 5th- and 7th-harmonic amplitudes fell by 39.72% and 29.27%, while the sixth-order electrical-position-error component decreased from 2.777° to 1.396° , a reduction of 49.73%. In the variable-speed hardware test, the maximum absolute mechanical-speed estimation error decreased from 62.40 to 34.1 r/min, and the maximum dynamic electrical-position error decreased from 14.86° to 5.13° . Under the 1000-r/min, $0 \rightarrow 0.5 \text{ N} \cdot \text{m}$ load step, the mean maximum mechanical-speed drop decreased from 55.04 to 42.30 r/min. The mean recovery time decreased from 1.364 to 0.827 s. These changes correspond to reductions of 23.15% and 39.40%, respectively. Across the three dead times, the steady-state means of $\hat{V}_{\text{inv}}$ were 0.58 V, 1.47 V, and 2.20 V. The added fast task required $6.52 \mu\text{s}$ in the worst case, equal to 6.52% of the current-control period.

The method is limited to the medium- and high-speed region where the back-EMF remains observable. It also depends on calibrated effective delay, and the online amplitude update is frozen during rapid current reversal, persistent current saturation, loss of lock, or protection states. The temperature-parameterized simulation evaluates a prescribed slow drift and does not replace chamber- or junction-temperature-controlled hardware validation.

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