

Article

Dynamic Duty Modulation to Enhance Voltage Equalization Performance of the Advanced Cell Balancer

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Abstract

Cell balancing is a critical requirement for ensuring the safety and longevity of supercapacitor (SC)-based energy storage systems (ESSs). While conventional series-parallel active balancing methods predominantly utilize a fixed 50% duty ratio, this static control mechanism fundamentally limits the energy transfer rate, particularly under severe initial voltage imbalances and non-ideal cell variations. To accelerate the equalization process without incurring the cost, volume, and complexity penalties of hardware modifications, this paper proposes a dynamic duty modulation (DDM) technique. The proposed DDM algorithm adaptively adjusts the switching duty ratios in real-time based on the instantaneous voltage deviations of individual cells. A discrete-time mathematical model is derived to evaluate the convergence behavior, analytically proving that the dynamic approach requires significantly fewer switching cycles than the conventional fixed-duty method. The mathematical superiority and practical feasibility of the proposed technique are strictly validated through comprehensive PSIM simulations. Quantitative simulation results confirm that the proposed DDM reduced the balancing time by over 48% and proportionally decreased the total number of switching cycles compared to the conventional method, providing an enhanced dynamic performance suitable for advanced battery management systems (BMSs).

Keywords: supercapacitor; energy management; cell balancing; dynamic duty modulation**MSC:** 93C55

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1. Introduction

Energy storage systems (ESSs) are essential for grid stability and renewable integration [1,2]. Among various storage technologies, supercapacitors (SCs) are increasingly crucial due to their high power density and rapid cycling capabilities [3,4]. However, utilizing SCs effectively requires advanced management strategies to handle critical operational challenges, particularly at the cell level [4]. To address these, recent research has focused on electrochemical property characterization and diverse applications, ranging from electric vehicles (EVs) to regenerative power systems [5,6].

In this context, cell balancing is a fundamental requirement for the performance, safety, and longevity of ESSs [7,8]. Voltage imbalances inevitably lead to capacity reduction and

potential hazards such as overheating, which can severely compromise the system lifespan and operational safety [9,10]. While various active and passive balancing methods exist, conventional research has focused primarily on efficiency and cost-effectiveness, leaving the investigation into improving dynamic performance and balancing speed relatively insufficient [11,12].

Recent efforts to overcome these speed limitations often rely on complex hardware-level optimizations, such as employing multi-winding transformers, active clamp circuits, or adding auxiliary switch matrices [13–15]. While these hardware-centric approaches can improve equalization speed, they inevitably increase the system volume, implementation cost, and overall design complexity [15,16]. On the other hand, existing adaptive or closed-loop control schemes applied to the balancing systems in the literature rely on hardware modifications or complex state observers to enhance the balancing performance [17–20]. Consequently, without relying on auxiliary hardware interventions or incurring excessive computational loads, it is difficult to adapt dynamically to instantaneous voltage variation, leading to performance degradation in severe initial imbalance scenarios [21–23]. To alleviate such computational loads, advanced mathematical approaches like characteristic value techniques [24] have recently been introduced to approximate complex device behaviors with efficient reduced-order models. However, while these modeling techniques reduce analytical complexity, achieving fast dynamic equalization in real-time embedded systems still necessitates a low-complexity control algorithm.

Therefore, this paper proposes a dynamic duty modulation (DDM) technique to enhance the balancing performance of a series-parallel cell balancer in supercapacitor ESSs. The proposed method accelerates the voltage equalization process by dynamically adjusting the duty ratios based on real-time voltage deviations, rather than relying on conventional fixed-duty switching. The key innovation of this paper lies in achieving convergence acceleration entirely through a computationally efficient method without requiring any auxiliary hardware modifications and complexity. By responding adaptively to the dynamic state of the energy transfer process, the proposed method significantly improves the equalization speed on the existing series-parallel topology. As a result, the proposed DDM method offers a fast and cost-effective balancing solution that is suitable for practical embedded implementations.

The remainder of this paper is organized as follows. Section 2 presents the theoretical foundation of the series-parallel cell balancer and analyzes the operational limitations of the conventional fixed-duty control mechanism. Section 3 details the proposed DDM technique and analytically demonstrates its mathematical superiority through a comparative convergence analysis. Section 4 provides comprehensive PSIM simulation results under various imbalance scenarios to validate the practical feasibility and accelerated balancing speed of the proposed approach. Finally, Section 5 concludes this paper with a summary of the key findings.

To facilitate the readability of the mathematical derivations presented in the subsequent sections, the most important symbols and parameters are defined in Table 1.

Table 1. Nomenclature of key parameters.

Symbol	Description
SC_n, BC_n	Supercapacitor cell and its corresponding balancing capacitor
$C_{SC}, C_{BC,n}$	Capacitance of the supercapacitor and balancing capacitor
$V_{SC,i}, V_{BC,i}$	Instantaneous voltage of the i -th supercapacitor and balancing capacitor
$I_{BC,i}$	Current flowing into the i -th balancing capacitor
V_{av}	Average voltage
$\Delta V_{SC,i}$	Voltage deviation of the i -th supercapacitor from the average voltage

Table 1. Cont.

Symbol	Description
R_s	Equivalent on-resistance of the active switches
D	Fixed PWM duty ratio (typically 0.5)
D_A, D_B	Dynamically modulated duty ratios for the upper and lower cells
$D_{\max}, D_{\min}$	Physical hardware saturation limits for the duty ratio
l_1, l_2	Gains for dynamic duty modulation
T_s, k	Sampling time (switching period) and discrete-time step index
α, ψ	Circuit-dependent exponential decay factors
ϵ	User-specified acceptable voltage imbalance threshold
k_{conv}, k_{prop}	Number of switching cycles required for convergence

2. Mathematical Formulation of Series-Parallel Cell Balancer Operation

In this section, we present the theoretical foundation and mathematical modeling of the series-parallel cell balancing topology. The operational structure of the cell balancer is shown in Figure 1, where each supercapacitor cell (SC_i) is connected through a balancing capacitor (BC_i) and four switches.

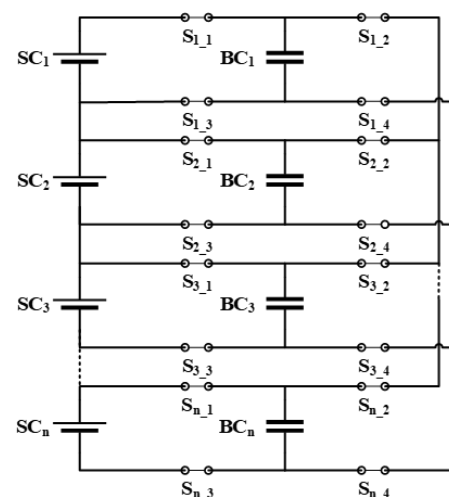


Figure 1. Series-parallel cell balancing topology.

2.1. Operational Principle of Series-Parallel Cell Balancer

The series-parallel cell balancing topology is depicted in Figure 1. This configuration consists of supercapacitors (SC_n), balancing capacitors (BC_n) and switches ($S_{n,m}$) ($\forall n \in N, m = 1, 2, 3, 4$). The operation of the series-parallel cell balancer can be categorized into two distinct stages, differentiated by the state of the odd-numbered ($m = 1, 3$) and even-numbered ($m = 2, 4$) switches.

During the 1st stage, the odd-numbered switches transition to the closed state, while the even-numbered switches remain in the open state. This configuration establishes a direct connection between each SC_n and its corresponding BC_n . The current flow is determined by the voltage potential difference between SC_n and BC_n , and continues until their voltages equalize.

Subsequently, in the 2nd stage, the odd-numbered switches transition to the open state, and the even-numbered switches close. This configuration connects all BC_n in parallel, allowing current to distribute and flow according to the individual voltage potentials of each BC_n . This current flow continues until the voltage differences converges to zero between the BC_n capacitors are equalized.

The 1st and 2nd stages alternate continuously until the voltage differential between all SC_n elements is deemed sufficiently equalized to meet the system's balance criteria.

Figure 2 illustrates the timing diagram of the conventional PWM control method used to implement this balancing strategy. In this scheme, T_s represents the sampling time and D denotes the duty ratio of the PWM signals. The complementary PWM signals are employed to control the operation of the odd-numbered and even-numbered switches, respectively.

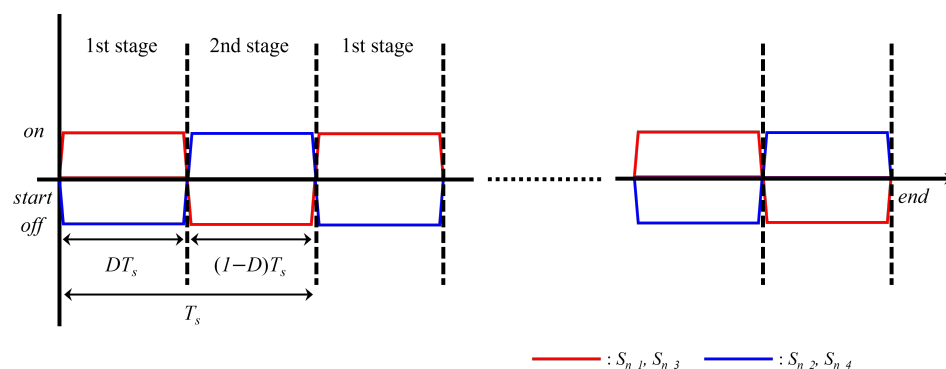


Figure 2. Timing diagram of PWM control.

2.2. Problem Statement

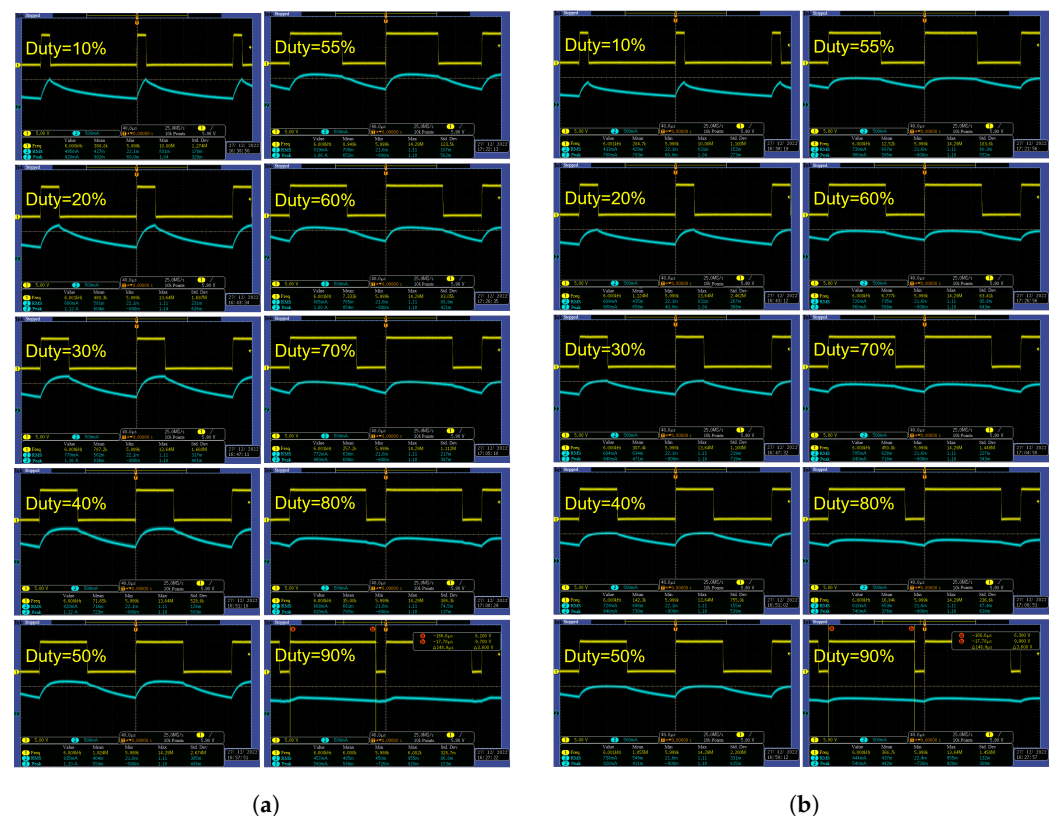
To evaluate the energy transfer characteristics of the conventional PWM control method, an experimental analysis was conducted across various duty ratios. Table 2 presents the measured balancing currents for experimental results under an identical condition, while Figure 3 visualizes the corresponding experimental waveforms. In ideal, symmetrical conditions, a 50% duty ratio is generally considered the theoretical optimal value for this topology [25].

However, the experimental results in Table 2 reveal a critical limitation of applying a single fixed-duty ratio in a real-world scenario. While Experimental result 1 achieves its maximum RMS current (835 mA) at exactly a 50% duty ratio, Experimental result 2 reaches its peak current (739 mA) at a 55% duty ratio. The variation in the optimal operational duty occurs because practical SC cells possess non-ideal characteristics, such as variations in initial voltage gaps, equivalent series resistance, and capacitance tolerances.

The discrepancy highlights the fundamental flaw of the conventional fixed-duty control mechanism. Because the maximum energy transfer point varies depending on the instantaneous physical state of each cell, applying a uniform 50% duty ratio across the entire system inevitably compromises the balancing speed under conditions similar to Experimental result 2. Conversely, fixing the duty ratio at 55% would deteriorate the energy transfer for conditions corresponding to Experimental result 1. Therefore, it is mathematically and practically difficult to define a static duty ratio that optimizes the equalization process for all cells simultaneously.

Table 2. Current measurements of a cell with different PWM duty ratios.

Duty Ratio	Experimental Result 1	Experimental Result 2
10%	495 mA	433 mA
20%	680 mA	609 mA
30%	779 mA	684 mA
40%	820 mA	729 mA
50%	835 mA	738 mA
55%	819 mA	739 mA
60%	805 mA	726 mA
70%	772 mA	705 mA
80%	668 mA	618 mA
90%	457 mA	444 mA

**Figure 3.** Experimental waveforms of the series-parallel cell balancer using the conventional method with different PWM duty ratios: (a) Experimental result 1 and (b) Experimental result 2.

Consequently, to maximize the balancing current and minimize the overall equalization time, it is necessary to move beyond a static duty ratio approach. The duty ratio must be individually and dynamically modulated in real time according to the instantaneous voltage differences of each cell. Therefore, we define the inherent operational limitation of the conventional method in the subsequent section.

2.3. Mathematical Formulation for the Conventional Method

At a given iteration k , the voltage of any cell i and its corresponding balancing capacitor are denoted $V_{SC,i}(k)$ and $V_{BC,i}(k)$. The current into BC_i is given by Ohm's law as

$$I_{BC,i}(k) = \frac{V_{SC,i}(k) - V_{BC,i}(k)}{R_s} \quad (1)$$

where R_s is the on-resistance of the switches. The same applies for another cell j :

$$I_{BC,j}(k) = \frac{V_{SC,j}(k) - V_{BC,j}(k)}{R_s} \quad (2)$$

The average system voltage, used as the balancing reference, is defined as

$$V_{av}(k) = \frac{1}{n} \sum_{h=1}^n [V_{BC,h}(k) - I_{BC,h}(k)R_s] \quad (3)$$

where $V_{BC,h}(k)$ and $I_{BC,h}(k)$ are h -th balancing capacitor's voltage and current and n is the total number of cells. This average ensures all cells are equilibrated with respect to global energy distribution.

The deviation of each cell is

$$\begin{aligned} \Delta V_{SC,i}(k) &= V_{SC,i}(k) - V_{av}(k) \\ \Delta V_{SC,j}(k) &= V_{SC,j}(k) - V_{av}(k) \end{aligned} \quad (4)$$

$\Delta V_{SC,i}$ and $\Delta V_{SC,j}$ represent the cell-to-mean error signals that must be minimized.

The dynamics of each balancing capacitor voltage are, for discrete time T_s with balancing capacitor $C_{BC,i}$,

$$V_{BC,i}(k+1) = V_{BC,i}(k) + \frac{T_s}{C_{BC,i}} I_{BC,i}(k) \quad (5)$$

and similarly for $C_{BC,j}$,

$$V_{BC,j}(k+1) = V_{BC,j}(k) + \frac{T_s}{C_{BC,j}} I_{BC,j}(k) \quad (6)$$

The supercapacitor voltages are updated as

$$V_{SC,i}(k+1) = V_{SC,i}(k) - \frac{T_s}{C_{SC}} I_{BC,i}(k) \quad (7)$$

$$V_{SC,j}(k+1) = V_{SC,j}(k) - \frac{T_s}{C_{SC}} I_{BC,j}(k) \quad (8)$$

C_{SC} is the supercapacitor's capacitance.

Expanding $I_{BC,i}(k)$ into Equations (5) and (7) yields

$$\begin{aligned} V_{BC,i}(k+1) &= V_{BC,i}(k) + \frac{T_s}{C_{BC,i}R_s} (V_{SC,i}(k) - V_{BC,i}(k)) \\ V_{SC,i}(k+1) &= V_{SC,i}(k) - \frac{T_s}{C_{SC}R_s} (V_{SC,i}(k) - V_{BC,i}(k)) \end{aligned} \quad (9)$$

The update laws for cell j can be derived identically.

For analytical convenience in the discrete-time modeling, it is assumed that ideal conditions apply where $C_{BC,i} = C_{BC,j} = C$ and parasitic elements (e.g., equivalent series resistance and parasitic inductance) are negligible. Define $\alpha = T_s / (CR_s)$. Then

$$\begin{aligned} V_{BC,i}(k+1) &= V_{BC,i}(k) + \alpha (V_{SC,i}(k) - V_{BC,i}(k)) \\ V_{SC,i}(k+1) &= V_{SC,i}(k) - \alpha (V_{SC,i}(k) - V_{BC,i}(k)) \end{aligned} \quad (10)$$

and likewise for j .

Applying the above update laws N times with a fixed PWM on-fraction D , the system follows an RC charging law for each cell:

$$\begin{aligned}\Delta V_{SC,i}(k+1) &= \Delta V_{SC,i}(k)(1 - D[1 - e^{-\alpha}]) \\ \Delta V_{SC,j}(k+1) &= \Delta V_{SC,j}(k)(1 - D[1 - e^{-\alpha}])\end{aligned}\quad (11)$$

where $1 - e^{-\alpha}$ is the normalized voltage equalization per switching step. Equation (11) thus governs the convergence speed of errors for SC_i, SC_j under fixed duty.

Recursively applying Equation (11) for k steps yields

$$\begin{aligned}\Delta V_{SC,i}(k) &= \Delta V_{SC,i}(0)(1 - D[1 - e^{-\alpha}])^k \\ \Delta V_{SC,j}(k) &= \Delta V_{SC,j}(0)(1 - D[1 - e^{-\alpha}])^k\end{aligned}\quad (12)$$

The condition for effective balancing is

$$|\Delta V_{SC,i}(k)| \leq \epsilon, \quad |\Delta V_{SC,j}(k)| \leq \epsilon \quad (13)$$

The system is regarded as successfully balanced, and the control algorithm is terminated, when all cell deviations are within a small positive threshold ϵ . Here, $\epsilon > 0$ is the user-specified allowed voltage imbalance at which the balancing is considered complete; that is, the cell bank is practically voltage-equalized whenever the maximum deviation is less than ϵ .

Solving Equation (12) for k gives the minimum cycles needed for cell i, j to balance:

$$k_{conv,i} = k_{conv,j} = \frac{\ln\left(\frac{|\Delta V_{SC}(0)|}{\epsilon}\right)}{-\ln(1 - D(1 - e^{-\alpha}))} \quad (14)$$

3. Dynamic Duty Modulation

In this section, we introduce the proposed method designed to enhance the balancing performance and efficiency of series-parallel energy systems. The balancing of cell voltages in series-parallel energy systems plays a critical role in determining system stability, longevity, and efficiency. To improve balancing performance, the dynamic duty modulation approach is proposed, wherein the duty ratios of balancing circuits are dynamically adjusted based on real-time voltage deviations. This section provides a detailed derivation of the required mathematical models and convergence analysis.

Figure 4 depicts the timing diagram of the proposed method. D_A is the duty ratio for S_{i-1} and S_{i+3} , and D_B is the duty ratio for S_{j-1} and S_{j+3} .

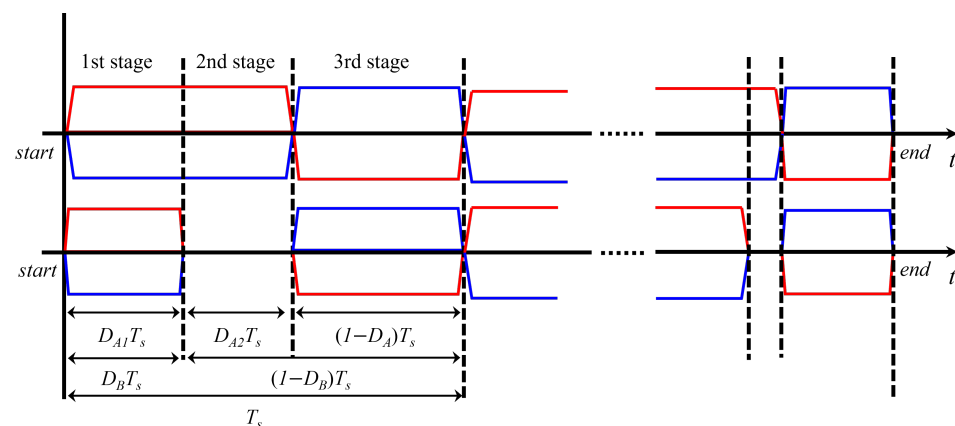


Figure 4. Timing diagram of the proposed control method.

During the first stage, as illustrated in Figure 5a,b, the switches S_{j-1} and S_{j+3} transition to the closed state. The proposed method implements adaptive duty modulation based on voltage differences.

We define the dynamic modulation of duty ratios as

$$D_A(k) = D + a(k), \quad D_B(k) = D - b(k) \quad (15)$$

where D is the baseline duty ratio, and $a(k)$ and $b(k)$ are voltage-dependent terms, expressed as

$$\begin{aligned} a(k) &= l_1 \max(0, V_{SC,i} - V_{av}) \\ b(k) &= l_2 \max(0, V_{av} - V_{SC,j}) \end{aligned} \quad (16)$$

To manage peak transient currents within the safe operating area of the switches, the modulated duty ratios are practically bounded to $D_A(k), D_B(k) \in [D_{\min}, D_{\max}]$, where $D_{\max} = 0.9$ and $D_{\min} = 0.1$ represent the physical hardware saturation limits.

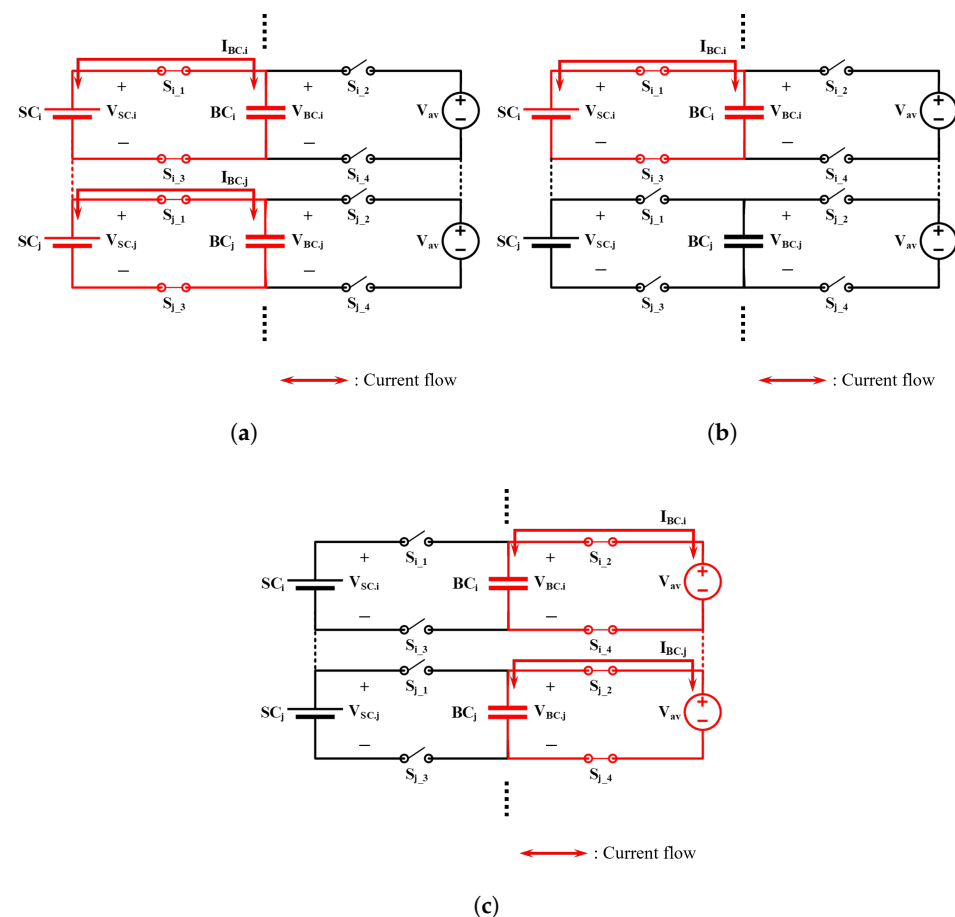


Figure 5. Operational principle of the proposed dynamic duty modulation: (a) 1st stage, (b) 2nd stage, (c) 3rd stage.

Remark 1. Here, Gains l_1 and l_2 utilize values normalized with respect to the voltage deviation ($\Delta V_{SC,i}$ and $\Delta V_{SC,j}$) to ensure that the adaptive modulation terms remain appropriately scaled. To maintain system stability and prevent oscillatory divergence, these gains must be strictly bounded. The stability criterion of the difference equations requires the absolute value of the error decay factor to be strictly less than 1. This establishes the mathematical upper bounds for gains, such that $|1 - D \cdot \psi - l_1 \cdot \psi| < 1$ and $|1 - D \cdot \psi + l_2 \cdot \psi| < 1$. Satisfying these conditions ensures that the iterative balancing process converges monotonically without exceeding the defined saturation limits.

The voltage deviation for the higher-voltage cell evolves according to the equation:

$$\Delta V_{SC,i}(k) = \Delta V_{SC,i}(k-1)[1 - D_A(k-1)(1 - e^{-\alpha})] \quad (17)$$

Substituting $D_A(k-1) = D + a(k-1)$, we rewrite the following:

$$\begin{aligned} \Delta V_{SC,i}(k) &= \Delta V_{SC,i}(k-1)[1 - (D + a(k-1))(1 - e^{-\alpha})] \\ &= \Delta V_{SC,i}(k-1)[1 - D \cdot \psi - a(k-1) \cdot \psi] \end{aligned} \quad (18)$$

where we define $\psi = 1 - e^{-\alpha}$.

Similarly, for the lower-voltage cell,

$$\Delta V_{SC,j}(k) = \Delta V_{SC,j}(k-1)[1 - D_B(k-1)(1 - e^{-\alpha})] \quad (19)$$

Substituting $D_B(k-1) = D - b(k-1)$, this becomes

$$\begin{aligned} \Delta V_{SC,j}(k) &= \Delta V_{SC,j}(k-1)[1 - (D - b(k-1))(1 - e^{-\alpha})] \\ &= \Delta V_{SC,j}(k-1)[1 - D \cdot \psi + b(k-1) \cdot \psi] \end{aligned} \quad (20)$$

The convergence of the system is defined as the point where all voltage deviations meet the following condition:

$$|\Delta V_{SC,i}(k)| \leq \epsilon, \quad |\Delta V_{SC,j}(k)| \leq \epsilon \quad (21)$$

where ϵ represents the threshold for acceptable voltage deviation. Iteratively expanding the evolution equations, we express

$$\Delta V_{SC,i}(k) = \Delta V_{SC,i}(0) \prod_{h=0}^{k-1} [1 - D \cdot \psi - l_1 \cdot \psi \cdot \max(0, V_{SC,i}(h) - V_{av})] \quad (22)$$

$$\Delta V_{SC,j}(k) = \Delta V_{SC,j}(0) \prod_{h=0}^{k-1} [1 - D \cdot \psi + l_2 \cdot \psi \cdot \max(0, V_{av} - V_{SC,j}(h))] \quad (23)$$

For convergence analysis, the number of iterations k_i and k_j required for the higher-voltage and lower-voltage cells, respectively, are derived as

$$k_i = \frac{\ln\left(\frac{|\Delta V_{SC,i}(0)|}{\epsilon}\right)}{-\ln(1 - D \cdot \psi - l_1 \cdot \psi)} \quad (24)$$

$$k_j = \frac{\ln\left(\frac{|\Delta V_{SC,j}(0)|}{\epsilon}\right)}{-\ln(1 - D \cdot \psi + l_2 \cdot \psi)} \quad (25)$$

In contrast, the convergence time for a fixed-duty modulation method, where $a(k) = b(k) = 0$, is given as

$$k_{conv} = \frac{\ln\left(\frac{|\Delta V_{SC}(0)|}{\epsilon}\right)}{-\ln(1 - D \cdot \psi)} \quad (26)$$

with $\psi = 1 - e^{-\alpha}$.

To prove the fast convergence performance of the proposed method mathematically, we compare the denominators. Because $l_1 > 0$ and the voltage deviation is strictly positive, the decay factor $1 - D \cdot \psi - l_1 \cdot \psi$ is strictly less than the conventional factor $1 - D \cdot \psi$. Since the natural logarithm $\ln(x)$ is a monotonically increasing function over its domain $(0, 1)$,

taking the natural logarithm yields $\ln(1 - D \cdot \psi - l_1 \cdot \psi) < \ln(1 - D \cdot \psi) < 0$. Multiplying both sides by -1 reverses the inequality:

$$-\ln(1 - D \cdot \psi - l_1 \cdot \psi) > -\ln(1 - D \cdot \psi) > 0 \quad (27)$$

As the denominator is strictly larger for the DDM method, the overall fraction k_i strictly decreases. An identical mathematical proof holds for k_j assuming an appropriately defined negative gain logic for the lower cell expansion. Therefore, comparing k_i , k_j , and k_{conv} , it logically follows as:

$$k_{prop} = \max(k_i, k_j) < k_{conv} \quad (28)$$

The proposed DDM method achieves superior performance by introducing adaptive terms $a(k)$ and $b(k)$, which accelerate voltage equalization by dynamically responding to voltage variations. The duty modulation process is shown in Figure 4, illustrating actual time series for $D_A(k)$, $D_B(k)$ and their impact on cell convergence according to Equations (15)–(28). Consequently, this sequential mathematical derivation conclusively demonstrates the superiority of the proposed DDM method.

4. Simulation

4.1. Simulation Setup

In this section, the mathematical superiority and practical performance of the proposed method are verified through comprehensive simulations. First, the simulation environment, including the circuit topology and critical control parameters, is detailed. Subsequently, the comparative simulation results are presented to demonstrate the accelerated voltage convergence speed of the proposed method against the conventional fixed-duty method.

To validate the operational principle of the series-parallel cell balancer, a simulation model was developed using the PSIM software (version 2025, Altair Engineering, Inc., Troy, MI, USA), as depicted in Figure 6. In this model, C_{SC} and C_{BC} were set to 10 F and 1 mF, respectively. To ensure high precision in capturing the transient dynamics of the balancing currents and cell voltages, the simulation time step was rigorously tuned to 100 μ s (0.0001 s). Furthermore, the control execution period and the switching frequency of the active MOSFETs were configured to 10 kHz. The initial test condition assumes an intentional voltage imbalance, where the supercapacitor cells start at 2.001 V and 1.999 V, respectively. To verify performance under more extreme scenarios, a larger initial imbalance condition (e.g., 2.1 V vs. 1.9 V) was also simulated. Additionally, to explicitly evaluate the impact of the equivalent series resistance (ESR), the SCs were configured at 0.001 Ω and 0.01 Ω as supplementary simulation conditions.

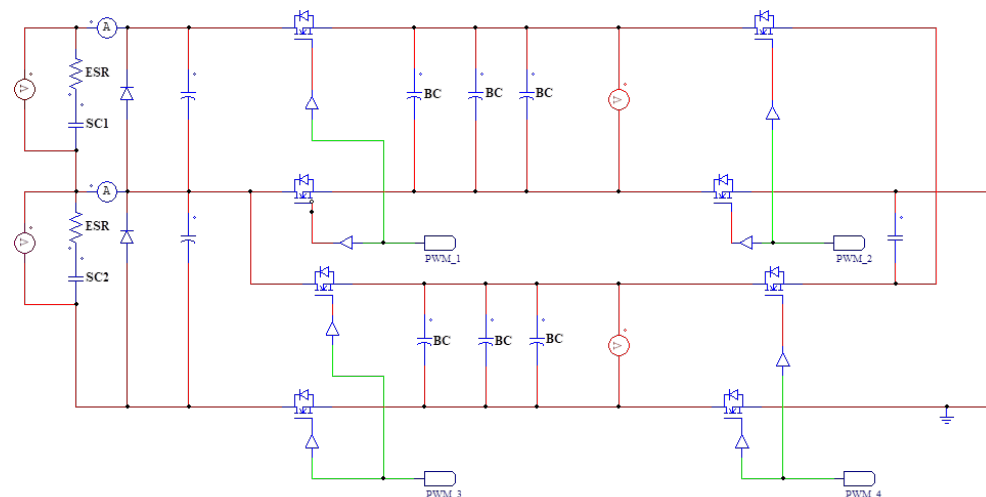


Figure 6. Simulator of the series-parallel cell balancer.

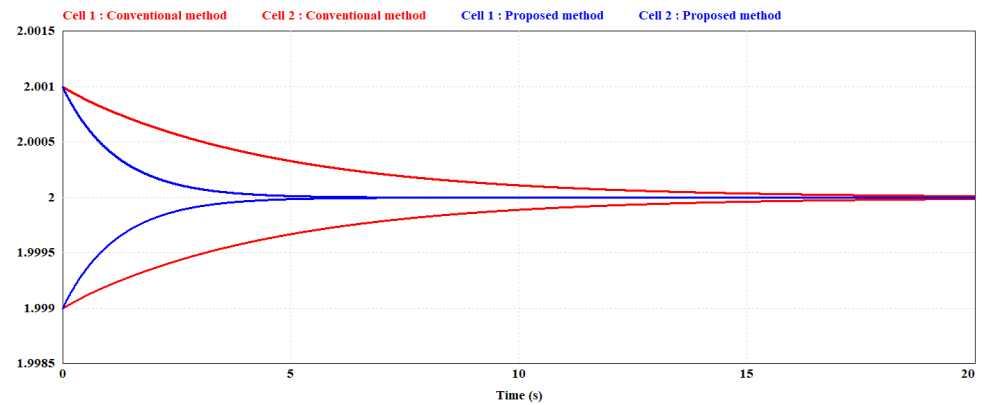
4.2. Simulation Result

Figure 7a presents the comparative simulation results, which illustrate the cell voltage trajectories during the equalization process. The red waveforms show the voltage convergence behavior under the conventional fixed-duty method. The blue waveforms show the dynamic response under the proposed method. As can be seen in the initial state, while the voltage deviation is at its maximum, the proposed method significantly increases the energy transfer rate by adaptively expanding the duty ratio in proportion to the voltage gap. Consequently, cell voltages under the proposed method converge to the target equalized voltage of 2.0 V more rapidly than under the conventional method. Furthermore, Figure 7b shows the comparison result of the balancing performance under a more severe initial imbalance condition (2.1 V and 1.9 V). In this extreme condition, the conventional fixed-duty method presents a prolonged equalization period due to its restricted static energy transfer. In contrast, the proposed DDM method actively sustains a faster convergence speed throughout the large voltage deviation period. To quantitatively validate this superiority, Table 3 compares the balancing times under each initial imbalance condition. The results confirm that the proposed DDM method significantly accelerates the equalization process, achieving an over 62.76% and 48.68% relative time reduction in each imbalance condition.

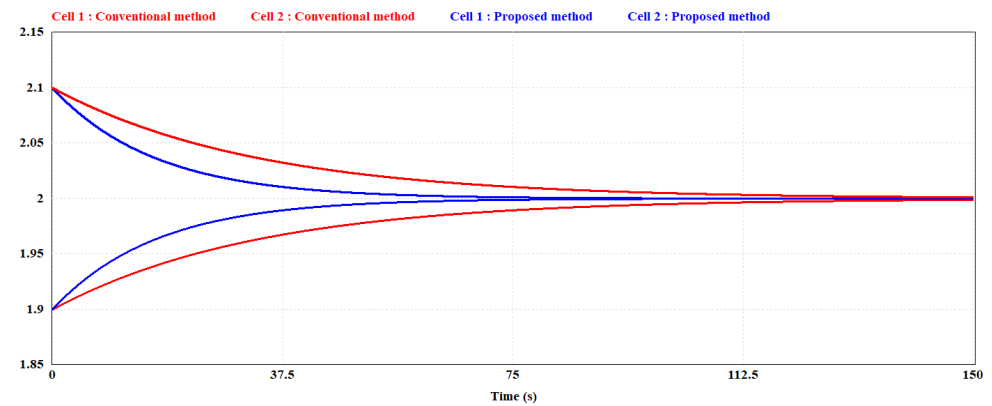
Figure 8 presents the comparative balancing current profiles for Cell 1. It is observed that the proposed method generates a higher peak current with an extended duty cycle compared to the conventional method. This adaptive behavior is the fundamental mechanism behind the accelerated balancing performance. The duty ratio modulated by the proposed method allows for a larger energy transfer across the balancing capacitor, thereby facilitating faster voltage convergence under imbalance conditions.

To explicitly evaluate the impact of real-world physical losses, which were simplified in the idealized mathematical model, additional simulations were conducted by integrating the ESR of SCs. Figure 9 illustrates the dampening effect of the ESR on the voltage convergence speed. As the ESR increases, the voltage applied to the balancing capacitor decreases due to internal IR drops, and a portion of the transferring energy is dissipated as heat. So, the actual charge transferred per switching cycle is reduced, which inevitably dampens the equalization speed and requires more balancing cycles to reach the equalized voltage compared to the ideal condition. Nevertheless, the results confirm that the proposed DDM method mitigates the degradation, achieving voltage equalization in 77.049 s—a 48.47 % relative time reduction compared to the 149.522 s required by the conventional method under the 0.001 Ω condition. Furthermore, under the 0.01 Ω condition, the proposed method completed the equalization in 78.997 s, maintaining a relative time reduction of 47.34 % against the conventional method

(>150 s). Consequently, by adaptively modulating the duty ratio, the proposed method allows for a larger energy transfer, thereby facilitating faster voltage convergence.



(a) 2.001 V and 1.999 V



(b) 2.1 V and 1.9 V

Figure 7. Comparative simulation results of the conventional method and the proposed method under different initial voltage imbalance conditions.

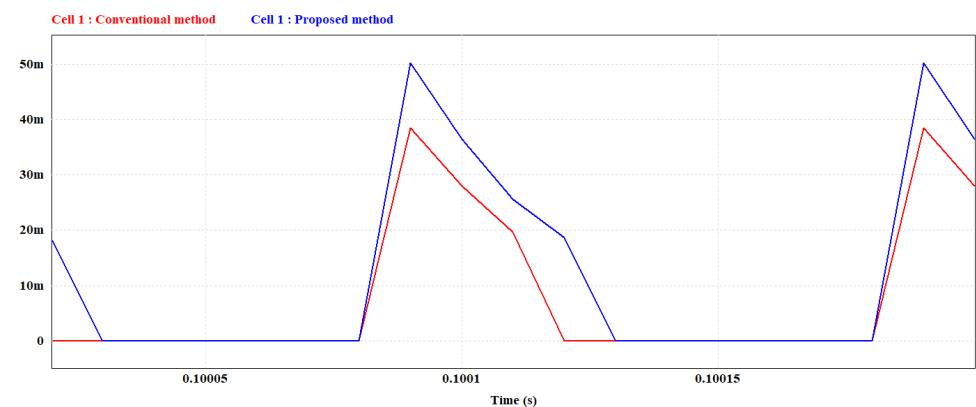


Figure 8. Comparative simulation result of $I_{BC,1}$ between the conventional method and the proposed method.

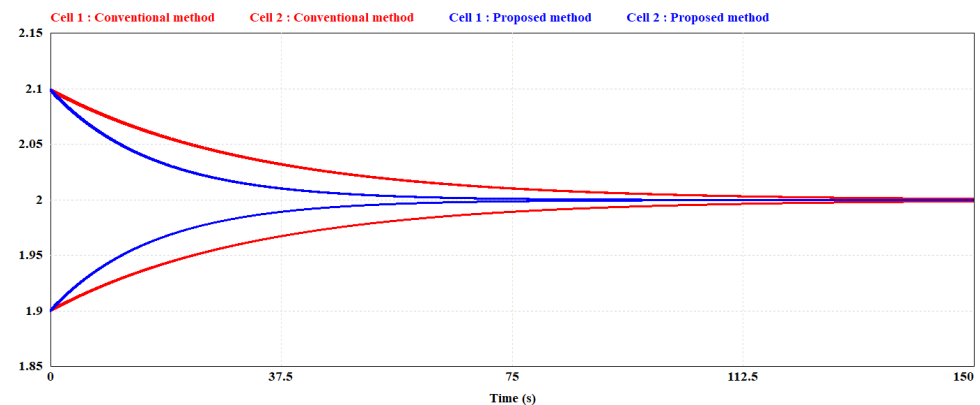
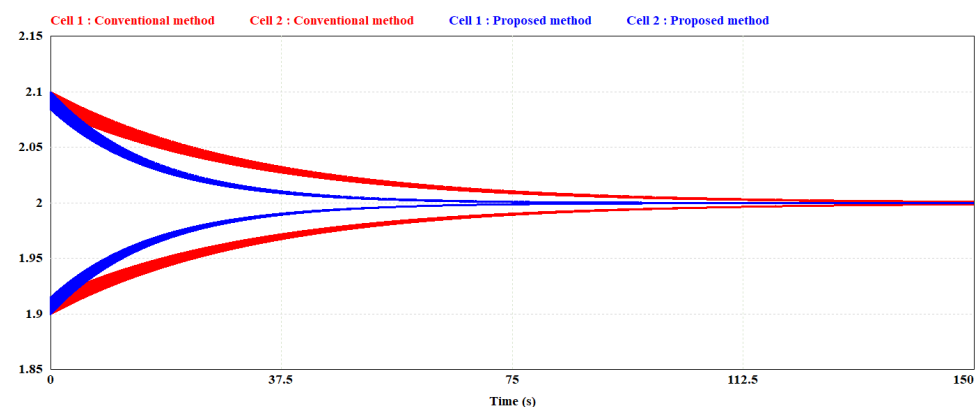
(a) 0.001 Ω (b) 0.01 Ω

Figure 9. Comparative simulation results of the conventional method and the proposed method under different equivalent series resistances.

Table 3. Quantitative comparison of balancing time under different initial voltage imbalances.

Control Method	Initial Voltages ($V_{SC,1}$ & $V_{SC,2}$)	Balancing Time (s)	Relative Time Reduction (%)
Conventional	2.001 V & 1.999 V	10.107	
Proposed DDM	2.001 V & 1.999 V	3.763	62.76
Conventional	2.1 V & 1.9 V	148.547	
Proposed DDM	2.1 V & 1.9 V	76.229	48.68

5. Conclusions

This paper proposed the DDM method to overcome the inherent speed limitations of conventional series-parallel cell balancers in supercapacitor ESSs. Through experimental analysis, it was demonstrated that a static 50% duty ratio fails to maximize energy transfer due to variations in real-time voltage gaps and non-ideal cell characteristics. To address this limitation, the proposed DDM method adaptively modulates the duty ratios based on instantaneous cell-to-average voltage deviations. A mathematical convergence analysis was conducted, conclusively proving that the proposed DDM method significantly reduces the required number of balancing cycles compared to the conventional fixed-duty approach. Furthermore, PSIM simulations verified that the DDM method considerably accelerates the equalization process, particularly under severe initial imbalance scenarios. Specifically, the quantitative evaluation demonstrated that the DDM method reduced the balancing time by up to 62.76% in simulation results, consistently ensuring a faster equalization

process and fewer switching cycles compared to the conventional static 50% duty ratio method. The key contribution of this study lies in achieving fast dynamic balancing performance through algorithmic advancements, eliminating the need for complex and costly hardware modifications. Ultimately, the proposed DDM offers a highly efficient, versatile, and cost-effective solution for advanced battery management systems.

While the proposed DDM method significantly accelerates the balancing speed, it inherently induces higher peak transient currents due to the expanded duty cycles, presenting a physical trade-off with the switching stress imposed on the MOSFETs. Furthermore, although the dampening effect of component conduction losses was evaluated via simulation, unmodeled hardware-level bottlenecks, such as sensor noise, ADC quantization errors, and processing delays, remain limitations of the current study. To address these practical issues, our future work involves establishing a Hardware-in-the-Loop Simulation (HILS) framework alongside a precision hardware prototype based on a high-performance digital microcontroller. By utilizing the HILS platform, we will verify the experimental performance of the proposed DDM method while explicitly reflecting real-world embedded implementation constraints. This subsequent research will integrate digital noise filtering, thermal stress analysis, and energy efficiency optimization to comprehensively evaluate the sustained performance and long-term reliability of the proposed DDM method in advanced BMS applications.

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