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Improved Properties of Post-Deposition Annealed Ga_2O_3/SiC and Ga_2O_3/Al_2O_3/SiC Back-Gate Transistors Fabricated by Radio Frequency Sputtering

Hee-Jae Lee [1], Geon-Hee Lee [1], Seung-Hwan Chung [1], Dong-Wook Byun [1], Michael A. Schweitz [1], Dae Hwan Chun [2], Nack Yong Joo [2], Minwho Lim [3], Tobias Erlbacher [3] and Sang-Mo Koo [1,*]

[1] Department of Electronic Materials Engineering, Kwangwoon University, Seoul 01897, Republic of Korea; tkrkek123@kw.ac.kr (H.-J.L.); ghlee117@kw.ac.kr (G.-H.L.); wkdrn1394@kw.ac.kr (S.-H.C.); byun1994@kw.ac.kr (D.-W.B.); michael.schweitz@schweitzlee.com (M.A.S.)
[2] Electronic Devices Research Team, Hyundai Motor Group, Uiwang-si 16082, Republic of Korea; chundh@hyundai.com (D.H.C.); n.y.joo@hyundai.com (N.Y.J.)
[3] Fraunhofer Institute for Integrated Systems and Device Technology, Schottkystrasse 10, 91058 Erlangen, Germany; minwho.lim@iisb.fraunhofer.de (M.L.); tobias.erlbacher@iisb.fraunhofer.de (T.E.)
* Correspondence: smkoo@kw.ac.kr; Tel.: +82-2-940-5763

Abstract: The high breakdown electric field, n-type doping capability, availability of high-quality substrates, and high Baliga's figure of merit of Ga_2O_3 demonstrate its potential as a next-generation power semiconductor material. However, the thermal conductivity of Ga_2O_3 is lower than that of other wide-bandgap materials, resulting in the degradation of the electrical performance and reduced reliability of devices. The heterostructure formation on substrates with high thermal conductivity has been noted to facilitate heat dissipation in devices. In this work, Ga_2O_3 thin films with an Al_2O_3 interlayer were deposited on SiC substrates by radio frequency sputtering. Post-deposition annealing was performed at 900 °C for 1 h to crystallize the Ga_2O_3 thin films. The Auger electron spectroscopy depth profiles revealed the interdiffusion of the Ga and Al atoms at the Ga_2O_3/Al_2O_3 interface after annealing. The X-ray diffraction (XRD) results displayed improved crystallinity after annealing and adding the Al_2O_3 interlayer. The crystallite size increased from 5.72 to 8.09 nm as calculated by the Scherrer equation using the full width at half maximum (FWHM). The carrier mobility was enhanced from 5.31 to 28.39 $cm^2\ V^{-1}\ s^{-1}$ in the annealed Ga_2O_3 thin films on Al_2O_3/SiC. The transfer and output characteristics of the Ga_2O_3/SiC and Ga_2O_3/Al_2O_3/SiC back-gate transistors reflect the trend of the XRD and Hall measurement results. Therefore, this work demonstrated that the physical and electrical properties of the Ga_2O_3/SiC back-gate transistors can be improved by post-deposition annealing and the introduction of an Al_2O_3 interlayer.

Keywords: gallium oxide; heterostructure; wide bandgap; transistor; aluminum oxide; semiconductor

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1. Introduction

Although Si-based semiconductors have been widely used in power electronic devices, the narrow bandgap of Si (1.1 eV) limits its applications owing to its instability in harsh environments, such as high temperatures [1,2]. Wide-bandgap semiconductors, such as GaN, 4H-SiC, and Ga_2O_3, are important materials for high-frequency, -power, and -temperature devices [2–4]. Among these, Ga_2O_3 has a bandgap (~4.9 eV) that is significantly higher than that of 4H-SiC (~3.3 eV) and GaN (~3.4 eV) [5–7]. Owing to its high breakdown electric field (~8 MV cm^{-1}), n-type doping capability, availability of high-quality substrates, and high Baliga's figure of merit (~3400), Ga_2O_3 is attracting extensive attention as a next-generation power semiconductor material [5,6,8–11].

Despite the advantages of Ga_2O_3, its thermal conductivity (11–27 $Wm^{-1}\ K^{-1}$) is lower than that of other wide-bandgap materials, such as SiC (370 $Wm^{-1}\ K^{-1}$) and GaN

(253 Wm^{-1} K^{-1}). The heat generated in Ga_2O_3 may thus increase the lattice temperature, thereby affecting the carrier mobility in current devices, potentially resulting in critical degradation of electrical performance and device reliability [10,11]. For high-power and -frequency applications, thermal management is an inevitable consideration for reducing device degradation [11,12]. By forming heterostructures on substrates with high thermal conductivity, such as 4H-SiC, heat dissipation in devices can be facilitated [10,13].

For ε-Ga_2O_3 and ZnO, which have similar crystal structures, previous studies showed that an amorphous Al_2O_3 interface buffer layer can improve the crystallinity of the thin films [14,15]. Moreover, as Ga_2O_3 has an ultra-wide bandgap, few gate dielectric materials can achieve conduction band offsets of over 1 eV, which is favorable for metal-oxide-semiconductor structures [16]. Recently, materials, including Al_2O_3 and its alloys, are being broadly investigated for use as a gate or buffer oxide layers in metal-oxide-semiconductor field-effect transistors [16–20].

Channel control of MOSFETs has been improved by adopting various gate structures. Multi-gate MOSFETs (MGMOS), as well as gate-all-around (GAA) transistors, are investigated to increase the gate control and the integration density [21]. The double-gate structure consisting of top and back gate also improves the gate controllability like short channel effects [22]. However, there are not many studies on Ga_2O_3 transistors that investigate the effect of multi-gate including back-gate transistors. Therefore, it is necessary to study the characteristics and improve the performance of Ga_2O_3 transistors using back gates.

In this work, we deposited Ga_2O_3 and Al_2O_3 films on n-type 4H-SiC substrates by radio frequency (RF) sputtering. Post-deposition annealing at 900 °C was performed to crystallize the Ga_2O_3 thin films. The structural and electrical characteristics of the films were analyzed by Auger electron spectroscopy (AES), X-ray diffraction (XRD), Hall measurements, and current–voltage (I–V) measurements.

2. Experimental Details

Figure 1a,b show schematics of the fabricated structures, comprising Ga_2O_3 on SiC and Ga_2O_3 on Al_2O_3/SiC, respectively. N-type 4H-SiC (0004) substrates with a doping concentration of 1×10^{19} cm^{-3} were cleaned using acetone, methanol, and deionized water for 15 min each. The native oxide layer was stripped using a buffered oxide etch with a 30:1 ratio of HF:NH_4F for 5 min. Substrate back-side metal in the form of a 100 nm thick Ni layer was deposited by an electron beam (E-beam) evaporator (KVE-T8065, Korea Vacuum Co., Ltd., Daegu, Republic of Korea) with a working pressure of 5×10^{-4} Pa. Ohmic contacts were formed at the 4H-SiC/Ni interface by rapid thermal annealing at 1000 °C for 60 s under an N_2 atmosphere. Ga_2O_3- and Al_2O_3-sintered ceramic targets (Toshima Manufacturing Co., Ltd., Saitama, Japan. purity of 99.99%) were used for RF sputtering. In Figure 1a, Ga_2O_3 films were deposited to a thickness of ~350 nm on cleaned N-SiC substrates for 200 min. In Figure 1b, Al_2O_3 (~100 nm, 200 min) and Ga_2O_3 (~350 nm, 200 min) films were deposited on the substrates. The sputtering chamber base and working pressures were maintained at 6×10^{-4} and 3 Pa, respectively. Sputtering was performed at room temperature (25 °C), with no external substrate heating, 120 W sputtering power. and Ar gas flow rate of 4 sccm. Thin films were subsequently annealed at 900 °C for 60 min under an N_2 atmosphere using a tube furnace at 101.325×10^3 Pa. The top Ti (20 nm)/Au (100 nm) electrodes were deposited on the Ga_2O_3 thin films using an E-beam evaporator. The distance between the source and drain was 100 μm.

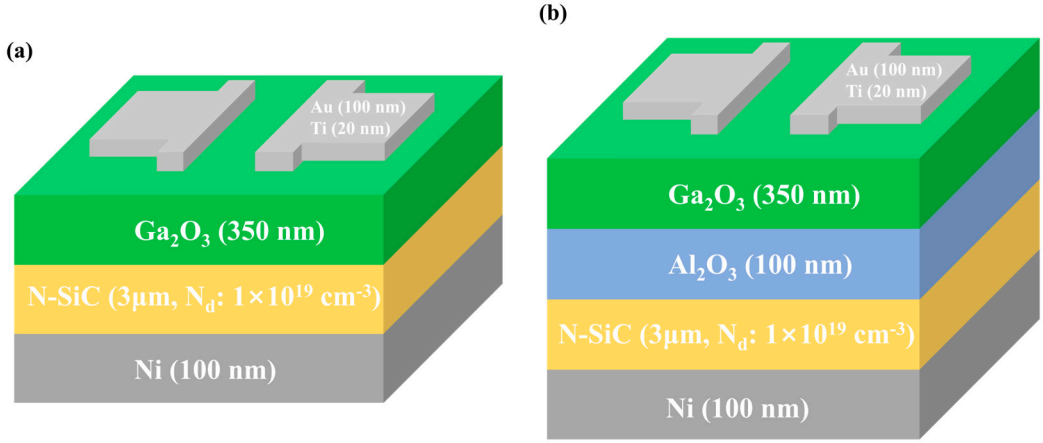

Figure 1. Schematic of the (**a**) Ga_2O_3/SiC and (**b**) Ga_2O_3/Al_2O_3/SiC structures.

3. Characterization and Instrumentation

AES depth profiling was conducted using a PHI 710 scanning Auger probe (ULVAC-PHI, Kanagawa, Japan)with electron beam energy of 5 kV, target current of 5 nA, and a SiO_2 sputtering rate of 29.4 nm·min^{-1} to confirm the depth-dependent atomic concentration of the samples. The crystallinity and orientations of the Ga_2O_3 thin films were examined using XRD (Dmax2500/PC, Rigaku, Tokyo, Japan) by 2θ scanning with CuKα radiation (λ = 0.15406 nm) at 200 mA and 40 kV. Electrical properties of the Ga_2O_3 thin films, including mobility, charge carrier concentrations, and resistivity, were analyzed by Hall effect measurements (HMS-5000, Ecopia Corporation, Anyang, Republic of Korea). I–V characteristics of the devices were measured by a Keithley 4200-SCS (Cleveland, OH, USA) parameter analyzer. Electrical measurements were carried out on the devices by sweeping the gate-to-source voltage (V_{GS}) from −6 to +2 V and drain-to-source voltage (V_{DS}) from 0 to +10 V.

4. Results and Discussion

The AES measurements were carried out to obtain a depth profile of Ga, Al, O, Si, and C elements in order to understand their diffusion behaviors at the interface during annealing. Figure 2a–d show depth profiles of the as-deposited and annealed Ga_2O_3/SiC and Ga_2O_3/Al_2O_3/SiC structures. In the Ga_2O_3/SiC structures (Figure 2a,c), sharp interfaces were observed between the Ga_2O_3 thin films and SiC substrates. Meanwhile, in the Ga_2O_3/Al_2O_3/SiC structures (Figure 2b,d), Al, O, Si, and C atoms had not diffused into the opposite SiC substrates or Al_2O_3 films. However, gradient changes of Ga and Al atomic concentrations at the Ga_2O_3/Al_2O_3 interface indicate the interdiffusion of Ga and Al atoms [23,24]. Therefore, $(Al_xGa_{1-x})_2O_3$ ternary compounds at the Ga_2O_3/Al_2O_3 interfaces were formed during the annealing of the devices.

In order to investigate the surface of Ga_2O_3 films, atomic force microscopy (AFM) was performed with a scanned area of 5 × 5 μm^2. Figure 3 shows morphological AFM 2D images of as-deposited and annealed Ga_2O_3 films on SiC and Al_2O_3. The root mean square (rms) roughness was (a) 0.821, (b) 0.845, (c) 1.324, and (d) 1.359 nm, respectively. The result shows that the surfaces of the annealed samples are rougher than the as deposited sample, and thus the annealing treatment may provide energy to atoms in the films and induce the recrystallization of Ga_2O_3 films.

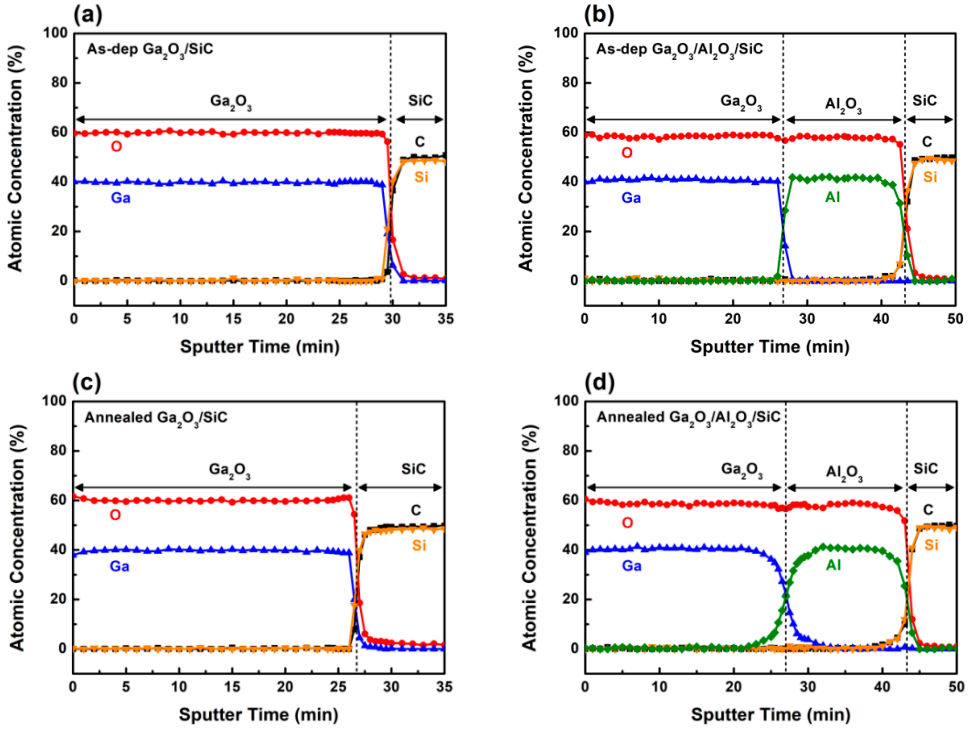

Figure 2. AES depth profiles of the as-deposited and annealed (900 °C) (**a**,**c**) Ga_2O_3/SiC and (**b**,**d**) Ga_2O_3/Al_2O_3/SiC structures, respectively.

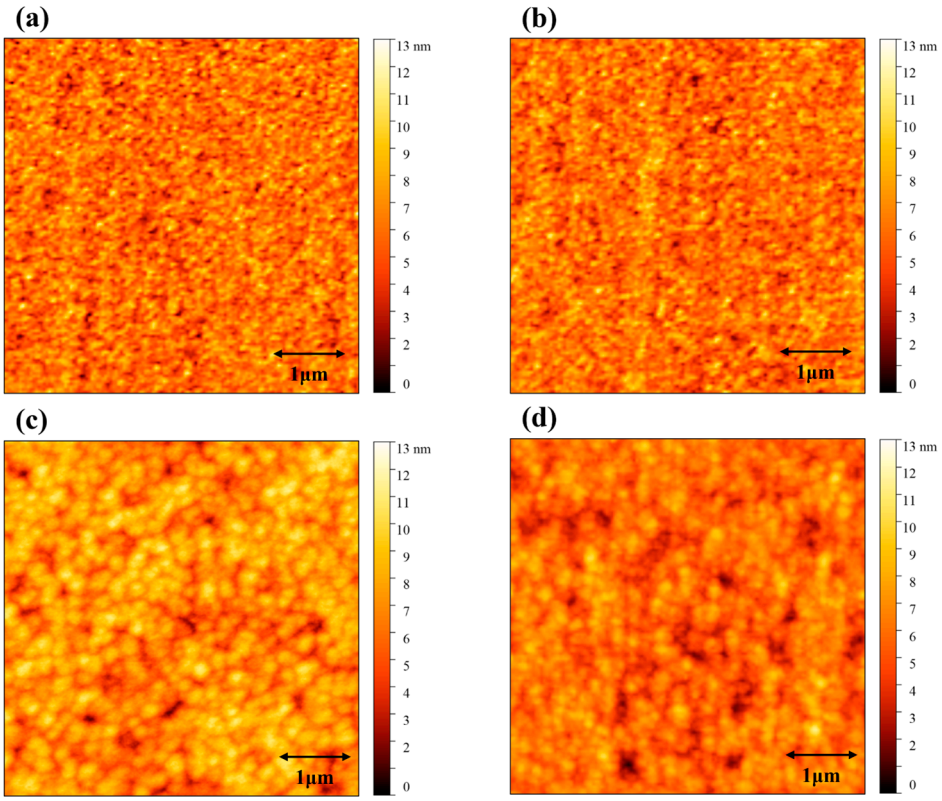

Figure 3. AFM images of the as-deposited and annealed (**a**,**c**) Ga_2O_3/SiC and (**b**,**d**) Ga_2O_3/Al_2O_3/SiC back-gate transistors, respectively.

Figure 4 illustrates the scanning electron microscopy (SEM) images of as deposited and annealed Ga_2O_3 films on SiC and Al_2O_3, respectively. It can be clearly seen that larger crystals were formed after the annealing process at 900 °C. Moreover, as shown in

Figure 4c,d, annealed Ga_2O_3 thin films possess well-defined grain boundaries which may affect the Hall mobility of devices.

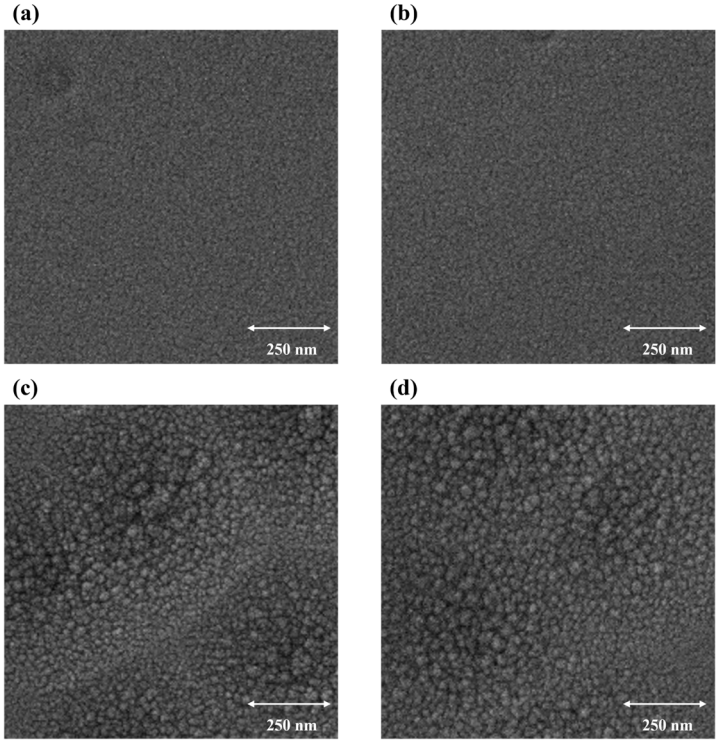

Figure 4. SEM images of the as-deposited and annealed (**a**,**c**) Ga_2O_3/SiC and (**b**,**d**) Ga_2O_3/Al_2O_3/SiC back-gate transistors, respectively.

The XRD 2θ–θ patterns at θ of 10–90° of the RF-sputtered Ga_2O_3 thin films with and without an Al_2O_3 interlayer are shown in Figure 5. For the as-deposited samples, only strong diffraction peaks of the 4H-SiC (0004) substrates were noted [25,26]. The absence of any Ga_2O_3 peaks indicates that the as-deposited thin films are in an amorphous state [27]. After annealing at 900 °C, three main peaks were noted at 30.36°, 64.36°, and 35.48°, corresponding to Ga_2O_3(–401) [28], Ga_2O_3(020) [9,29], and 4H-SiC(0004), respectively. Furthermore, diffraction peaks of Al_2O_3 were not observed in the Ga_2O_3/Al_2O_3/SiC structure, indicating that the deposited Al_2O_3 films remained amorphous, even after annealing at 900 °C. This can be attributed to the low annealing temperature in this experiment, which, according to the literature, is too low to cause a phase change from amorphous to crystalline Al_2O_3 [30]. The presence of the lattice mismatch buffering Al_2O_3 interlayer, along with any $(Al_xGa_{1-x})_2O_3$ formed at the Ga_2O_3/Al_2O_3 interface, resulted in enhanced diffraction peak intensities from the (–401) and (020) Ga_2O_3 crystal faces [14,15,31,32], which may connect to increased crystallite size.

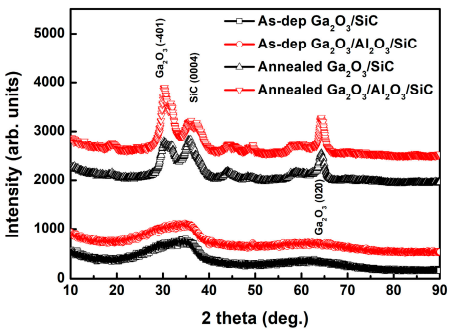

Figure 5. XRD 2θ—θ wide-scan spectra of the Ga_2O_3 thin films.

The full width at half maximum (*FWHM*) and crystallite sizes were extracted from the (020) peaks to compare the effects of the Al_2O_3 interlayer on the crystallinity of the annealed Ga_2O_3 thin films. Figure 6 shows XRD patterns of the (020) peaks and FWHM values of the annealed Ga_2O_3 thin films. The Scherrer equation (Equation (1)) was used to calculate the crystallite sizes:

$$FWHM = \frac{K\lambda}{L\cos\theta} \quad (1)$$

where K is the shape factor (0.9), L is the crystallite sizes, θ is the Bragg diffraction angle [2], and λ is the wavelength of the CuKα X-ray source (0.15406 nm). The crystallite size of the Ga_2O_3 thin films tends to increase from 5.72 to 8.09 nm with the addition of the Al_2O_3 interlayer. The crystallite size is inversely proportional to the number of grain boundaries, which are a major factor in carrier mobility degradation [33]. This suggests that the samples with the Al_2O_3 interlayer may exhibit improved electrical characteristics.

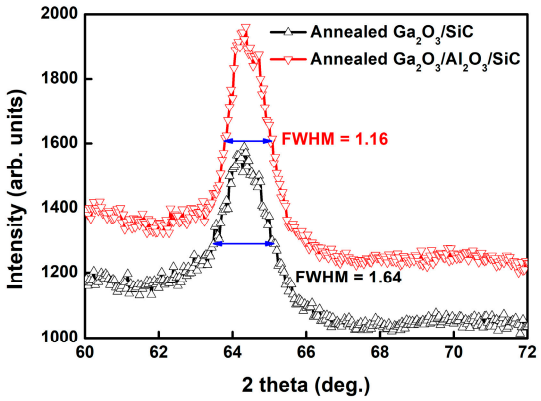

Figure 6. XRD patterns of (020) peaks and the extracted FWHM values of annealed Ga_2O_3 thin films, with or without an Al_2O_3 interlayer.

Hall measurements of the Ga_2O_3 thin films were performed (at room temperature) to examine the influence of annealing and the presence or absence of an Al_2O_3 interlayer on the electrical properties of the sample devices. Figure 7 shows the carrier concentration, mobility, and resistivity of the different Ga_2O_3 thin films, according to whether they had been annealed after deposition or not, and relating to the device structure, with or without an Al_2O_3 interlayer. After annealing of the thin films, the Hall mobility increased, indicating the effect of Ga_2O_3 crystallization on the Hall mobility. The annealed $Ga_2O_3/Al_2O_3/SiC$ devices exhibited the highest charge carrier concentration and mobility (4.52×10^{14} cm^{-3} and 25.65 cm^2 V^{-1} s^{-1}, respectively) and lowest resistivity (19.86×10^3 Ωm). As previously hypothesized, the improved Hall mobility can be attributed to the larger crystallite size due to the reduction in grain boundary scattering [34–36].

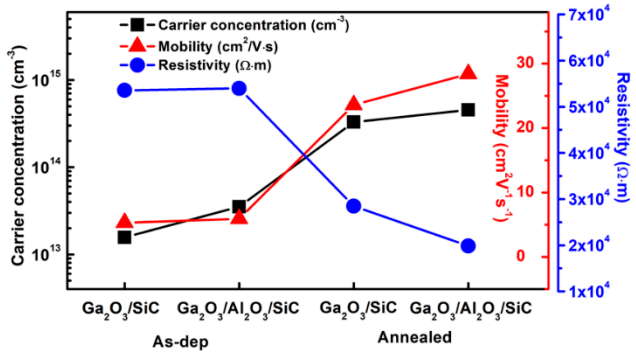

Figure 7. Hall mobility, carrier concentration, and resistivity of the Ga_2O_3 thin films.

The back-gate transistors, as shown in Figure 1a,b, have a source–drain spacing of 100 µm with highly doped SiC/Ni back gates. Figure 8a,b show the electrical transfer characteristics of the as-deposited and annealed Ga_2O_3/SiC and Ga_2O_3/Al_2O_3/SiC back-gate transistors. The subthreshold swing (*SS*), defined by the V_{GS} variations required for the ten-fold increase in I_{DS}, is given by the maximum slope in the transfer curve in a logarithmic scale [37] and can be extracted by (Equation (2)):

$$SS = \frac{dV_{GS}}{d(\log I_{DS})} \quad (2)$$

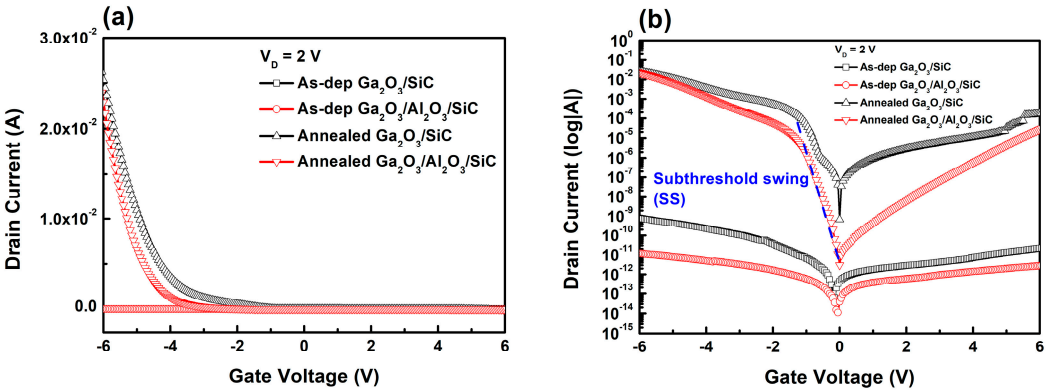

Figure 8. Transfer characteristics of the as-deposited and annealed Ga_2O_3/SiC and Ga_2O_3/Al_2O_3/SiC back-gate transistors in (**a**) linear and (**b**) logarithmic scales.

The on and off currents, on/off ratio (V_{GS} = ±6 V), and *SS* of the devices are shown in Table 1. The annealed Ga_2O_3/Al_2O_3/SiC transistors have the highest on/off ratio of 8.27×10^2 and the lowest *SS* of 154 mV·dec^{-1}.

Table 1. Electrical characteristics of fabricated back-gate transistors.

	As-Deposited		Annealed at 900 °C	
	Ga_2O_3/SiC	**Ga_2O_3/Al_2O_3/SiC**	**Ga_2O_3/SiC**	**Ga_2O_3/Al_2O_3/SiC**
On current [A] (+6 V)	8.03×10^{-10}	1.19×10^{-11}	2.53×10^{-2}	2.27×10^{-2}
Off current [A] (−6 V)	-2.14×10^{-11}	-2.78×10^{-12}	-1.73×10^{-4}	-2.75×10^{-5}
On/off ratio	3.74×10	4.29	1.46×10^2	8.27×10^2
SS (mV·dec^{-1})	233	234	182	154

The I_{DS}-V_{DS} output curves were measured by sweeping the V_{DS} from 0 to +10 V, whereas V_{GS} was biased from −6 to +2 V. Figure 9a–d show the electrical output characteristics of the back-gate transistors. The transistors with the as-deposited Ga_2O_3 films exhibited a maximum I_{DS} below 10^{-9} A, whereas the transistors with annealed Ga_2O_3 films featured currents over 10^{-4} A. Annealed samples with an Al_2O_3 layer exhibited the highest carrier mobility, resulting in the highest on-current level. This result is mainly attributed to the improved crystallinity of the Ga_2O_3 films by annealing [38] and the addition of the Al_2O_3 interlayer [14,15,31,32]. The larger crystallite grains, and thus enhanced crystallinity, apparently mitigate the parasitic resistance [39] and grain boundary scattering of thin films [33,36] of the Ga_2O_3 thin films, resulting in improved device performance.

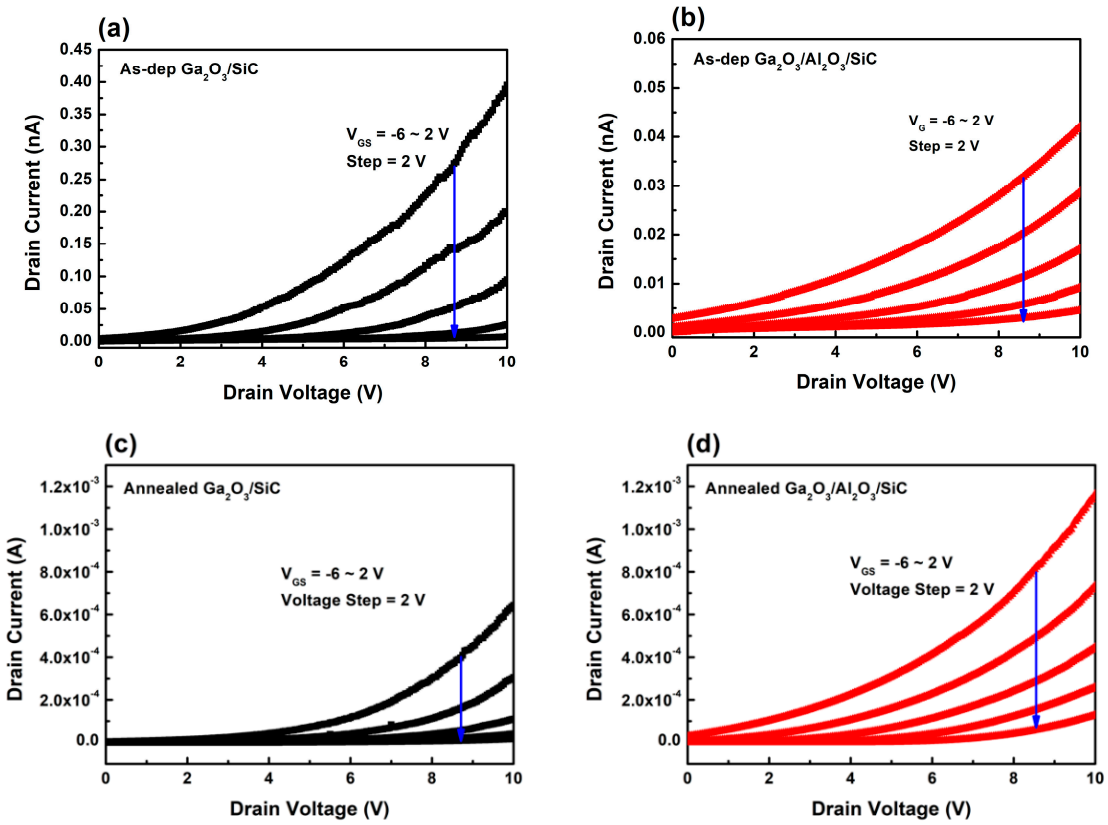

Figure 9. Output characteristics of the as-deposited and annealed (**a**,**c**) Ga_2O_3/SiC and (**b**,**d**) Ga_2O_3/Al_2O_3/SiC back-gate transistors, respectively.

5. Conclusions

In this study, Ga_2O_3 and Al_2O_3 thin films were deposited on 4H-SiC substrates using RF sputtering to compare the effects of an Al_2O_3 interlayer on the morphological and electrical properties of the manufactured thin films and resulting devices. Through AES depth profiling, we confirmed that Al and Ga atoms interdiffusion at the Ga_2O_3/Al_2O_3 interface during annealing at 900 °C. XRD results brought to light an improved crystallinity of the Ga_2O_3 thin films after annealing and adding the Al_2O_3 layer. Annealed Ga_2O_3 film on Al_2O_3/SiC displayed the highest carrier concentration and mobility of 4.52×10^{14} cm^{-3} and 25.65 cm^2 V^{-1} s^{-1}, respectively, as well as the lowest resistivity of 19.86×10^3 Ω·m. These enhanced electrical properties of the annealed Ga_2O_3 on Al_2O_3/SiC affected the transfer and output characteristics, resulting in the highest on/off ratio (8.27×10^2) and lowest SS (154 mV·dec^{-1}). Thus, introducing an Al_2O_3 interlayer in RF-sputtered Ga_2O_3/SiC back-gate transistors improved the electrical characteristics of the devices.

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Data Availability Statement: Data supporting the published results can be obtained from the authors upon reasonable request.

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Conflicts of Interest: The authors declare no conflict of interest.

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