

Article

Mitigation of the Row-Hammer Effect in Sub-20 nm Dynamic Random-Access Memory (DRAM) Using Low- k Dielectrics

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Abstract

As dynamic random-access memory (DRAM) continues to scale down and achieve higher integration density, the cell layout has transitioned to $6F^2$, resulting in narrower spacing between adjacent word lines (WLs). Consequently, cell-to-cell disturbance has become more severe. In particular, the row-hammer effect (RHE) has emerged as a critical reliability issue that must be mitigated to ensure stable operation in next-generation DRAM devices. In this study, a novel DRAM cell structure is proposed, in which a low- k dielectric material is embedded beneath the storage node (SN) to mitigate the electric field. This structural modification effectively suppresses the RHE compared to the conventional partial-isolation type buried channel array transistor (Pi-BCAT). The feasibility and performance of the proposed structure were verified through 2D Sentaurus technology computer-aided design (TCAD) simulations. The device embedding the low- k dielectric beneath the SN exhibits a mitigation of approximately 20.45% in D0 failure and about 12.12% in D1 failure. This improvement is attributed to the reduced electric field in the region underneath the SN, which suppresses stored charge leakage. These results confirm that the proposed structure not only enhances DRAM reliability in advanced process nodes but also provides an effective design guideline for highly integrated and low-power memory devices.

Keywords: row-hammer effect (RHE); low- k dielectrics; buried channel array transistor (BCAT); disturbance

1. Introduction

Dynamic random-access memory (DRAM) has continuously increased its integration density through cell size scaling to achieve larger storage capacity, higher operation speed, and lower cost per bit [1–4]. As the integration continues to advance, the spacing between DRAM cells becomes narrower, and the distance between adjacent word lines (WLs) is reduced, aggravating electrical disturbance between neighboring cells [5–10]. As one of the major disturbance mechanisms in DRAM, the row-hammer effect (RHE) has emerged as a critical reliability concern. RHE occurs when a WL is repeatedly activated within a short time interval, which induces electromagnetic disturbance between physically adjacent rows and results in unintended bit flips in adjacent cells [11–14]. In addition, RHE-induced errors are known to depend on the stored data pattern. In particular, it has been reported that cells with stored data ‘0’ tend to be relatively more vulnerable [15]. The study that first introduced the RHE tests on commodity DDR3 DRAM modules from three major



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DRAM manufacturers showed that more than 80% of the modules were susceptible to RHE [12]. In the last decade, the minimum number of aggressor row activations required to trigger a bit flip has decreased by more than a factor of 10, while the frequency of bit flips occurring with the same number of row activations has increased by a factor of 500 [8]. Studies by Google Project Zero have shown that row hammer can corrupt system memory, trigger system crashes, and be exploited as a serious security threat [15]. Various attack techniques exploiting row-hammer vulnerabilities have also been reported. Accordingly, extensive research has been conducted to mitigate RHE from system-level, circuit-level, and device-level perspectives. At the system level, mitigation schemes such as Per-Row Activation Counting (PRAC) and BlockHammer have been studied, in which the activation count of each row is monitored and ACT commands to frequently activated aggressor rows are delayed or temporarily throttled to prevent exceeding the row-hammer threshold [16–18]. However, these approaches can incur performance overhead due to monitoring and throttling, and there is a limitation that detection and throttling may be incomplete due to bypass patterns [19,20]. At the circuit level, techniques such as target row refresh (TRR), which selectively performs additional refreshes on the row adjacent to aggressor rows, and approaches that reduce the impact of row-hammer-induced bit flips by detecting and correcting errors using error code correction Error Correcting Code (ECC), are being studied. However, these approaches can increase peripheral circuit area and power consumption, and ECC remains vulnerable to multi-bit flips due to its limited correction capability [21–25].

Therefore, a fundamental solution through device structure and material optimization is required to effectively suppress the RHE. At the device level, several studies have proposed various device structures, forming buried oxides or airgaps beneath the storage node (SN) and the field region containing the passing WL (PWL), reducing electrical disturbance between adjacent cells [26–29]. In this study, considering the mechanism of the RHE in DRAM, a structure embedding a low- k dielectric material beneath the SN is proposed. The effectiveness of the proposed structure is verified using technology computer-aided design (TCAD) simulation, demonstrating the proposed structure effectively suppressing the RHE compared to the partial-isolation type buried channel array transistor (Pi-BCAT). Compared to Pi-BCAT, the proposed structure can improve D0 failure by 20.45% and D1 failure by 12.12%, with minimal degradation in electrical performance. Finally, we analyzed the reasons for the disparity in improvement between D1 failure and D0 failure conditions.

2. Device Structure and Physics

Figure 1a,b shows the open bit-line (BL) structure used in the $6F^2$ DRAM cell and the corresponding simulated device structure. Two cells are formed within a single active region, and these cells share the same BL. Each cell operation is controlled by the active word line (AWL), while the passing word line (PWL) is placed in the field region as a dummy WL to maintain a constant WL pitch.

The detailed device parameters and bias conditions are presented in Table 1 [29,30]. In this work, silicon oxycarbide (SiOC) is chosen as the low- k dielectric material, which is reported to exhibit thermal stability up to 550 °C, and the dielectric constant of 2.8 for SiOC is applied for the simulation [31]. The work function of titanium nitride (TiN) is set to 4.5 eV [32]. A Gaussian profile is adopted for the source and drain doping, and acceptor-like interface traps are introduced with a concentration of $1 \times 10^{14} \text{ cm}^{-3}$ in exponential distribution. The simulation is performed based on the timing parameters of DDR5, and additional details are provided in Figure 1c and Table 2 [33].

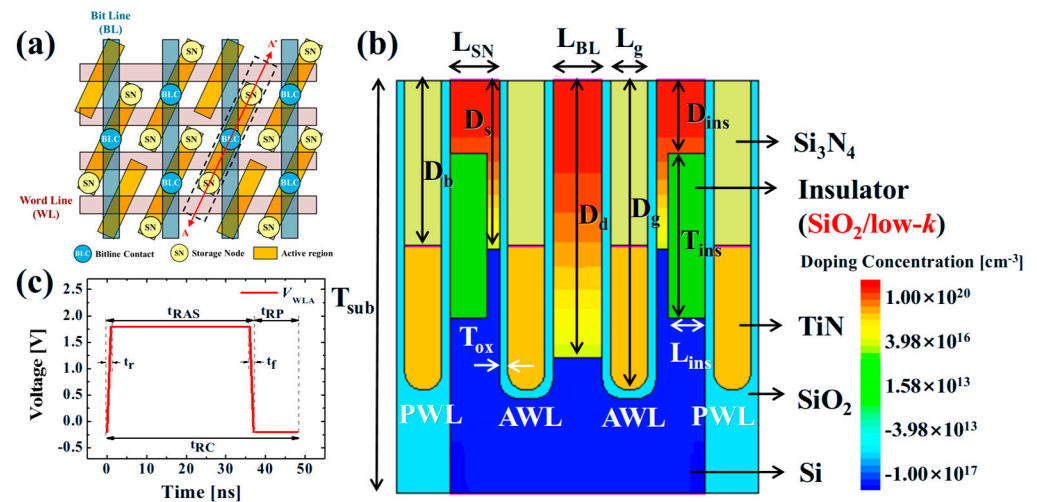


Figure 1. (a) Open BL structure used in the 6F² DRAM layout; (b) device structure of 6F² BCAT used in the TCAD simulation; (c) applied bias scheme of WL_A and defined timing parameters.

Table 1. Device parameters.

Parameter	Value
Gate length (L_g)	18 nm
Source/drain length (L_{SN} , L_{BL})	24 nm
Source depth (D_s)	82 nm
Drain depth (D_d)	134 nm
Substrate thickness (T_{sub})	200 nm
Gate oxide thickness (T_{ox})	4 nm
Recessed depth (D_g)	150 nm
Gate depth (D_b)	70 nm
Insulator length (L_{ins})	18 nm
Insulator thickness (T_{ins})	80 nm
Insulator depth (D_{ins})	35 nm
SN _A , SN _V capacitor	15 fF
BL capacitor	150 fF
N-type doping concentration	$1 \times 10^{20} \text{ cm}^{-3}$
P-type doping concentration	$1 \times 10^{17} \text{ cm}^{-3}$
Acceptor like trap density	$1 \times 10^{14} \text{ cm}^{-3}$
V_{PP}	1.8 V
V_{BBW}	−0.2 V
V_{CORE}	1.1 V

Table 2. Timing parameters.

Parameter	Value
t_{RAS}	36 ns
t_{RC}	48 ns
t_{RP}	12 ns
Rise/fall time	1 ns

For accurate calculation of the simulation results, the following models are included: (1) drift-diffusion; (2) doping-dependent mobility (PhuMob) and mobility degradation; (3) velocity saturation; (4) Shockley–Read–Hall recombination (doping and temperature dependent, field enhancement); (5) Auger recombination; (6) Avalanche generation; (7) band-to-band tunneling (Hurkx); and (8) band-gap narrowing (Slotboom). In this study,

comprehensive physical models reflecting high-field effects and carrier transport phenomena in actual operating environments were applied to accurately predict the physical behavior of the device and ensure simulation reliability. First, the drift-diffusion model was adopted as the fundamental carrier transport framework, solving the coupled Poisson and continuity equations. As carrier mobility is a key factor determining the driving current, the Philips Unified Mobility (PhuMob) model was employed to precisely simulate scattering effects according to doping concentrations. Additionally, the mobility degradation effect at the interface and velocity saturation under strong electric fields were simultaneously considered to prevent overestimation of current during high-voltage operation. The generation and recombination of charge carriers are critical factors determining the leakage current and breakdown characteristics of the device. Specifically, the Shockley–Read–Hall (SRH) model, which includes doping concentration and field dependence, was used to reflect non-ideal recombination current caused by traps. The Auger recombination model was incorporated to improve physical accuracy under high-injection conditions. Furthermore, an Avalanche generation model was applied to simulate impact ionization in high-field regions, and the Hurkx band-to-band tunneling (BTBT) model was included to analyze leakage current components resulting from strong electric fields at the junctions. Finally, the bandgap narrowing effect based on the Slotboom model was applied to account for energy band contraction in heavily doped regions, thereby minimizing calculation errors in threshold voltage and current density caused by variations in intrinsic carrier concentration [34].

Figure 2 shows the transfer curves of the low- k -embedded structure, the SiO₂-embedded structure and the conventional BCAT structure. Detailed electrical characteristics are presented in Table 3. The device characteristics such as subthreshold swing, DIBL, and off current exhibit differences in less than 0.5% among the three structures. Furthermore, no significant difference in electrical characteristics is observed between low- k and SiO₂-embedded structures. However, up to ~11.7% degradation of on current is observed in the low- k -embedded structure compared to the conventional BCAT structure, due to the reduced doping region induced by the buried insulator.

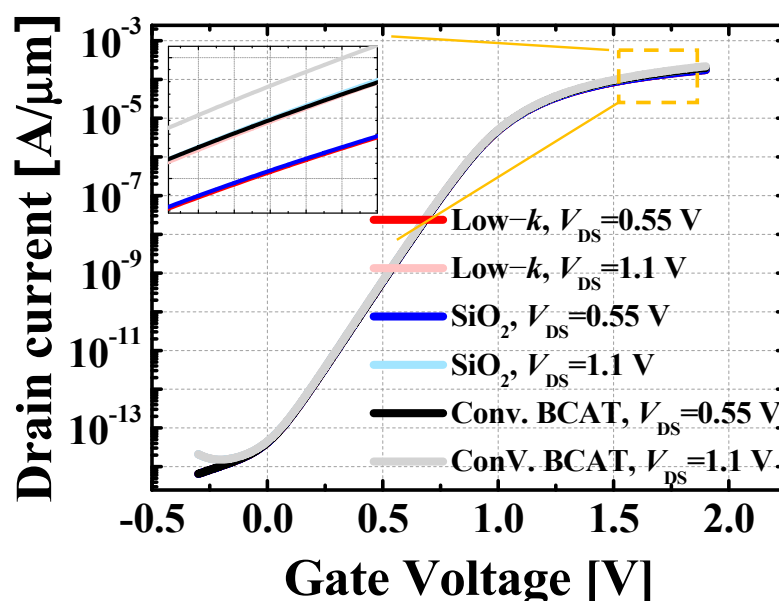


Figure 2. Transfer curves of the low- k -embedded structure, the SiO₂-embedded structure and the conventional BCAT structure at $V_{DS} = 0.55$ V and 1.1 V (log scale).

Table 3. Device electrical characteristics.

Parameter	Low- <i>k</i> -Embedded	SiO ₂ -Embedded	Conventional BCAT
Subthreshold swing [mV/dec]	114.59	114.65	114.49
DIBL [mV/V]	5.14	5.12	5.13
On current (WL = 1.8 V) [$\mu\text{A}/\mu\text{m}$]	152.23	152.89	172.45
Off current (WL = 0 V) [fA/ μm]	41.61	41.59	41.81

This degradation of current in low-*k*-embedded structure shows trade-off relationship between row-hammer tolerance, which will be discussed in Sections 3 and 4.

3. Results and Discussion

3.1. Alleviation of the D0 Failure

The D0 failure occurs when a PWL acts as an aggressor to induce the bit flip of the stored '0' data in the victim SN (SN_V). Figure 3 shows the mechanism of the D0 failure. When the aggressor PWL (PWL_A) is activated under the condition that the SN_V stores data '0', electrons stored in the victim capacitor are emitted due to the electric field. The emitted electrons are then trapped at the Si/dielectric interface [Figure 3a,b]. Subsequently, when the PWL_A is deactivated, the captured electrons are de-trapped. Most of the de-trapped electrons return to the SN_V , some move toward the BL or the bulk region [Figure 3c,d]. During this process, the potential of the SN_V increases, and when the PWL_A is repeatedly accessed, the stored data in the SN_V flip from '0' to '1'.

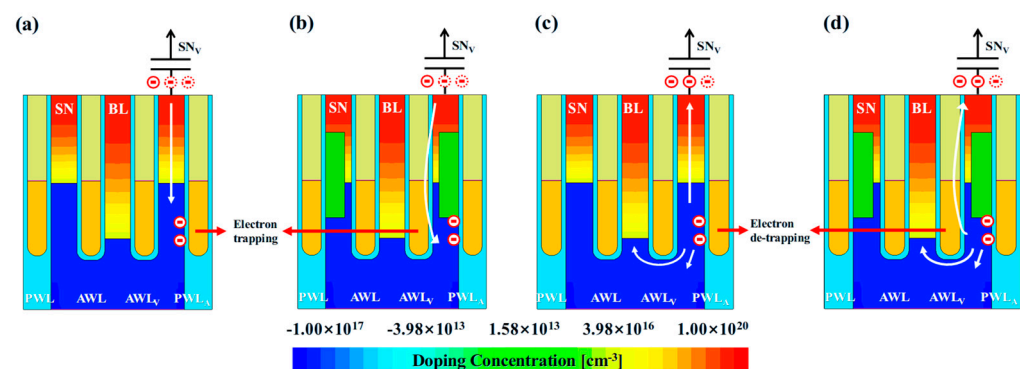


Figure 3. Schematic diagram of the D0 failure in DRAM operation. The arrows indicate the direction of electron migration.: (a) electrons emitted from the SN_V as the PWL_A is activated in the conventional BCAT and (b) in dielectric-embedded structure. (c) Trapped electrons in the Si/dielectric interface are either de-trapped to BL or SN_V as PWL_A is deactivated in the conventional BCAT and (d) in dielectric-embedded structure.

To verify the D0 failure using TCAD simulations, the PWL_A is repeatedly toggled in the low-*k*, SiO₂-embedded structures beneath the SN and in the conventional BCAT structure, followed by analysis of the resulting potential drops of SN_V . Figure 4a shows the variation in the data stored in the SN_V according to the PWL_A toggling.

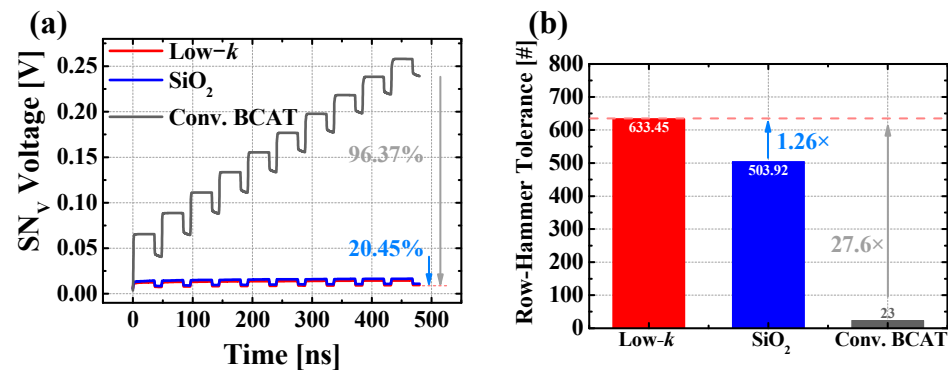


Figure 4. (a) Evolution of the victim SN voltage with increasing number of aggressor WL activations (up to 10 cycles) under D0 failure condition, comparing the proposed low- k -embedded structure, the SiO₂-embedded structure and the conventional BCAT structure. (b) Row-hammer tolerance calculated in the low- k , SiO₂-embedded and conventional BCAT structures.

The low- k -embedded structure exhibited approximately 20.45% and 96.37% smaller SN_V voltage variation than the SiO₂-embedded and the conventional BCAT structures, respectively. The row-hammer tolerance is defined as the number of toggles required for the SN_V voltage to reach half of the V_{CORE} , which corresponds to 0.55 V in this study. For D0 failure, it corresponds to the number of toggles needed for the SN_V voltage to rise from 0 V to 0.55 V. Based on the calculated SN variation (ΔV_{SN}) per toggle, row-hammer tolerance is obtained in the low- k , SiO₂-embedded and conventional BCAT structures. The low- k -embedded structure achieved approximately 1.26 times and 27.6 times higher row-hammer tolerance than the SiO₂-embedded and conventional BCAT structures, respectively [Figure 4b].

By analyzing the electron behavior with the toggling of the PWL_A, the cause of the mitigated RHE in the low- k -embedded structure under the D0 failure is identified. When the PWL_A is activated, electrons stored in the SN_V are emitted due to the electric field and then trapped at the Si/dielectric interface [Figure 5a–c]. The electron current density is lowest in the low- k -embedded structure, indicating that electrons emitted from the SN_V are effectively suppressed in the low- k -embedded structure. Subsequently, when the PWL_A is deactivated, the captured electrons are de-trapped, and while most of them return to the SN_V, some migrate toward the BL and the bulk region. It is also observed that the number of electrons migrating to the BL and the bulk region after being de-trapped is lowest in the low- k -embedded structure, confirming the alleviation of the RHE in the low- k -embedded structure [Figure 5d–f].

The mitigation of the electric field by the introduction of the low- k material is confirmed by analyzing the electric field distribution beneath the SN_V when the AWL_V is deactivated [Figure 6]. Since the carrier transport direction and current density are determined by the direction and magnitude of the electric field, the cut line was taken along the dominant current path. As the PWL_A is activated, both the number of electrons emitted from the SN_V and their migration paths after de-trapping are primarily governed by the electric field. In the low- k -embedded structure, the smallest electric field is formed beneath the SN_V, owing to the continuity condition of the electric field at the material interface derived from Gauss's law. This condition of the electric field at the material interface is expressed as follows.

$$\epsilon_{\text{Si}} E_{\text{Si}} = \epsilon_{\text{ins}} E_{\text{ins}} \quad (1)$$

$$E_{\text{Si,new}} = \frac{\epsilon_{\text{low-k}}}{\epsilon_{\text{ox}}} = \frac{2.8}{3.9} \approx 0.718 \quad (2)$$

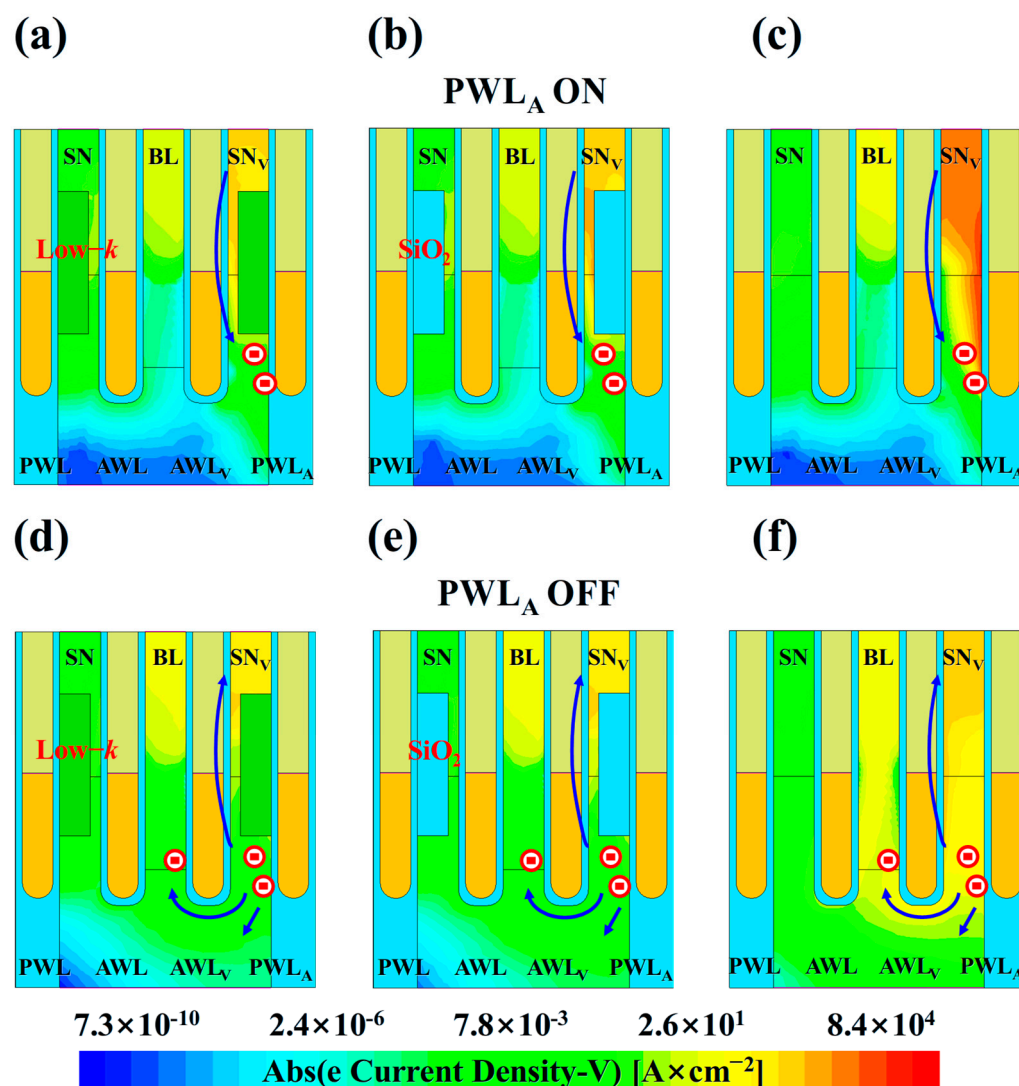


Figure 5. Electron current density distribution of the device in AWL off-state when (a) PWL_A is activated in the low-*k*, (b) SiO₂-embedded and (c) the conventional BCAT structure. Followed by when (d) PWL_A is deactivated in the low-*k*, (e) SiO₂-embedded and (f) the conventional BCAT structure. The arrows indicate the direction of electron migration.

The dielectric constant of the insulator used in this study is 2.8, and according to Equation (2), the electric field beneath the SN_V is expected to decrease by approximately 28%. The simulation results confirm that the electric field beneath the SN_V is reduced by up to 15.39%. Accordingly, when the PWL_A is activated, the electric field beneath the SN_V is lowest in the low-*k*-embedded structure, resulting in reduced electron pulled toward the PWL_A [Figure 6c]. The leakage of storage node induced by row-hammer is related to field enhancement. In this study, the carrier lifetime is determined by SRH recombination, and the Hurkx model is employed. The leakage current is proportional to an exponential term of the inverse electric field. Therefore, the mitigation rate of row hammer exceeds the relaxation rate of the electric field [35,36].

Furthermore, the conduction band energy distribution beneath the SN_V is analyzed [Figure 7]. When the PWL_A is activated, the conduction band energy is highest in the low-*k*-embedded structure [Figure 7c]. This indicates that electron emission from the SN_V is suppressed in the low-*k*-embedded structure. The difference in the conduction band energy suppresses the net charge loss of the SN_V during the toggling processes and efficiently alleviates the RHE.

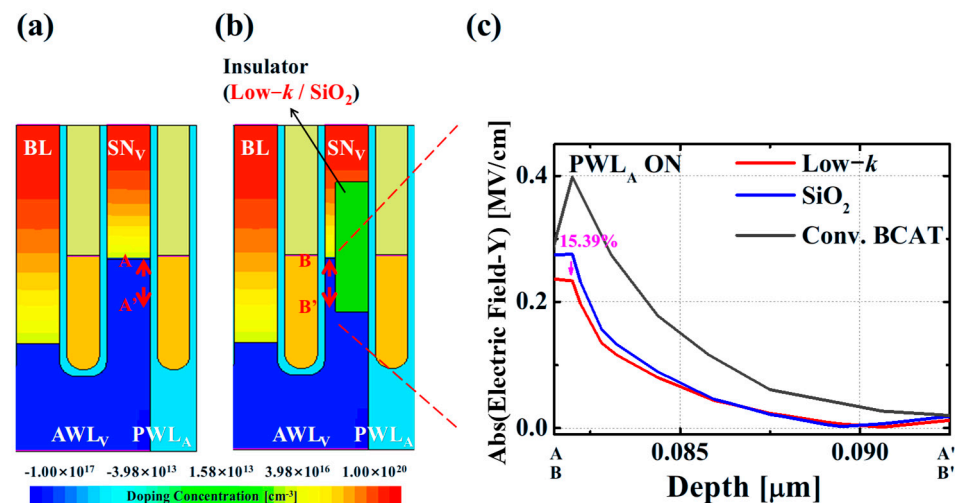


Figure 6. (a) Device structure with cut line A-A' in the conventional BCAT structure, (b) with cut line B-B' in the dielectric-embedded structure. (c) Electric-field distribution along the depth direction when PWL_A is ON in the low-*k*, SiO₂-embedded and conventional BCAT structures.

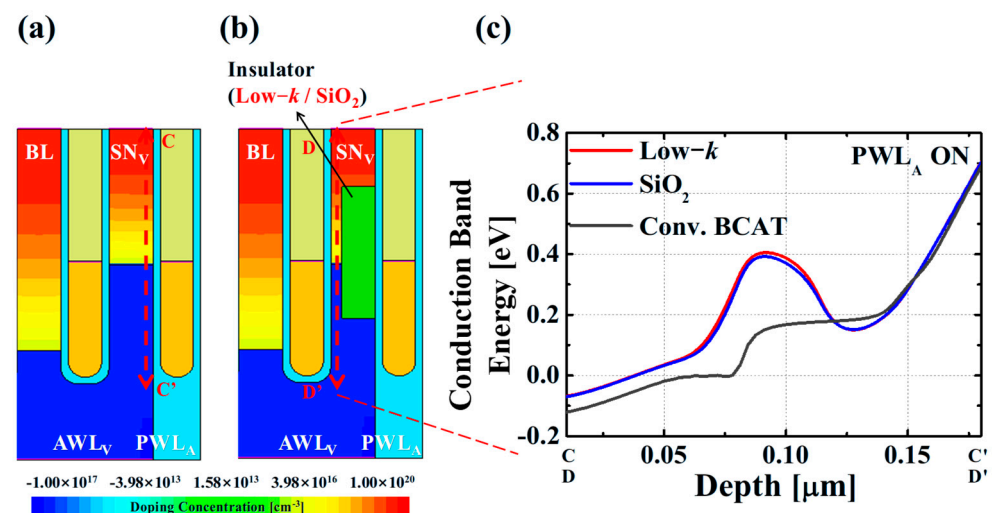


Figure 7. (a) Device structure with cut line C-C' in the conventional BCAT structure, (b) with cutline D-D' in dielectric-embedded structure. (c) Conduction band energy distribution along the depth direction when PWL_A is ON in the low-*k*, SiO₂-embedded and conventional BCAT structures.

Finally, the mitigation of the RHE by the low-*k* embedding is verified by analyzing the leakage current flow of the BL and the bulk with PWL_A access. When the PWL_A is activated, no current flows through the BL or the bulk, whereas transient current flow is observed at the falling edge of the PWL_A pulse [Figure 8]. This phenomenon verifies that the electrons trapped at the Si/dielectric interface are released through the de-trapping process when the PWL_A is deactivated. Compared to the conventional BCAT structure, the peak value of the BL current is reduced by approximately 57.27% and 65.37% in the SiO₂, low-*k*-embedded structures, respectively [Figure 8a]. In addition, the bulk current results indicate that embedding the dielectric effectively suppresses the leakage current flowing into the substrate [Figure 8b]. These results clearly confirm that the least data loss occurs in the low-*k*-embedded structure.

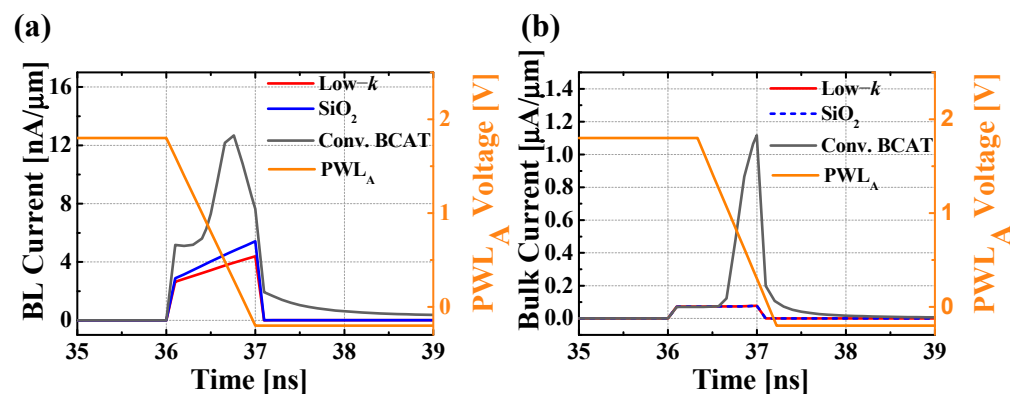


Figure 8. (a) BL current and (b) bulk current of the victim-cell in the falling edge of PWL_A access.

3.2. Alleviation of the D1 Failure

D1 failure occurs when the AWL acts as an aggressor, inducing a bit flip of the data '1' stored in the SN_V . The mechanism of D1 failure is shown in Figure 9. When data '1' are stored in the SN_V and data '0' are stored in the aggressor SN (SN_A), electrons in the SN_A are emitted due to the electric field when the aggressor AWL (AWL_A) is activated. The emitted electrons are then trapped at the Si/dielectric interface [Figure 9a,b]. Subsequently, when the AWL_A is deactivated, the captured electrons are de-trapped and migrate toward the BL, the bulk or SN_V . As the electrons migrate into the SN_V , recombination with the holes stored in the SN_V occurs, thereby decreasing the potential of the SN_V . As the AWL_A is repeatedly accessed, the data stored in the SN_V eventually flip from '1' to '0' [Figure 9c,d].

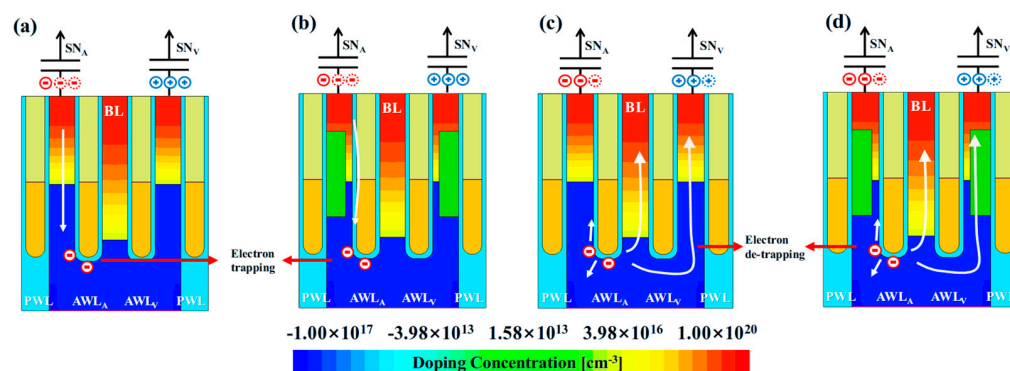


Figure 9. Schematic diagram of the D1 failure in DRAM operation: (a) electrons emitted from the SN_A as the AWL_A is activated in the conventional BCAT and (b) in dielectric-embedded structure. (c) Trapped electrons in the Si/dielectric interface are either de-trapped to BL or SN_V or substrate as AWL_A is deactivated in the conventional BCAT and (d) in dielectric-embedded structure.

The variation in the data stored in the SN_V due to AWL_A toggling is observed. When the AWL_A is toggled 10 times, the low- k -embedded structure exhibits approximately 12.12% and 34.09% smaller SN_V voltage variation than the SiO_2 -embedded and the conventional BCAT structures, respectively [Figure 10a]. As in the case of D0 failure, the row-hammer tolerance is evaluated as well, and it is confirmed that the low- k -embedded structure achieved approximately 1.14 times and 1.52 times higher row-hammer tolerance than the SiO_2 -embedded and conventional BCAT structures, respectively [Figure 10b]. Also, the electron behavior during AWL_A toggling is analyzed to identify the cause of the alleviation of the RHE in the D1 failure. When the AWL_A is activated, electrons stored in the SN_A are emitted by the electric field and trapped at the Si/dielectric interface [Figure 11a–c]. The electron current density is lowest in the low- k -embedded structure, indicating that electrons emitted from the SN_A are effectively suppressed in the low- k -embedded structure.

The electrons emitted from the SN_A and trapped at the Si/dielectric interface are de-trapped as the AWL_A is deactivated, and most of them migrate between the SN_A and the BL, while some move toward the SN_V and recombination with holes in SN_V occurs. It is also observed that the number of electrons migrating into the SN_V is lowest in the low- k -embedded structure, confirming the alleviation of the RHE in the low- k -embedded structure [Figure 11d–f].

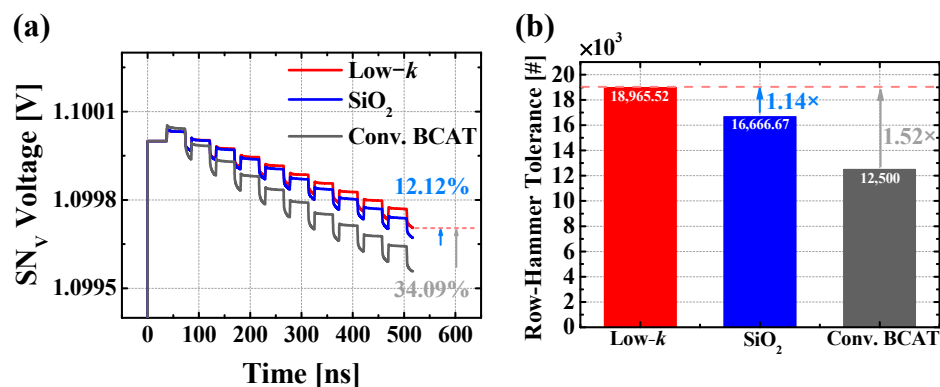


Figure 10. (a) Evolution of victim SN voltage with increasing aggressor WL activations (up to 10 cycles) under the D1 failure condition. The proposed low- k -embedded structure shows reduced ΔV_{SN} degradation compared to the SiO_2 -embedded and conventional BCAT structures. (b) Row-hammer tolerance calculated in low- k -, SiO_2 -embedded and conventional BCAT structures.

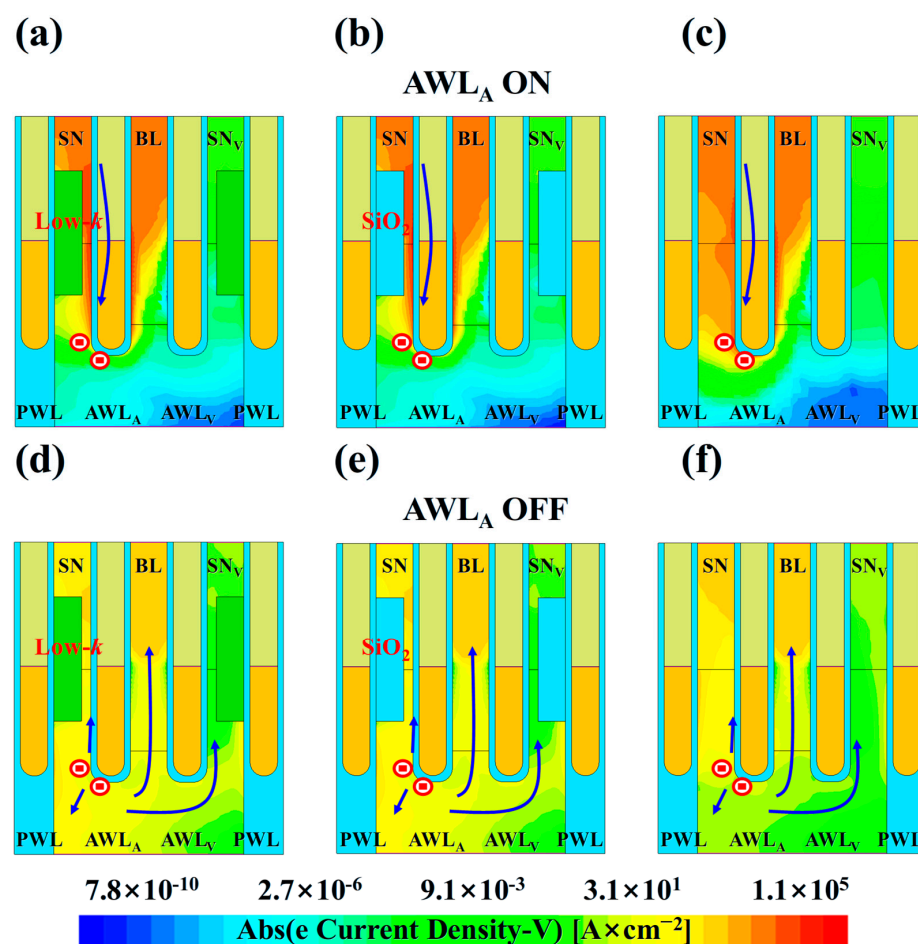


Figure 11. Electron current density distribution of the device when (a) AWL_A is activated in the low- k and (b) SiO_2 -embedded and (c) conventional BCAT structure and when (d) AWL_A is deactivated in the low- k and (e) SiO_2 -embedded and (f) conventional BCAT structure.

The electric field distribution beneath the SN_V when the AWL_V is deactivated confirms that the embedding of the low- k material effectively suppresses charge leakage [Figure 12]. When the AWL_A is activated, the electric field formed beneath the SN_A is weakened in the low- k -embedded structure, resulting in a reduced attractive force pulling electrons toward the AWL_A [Figure 12c]. When the AWL_A is deactivated, the electric field beneath the SN_V is weakened, thereby reducing electron migration toward the SN_V after de-trapping [Figure 12f].

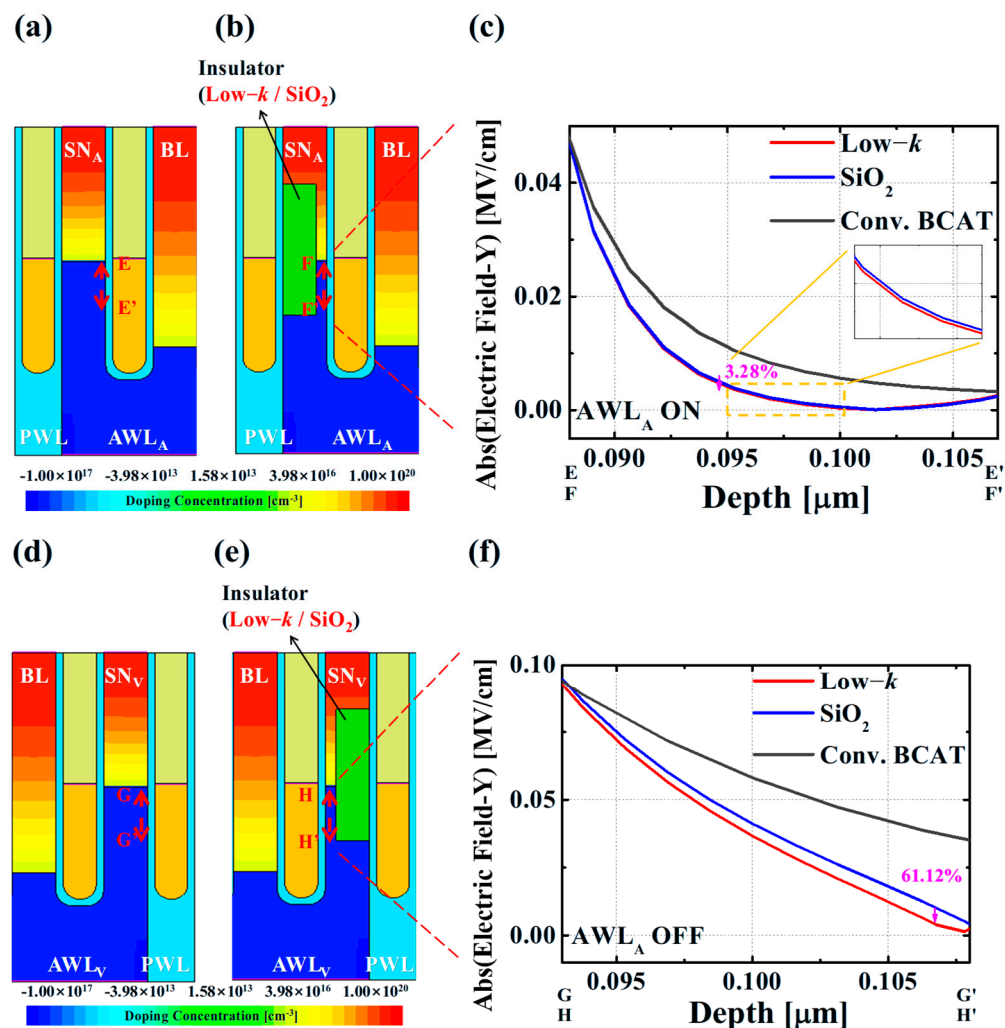


Figure 12. (a) Cross-sectional schematic of the device with the cut lines E-E' and (b) F-F'. (c) Electric-field distribution along the depth direction when AWL_A is ON in the low- k , SiO_2 -embedded and conventional BCAT structures beneath the SN_A . (d) Cross-sectional schematic of the device with the cut lines G-G' and (e) H-H'. (f) Corresponding distribution when AWL_A is OFF beneath the SN_V .

In addition, when the AWL_A is activated, the conduction band energy beneath the SN_A is highest in the low- k -embedded structure, indicating that electron emission from the SN_A is most suppressed in the low- k -embedded structure [Figure 13c]. Subsequently, when the AWL_A is deactivated, the conduction band energy beneath the SN_V is also highest in the low- k -embedded structure, which suppresses electron migration into the SN_V after de-trapping and consequently contributes to the alleviation of the RHE [Figure 13f]. Notably, the RHE mitigation effect in the D1 failure is relatively smaller than that in the D0 failure. This difference arises from the distinct failure mechanisms. In the D0 failure case, data flip occurs as electrons emitted from the SN_V are trapped and subsequently migrate toward the BL or the bulk after the de-trapping process. Therefore, the electric field has a

dominant influence on charge migration, and the reduction in the electric field achieved by embedding the low- k dielectric effectively suppresses electron movement, resulting in an excellent mitigation of the RHE. In contrast, D1 failure occurs as electrons emitted from the SN_A are trapped and subsequently migrate to the SN_V after de-trapping, where they recombine with the stored holes. That is, mechanism of D1 failure not only involves electron migration but also the recombination process with holes in the SN_V takes place. Therefore, reducing the electric field is relatively insufficient to fully suppress the overall mechanism, and the RHE mitigation in the D1 failure induced by the low- k embedding is relatively smaller than that observed in the D0 failure.

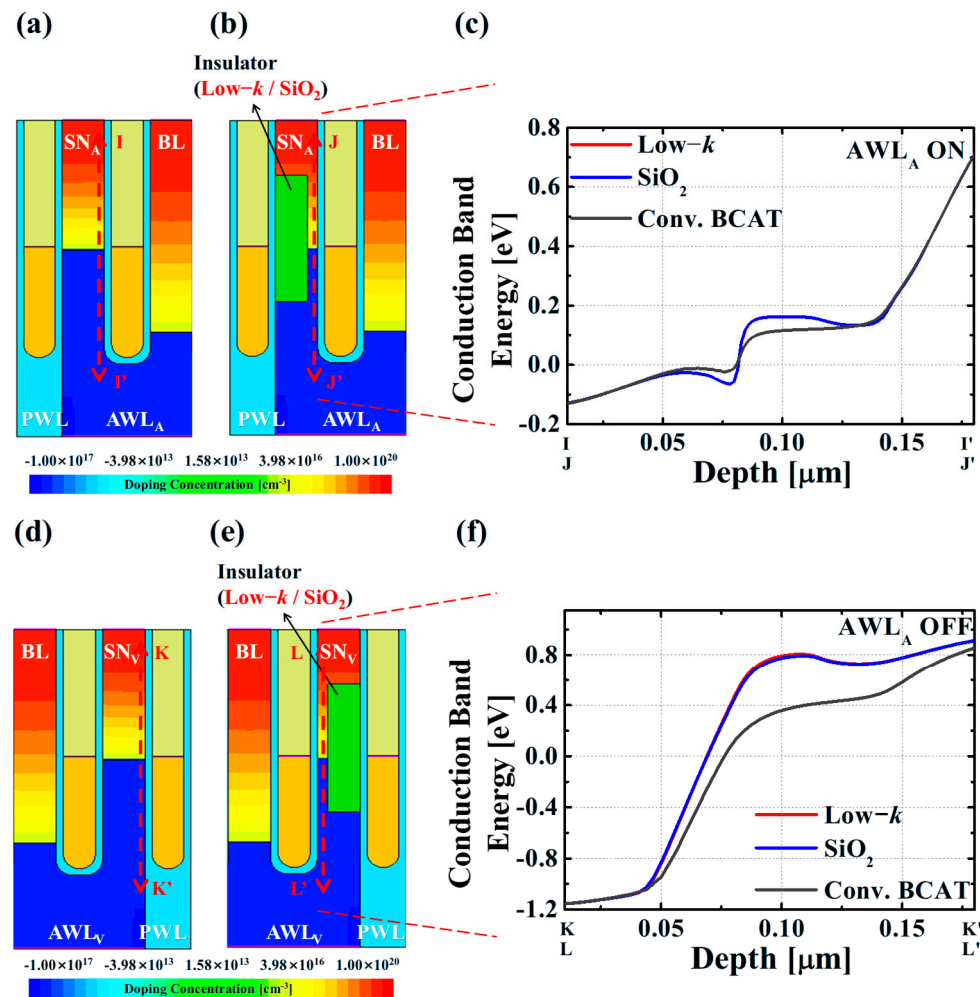


Figure 13. (a) Cross-sectional schematic of the device with the cut lines I-I' and (b) J-J'. (c) Conduction band energy profile along the depth direction when AWL_A is ON in the low- k , SiO_2 -embedded and conventional BCAT structures beneath the SN_A . (d) Cross-sectional schematic of the device with the cut lines K-K' and (e) L-L'. (f) Corresponding distribution when AWL_A is OFF beneath the SN_V .

3.3. Process Compatibility

The fabrication of the device proposed in this study can be achieved following the process flow of the Pi-BCAT [29]. A possible process flow for embedding the low- k dielectric is shown in Figure 14. First, the PWL trench patterning is performed through etching process [Figure 14a]. Steps 2–5 correspond to the process module for low- k dielectric embedding. A sacrificial layer is introduced to protect the trench sidewalls [Figure 14b]. Isotropic etching is then performed to create a cavity at the bottom of the trench for low- k dielectric deposition [Figure 14c] [37,38]. Then, the sacrificial layer is removed using an oxide wet cleaning process [Figure 14d]. The low- k dielectric is subsequently deposited

using atomic layer deposition (ALD) [Figure 14e]. The low- k material used in this work can exhibit a reduced dielectric constant when it becomes porous, but it may also become vulnerable to mechanical stress [39]. Therefore, conformal deposition is required.

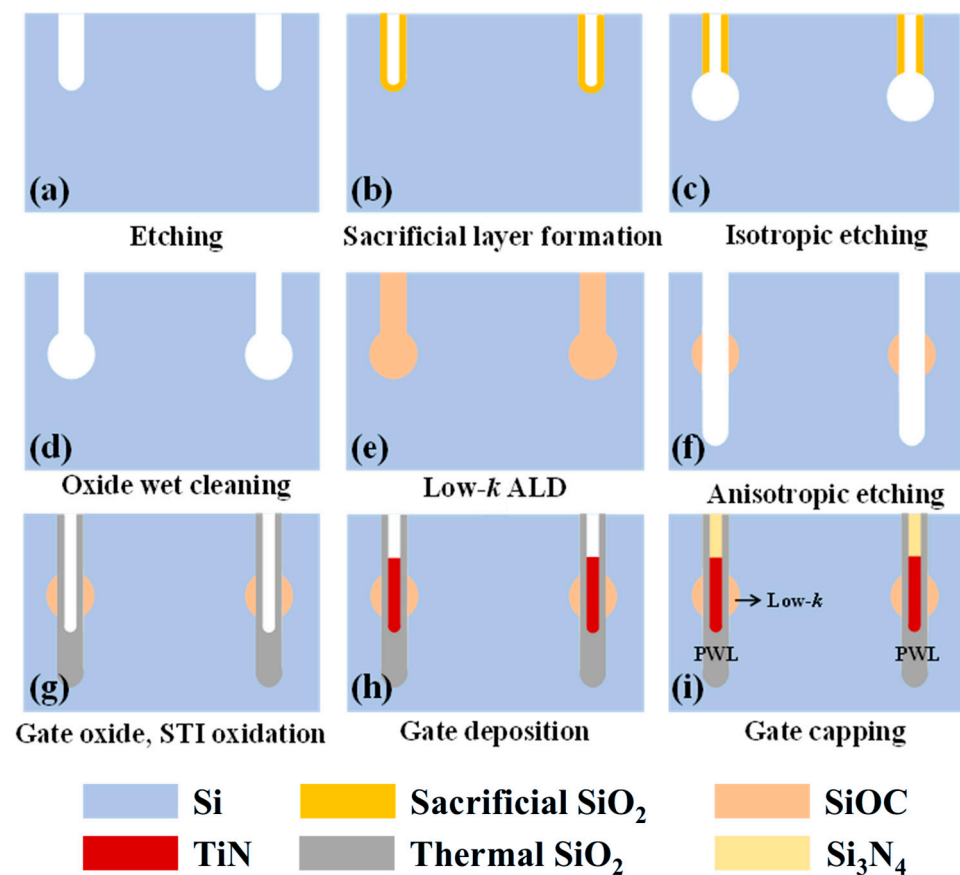


Figure 14. Process flow for the proposed buried low- k -embedded BCAT structure.

Anisotropic etching is subsequently carried out to achieve the target gate aspect ratio [Figure 14f]. After embedding low- k dielectric, oxidation for gate oxide and STI formation occurs [Figure 14g]. Finally, TiN gate deposition is then performed, followed by gate capping to form the BCAT structure [Figure 14h,i]. Figure 14 indicates that the proposed structure can be realized by adding only additional process modules (Steps 1–5) to the conventional BCAT process flow. In particular, the added process steps are confined to the PWL formation region, where they create the cavity for low- k dielectric embedding and fill it, while the process flow for AWL used for device operation remains identical to that of the conventional BCAT process. Therefore, the proposed structure can maintain compatibility with the current process flow while minimizing process modifications.

4. Conclusions

In this study, we demonstrate that embedding a low- k dielectric beneath the SN in the 6F² BCAT structure effectively mitigates the RHE. The proposed structure reduces the electric field between adjacent WL through the introduction of low- k material, thereby successfully alleviating the RHE-induced disturbance. Due to the electric-field continuity condition at material interfaces, the embedded low- k dielectric directly reduces the effective electric field applied to the bottom of the SN_v. This electric-field mitigation suppresses electron emission and charge trapping during aggressor WL operation and changes the local energy-band profile, thereby facilitating the return of leaked charge. In result, for the D0 failure, the electric field beneath the SN_v is reduced, suppressing the emission of electrons

stored in the SN_V , resulting in approximately 20.45% alleviation in D0 failure compared to the Pi-BCAT structure. In contrast, D1 failure involves a complex mechanism that extends beyond simple charge loss, including trapping, de-trapping, migration, and recombination processes. For the D1 failure, the proposed structure suppresses electron emission from the SN_A and reduces the electric field toward the SN_V , achieving a 12.12% alleviation in D1 failure compared to Pi-BCAT structure. Notably, the proposed low- k -embedded structure shows effective mitigation of the RHE disturbance caused by the PWL, exhibiting higher suppression efficiency for the D0 failure than the D1 failure. This is because the localized electric-field mitigation region introduced by the low- k dielectric spatially matches the dominant leakage and recovery paths. According to prior studies, the row-hammer phenomenon has been reported to be particularly vulnerable to disturbance when data '0' are stored. Given this background, the proposed structure effectively suppresses D0 failure, which is significant because it improves reliability under the most vulnerable operating condition. Additionally, despite ~11.7% degradation in on current in the low- k -embedded structure compared to the conventional BCAT structure, the $\times 27.6$ and $\times 1.52$ improvement in row-hammer tolerance in D0, D1 failure condition indicates that the reliability gain outweighs the performance degradation. As a result, the proposed low- k -embedded structure provides an effective structural design approach for fundamentally suppressing WL-to-WL disturbance, providing a promising basis for ensuring the reliability and stable operation of next-generation high-density, low-power DRAM devices.

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Abbreviations

The following abbreviations are used in this manuscript:

WL	Word line
RHE	Row-hammer effect
SN	Storage node
Pi-BCAT	Partial-isolation type buried channel array transistor
BCAT	Buried channel array transistor
ECC	Error correcting code
TRR	Target row refresh
PWL	Passing word line

BL	Bit line
AWL	Active word line
SN _V	Victim storage node
PWL _A	Aggressor passing word line
AWL _V	Victim active word line
AWL _A	Aggressor active word line
SN _A	Aggressor storage node

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