micromachines

MDPI

Article

A 5-nV/√Hz Chopper Negative-R Stabilization Preamplifier for Audio Applications

Jamel Nebhen [1,*], Khaled Alnowaiser [1] and Stephane Meillere [2]

[1] College of Computer Engineering and Sciences, Prince Sattam bin Abdulaziz University, P.O. Box 151, Alkharj 11942, Saudi Arabia; k.alnowaiser@psau.edu.sa

[2] Aix Marseille University, CNRS, IM2NP UMR 7334, 13451 Marseille, France; s.meillere@im2np.fr

* Correspondence: j.nebhen@psau.edu.sa

Received: 11 April 2020; Accepted: 1 May 2020; Published: 2 May 2020

Abstract: This paper presents a low-noise and low-power audio preamplifier. The proposed low-noise preamplifier employs a delay-time chopper stabilization (CHS) technique and a negative-R circuit, both in the auxiliary amplifier to cancel the non-idealities of the main amplifier. The proposed technique makes it possible to mitigate the preamplifier 1/*f* noise and thermal noise and improve its linearity. The low-noise preamplifier is implemented in 65 nm complementary metal-oxide semiconductor (CMOS) technology. The supply voltage is 1.2 V, while the power consumption is 159 μW, and the core area is 192 μm^2. The proposed circuit of the preamplifier was fabricated and measured. From the measurement results over a signal bandwidth of 20 kHz, it achieves a signal-to-noise ratio (SNR) of 80 dB, an equivalent-input referred noise of 5 nV/√Hz and a noise efficiency factor (NEF) of 1.9 within the frequency range from 1 Hz to 20 kHz.

Keywords: preamplifier; chopper stabilization; negative-R; CMOS operational transconductance amplifier (OTA); 1/f noise

1. Introduction

The Internet of Things (IoT) is now recognized by the industry, and in particular the electronics industry, as one of the main engines of growth for the decade to come, if not longer. The IoT refers to any application taking advantage of the networking of objects capable of interacting with their environment to measure key parameters of this environment, transmitting this data for analysis, sometimes in real time, and making decisions to control or optimize a system. Detection is the starting point for the IoT and smart home applications. It is also the first problem faced by maker followers and professional designers. The design of many economical transducers such as accelerometers, force sensors, extensometers and pressure transducers is based on resistive Wheatstone bridges for differential voltages in millivolts (mV). Before going into detail, it is essential to accurately capture these low-level signals and amplify them to levels compatible with analog-to-digital converters (ADCs), without DC offset or noise. Likewise, current detection using high potential ammeter shunts requires amplifiers without inputs referenced to ground, and capable of tolerating high common mode voltages. Micro-Electro-Mechanical Systems (MEMS) are sensors or actuators whose lateral dimensions and thickness are of the order of a micrometer. For decades, and still today, MEMS sensors have been manufactured on a large scale for many consumer applications, such as aerospace [1]; inertial sensors in mobile phones, such as gyrometers and accelerometers [2,3]; video game controllers; and airbag triggers. These devices, which are the basis of research tools [4], have reached a sufficient maturity to be directly developed and integrated by large industrial groups, such as STMicroelectronics [5].

In the world of transistors, it is known that the reduction of dimensions mainly makes it possible to integrate more devices on a given surface. Therefore, it enables a reduction of the manufacturing

cost of the transistor, to increase the performance of the integrated circuit and to reduce the operating voltage. Regarding sensors, reduced dimensions are other benefits that enabled the development of emerging applications. Therefore, since the 2000s, these sensors are reduced to the nanometer scale with the name "Nano-Electro-Mechanical Systems" (NEMS). These devices allow the study and detection of objects at the molecular scale [6,7] and also at the quantum scale [8]. The constant times are likewise reduced, which implies a limited response time, only because of the electronics control and not the NEMS itself. In addition, in the nanoscale era, we can see a modification in the intrinsic properties of materials as in silicon nanowires, and their thermal and conductive properties modified by the size effect. Hearing implants are technological devices developed to correct hearing loss. Today, the cochlear implant is the most complete system. It implements the fields of acoustics, electronics, signal processing and information, biology, and knowledge of the human physiology. The objective of the microphone is to transduce acoustic waves to an electrical signal. Consequently, it operates in the frequency range from 20 Hz to 20 kHz [9]. The low noise amplifier (LNA) is one of the key devices of an audio system. Located just after the audio sensor, the LNA receives a variety of low-level signals from this sensor. The LNA is placed on top of the audio conditioning chain. Therefore, it must reach a very important signal-to-noise ratio (SNR) output, to facilitate the processing of the audio signal information by the downstream components [10]. The major function of the LNA consists of amplifying the useful signal, while minimizing the noise contribution, and thus allowing the detection of signals at very low powers. Therefore, its linearity, selectivity, lower consumption and reduced surface require a very fine design [11].

There are three types of CMOS dynamic offset cancellation techniques: trimming, chopping, and auto-zeroing [12–14]. To eliminate offset during production, trimming technique is usually performed. Chopping involves modulating offset and 1/*f* noise to a chopping frequency, leaving only white noise in the base band. However, due to the up-modulated offset and 1/*f* noise, a chopper ripple appears at the amplifier's output. Auto-zeroing involves sampling the offset and low frequency 1/*f* noise on an auto-zero capacitor, and then subtracted in subsequent clock phases. However, the noise folding associated with sampling results in increased base band noise [15]. Thus, to achieve high power efficiency, chopping is the technique of choice, provided that associated ripple can be sufficiently suppressed. Chopper amplifiers are widely adopted in these systems for their advantageous low noise, high input impedance, and high common mode rejection ratio (CMRR). Various types of amplifiers for bio-potential measurements have been reported [16–23]. The amplifier reported in [17,18] used a capacitive feedback network and chopper modulation method with a DC servo loop for 1/*f* noise reduction, but it required a very large capacitor array, which significantly increased its die area [17]. The amplifier reported in [19,20] employed a chopper implemented inside of the feedback loop and thus suffered from CMRR reduction. The instrumentation amplifier reported in [21,22] overcame the CMRR reduction problem with an input impedance boosting loop that added the expense of extra circuitry.

In this paper, we present a high-linear chopper negative-R stabilization audio preamplifier, which employs two proposed techniques to reduce the 1/*f* noise and the thermal noise at the same time. The two proposed techniques are the delay-time chopper stabilization (CHS) technique [24,25] and the negative-R technique [26]. The paper is organized as follows. Section 2 analyses the delay-time chopper stabilization circuit. Section 3 analyses the chopper negative-R circuit. Section 4 describes the CMOS implementation of the LNA. Section 5 presents the simulation results. Finally, the conclusion is drawn in Section 6.

2. Analysis of the Delay-Time Chopper Stabilization Preamplifier

To reduce the input-equivalent noise of the preamplifier, we propose to use the well-known CHS technique. The CHS preamplifier circuit is shown in Figure 1 [27]. It is composed by the main amplifier, $A_{\text{main}}(s)$, and by the auxiliary amplifier, $A_{\text{aux}}(s)$. The non-idealities of $A_{\text{main}}(s)$ in low-frequency path are canceled by the $A_{\text{aux}}(s)$. Firstly, the input signal at $A_{\text{main}}(s)$ is measured by $A_{\text{aux}}(s)$. Then, the virtual

ground $V_X = V_{XP} - V_{XN}$ is derived toward zero by $A_{\text{aux}}(s)$. Therefore, a compensation voltage $V_Y = V_{YP} - V_{YN}$ is generated by the $A_{\text{aux}}(s)$ to the $A_{\text{main}}(s)$. The virtual ground V_X can be written as

$$V_X = \frac{V_{\text{OUT}}}{[A_{\text{main}}(s)\cdot(1 + A_{\text{aux}}(s))]}, \tag{1}$$

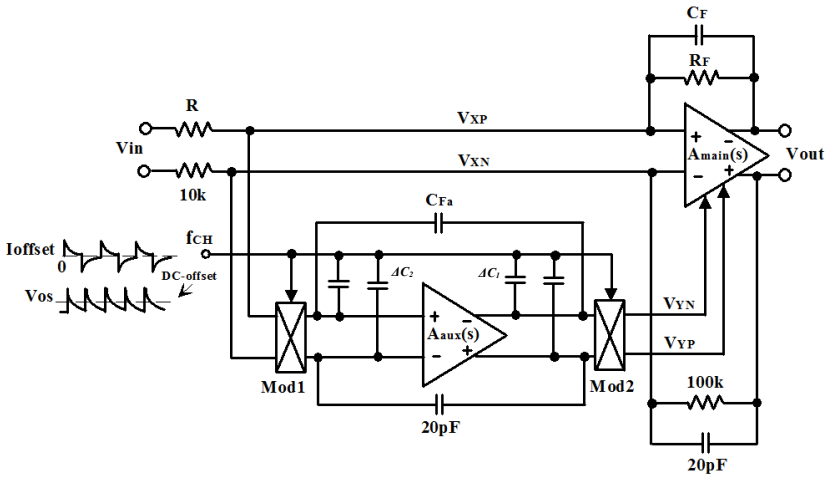

Figure 1. Chopper stabilization preamplifier.

Namely, the auxiliary amplifier allows attenuating the main amplifier noise portion as

$$v^2_{\text{n,main\_in}} = \frac{v^2_{\text{n,main0\_in}}}{\left|A_{\text{aux\_int}}(s)\right|^2}, \tag{2}$$

where $v^2_{n,\text{main\_in}}$ is the input noise of the main amplifier with the auxiliary amplifier and $v^2_{\text{n,main0\_in}}$ is the input noise of the main amplifier without the auxiliary amplifier. $A_{\text{aux\_int}}(s)$ represents the active RC-integrator signal transfer function (STF), which can be written as

$$A_{\text{aux\_int}}(s) = \frac{A_{\text{aux}}(s)}{[1 + sRC_{Fa}\cdot(1 + A_{aux}(s))]}. \tag{3}$$

The signal path mismatch and the demodulated current spikes generate a residual offset V_{os}. Therefore, AC current spike is caused by the mismatch between the capacitances, due to clock feed-through at the chopper clocks transition moments. The first modulator Mod1 rectify this AC current. Therefore, a DC spike current appears at its input. The resulting DC spike current has an average value I_{offset} of

$$I_{\text{offset}} = 2(\Delta C_1 - \Delta C_2)V_{\text{clk}}f_{\text{CH}}, \tag{4}$$

where ΔC_1 and ΔC_2 denote the CHS mismatch parasitic capacitance, V_{clk} denotes the clock signal magnitude, and f_{CH} denotes the Chopping clock frequency. The chopper series impedance and the input signal source are going through by this noise current. Therefore, it depicts as an input voltage spike. The residual offset V_{os} resulting from the spike average DC value can be written as

$$V_{\text{os}} = 2R(\Delta C_1 - \Delta C_2)V_{\text{clk}}f_{\text{CH}}, \tag{5}$$

where R denotes the equivalent input impedance. Therefore, a residual offset V_{os} depicts the spike average DC value. Moreover, a spike voltage V_{os} is created in the input of the Mod1. This spike voltage causes a low-frequency interference.

To cancel out this interference, we propose to create a proper delay Δt between Mod1 and Mod2. The proposed preamplifier CHS technique is shown in Figure 2. The auxiliary amplifier is located

between two modulating clock signals: m1(t) and m2(t) with period T. Moreover, we introduce a delay Δt between the two clock signals m1(t) and m2(t) at the same time. Due to the introduction of the delay Δt, this technique causes a chopping of the spike signal itself. Therefore, the DC content of the output signal V_{out}(t) is minimized. The residual output DC offset is completely cancelled if an optimum delay value Δt_{opt} exists, which can be written as

$$\Delta t_{\text{opt}} = \ln(2) \times \tau, \tag{6}$$

where $\tau = R \times C_{\text{in}}$ with R, and C_{in} denotes respectively the input resistance and the amplifier's input capacitance.

The major weakness of this technique is the τ itself, which not only depends on the amplifier's source resistance R, but also on its input capacitance C_{in}. The input preamplifier's spike signal is amplified and then multiplied with m2(t). The resulting output signal V_Y then contains, apart from higher order harmonics of the chopping frequency, a DC part or residual offset, which is due to chopping artifacts. To solve this problem, shaping of the spike can be introduced by the addition of a first order low-pass filter with time constant τ_c after $A_{\text{aux}}(s)$. We must have $T >> \tau_c >> \tau$ with T is the period of the square wave signal m1(t). The shape of the time response of the filtered spike is primarily determined by τ_c. Since the output offset is still linearly dependent on τ, the optimization of Δt_{opt} has been done in such a way that offset reduction is most effective for a worst-case preamplifier resistance. For our specific implementation $\Delta t_{\text{opt}}/\tau_c = 0.8$ has been chosen. The low-pass filter has a cut-off frequency of 300 kHz. The nominal chopping frequency f_{CH} is 120 kHz.

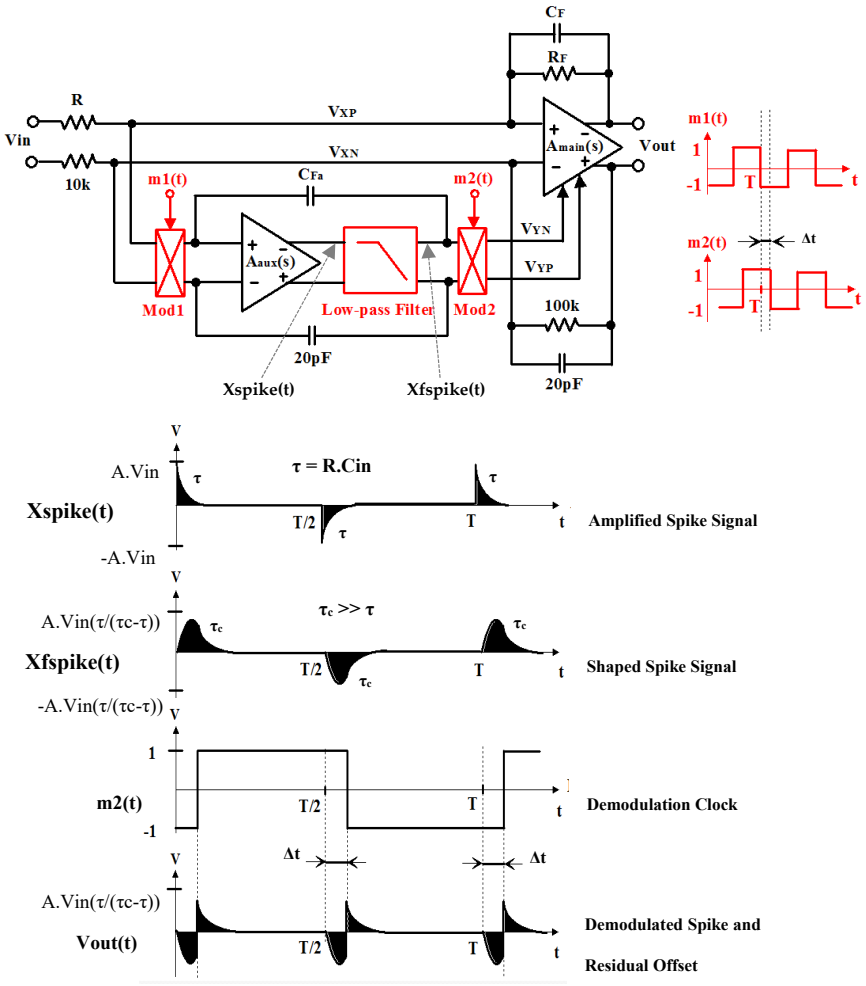

Figure 2. Delay-time chopper stabilization preamplifier.

3. Analysis of the Chopper Negative-R Stabilization Preamplifier

The delay-time chopper stabilization removes only the 1/*f* noise of the preamplifier. However, the chopper does not affect the $A_{aux}(s)$ thermal noise, and the overall noise level of the preamplifier is not reduced. Likewise, a large bandwidth of $A_{aux}(s)$ is required in order to keep its high gain at f_{CH}. To reduce both the 1/*f* noise and the thermal noise, we propose to use the chopper negative-R stabilization circuit as shown in Figure 3. This proposed technique allows removing the preamplifier non-ideality at V_X. It will compensate for the error current I_R and I_{RF} generated by R and R_F, respectively at V_X. Therefore, we choose the negative-R value in order to matching the value of the parallel resistors $R//R_F$. As a result, the chopper negative-R stabilization technique allows mitigating the V_X error. In the first case, the preamplifier noise is analyzed without the negative-R circuit. The overall main and auxiliary opamps noise transfer function (NTF) can be written as

$$\frac{v^2_{n,in}}{v^2_{n,opamps}} = \left(1 + \frac{R}{R_F}\right)^2 [1 + s(R \parallel R_F)C_F]^2, \tag{7}$$

where $v^2_{n,in}$ denotes the input-referred noise of preamplifier, and $v^2_{n,opamps}$ denotes the noise of opamps. The $v^2_{n,opamps}$ noise are calculated at the preamplifier input node. In the second case, the preamplifier noise is analyzed with the chopper negative-R circuit. The overall main and auxiliary opamps NTF becomes

$$\frac{v^2_{n,in}}{v^2_{n,opamps}} = \left(1 + \frac{R}{R_F}\right)^2 [1 + s(R \parallel R_F)C_F]^2 \left(\frac{\alpha - 1}{\alpha}\right)^2, \tag{8}$$

where the very important coefficient α denotes the negative-R matching coefficient of the parallel resistors $R//R_F$. If α becomes closer to 2, ideal compensation for $\alpha = 1$, the noise opamps decreases.

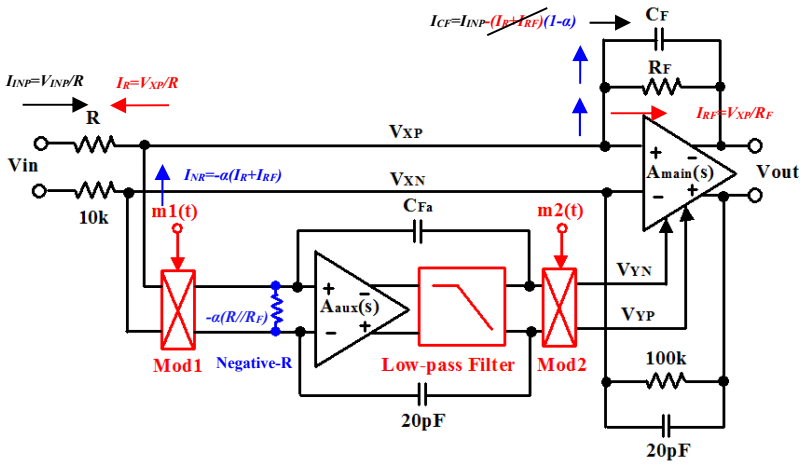

Figure 3. Chopper negative-R stabilization preamplifier.

However, the negative-R circuit adds an amount of noise of $2 \cdot (R/R_N) \cdot 4kTR_N$, with $R_N = -\infty (R \parallel R_F)$ in this case. As a result, the proposed negative-R preamplifier has an input-referred noise of

$$v^2_{n,in} = 2 \times \left[4kTR + 4kTR_F\left(\frac{R}{R_F}\right)^2\right] + |H(s)|^2 \times v^2_{n,opamps}, \tag{9}$$

where $|H(s)|^2$ denotes the NTF of the negative-R opamps of Equation (8). Therefore, the chopper negative-R circuit allows attenuating the opamps mismatch and offset.

4. CMOS Amplifier Implementation

If the amplifier is designed with a single-stage topology under low-voltage operation, then its output swing and its gain are limited. Usually, an amplifier with a two-stage topology, as shown in Figure 4, is used to increase the gain and the output swing. The first stage of the amplifier contributes to the total gain while the second stage contributes to enable a large output swing. The compensation capacitor (C_S) allows stabilizing the two-stage amplifier. In order to improve the frequency response, a resistor is connected in series with the capacitor C_S. Therefore, the amplifier receives a left half plane zero [28].

A desired gain-bandwidth (GBW) and a load capacitance (C_L) are considered to evaluate the amplifier power consumption. If all amplifier transistors have the same overdrive voltage $V_{OV} = V_{GS} - V_T$, and if the output non-dominant pole is at least three times of the GBW, then the current consumption $I_{two\text{-}stage}$ of the two-stage operational transconductance amplifier (OTA) can be written as [29,30].

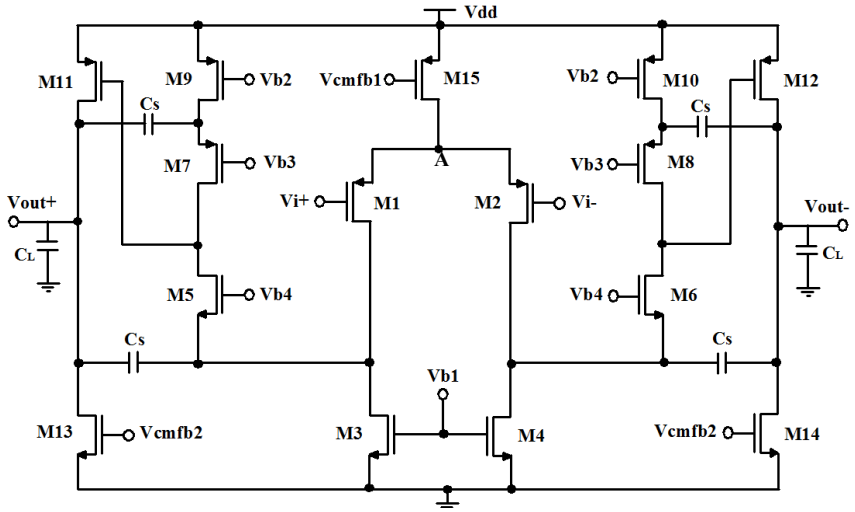

Figure 4. Folded-cascode operational transconductance amplifier (OTA) circuit.

$$I_{two-stage} = 2\pi \times GBW \times V_{OV} \times (4C_S + 3C_L). \quad (10)$$

From Equation (10), it is clear that the maximum of the current is used to drive the compensation capacitors.

Figure 4 shows the schematic of two-stage amplifier. The first stage is a differential OTA providing high gain, while the second stage is configured as a simple common-source stage to give maximum output swing. In contrast to cascode opamps, this topology isolates the gain and output swing requirements [29,30]. The DC-gain Ad and GBW expressions of the amplifier is given as

$$A_d = g_{m1}(r_{o1} \times r_{o2}) \times g_{m3}(r_{o3} \times r_{o11}), \quad (11)$$

$$GBW = \frac{g_{m1}g_{m3}(r_{o1} \times r_{o2})}{2\pi \times C_L}, \quad (12)$$

where g_{m1} and g_{m3} denote the transconductance of transistor M1 and M3, r_{01}, r_{02}, r_{03}, and r_{011} denote the output resistance of transistors M1, M2, M3, and M11, respectively. Assuming all the transistors have the same overdrive voltage, the transconductance g_m of M1 and M3 can be written as

$$g_{m1} = \frac{2I_{D1}}{V_{GS} - V_T}, \quad (13)$$

$$g_{m3} = \frac{2I_{D3}}{V_{GS} - V_T}, \tag{14}$$

where I_D denotes the drain current, V_T denotes the threshold voltage, and V_{GS} denotes the gate-source voltage of the MOSFET. Further, assuming all branches have the same current and ignoring parasitic capacitance at node A, Equation (12) can be modified as

$$GBW = \frac{g_m^2(r_{o1} \times r_{o2})}{2\pi \times C_L} = \frac{g_m^2}{2\pi \times C_L\left(\lambda_n + \lambda_p\right) \times I_D}, \tag{15}$$

where λ denotes the channel-length modulation parameter of the MOSFET. Combining Equations (13)–(15), the total current of the two-stage OTA is then

$$I_{two-stage} = GBW \times \pi \times (V_{GS} - V_T)^2 \times \left(\lambda_n + \lambda_p\right) \times (2C_L), \tag{16}$$

Since the parasitic capacitor at node A is negligible, for more power saving, the frequency compensation is performed by the load capacitance, and no miller compensation is used. The maximum output swing that this amplifier can achieve is $V_{DD} - |V_{overdrive4}| - V_{overdrive5}$. To achieve a higher signal swing, the overdrive voltage of transistors M4 and M5 are minimized in this design. The two-stage OTA has an open-loop gain of 65-dB, a phase margin of 62°, and a GBW of 16-MHz, with a power consumption of only 72-µW.

The noise sources of the CMOS operational amplifier originate from flicker noise and thermal noise components. The flicker noise component is usually larger than the thermal noise component for frequencies from 1 Hz to 20 kHz for a typical bias conditions and device geometries. The total noise current of a MOSFET is given as [30]

$$\frac{\overline{i_t^2}}{\Delta f} = \frac{K_F g_m^2}{C_{OX} WLf} + \frac{8KTg_m}{3}. \tag{17}$$

Neglecting the thermal noise contribution, the total noise current can be approximated as:

$$\frac{\overline{i_t^2}}{\Delta f} = \frac{K_F g_m^2}{C_{OX} WLf}, \tag{18}$$

with:

$$g_m = \sqrt{2\mu C_{OX} \frac{W}{L} I_D}, \tag{19}$$

where K_F is the flicker noise coefficient, g_m is the transconductance parameter of the MOSFET device, C_{OX} is the gate-oxide capacitance per unit area, W is the channel width, L is the channel length, f is the frequency, m represents the effective mobility, I_D is the drain current, and Δf is the bandwidth. Thus, the equivalent input-referred voltage noise can be written as:

$$\frac{\overline{v_{eq}^2}}{\Delta f} \approx \frac{K_F}{C_{OX} WLf}. \tag{20}$$

Noise analysis of the two-stage operational amplifier of Figure 4 yields

$$\frac{\overline{v_{eq}^2}}{\Delta f} \approx 2\left[\overline{v_{n1}^2} + \overline{v_{n3}^2}\left(\frac{g_{m3}}{g_{m1}}\right)^2\right]. \tag{21}$$

where $\overline{v_{n1}^2}$ denotes the thermal noise of transistor M1, and $\overline{v_{n3}^2}$ denotes the thermal noise of transistor M3. Substituting Equations (19) and (20) into Equation (21), we have

$$\frac{\overline{v_{eq2S}^2}}{\Delta f} \approx \frac{2K_F}{C_{OX}W_1 f}\left[\frac{1}{L_1} + \left(\frac{K_{F3\mu n}}{K_{F1\mu p}}\right)\cdot\frac{L_1}{L_3^2}\right], \tag{22}$$

where the symbols have their usual meanings, and the subscript n represents n-channel device, and subscript p represents p-channel device. It is apparent from Equation (22) that there exists a minimum as L_1 varies. For very low values of L_1, the first term is dominant, whereas for large L_1 values, the second term is dominant. Although the low-noise design practice adapts long channel length L_3 for active load and short channel length L_1 for good phase margin.

The transistor-level circuit of the negative-R is shown in Figure 5. It is implemented in a topology of MOSFET source-degeneration. It consumes only 12-µW. In this topology, the degeneration resistor and the current source allows enhancing the accuracy of matching the circuit within 10%. Moreover, a stable g_m of the negative-R is maintained over the temperature and power supply variations [26].

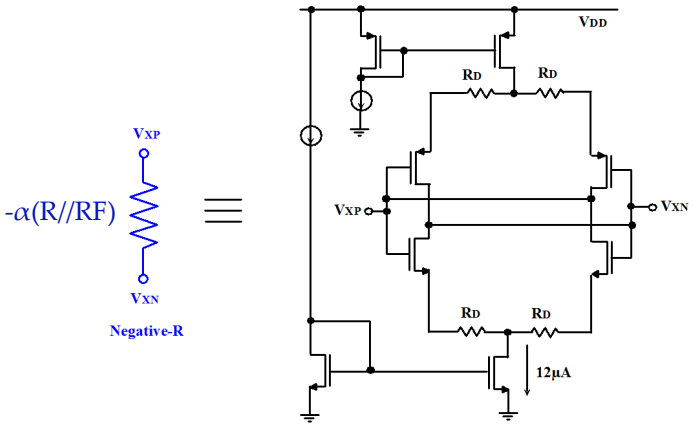

Figure 5. Negative-R circuit.

5. Measurement Results

Prototypes of the low-noise preamplifier are fabricated and experimentally characterized. The die microphotograph of the preamplifier is shown in Figure 6. The measurement result of the preamplifier input-referred noise with CHS circuit and with chopper negative-R circuit is shown in Figure 7. The preamplifier has a bandwidth of 20 kHz. From measurement result, if the preamplifier is with CHS circuit, then its input-referred noise is 11 nV/√Hz. If the preamplifier is with chopper negative-R circuit, then its input-referred noise is almost limited by the R, R_F, and negative-R thermal noise and it is attenuated to 5 nV/√Hz. Moreover, it is clear from measurement result that the chopper negative-R circuit allows to mitigate the opamps 1/*f* noise and thermal noise. As a result, the proposed chopper negative-R stabilization preamplifier allows a noise reduction of 2.2 times, compared to the conventional preamplifier. The curves in Figure 8 show the SNR of the preamplifier as a function of the power consumption. Simulation results have been added for comparison. It appears that the evolution of the experimentally measured SNR is consistent with that obtained with the simulation results. The maximum measured SNR is 80 dB. This value is nearly the same as the simulation result. It is obtained for a current of 132 µA. It corresponds to a power consumption of 159 µW.

Figure 6. Chip microphotograph of the proposed chopper negative-R stabilization preamplifier in 65 nm CMOS process with an area of 192 μm^2.

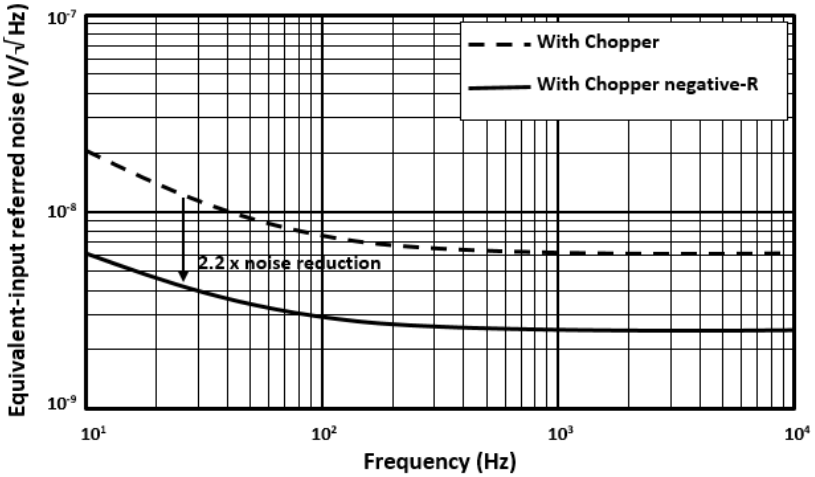

Figure 7. Equivalent-input referred noise of the proposed chopper negative-R stabilization preamplifier.

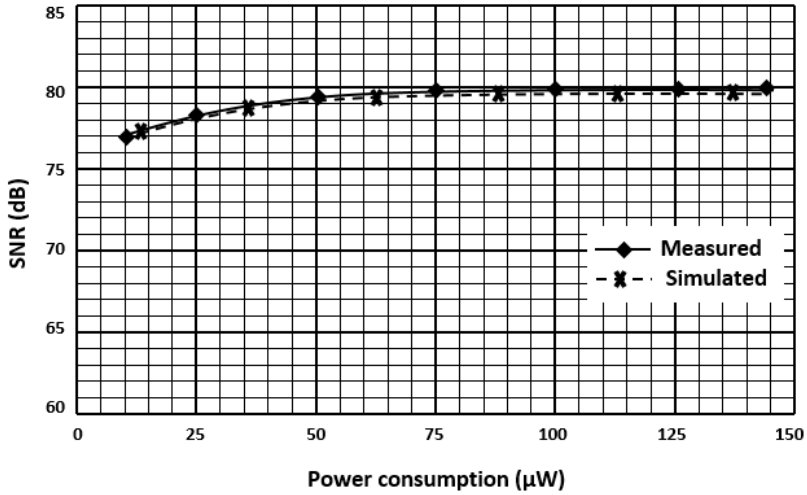

Figure 8. Signal-to-noise ratio (SNR) of the proposed chopper negative-R stabilization preamplifier versus power consumption.

The measurement results of the proposed low-noise preamplifier and the comparison with other amplifiers is reported in Table 1. A fundamental parameter is used to evaluate the overall power efficiency of the preamplifier. This parameter is the noise efficiency factor parameter (NEF), which can be written as [31]

$$NEF = V_{\text{rms}} \sqrt{\frac{2 \times I_{\text{total}}}{\pi \times U_{\text{th}} \times 4\text{kT} \times BW}}, \quad (23)$$

where I_{total} is the total current consumption, V_{rms} is the root-mean square (RMS) input-referred noise, U_{th} is the thermal voltage, and BW is the bandwidth of the preamplifier. From Equation (23), it is clear that the NEF parameter includes almost every performance shown in Table 1, namely the equivalent-input referred noise, the power consumption, the bandwidth and indirectly the power-supply rejection ratio (PSRR), and the common-mode rejection ratio (CMRR). In [32,33], the preamplifier has a high CMRR and high PSRR. However, it has also a high equivalent-input referred noise at list of about 18 nV/$\sqrt{\text{Hz}}$. In [22,23], the measured preamplifier has a low CMRR and low PSRR. Moreover, it has a worse equivalent-input referred noise at least 47 nV/$\sqrt{\text{Hz}}$. Therefore, this noise level affects drastically the preamplifier and degrades its performances. As a result, all compared preamplifiers have an equivalent-input referred noise greater than 18 nV/$\sqrt{\text{Hz}}$. On the other hand, our measured preamplifier has a high CMRR and high PSRR. Moreover, it has the lowest equivalent-input referred noise of only 5 nV/$\sqrt{\text{vHz}}$. As a result, for the same performances, our preamplifier has a good tradeoff between the supply voltage, the PSRR, and the CMRR. Our proposed circuit achieves a NEF of 1.9, a PSRR of 110 dB and a CMRR of 121 dB. Therefore, it proves a competitive performance compared to the state-of-the art.

Table 1. Performances Comparison of the Proposed Preamplifier with the State-of-the Art.

Specifications	**[32]**	**[33]**	**[23]**	**[22]**	**This Work**
Technology, nm	180	320	130	40	65
Supply, V	3.3	3.3	1.2	1.2	1.2
Power, µW	558	561	3	2	159
CMRR, dB	162	120	85	87	121
PSRR, dB	111	115	-	-	110
Bandwidth, kHz	59	40	5	20	20
Technique of noise reduction	Chopper	Chopper	Chopper	Chopper	Chopper-negative R
Noise, nV/$\sqrt{\text{Hz}}$	28.3	18	47	110	5
NEF	4.2	10.6	3.9	4.9	1.9

6. Conclusions

Two proposed techniques to reduce 1/*f* noise, thermal noise and power consumption of an audio preamplifier are presented in this paper. The preamplifier includes a chopper negative-R stabilization preamplifier, which employs a delay-time chopper stabilization and a negative-R circuit both in the auxiliary amplifier path to cancel the non-idealities of the main amplifier. The low-noise preamplifier is implemented in a 65 nm CMOS technology. The supply voltage is 1.2 V while the power consumption is 159 µW and the core area is 192 µm^2. The low-noise preamplifier was fabricated and measured. From measurement results over a signal bandwidth of 20 kHz, the proposed preamplifier achieves an SNR of 80 dB, and an equivalent input-referred noise of 5 nV/$\sqrt{\text{Hz}}$. The proposed chopper negative-R stabilization technique mitigates the requirements including thermal noise, 1/*f* noise, and linearity, thus reducing the power dissipation of the preamplifier.

Author Contributions: Conceptualization, J.N. and K.A.; methodology, J.N.; validation, J.N., K.A. and S.M.; formal analysis, J.N.; investigation, K.A.; resources, S.M.; writing—original draft preparation, J.N.; writing—review and editing, J.N.; supervision, J.N.; All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Acknowledgments: This project was supported by the Deanship of Scientific Research at Prince Sattam Bin Abdulaziz University under the research project 2017/01/6899.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Barbour, N.; Hopkins, R.; Kourepenis, A.; Ward, P. Inertials MEMS systems and applications. *Lect. NATO Sci. Technol. Organ.* **2011**, *116*, 1–18.
2. Yazdi, N.; Ayazi, F.; Najafi, K. Micromachined inertial sensors. *Proc. IEEE* **1998**, *86*, 1640–1659. [CrossRef]
3. Bell, D.J.; Lu, T.J.; Fleck, N.A.; Spearing, S.M. MEMS actuators and sensors: Observation on their performance and selection for purpose. *J. Micromech. Microeng.* **2005**, *15*, 153–164. [CrossRef]
4. Duraffourg, L.; Laurent, L.; Moulet, J.; Arcamone, J.; Yon, J. Array of Resonant Electromechanical Nanosystems: A Technological Breakthrough for Uncooled Infrared Imaging. *Micromachines* **2018**, *9*, 401. [CrossRef]
5. Yole Developpement. *Technology Trends for Inertial MEMS*; Cision PR Newswire: New York, NY, USA, 2012; pp. 1–12.
6. Li, M.; Tang, H.X.; Roukes, M.L. Ultra-sensitive NEMS-based cantilevers for sensing, scanned probe and very high frequency applications. *Nat. Nanotechnol.* **2007**, *2*, 114–120. [CrossRef]
7. Naik, A.K.; Hanay, M.S.; Hiebert, W.K.; Feng, X.L.; Roukes, M.L. Towards single-molecule nanomechanical mass spectrometry. *Nat. Nanotechnol.* **2009**, *4*, 445–450. [CrossRef]
8. Keith, S.C.; Roukes, C.L. Putting mechanics into quantum mechanics. *Phys. Today* **2005**, *58*, 36–42.
9. Kitchin, C.; Counts, L. *A Designer's Guide to Instrumentation Amplifiers*; Analog Devices: Norwood, MA, USA, 2006.
10. Mehta, N.; Huijsing, J.H.; Stojanovic, V. A 1-mW Class-AB Amplifier with -101 dB THD+N for High Fidelity 16 Ω Headphones in 65-nm CMOS. *IEEE J. Solid State Circuits* **2019**, *54*, 948–958. [CrossRef]
11. Lee, J.; Lee, K.R.; Ha, U.; Kim, J.H.; Lee, K.; Gweon, S.; Jang, J.; Yoo, H.J. A 0.8-V 82.9-μ W In-Ear BCI Controller IC with 8.8 PEF EEG Instrumentation Amplifier and Wireless BAN Transceiver. *IEEE J. Solid State Circuits* **2019**, *54*, 1185–1195. [CrossRef]
12. Michiel, A.P.; Pertijs, M.; Kindt, W.J. A 140-dB CMRR current-feedback instrumentation amplifier employing ping-pong auto-zeroing and chopping. *IEEE J. Solid State Circuits* **2010**, *45*, 2044–2056.
13. Wu, J.; Law, M.K.; Martins, R.P. A 2-lW 45-nV/HHz readout front end with multiple-chopping active-high-pass ripple reduction loop and pseudo-feedback DC servo loop. *IEEE Trans. Circuits Syst. II* **2016**, *63*, 351–355. [CrossRef]
14. Wu, R.; Huijsing, J.H.; Makinwa, K.A.A. A chopper current-feedback instrumentation amplifier with a 1 mHz 1/f noise corner and an AC-coupled ripple-reduction loop. *IEEE J. Solid State Circuits* **2009**, *44*, 3232–3243. [CrossRef]
15. Enz, C.C.; Temes, G.C. Circuit techniques for reducing the effects of op-amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization. *Proc. IEEE* **1996**, *84*, 1584–1614. [CrossRef]
16. Luo, D.; Zhang, M.; Wang, Z. A Low-Noise Chopper Amplifier Designed for Multi-Channel Neural Signal Acquisition. *IEEE J. Solid State Circuits* **2019**, *54*, 2255–2265. [CrossRef]
17. Denison, T.; Consoer, K.; Santa, W.; Avestruz, A.T.; Cooley, J.; Kelly, A. A 2 μW 100 nV/√Hz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials. *IEEE J. Solid State Circuits* **2007**, *42*, 2934–2945. [CrossRef]
18. Yeager, D.; Zhang, F.; Zarrasvand, A.; George, N.T.; Daniel, T.; Otis, B.P. A 9 μA addressable Gen2 sensor tag for biosignal acquisition. *IEEE J. Solid State Circuits* **2010**, *45*, 2198–2209. [CrossRef]
19. Verma, N.; Shoeb, A.; Bohorquez, J.; Dawson, J.; Guttag, J.; Chandrakasan, A.P. A micro-power EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system. *IEEE J. Solid State Circuits* **2010**, *45*, 804–816. [CrossRef]
20. Abdelhalim, K.; Jafari, H.M.; Kokarovtseva, L.; Velazquez, J.L.P.; Genov, R. 64-channel UWB wireless neural vector analyzer SOC with a closed-loop phase synchrony-triggered neurostimulator. *IEEE J. Solid State Circuits* **2013**, *48*, 2494–2510. [CrossRef]
21. Fan, Q.; Sebastiano, F.; Huijsing, H.; Makinwa, K.A.A. A 1.8 μW 60 nV/√Hz capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes. *IEEE J. Solid State Circuits* **2011**, *46*, 1534–1543. [CrossRef]
22. Chandrakumar, H.; Markovi¢, D. A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation. *IEEE J. Solid State Circuits* **2017**, *52*, 645–656. [CrossRef]

23. Zheng, J.; Ki, W.H.; Hu, L.; Tsui, C.Y. Chopper capacitively coupled instrumentation amplifier capable of handling large electrode offset for biopotential recordings. *IEEE Trans. Circuits Syst. II Express Briefs* **2017**, *63*, 1392–1396. [CrossRef]
24. Lee, H.S.; Nguyen, V.N.; Pham, X.L.; Lee, J.W.; Park, H.K. A 250-μW, 18-nV/√Hz current-feedback chopper instrumentation amplifier in 180-nm CMOS for high-performance bio-potential sensing applications. *Analog Circuits Signal Process.* **2017**, *90*, 137–148. [CrossRef]
25. Nebhen, J.; Ferreira, P.M.; Mansouri, S. A chopper stabilization audio instrumentation amplifier for IoT applications. *J. Low Power Electron. Appl.* **2020**, *10*, 13. [CrossRef]
26. Jang, M.; Lee, C.; Chae, Y. Analysis and design of low power continuous-time Delta-Sigma modulator using negative R assisted integrator. *IEEE J. Solid State Circuits* **2019**, *54*, 277–287. [CrossRef]
27. Burt, R.; Zhang, J.A. Micropower chopper-stabilized operational amplifier using a SC notch filter with synchronous integration inside the continuous-time signal path. *IEEE J. Solid State Circuits* **2006**, *41*, 2729–2736. [CrossRef]
28. Gray, P.R.; Meyer, R.G. *Analysis and Design of Analog Integrated Circuits*, 2nd ed.; Wiley: New York, NY, USA, 1984; pp. 750–752.
29. Nebhen, J.; Masmoudi, M.; Rahajandraibe, W.; Aguir, K. High DC-gain Two-Stage OTA Using Positive Feedback and Split-Length Transistor Techniques. In *Advances in Data Science, Cyber Security and IT Applications. ICC, Communications in Computer and Information Science*; Alfaries, A., Mengash, H., Yasar, A., Shakshuki, E., Eds.; Springer: Cham, Switzerland, 2019; Volume 1098.
30. Nebhen, J.; Savary, E.; Rahajandraibe, W.; Dufaza, C.; Meillere, S.; Kussener, E.; Barthelemy, H.; Czarny, J.; Lhermet, H. Low-noise CMOS amplifier for readout electronic of resistive NEMS audio sensor. In Proceedings of the 2014 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP), Cannes, France, 1–4 April 2014.
31. Harrison, R.; Charles, C. A low-power low-noise CMOS amplifier for neural recording applications. *IEEE J. Solid State Circuits* **2003**, *38*, 958–965. [CrossRef]
32. Kwon, Y.; Kim, H.; Kim, J.; Han, K.; You, D.; Heo, H.; Cho, D.; Ko, H. Fully Differential Chopper-Stabilized Multipath Current-Feedback Instrumentation Amplifier with R-2R DAC Offset Adjustment for Resistive Bridge Sensors. *Appl. Sci.* **2019**, *10*, 63. [CrossRef]
33. Butti, F.; Piotto, M.; Bruschi, P. A Chopper Instrumentation Amplifier with Input Resistance Boosting by Means of Synchronous Dynamic Element Matching. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 753–794. [CrossRef]