



Communication

Broadband High-Efficiency Grating Couplers for Perfectly Vertical Fiber-to-Chip Coupling Enhanced by Fabry-Perot-like Cavity

Zan Zhang ^{1,*} , Beiju Huang ², Zanyun Zhang ³, Chuantong Cheng ², Bing Bai ¹, Tianxi Gao ¹, Xiaobo Xu ¹ , Wenping Gu ¹, Lin Zhang ¹ and Hongda Chen ²

¹ School of Electronics and Control Engineering, Chang'an University, Xi'an 710064, China; baibing@chd.edu.cn (B.B.); tianxigao@chd.edu.cn (T.G.); xuxiaobo@chd.edu.cn (X.X.); wpgu@chd.edu.cn (W.G.); zhanglin_dk@chd.edu.cn (L.Z.)

² State Key Laboratory on Integrated Optoelectronics, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, China; bjhuang@semi.ac.cn (B.H.); chengchuantong@semi.ac.cn (C.C.); hdchen@semi.ac.cn (H.C.)

³ School of Electronics and Information Engineering, Tianjin Polytechnic University, Tianjin 300387, China; zhangzanyun@tjpu.edu.cn

* Correspondence: z.zhang@chd.edu.cn

Received: 14 August 2020; Accepted: 16 September 2020; Published: 17 September 2020



Abstract: We propose a broadband high-efficiency grating coupler for perfectly vertical fiber-to-chip coupling. The up-reflection is reduced, hence enhanced coupling efficiency is achieved with the help of a Fabry-Perot-like cavity composed of a silicon nitride reflector and the grating itself. With the theory of the Fabry-Perot cavity, the dimensional parameters of the coupler are investigated. With the optimized parameters, up-reflection in the C-band is reduced from 10.6% to 5%, resulting in an enhanced coupling efficiency of 80.3%, with a 1-dB bandwidth of 58 nm, which covers the entire C-band. The minimum feature size of the proposed structure is over 219 nm, which makes our design easy to fabricate through 248 nm deep-UV lithography, and lowers the fabrication cost. The proposed design has potential in efficient and fabrication-tolerant interfacing applications, between off-chip light sources and integrated chips that can be mass-produced.

Keywords: silicon photonics; grating coupler; Fabry-Perot cavity; photonic integrated circuit

1. Introduction

Benefitting from mature complementary metal-oxide-semiconductor (CMOS) technology, various photonic devices have been demonstrated based on low loss silicon-on-insulator (SOI) waveguides, showing great promise for electronic-photonic integrated circuits, high-density photonic integrated circuits (PICs), and three-dimensional (3D) photonic integration [1–5]. Grating couplers (GCs) enable optical coupling between standard single-mode optical fiber and high index contrast SOI waveguides, and have gained widespread usage as fiber-to-chip couplers for SOI PICs [6–8]. Compared to edge couplers, GCs enable position-friendly interfacing of silicon chips by optical fibers so that wafer-scale optical measurements can be performed without dicing [8,9].

In the past, much effort has been devoted to the design and optimization of GCs [10–13] for interfacing between single mode fiber and silicon photonic chips. However, off-normal GCs couple light from tilted fiber (usually $\sim 10^\circ$), to avoid second-order reflection [10], which is disadvantageous for rapid wafer-scale tests and low-cost photonic packaging [8]. Therefore, perfectly vertical GCs are appealing, as they facilitate easier alignment and packaging processes.

Perfectly vertical GCs, with increased coupling efficiency, (CE) have been widely explored over the past decade. Various approaches have been proposed, including employing slanted grating [14], chirping the GC [15–17], relying on a tilted silicon membrane structure [18,19], adding an anti-back reflection structure [20–22], and employing a dual-layer grating structure [23–25]. However, the above reported high-efficiency approaches require either extra fabrication processes or sophisticated device structure, with a minimum feature size below 200 nm, which increases the fabrication cost drastically, and affects the fabrication error tolerance.

In this work, by taking advantage of silicon nitride (Si_3N_4) material and the idea of Si-overlay for a GC, we present a broadband high-efficiency bidirectional perfectly vertical GC, with numerical demonstration. The bidirectional GC functions as both a fiber coupler and a 3-dB optical power splitter, so that it can, not only act as a highly efficient fiber-to-chip coupler, but also work in Mach–Zehnder interferometer based optical components [26,27]. Si-overlay on GC is utilized to increase directionality [7]. A Fabry-Perot-like cavity, composed of the Si_3N_4 layer and the grating itself, is introduced into the coupler to suppress the light back-reflected into the launching fiber, thus enhancing the coupling into the on-chip waveguides. Numerical calculations based on the finite-difference time-domain (FDTD) were implemented to determine the dimensional parameters. With the help of the Fabry-Perot-like cavity, reflection back towards the fiber is decreased to 5%, and an enhanced CE of 80.3% is achieved. In addition, since there are fewer grating periods than most other designs, the proposed GC shows a 58 nm-wide 1-dB bandwidth that covers the whole C-band, which is favorable for wide band operation. The minimum line width of the proposed GC is larger than 219 nm, which will lower the fabrication cost and improve the fabrication tolerance.

In Figure 1, our simulated result is plotted next to a summary of perfectly vertical GC demonstrations; the numbers next to the markers indicate the references. As shown in Figure 1a, we have achieved competitive high CE with the largest feature size. The 1-dB bandwidth demonstrated here is a record among high-efficiency GCs, shown in Figure 1b. Such a design can provide efficient, robust, and cost-effective coupling interfaces for sub-micrometric SOI waveguides, as desired for silicon PIC packaging, with fiber or integrating with VCSLE.

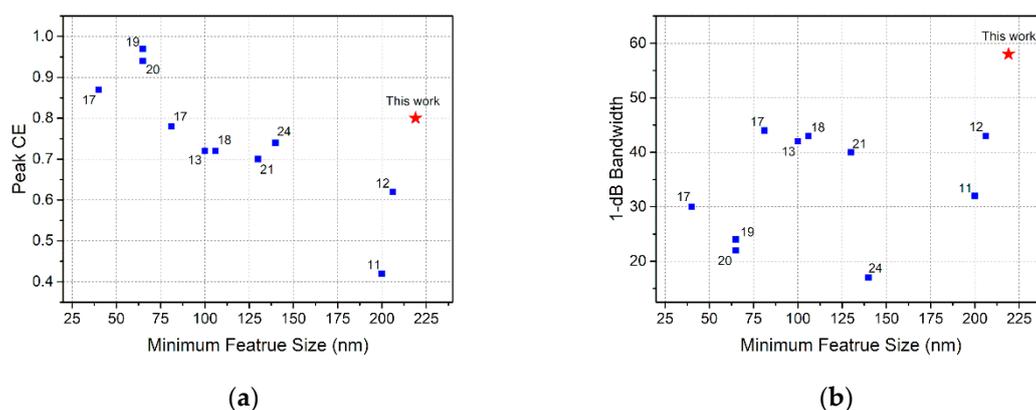


Figure 1. Comparison of our perfectly vertical grating coupler (GC) simulation result, with previously reported works with different minimum feature size: (a) coupling efficiency; (b) 1-dB bandwidth. The numbers next to the markers are the references.

2. Device Structure and Principle

Figure 2 shows our proposed perfectly vertical silicon fiber-to-chip GC. The proposed structure is a so-called bi-directional GC, which is based on a uniform Si-overlay grating, with two opposite in-plane transmission ports. Si-overlay is employed here to improve the vertical asymmetry of the grating, in order to achieve high directionality (defined as the ratio of power diffracted upward to the total diffracted optical power), and thus coupling efficiency. Differently from off-normal GCs,

the period Λ of the proposed grating equals the wavelength divided by the effective refractive index n_{eff} , so that the first-order diffraction couples light out of the waveguide, producing a surface-normal propagating field, to achieve perfectly vertical coupling [28]. One may argue that, with this typical Λ described above, the uniform grating is under resonance status, which is commonly unwelcome in most coupler applications. Considering chip-to-fiber coupling, the second-order diffracted mode will cause a strong reflection back into the waveguide. However, thanks to the symmetry of the bi-directional GC, with two in-plane ports, the reflected wave in one in-plane port will be diminished by the destructive interference, with the wave transmitted from the other in-plane port, as discussed in our previous work [29].

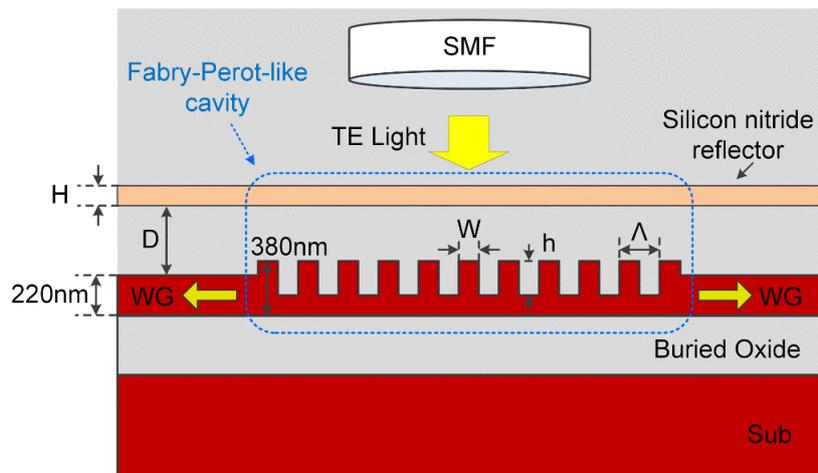


Figure 2. Schematic diagram of the device configuration. The Si_3N_4 layer and the grating, together form a Fabry-Perot-like cavity to reduce the up-reflection, thus enhancing the coupling efficiency (CE).

For coupling from fiber to chip, a light wave from a perfectly vertical single mode fiber is launched to the center of the uniform grating and coupled into two SOI waveguides, on both sides of the grating. The total CE for perfectly vertical in-plane coupling is mainly affected by up-reflection and substrate leakage. Up-reflected light, towards the launching fiber, attracts more concern in perfectly vertical coupling schemes, as it can significantly deteriorate the operation of the out-of-plane active launching element.

Most of the reported structures so far have studied the back-reflection to the waveguide, when the GC is used as the chip-to-fiber coupler. When the GC is used as the incoming coupler to the chip, as will be the case for most VCSEL to SOI assembly, there is little discussion on the up-reflection to the fiber. To reduce the up-reflection, and thus enhancing the whole CE, we introduced a Fabry-Perot-like cavity by adding a Si_3N_4 layer over the grating. Si_3N_4 is a dielectric commonly used as the passivation layer in back-end-of-line in the CMOS process, which ensures our design is compatible with CMOS process. The Si_3N_4 layer, and the grating itself, both work as reflective surfaces of the cavity. When the cavity is under resonance, the reflection of the whole cavity will reach the minimum value. The reflection of an asymmetric Fabry-Perot cavity can be obtained by [30]:

$$R_{\text{cavity}} = \frac{(\sqrt{R_1} - \sqrt{R_2})^2 + 4\sqrt{R_1}\sqrt{R_2}\sin^2(\varphi)}{(1 - \sqrt{R_1}\sqrt{R_2})^2 + 4\sqrt{R_1}\sqrt{R_2}\sin^2(\varphi)} \quad (1)$$

where R_1 and R_2 are the reflectivity of the two reflective surfaces, and the phase φ is given by:

$$2\varphi = \frac{4\pi nD}{\lambda} + \rho_1 + \rho_2 \quad (2)$$

where n is the index of refraction of the cavity medium, D is the cavity spacing, and ρ_1 and ρ_2 are the phase shifts of the two reflecting surface, respectively. Apparently, R_{cavity} is a periodic function of the cavity spacing D . Note that, zero reflection is possible, only when $R_1 = R_2$ and $\varphi = m\pi$ (m is an integer), according to Equations (1) and (2). In other words, the closer R_1 is to R_2 , the less reflection there will be for the Fabry-Perot cavity around the resonance wavelength.

In order to obtain a high-efficiency vertical GC, with zero up-reflection at the target wavelength, one should introduce a reflective surface with the same reflection characteristic of the grating, to form a symmetric Fabry-Perot cavity, and carefully design the distance between the reflector and the grating, to ensure the cavity is resonant at the desired wavelength. However, the reflection coefficient of the grating varies with the wavelength, moreover, the up-reflected wave of the grating cannot be seen as a plane wave, since the length of the grating is comparable to the mode size of the incident wave. Hence, if one want to achieve exactly the same reflection characteristics of the grating, a delicate design of reflector, with a complicated structure, might be needed, which will lead to extra fabrication processes and higher cost.

Therefore, considering the balance between the fabrication cost and the device performance, we employed a simple layer of Si_3N_4 , a commonly used dielectric in CMOS technology, to act as a reflector, with a similar reflection coefficient to the grating at the desired wavelength, as shown in Figure 2. The Si_3N_4 layer and the grating together form a Fabry-Perot-like cavity, and obtain a reduced reflection around the resonant wavelength.

For the Si_3N_4 reflector, the reflection characteristic can be modeled as a symmetric Fabry-Perot cavity, so that the reflection coefficient and the phase shift of the reflector are written as:

$$R_1 = \frac{4R_{\text{SiN}} \sin^2(\varphi_{\text{SiN}})}{(1 - R_{\text{SiN}})^2 + 4R_{\text{SiN}} \sin^2(\varphi_{\text{SiN}})} \quad (3)$$

$$\rho_1 = \arctan \frac{(1 - R_{\text{SiN}}) \sin 2\varphi_{\text{SiN}}}{(1 + R_{\text{SiN}})(1 - \cos 2\varphi_{\text{SiN}})} \quad (4)$$

where R_{SiN} is the reflection coefficient of the $\text{Si}_3\text{N}_4/\text{OX}$ interface which is 0.02541, and φ_{SiN} is the one-pass phase shift in the Si_3N_4 layer, which is given by $\varphi_{\text{SiN}} = \frac{2\pi nH}{\lambda}$, where H is the thickness of the Si_3N_4 layer. Obviously, R_1 and ρ_1 are both functions of the thickness of the Si_3N_4 layer. Combined with the Equations (1)–(4), as long as D and H are carefully designed to make sure that $R_1 = R_2$ and $\varphi = m\pi$ for the desired wavelength, the Fabry-Perot-like cavity will be under resonance, hence reduced reflection and enhanced CE will be achieved.

3. Design and Optimization

Our proposed coupling structure shown in Figure 2 is investigated in a commercial Finite-difference Time-domain (FDTD) solver (FDTD Solutions, Lumerical Inc., Vancouver, BC, Canada). The goal of the simulation is to obtain the highest CE for TE polarized light near 1550 nm. The width of the SOI waveguide is much larger than the height, so all of the simulations are two-dimensional. Table 1 shows the main parameters used in simulations. A TE polarized Gaussian beam with 1/e full width of 10.4 μm was launched onto the corrugated surface, and the coupling efficiency to the fundamental TE mode was examined. The proposed GC structures are based on an SOI substrate (shown in Figure 2), consisting of a standard 2 μm thick buried oxide (BOX) and a 220 nm thick top silicon layer, with a 160 nm thick Si-overlay; while the grating groove depth h is 230 nm, according to the IMEC MPW [31]. The values of the grating period, Λ , and filling-factor ($\text{FF} = W/\Lambda$, where W is the grating teeth width) are varied to optimize the fiber-to-chip CE. Notice that, due to the reciprocity of this coupling structure, the same CE is expected for the chip-to-fiber coupling.

Figure 3a shows the obtained contour for the CE at 1550 nm, when Λ is varied from 560 nm to 590 nm and FF is varied from 30% to 50%. When the grating structure has a $\Lambda \sim 578$ nm and a FF $\sim 38\%$, the CE can reach a maximum value of nearly 74%. Figure 3b shows the wavelength-dependent CE

for in-plane coupling, up-reflection, and substrate leakage, for an optimized grating structure, with a Λ of 578 nm and an FF of 38%, determined from Figure 3a. Clearly, although the peak CE is as high as 74% at 1551 nm, there is about a quarter of the incident optical power, either coupled to the substrate, or reflected back to fiber. The up-reflection power is so high that the return loss reaches -9.7 dB. High return loss will induce damage to the off-chip light source, which is unacceptable in a practical system.

Table 1. Main parameters used in simulations at 300 K.

Waveguide Thickness (μm)	0.22
Buried Oxide Thickness (μm)	2
Si-overlay Thickness (μm)	0.16
Grating Groove Depth (μm)	0.23
Grating Periods Number	17
Si ₃ N ₄ Refractive Index ($\lambda = 1.55 \mu\text{m}$)	2.03 ^a
Fiber Gaussian Mode Waist Radius (μm)	5.2
Fiber Gaussian Mode Polarization Angle (deg)	90

^a From Ref [32].

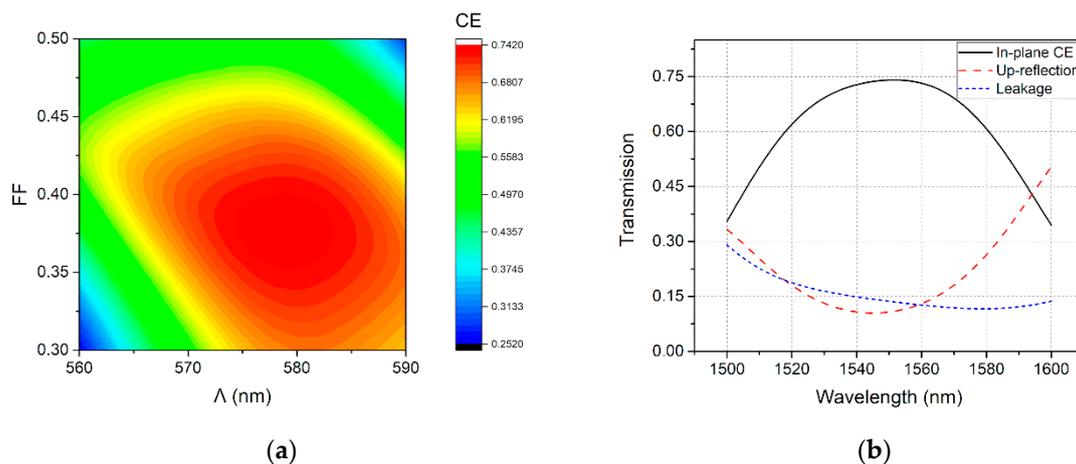


Figure 3. (a) The CE at 1550 nm with different Λ and filling factor (FF). The grating coupler with $\Lambda = 578$ nm and FF = 0.38 achieves CE of 74%. (b) Calculated transmission spectra of the Si-overlay grating coupler with $\Lambda = 578$ nm and FF = 0.38.

With the optimized grating period and filling-factor, we did a series of simulations to investigate the reflection characteristic of the GC. A field power monitor was positioned just above the grating and the light source to calculate the reflection coefficient and phase shift of the grating, R_2 and ρ_2 , respectively. The length of the monitor was the same as the length of the grating to examine the up-reflected wave that resonated in the cavity. The optical path length accumulated from the light source to the field power monitor was taken into account for the calculation of ρ_2 . Figure 4a shows the calculated R_2 and ρ_2 as a function of wavelength. At 1550 nm, we obtained that $R_2 = 0.0847$ and $\rho_2 = 0.975\pi$. According to Equation (3), the corresponding thickness for the Si₃N₄ reflector could be obtained. It is worth noting that R_1 is a periodic function of H as shown in Figure 4b. Here we chose the smallest value for H , which is 148 nm, since the longer the cavity length is, the higher the quality factor of a Fabry-Perot cavity will be [30], which is unwelcome in a wide-bandwidth application, such as optical coupling. With $H = 148$ nm, phase shift of the reflector ρ_1 is obtained as 0.115π according to Equation (4). Combined with Equation (2) while $m = 1$ is assumed, D is obtained as 243 nm. Here we set $m = 1$, to get the smallest value of D , because a lower Q is favorable, as in the case of the value of H .

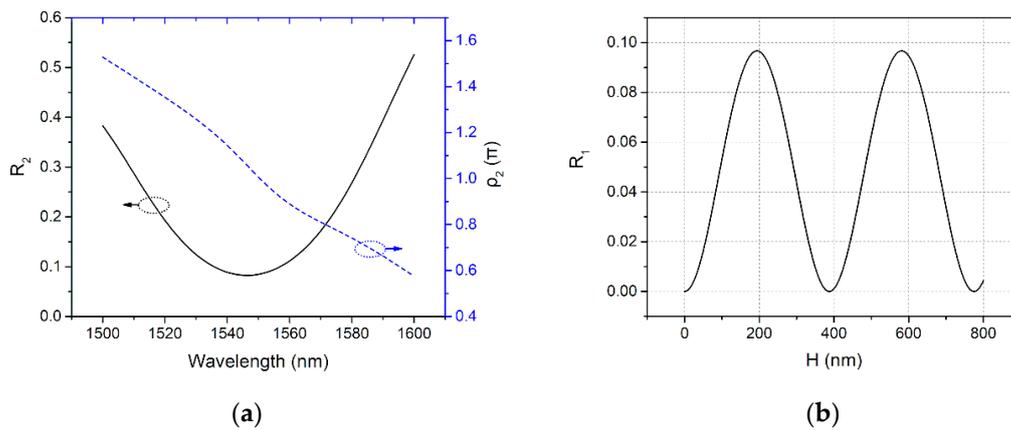


Figure 4. (a) Calculated R_2 and ρ_2 as a function of wavelength; (b) Calculated R_1 with various H .

2D FDTD simulations were carried out to verify the performance of the GC, enhanced by the Fabry-Perot-like cavity. As depicted in Figure 5a, the peak CE was enhanced to 78.5% at 1537 nm and the up-reflection was reduced to 5.4%, on account of the cavity. The values for D and H were swept in the simulations to verify if the optimal parameters were obtained. Figure 5b shows the contour for the CE at 1550 nm, when D is varied from 220 nm to 320 nm and H is varied from 120 nm to 170 nm. As can be seen, the optimal values for D and H are 302 nm and 149 nm respectively, which is a little different from the result calculated from the model discussed above. The reason for this difference may be that the profiles of the reflected fields of the grating and the Si_3N_4 reflector are not identical. Therefore, although the phase condition is met, completely destructive interference will not occur. Moreover, the reflection from the silicon substrate may affect the performance of the cavity as well. With the optimized $D = 302$ nm and $H = 149$ nm, the CE and up-reflection were calculated, as shown in short-dash curve and dot curve in Figure 5a, respectively. Thanks to the cavity, the peak CE reached 80.3% at 1551 nm and up-reflection was reduced to 5%.

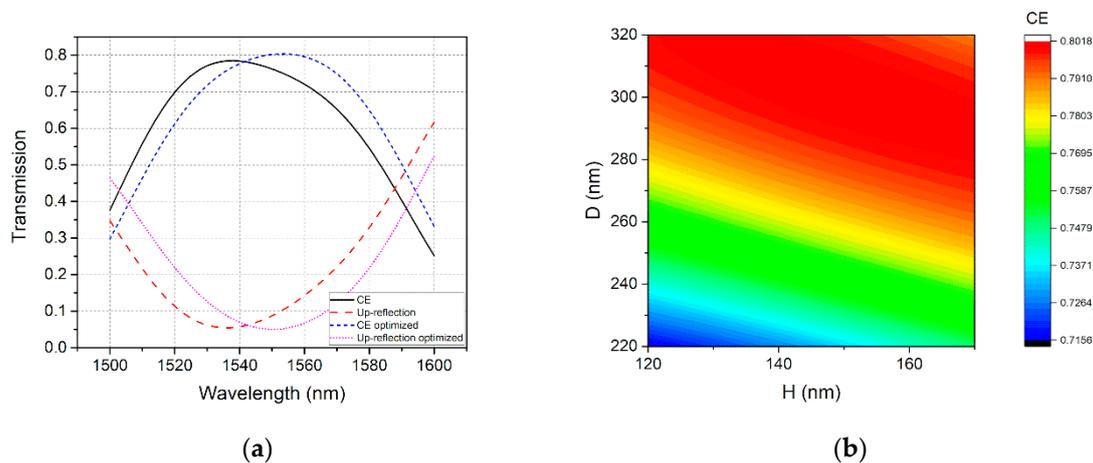


Figure 5. (a) Calculated transmission spectra of the cavity enhanced GC. (b) Calculated CE with D varying from 220 nm to 320 nm and H varying from 120 nm to 170 nm.

As we have discussed above, R_{cavity} varies periodically with H and D , leading to periodic relationships between enhanced CE and these two parameters. In order to further confirm whether $H = 149$ nm and $D = 302$ nm are optimal, a wide range parameter sweep was carried out through a series of simulations. Figure 6 shows the contour for the CE at 1550 nm obtained from the simulations, with H varying from 20 nm to 800 nm and D varying from 0 nm to 1000 nm. As clearly depicted, the CE changes periodically, with the value of H and D , and peak CE occurs with $H = 149$ nm and $D = 302$ nm.

It is worth noting that, the peak value of the CE in every period is slowly decreasing while H and D are increasing. In order to show the decrease more clearly, the calculated CE, with $D = 302$ nm and varying H , is plotted in Figure 7. This decrease of CE was mainly because a small amount of the light power leaked from both sides of the Fabri-Perot-like cavity, along the horizontal direction. With larger values of H and D , more light leaks from the cavity, resulting in the decrease of the whole CE.

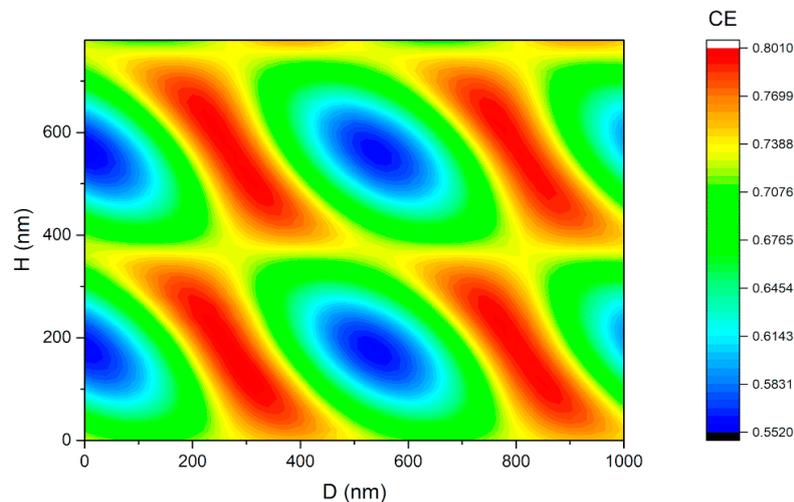


Figure 6. The CE at 1550 nm with H varying from 20 nm to 800 nm and D varying from 0 nm to 1000 nm. The CE changes periodically with the value of H and D .

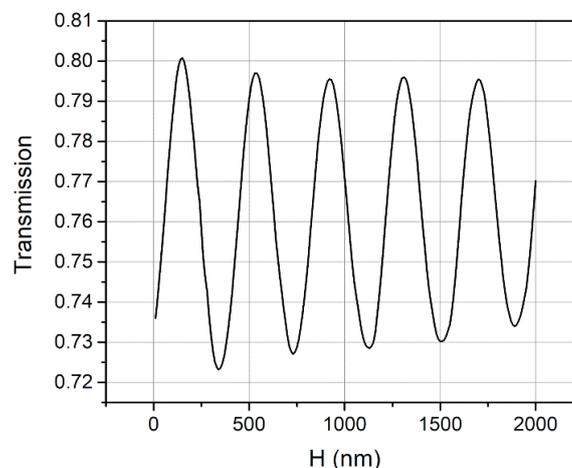


Figure 7. Calculated CE at 1550 nm with $D = 302$ nm and varying H . The peak value of the CE is slowly decreasing while H is increasing.

4. Discussion

4.1. Fabrication Process and Tolerance

The grating structure with silicon overlay can be fabricated through polysilicon deposition, lithography, and etching based on SOI wafers with 220 nm thick silicon, as described in ref [7]. After the grating structure was accomplished, SiO_2 was deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) to cover the grating, following chemical-mechanical polishing (CMP) to get a planarized surface. Then additional deposition of SiO_2 was needed to achieve the certain thickness of SiO_2 we desired. After that, Si_3N_4 layer was deposited through PECVD to form the upper reflector of the Fabri-Perot-like cavity. Finally, SiO_2 was deposited, acting as a passivation layer. The fabrication process flow of the Si_3N_4 reflector over the grating is illustrated in Figure 8.

As depicted in [33–35], 3D vertical integration of photonics devices is achievable through CMP and PECVD processes, with root-mean-square roughness of the SiO₂ surface below 5 nm. Moreover, the thickness error of the dielectric layer obtained through PECVD is about a few nanometers according to [36,37], which has little effect on the in-plane coupling efficiency. Therefore, the additional Si₃N₄ layer over the grating, with desired thickness at a certain position over the grating, can be easily fabricated through CMP and PECVD processes, ensuring that the idea of CE enhancement by Fabry-Perot-like cavity is feasible in the lab.

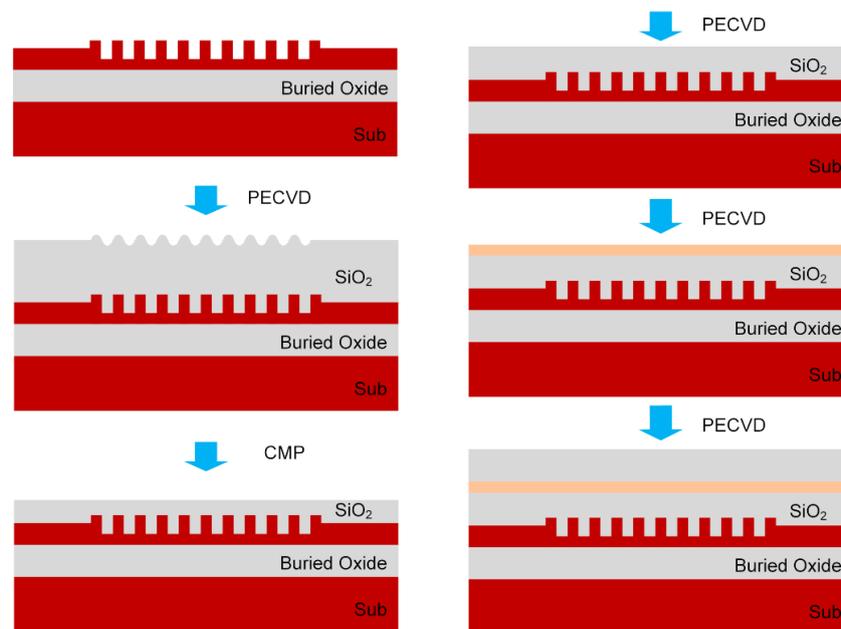


Figure 8. Process flow of the Si₃N₄ reflector over the grating for the Fabry-Perot-like cavity.

To investigate the robustness of our optimized devices, four sets of studies were performed that represent commonly encountered fabrication errors: variation of the grating width, of the etch depth, of the thickness of the deposited Si₃N₄ layer, and of the cavity distance. In Figure 9a, we plot the CE for grating tooth width variation, δ_w varies in the range of ± 20 nm. As seen, over a variation of ± 20 nm, the CE changes are small. In Figure 9b, we repeat the same analysis for variation of etch depth δ_h . Such deviations are expected to be within ± 10 nm [38]. A CE of $>70\%$ can be maintained around 1550 nm for deviations of $<\pm 10$ nm. The CE is more sensitive to the variation of δ_h , since etch depth plays an important role in the phase matching condition of the up-diffracted wave for Si-overlay GCs.

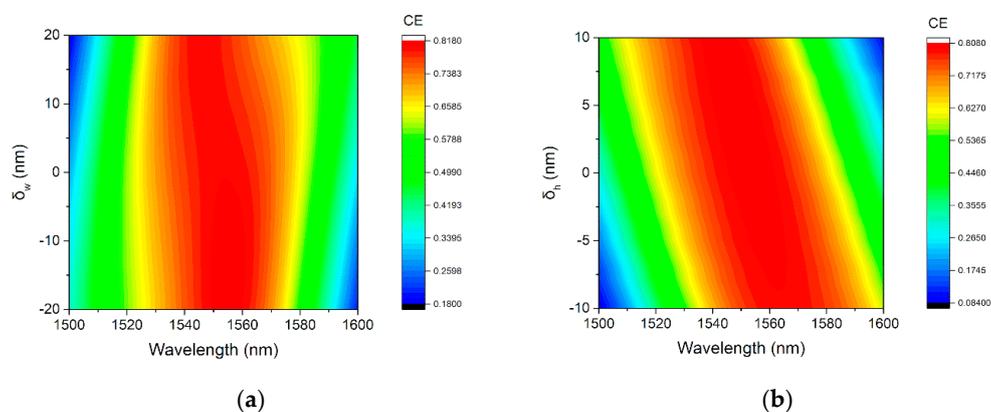


Figure 9. (a) Dependence of CE on width errors of the grating tooth. (b) Dependence of CE on grating etch depth errors.

Finally, in Figure 10, we show an additional analysis, where variations of the thickness of the Si_3N_4 layer δ_H and of the cavity distance δ_D are considered. According to Figure 10, little degradation of the CE is expected. Therefore, subjected to fabrication variations, the CE profile for the proposed GC is quite robust.

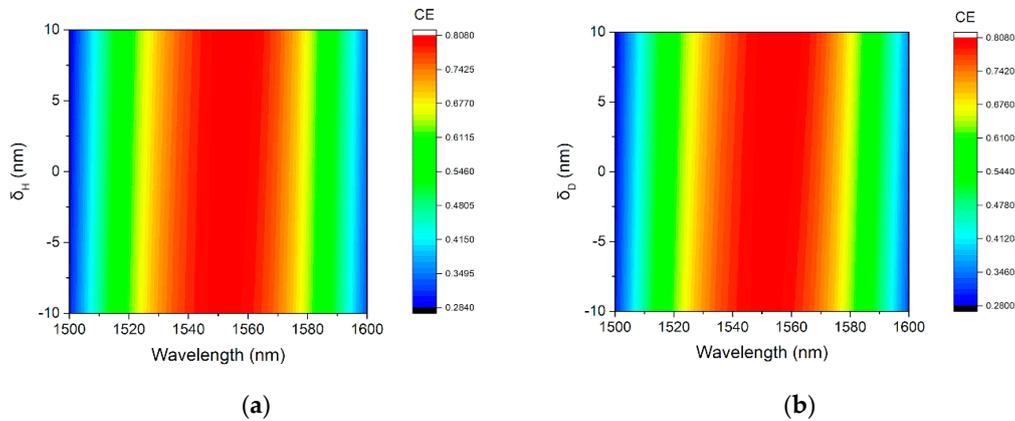


Figure 10. Fabrication tolerances of the CE: (a) Thickness error of the Si_3N_4 layer. (b) Thickness error of the SiO_2 between grating and Si_3N_4 layer.

4.2. Tolerance of the Polarization Angle

The grating coupler proposed here is designed to couple transverse-electric (TE) polarized light into on-chip waveguides, since lots of SOI waveguide devices operate in quasi TE mode. Therefore, the coupling efficiency of our coupler is quite poor for transverse-magnetic (TM) polarized light. As shown in Figure 11, the CE can be maintained above 70% when the deviation of the polarization angle δ_{p_angle} varies from -20 degree to $+20$ degree (the polarization angle for TE polarized light is 0 degree), but drops to nearly 1% when the polarization angle reaches -90 degree or $+90$ degree, which corresponds to TM polarized light. So far, we have been focusing on improving the performance of the grating coupler, considering TE polarization. The coupling of TM polarized light will be studied in future works.

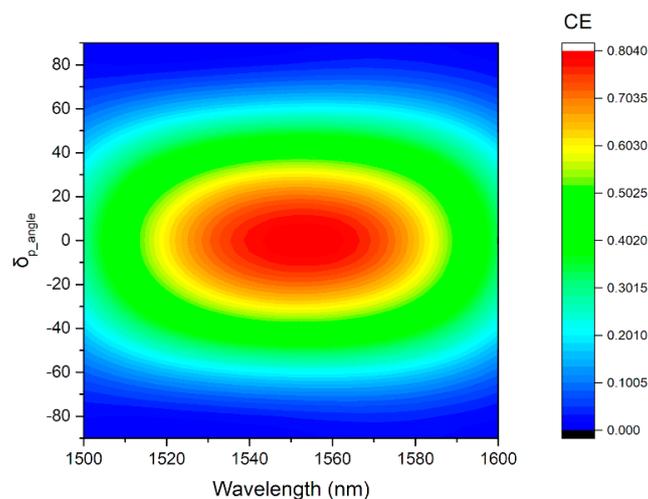


Figure 11. Dependence of coupling efficiency on deviation of the angle of polarization δ_{p_angle} .

5. Conclusions

In conclusion, we have presented a broadband high-efficiency perfectly vertical GC, with minimum feature size larger than 219 nm. By taking advantage of an additional Si_3N_4 layer and the idea of

Si-overlay for a GC, the peak CE reaches up to 80.3%, with up-reflection below 5%. The Si₃N₄ layer over the GC acts as a reflector and forms a Fabry-Perot-like cavity combined with the GC. With the help of the cavity, the light back-reflected towards the launching fiber is suppressed, thus enhancing the coupling into on-chip waveguides. In addition, since there are fewer grating periods, the proposed GC shows a wide-band character with a 1-dB bandwidth of 58 nm, ranging from 1522 to 1580 nm. The minimum feature size of the designed device is over 219 nm, which makes our design more cost-effective compared to other GC demonstrations. Moreover, our design maintains these high levels of CE even when subjected to typical fabrication variations, including grating width, etch depth, and deposition variation. Our perfectly vertical GC is believed to be suitable for efficient and fabrication-tolerant interfacing application between off-chip light sources and integrated chips that can be mass-produced.

Author Contributions: Conceptualization, Z.Z. (Zan Zhang); simulation, Z.Z. (Zan Zhang); results, analysis, and discussion, B.H., B.B., Z.Z. (Zanyun Zhang), C.C., and T.G.; writing—original draft preparation, Z.Z. (Zan Zhang); writing—review and editing, X.X., W.G., L.Z., and H.C.; supervision, H.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Key R&D Program of China (Grant Nos. 2018YFA0209000), the Natural Science Foundation of China (Grant Nos. 61704009, 61675191, 61974099, 61634006, and 61805020), the National Natural Science foundation of Shaanxi Province, China (Grant No. 2018JZ6004, 2020JQ-341), and the Fundamental Research Funds for the Central Universities, CHD (Grant No. 300102320106).

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Soref, R. The Past, Present, and Future of Silicon Photonics. *IEEE J. Sel. Top. Quantum Electron.* **2006**, *12*, 1678–1687. [[CrossRef](#)]
2. Huang, B.; Zhang, Z.; Zhang, Z.; Cheng, C.; Zhang, H.; Zhang, H.; Chen, H. 100 Gb/s Silicon Photonic WDM Transmitter with Misalignment-Tolerant Surface-Normal Optical Interfaces. *Micromachines* **2019**, *10*, 336. [[CrossRef](#)]
3. Zhang, Z.; Li, H.; Huang, B.; Zhang, Z.; Cheng, C.; Gao, T.; Yu, Y.; Li, Y.; Chen, H. Multi-channel silicon photonic receiver based on compact second-order microring resonators. *Opt. Commun.* **2019**, *437*, 168–173. [[CrossRef](#)]
4. Madani, A.; Kleinert, M.; Stolarek, D.; Zimmermann, L.; Ma, L.; Schmidt, O.G. Vertical optical ring resonators fully integrated with nanophotonic waveguides on silicon-on-insulator substrates. *Opt. Lett.* **2015**, *40*, 3826. [[CrossRef](#)] [[PubMed](#)]
5. Sun, C.; Wade, M.T.; Lee, Y.; Orcutt, J.S.; Alloatti, L.; Georgas, M.S.; Waterman, A.S.; Shainline, J.M.; Avizienis, R.R.; Lin, S.; et al. Single-chip microprocessor that communicates directly using light. *Nature* **2015**, *528*, 534–538. [[CrossRef](#)]
6. Kopp, C.; Bernabé, S.; Bakir, B.B.; Fedeli, J.; Orobtcouk, R.; Schrank, F.; Porte, H.; Zimmermann, L.; Tekin, T. Silicon Photonic Circuits: On-CMOS Integration, Fiber Optical Coupling, and Packaging. *IEEE J. Sel. Top. Quantum Electron.* **2011**, *17*, 498–509. [[CrossRef](#)]
7. Roelkens, G.; Vermeulen, D.; Selvaraja, S.; Halir, R.; Bogaerts, W.; Van Thourhout, D. Grating-Based Optical Fiber Interfaces for Silicon-on-Insulator Photonic Integrated Circuits. *IEEE J. Sel. Top. Quantum Electron.* **2011**, *17*, 571–580. [[CrossRef](#)]
8. Marchetti, R.; Lacava, C.; Carroll, L.; Gradkowski, K.; Minzioni, P. Coupling strategies for silicon photonics integrated chips [Invited]. *Photonics Res.* **2019**, *7*, 201–239. [[CrossRef](#)]
9. Almeida, V.R.; Panepucci, R.R.; Lipson, M. Nanotaper for compact mode conversion. *Opt. Lett.* **2003**, *28*, 1302–1304. [[CrossRef](#)]
10. Chen, X.; Cheng, Z.; Fung, C.K.Y.; Tsang, H.K. Design and applications of silicon waveguide grating couplers. In Proceedings of the Silicon Photonics VII., International Society for Optics and Photonics, San Francisco, CA, USA, 2 February 2012; Volume 8266, p. 82660.
11. Roelkens, G.; Thourhout, D.V.; Baets, R. High efficiency Silicon-on-Insulator grating coupler based on a poly-Silicon overlay. *Opt. Express* **2006**, *14*, 11622–11630. [[CrossRef](#)]

12. Benedikovic, D.; Alonso-Ramos, C.; Pérez-Galacho, D.; Guerber, S.; Vakarin, V.; Marcaud, G.; Le Roux, X.; Cassan, E.; Marris-Morini, D.; Cheben, P.; et al. L-shaped fiber-chip grating couplers with high directionality and low reflectivity fabricated with deep-UV lithography. *Opt. Lett.* **2017**, *42*, 3439. [[CrossRef](#)] [[PubMed](#)]
13. Marchetti, R.; Lacava, C.; Khokhar, A.; Chen, X.; Cristiani, I.; Richardson, D.J.; Reed, G.T.; Petropoulos, P.; Minzioni, P. High-efficiency grating-couplers: Demonstration of a new design strategy. *Sci. Rep.* **2017**, *7*, 16670. [[CrossRef](#)] [[PubMed](#)]
14. Wang, B.; Jiang, J.; Nordin, G.P. Embedded slanted grating for vertical coupling between fibers and silicon-on-insulator planar waveguides. *IEEE Photonics Technol. Lett.* **2005**, *17*, 1884–1886. [[CrossRef](#)]
15. Chen, X.; Li, C.; Tsang, H.K. Fabrication-Tolerant Waveguide Chirped Grating Coupler for Coupling to a Perfectly Vertical Optical Fiber. *IEEE Photonics Technol. Lett.* **2008**, *20*, 1914–1916. [[CrossRef](#)]
16. Tong, Y.; Zhou, W.; Tsang, H.K. Efficient perfectly vertical grating coupler for multi-core fibers fabricated with 193 nm DUV lithography. *Opt. Lett.* **2018**, *43*, 5709–5712. [[CrossRef](#)]
17. Zhang, Z.; Chen, X.; Cheng, Q.; Khokhar, A.Z.; Yan, X.; Huang, B.; Chen, H.; Liu, H.; Li, H.; Thomson, D.J.; et al. High-efficiency apodized bidirectional grating coupler for perfectly vertical coupling. *Opt. Lett.* **2019**, *44*, 5081. [[CrossRef](#)]
18. Liu, L.; Zhang, J.; Zhang, C.; Wang, S.; Jin, C.; Chen, Y.; Chen, K.; Xiang, T.; Shi, Y. Silicon waveguide grating coupler for perfectly vertical fiber based on a tilted membrane structure. *Opt. Lett.* **2016**, *41*, 820–823. [[CrossRef](#)] [[PubMed](#)]
19. Wang, S.; Hong, Y.; Zhu, Y.; Chen, J.; Gao, S.; Cai, X.; Shi, Y.; Liu, L. Compact high-efficiency perfectly-vertical grating coupler on silicon at O-band. *Opt. Express* **2017**, *25*, 22032–22037. [[CrossRef](#)]
20. Roelkens, G.; Thourhout, D.V.; Baets, R. High efficiency grating coupler between silicon-on-insulator waveguides and perfectly vertical optical fibers. *Opt. Lett.* **2007**, *32*, 1495–1497. [[CrossRef](#)]
21. Watanabe, T.; Ayata, M.; Koch, U.; Fedoryshyn, Y.; Leuthold, J. Perpendicular Grating Coupler Based on a Blazed Antireflection Structure. *J. Light. Technol.* **2017**, *35*, 4663–4669. [[CrossRef](#)]
22. Dezfouli, M.K.; Grinberg, Y.; Melati, D.; Cheben, P.; Schmid, J.H.; Sánchez-Postigo, A.; Ortega-Moñux, A.; Wangüemert-Pérez, G.; Cheriton, R.; Janz, S.; et al. Perfectly vertical surface grating couplers using subwavelength engineering for increased feature sizes. *Opt. Lett.* **2020**, *45*, 3701–3704. [[CrossRef](#)]
23. Michaels, A.; Yablonovitch, E. Inverse design of near unity efficiency perfectly vertical grating couplers. *Opt. Express* **2018**, *26*, 4766–4779. [[CrossRef](#)]
24. Su, L.; Trivedi, R.; Sapra, N.V.; Piggott, A.Y.; Vercruyse, D.; Vučković, J. Fully-automated optimization of grating couplers. *Opt. Express* **2018**, *26*, 4023–4034. [[CrossRef](#)]
25. Dai, M.; Ma, L.; Xu, Y.; Lu, M.; Liu, X.; Chen, Y. Highly efficient and perfectly vertical chip-to-fiber dual-layer grating coupler. *Opt. Express* **2015**, *23*, 1691–1698. [[CrossRef](#)]
26. Zhang, Z.; Huang, B.; Zhang, Z.; Cheng, C.; Liu, H.; Li, H.; Chen, H. Integrated silicon photonic interconnect with surface-normal optical interface. *Opt. Commun.* **2016**, *367*, 206–213. [[CrossRef](#)]
27. Li, H.; Ma, X.; Cui, B.; Wang, Y.; Zhang, C.; Zhao, J.; Zhang, Z.; Tang, C.; Li, E. Chip-scale demonstration of hybrid III-V/silicon photonic integration for an FBG interrogator. *Optica* **2017**, *4*, 692–700. [[CrossRef](#)]
28. Taillaert, D.; Bogaerts, W.; Bienstman, P.; Krauss, T.F.; Van Daele, P.; Moerman, I.; Verstuyft, S.; De Mesel, K.; Baets, R. An out-of-plane grating coupler for efficient butt-coupling between compact planar waveguides and single-mode fibers. *IEEE J. Quantum Electron.* **2002**, *38*, 949–955. [[CrossRef](#)]
29. Zhang, Z.; Shan, X.; Huang, B.; Zhang, Z.; Cheng, C.; Bai, B.; Gao, T.; Xu, X.; Zhang, L.; Chen, H. Efficiency Enhanced Grating Coupler for Perfectly Vertical Fiber-to-Chip Coupling. *Materials* **2020**, *13*, 2681. [[CrossRef](#)]
30. Yariv, A.; Yeh, P. *Photonics: Optical Electronics in Modern Communications*; Oxford University Press: New York, NY, USA; Oxford, UK, 2007; ISBN 978-0-19-517946-0.
31. Vermeulen, D.; Selvaraja, S.; Verheyen, P.; Lepage, G.; Bogaerts, W.; Absil, P.; Thourhout, D.V.; Roelkens, G. High-efficiency fiber-to-chip grating couplers realized using an advanced CMOS-compatible Silicon-On-Insulator platform. *Opt. Express* **2010**, *18*, 18278–18283. [[CrossRef](#)]
32. Xiao, X.; Yang, B.; Chu, T.; Yu, J.-Z.; Yu, Y.-D.; Anastasia, N. Design and Characterization of a Top Cladding for Silicon-on-Insulator Grating Coupler. *Chin. Phys. Lett.* **2012**, *29*, 114213. [[CrossRef](#)]
33. Amirzada, M.R.; Tatzel, A.; Viereck, V.; Hillmer, H. Surface roughness analysis of SiO₂ for PECVD, PVD and IBD on different substrates. *Appl. Nanosci.* **2016**, *6*, 215–222. [[CrossRef](#)]
34. Feng, J.; Akimoto, R. A Three-Dimensional Silicon Nitride Polarizing Beam Splitter. *IEEE Photonics Technol. Lett.* **2014**, *26*, 706–709. [[CrossRef](#)]

35. Petra, R.; Oo, S.Z.; Tarazona, A.; Cernansky, R.; Reynolds, S.A.; Khokhar, A.Z.; Mittal, V.; Thomson, D.J.; Politi, A.; Mashanovich, G.Z.; et al. HWCVD a-Si:H interlayer slope waveguide coupler for multilayer silicon photonics platform. *Opt. Express* **2019**, *27*, 15735. [[CrossRef](#)] [[PubMed](#)]
36. Barwicz, T.; Popovic, M.A.; Watts, M.R.; Rakich, P.T.; Ippen, E.P.; Smith, H.I. Fabrication of add-drop filters based on frequency-matched microring resonators. *J. Light. Technol.* **2006**, *24*, 2207–2218. [[CrossRef](#)]
37. Mittal, V.; Tarazona, A.; Khokhar, A.; Banakar, M.; Thomson, D.; Reed, G.T.; Chong, H.M.H. 3D Vertical Directional Coupler using Slope Waveguides on Si. In Proceedings of the 2019 Conference on Lasers and Electro-Optics Europe & European Quantum Electronics Conference (CLEO/Europe-EQEC), Munich, Germany, 23–27 June 2019.
38. Xu, D.-X.; Schmid, J.H.; Reed, G.T.; Mashanovich, G.Z.; Thomson, D.J.; Nedeljkovic, M.; Chen, X.; Van Thourhout, D.; Keyvaninia, S.; Selvaraja, S.K. Silicon Photonic Integration Platform—Have We Found the Sweet Spot? *IEEE J. Sel. Top. Quantum Electron.* **2014**, *20*, 189–205. [[CrossRef](#)]



© 2020 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<http://creativecommons.org/licenses/by/4.0/>).