A High-Performance InGaAs Vertical Electron–Hole Bilayer Tunnel Field Effect Transistor with P+-Pocket and InAlAs-Block

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Abstract: To give consideration to both chip density and device performance, an In0.53Ga0.47As vertical electron–hole bilayer tunnel field effect transistor (EHBTFET) with a P+-pocket and an In0.52Al0.48As-block (VPB-EHBTFET) is introduced and systematically studied by TCAD simulation. The introduction of the P+-pocket can reduce the line tunneling distance, thereby enhancing the on-state current. This can also effectively address the challenge of forming a hole inversion layer in an undoped InGaAs channel during device fabrication. Moreover, the point tunneling can be significantly suppressed by the In0.52Al0.48As-block, resulting in a substantial decrease in the off-state current. By optimizing the width and doping concentration of the P+-pocket as well as the length and width of the In0.52Al0.48As-block, VPB-EHBTFET can obtain an off-state current of 1.83 × 10⁻¹⁹ A/µm, on-state current of 1.04 × 10⁻⁴ A/µm, and an average subthreshold swing of 5.5 mV/dec. Compared with traditional InGaAs vertical EHBTFET, the proposed VPB-EHBTFET has a three orders of magnitude decrease in the off-state current, about six times increase in the on-state current, 81.8% reduction in the average subthreshold swing, and stronger inhibitory ability on the drain-induced barrier-lowering effect (7.5 mV/V); these benefits enhance the practical application of EHBTFETs.

Keywords: tunnel field effect transistor; line tunneling; P+-pocket; InGaAs/InAlAs

1. Introduction

Due to the emergence of the cloud, big data and real-time data transmission have become the main trends in the development of information technology, and they require integrated circuits to have ultra-low power dissipation. However, as the core of current integrated circuits, MOSFETs suffer from the increasing static power consumption with the decrease in feature size, inhibiting the development of integrated circuits. The decrease of subthreshold swing (SS) is an effective approach to deal with this issue. Limited by the injection mechanism of thermal emission, the SS of MOSFETs cannot be lower than 60 mV/dec; thus, there is an urgent need to develop steep SS (<60 mV/dec) devices to satisfy the cloud applications.

The tunnel field effect transistor (TFET) [1–3], as a steep SS device, has received widespread attention because of its CMOS process compatibility and low standby power consumption. However, the on-state current (I_on) of TFETs is too low for reasonable performance, which makes most research focus on overcoming this drawback. Therefore, TFETs with new structures or operation mechanisms have appeared in large numbers, such as two-dimensional material TFETs [4–6], negative capacitance TFETs [7–9], heterojunction TFETs [10–12], nanowire TFETs [13–15], line tunneling (L-tunneling) TFETs [16–29], etc. Comprehensive analysis shows that expanding the tunneling area based on the L-tunneling mechanism is a very effective approach to improving I_on. The electron–hole bilayer TFET (EHBTFET) [19–29] is a new type of L-tunneling TFET that was first proposed by Lattanzio [19] and has been developed in recent years because of its novel tunneling mechanism. Different from the L-tunneling TFETs with the L/U/T-type gate structure [16–18]...
that create the L-tunneling by overlapping the gate and heavily doped source region, EHBTFETs can generate the L-tunneling perpendicular to the channel in the electron–hole bilayer formed by the gate engineering or bias-induced method. So far, research has mainly focused on the transverse EHBTFETs, from which it has been found that the vertical L-tunneling not only boosts $I_{on}$ but also leads to high off-state current ($I_{off}$). To solve this issue, many methods, such as counterdoping in the gate underlap region [23], partial light doping in the source and drain regions [24], heterogate structure [25], and implantation of a dielectric barrier layer in the gate underlap region [26] have been adopted, and $I_{off}$ has been suppressed to a certain extent. However, it should be noted that the $I_{on}$ of the transverse EHBTFETs is directly proportional to the gate overlap area, which means that the increase of $I_{on}$ is at the expense of chip density. To simultaneously improve device performance and chip density, new EHBTFETs need to be investigated.

Vertical EHBTFETs [27–29] can improve $I_{on}$ by expanding the tunneling area in the vertical direction without sacrificing the chip density, which attracts researchers’ attention. To further improve $I_{on}$, III-V materials are usually adopted in vertical EHBTFETs due to their smaller electron effective mass and band gap ($E_g$) [30], but which can also exacerbate the deterioration of $I_{on}$. Our previous research [29] demonstrates that the impact of the point tunneling (P-tunneling) between the gate underlap region and the drain on the $I_{on}$ is significant, which cannot be effectively attenuated through the approaches used in transverse EHBTFETs. Although our proposed DGNP-EHBTFET in Reference [29] can solve this problem well, $I_{on}$ can only be maintained without degradation and cannot be improved. To obtain better off- and on-state device performance, an improved vertical EHBTFET is proposed in this paper, namely, an In$_{0.53}$Ga$_{0.47}$As EHBTFET with a P$^+$-pocket and an In$_{0.52}$Al$_{0.48}$As-block (VPB-EHBTFET). Since the line tunneling of EHBTFETs depends on the concentration of the electron–hole bilayer in the channel, the P$^+$-pocket can be used to generate the hole layer in real operation. This is due to that for high-K/InGaAs interface, a large number of interface states near the valence band in InGaAs will inhibit the formation of the hole layer in the InGaAs channel without any acceptor doping. Alternatively, the P$^+$-type doping performed in the right-side channel may be the best method for creating the hole layer in real operation. More importantly, the P$^+$-pocket can reduce the tunneling distance of the L-tunneling, which enhances the electron tunneling and achieves the goal of improving the on-state current. In$_{0.52}$Al$_{0.48}$As possesses greater $E_g$ and carrier effective mass and matches the lattice of In$_{0.53}$Ga$_{0.47}$As. Due to its excellent material properties, placing In$_{0.52}$Al$_{0.48}$As in the gate underlap region near the drain can inhibit the point tunneling in this region. Moreover, it can also effectively avoid potential performance degradation caused by the lattice mismatch in the device fabrication. Herefore, since investigations on suppressing off-state leakage and improving on-state performance for vertical EHBTFETs are relatively few, revealing the physical mechanism of the proposed VPB-EHBTFET is necessary, thereby providing theoretical guidance for device manufacturing.

The content of this paper focuses on the following aspects. Device structures and corresponding parameters, key manufacturing processes, and physical models for simulations are introduced in Section 2. Section 3 examines in detail the performance comparison between conventional and improved EHBTFETs and the effects of P$^+$-pocket and InAlAs-block on the proposed VPB-EHBTFET. Finally, a concise summary of the current studies is provided in Section 4.

2. Device Structures and Simulation Methods

For comparison, we bring in two other EHBTFETs, namely, (1) a traditional vertical EHBTFET (V-EHBTFET) and (2) a vertical EHBTFET with a P$^+$-pocket (VP-EHBTFET). Cross-sectional views and corresponding device parameters of the three EHBTFETs are given in Figure 1 and Table 1, respectively. It is found that EHBTFETs’ difference only
exists in the channel. The bulk material of the three EHBTFETs is In\(_{0.53}\)Ga\(_{0.47}\)As, but there is an In\(_{0.52}\)Al\(_{0.48}\)As-block in the channel of VPB-EHBTFET compared with the other two devices. Moreover, only the channel near the right gate (RG) of VP-EHBTFET and VPB-EHBTFET possesses the P\(^+\)-pocket with the doping concentration of 6 × 10\(^{19}\) cm\(^{-3}\). For these three EHBTFETs, since the L-tunneling occurs in the electron–hole bilayer of the gate overlap region (GO region) (see yellow arrows in Figure 1c), the appropriate carrier concentration is required in this region. According to the charge plasma concept [34], chromium (work-function = 4.5 eV) is employed as the left gate (LG) to induce a two-dimensional electron gas layer, and aurum (work-function = 5.3 eV) is adopted as RG to create a two-dimensional hole gas layer [35]. To induce a uniform carrier distribution, the width of bulk material is set to 10 nm. Furthermore, some key material parameters used in simulations refer to reference [10].

![Figure 1](image)

**Figure 1.** Schematics of (a) V-EHBTFET; (b) VP-EHBTFET; and (c) VPB-EHBTFET.

**Table 1.** Device structure parameters used in simulations.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
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</thead>
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<tr>
<td>Source length (L(_S))</td>
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<tr>
<td>Gate/source space (L(_{GS}))</td>
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</tr>
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<td>Drain length (L(_D))</td>
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<tr>
<td>Right gate length (L(_{RG}))</td>
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</tr>
<tr>
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<tr>
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<td>Gate/drain space (L(_{GD}))</td>
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<tr>
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</tr>
<tr>
<td>Left gate work-function</td>
<td>4.5 eV</td>
</tr>
<tr>
<td>Right gate work-function</td>
<td>5.3 eV</td>
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</table>

The proposed VPB-EHBTFET can be fabricated with the most advanced process technology currently available, in which the In\(_{0.53}\)Ga\(_{0.47}\)As epitaxial layer with the In\(_{0.52}\)Al\(_{0.48}\)As-block can be grown vertically on the InP substrate by molecular beam epitaxy technology, and the P\(^+\)-pocket is created by ion implantation. Inductively coupled plasma etching is employed to etch dielectric and epitaxial layer materials, and the atom layer deposition technique can be adopted to deposit dielectrics and metal electrodes. The key process is
the fabrication of the P⁺-pocket and the Inₐ₅₂Alₙ₅₈As-block, which is closely related to the accurate control of doping depth and concentration in the ion implantation, as well as the precise design of the mask pattern.

All device simulations are performed using the Silvaco-Atlas 2-D numerical simulation platform. In simulations, the density gradient model is included to take into account the quantum confinement effect. Additionally, models included in references [10,29] are considered, such as the non-local band-to-band tunneling (BTBT) model, the Lombardi mobility model, the strained two-band zincblende model, etc. To compare under the same conditions, the influence of trap is not considered in the simulations.

3. Results and Discussion

3.1. Performance Comparison between V-EHBTFET, VP-EHBTFET, and VPB-EHBTFET

Referring to our previous research on EHBTFETs [29], it is known that there are two tunneling mechanisms in this kind of device, namely, the P-tunneling and L-tunneling parallel to and perpendicular to the channel, respectively. The P-tunneling basically occurs in the gate underlap region near the source or drain (named GUS region or GUD region, respectively), while the L-tunneling occurs in the GO region. Both tunneling mechanisms are closely related to \( P_{\text{tun}} \), which can be expressed as Equation (1) [29]:

\[
P_{\text{tun}} \propto \exp \left( \frac{4\lambda \sqrt{2m^*E_{\text{g}}^{3/2}}}{3 e |h(E_g + \Delta\phi)} \right) = \exp \left( \frac{4\sqrt{2m^*E_{\text{g}}^{3/2}}}{3 e |hE_{\text{g}}} \right) \tag{1}\]

Two key factors affecting \( P_{\text{tun}} \), the tunneling distance (\( \lambda \)) and the energy range used for tunneling (\( \Delta\phi \)), can be extracted from the energy band. Therefore, to interpret the tunneling mechanism in detail, energy bands in the off-state [gate voltage \( (V_{\text{gs}}) = 0 \text{ V} \), drain voltage \( (V_{\text{ds}}) = 0.5 \text{ V} \)] for these three EHBTFETs are calculated along A-A‘, B-B‘, and C-C‘ (gray dotted lines in Figure 1b), respectively, and plotted in Figure 2a–c, respectively.

As shown in Figure 2a, although \( \Delta\phi \) appears in the GUD region, the P-tunneling in the left-side channel of the three EHBTFETs is suppressed due to the very long \( \lambda \). It is observed from Figure 2b that the P-tunneling in the right-side channel also occurs in the GUD region. Since the introduction of a P⁺-pocket can enlarge \( \Delta\phi \) and decrease \( \lambda \), the P-tunneling in the off-state for VP-EHBTFET is stronger than that for V-EHBTFET, according to Equation (1). Although VPB-EHBTFET also possesses the P⁺-pocket like VP-EHBTFET, its P-tunneling can better be suppressed compared with the other two EHBTFETs. This is because there is an Inₐ₅₂Alₙ₅₈As-block with wider \( E_g \) in the GUD region of VPB-EHBTFET, which significantly degrades the \( P_{\text{tun}} \). Figure 2c shows the energy band profiles in the GO region, from which it is found that the L-tunneling does not take place in the off-state due to no \( \Delta\phi \). Based on the analyses in Figure 2a–c, it is concluded that in the off-state, the P-tunneling in the right-side channel is dominant, and the proposed VPB-EHBTFET has the weakest tunneling capacity. \( I_{\text{off}} \) is an important parameter to test the off-state performance of devices, which can be extracted from the transfer characteristic curve (i.e., \( I_{\text{ds}}-V_{\text{gs}} \) curve).

To verify the above mechanism analysis, \( I_{\text{off}}-V_{\text{gs}} \) curves of these three EHBTFETs are computed and shown in Figure 2d. As observed from the figure, it results that \( I_{\text{off}} \) of VPB-EHBTFET approaches as low as \( 1.83 \times 10^{-19} \text{ A/\mu m} \). Compared with the \( I_{\text{off}} \) of V-EHBTFET and VP-EHBTFET \( (2.29 \times 10^{-16} \text{ A/\mu m} \) and \( 8.37 \times 10^{-11} \text{ A/\mu m} \), respectively), that of VPB-EHBTFET is reduced by approximately three and eight orders of magnitude, respectively. It follows that VPB-EHBTFET has the best off-state performance, which is consistent with the tunneling mechanism analyzed above.
Figure 2. Off-state energy band profiles for EHBTFETs along (a) A-A’, (b) B-B’, and (c) C-C’, respectively; (d) $I_{ds}$-$V_{gs}$ curves of EHBTFETs.

$I_{on}$, a key performance indicator in the on-state ($V_{ds} = 1$ V and $V_{ds} = 0.5$ V in simulations), can also be extracted from Figure 2d. $I_{on}$ of VPB-EHBTFET approaches $1.04 \times 10^{-4}$ A/µm, which is basically the same as that of VP-EHBTFET but about 5.7 times higher than that of V-EHBTFET ($1.84 \times 10^{-5}$ A/µm). Here, we still explain their differences from the perspective of the energy band. Similarly, energy band profiles in the on-state for the three EHBTFETs are extracted and plotted in Figure 3.

From Figure 3a,b, the P-tunneling in the left-side channel occurs in the GUS region, which is different from that in the off-state, but that in the right-side channel still occurs in the GUD region. Based on the previous analysis, it can be known that the effect of the P-pocket and the In$_{0.52}$Al$_{0.48}$As-block on the P-tunneling in the on-state is the same as that in the off-state. Combined with the P-tunneling in the left- and right-side channels, it can be inferred that the adoption of the P-pocket is conducive to the enhancement of P-tunneling in the on-state. Furthermore, it is observed from Figure 3c that the energy bands in the GO region of VP-EHBTFET and VPB-EHBTFET bend upward due to the existence of the P-pocket, which can reduce the $\lambda$ of the L-tunneling and eventually enhance their L-tunneling. Since the L-tunneling occurs in the whole GO region (50 nm in length), while the P-tunneling region only exists within a range of a few nanometers near the gate, and the $\lambda$ of L-tunneling is much smaller than that of P-tunneling, both of these cause the L-tunneling to dominate in the on-state. As a result, the tunneling ability of VP-EHBTFET and VPB-EHBTFET is basically the same in the on-state and stronger than that of V-EHBTFET, eventually resulting in better on-state performance in VP-EHBTFET and VPB-EHBTFET.
To better understand the tunneling mechanism of devices, it can be further investigated from the point of view of the non-local electron BTBT (e-BTBT) rate. According to the results of energy band analysis, only the off-state e-BTBT rate in the right-side channel and the on-state one in the GO region of V-EHBTFET, VP-EHBTFET, and VPB-EHBTFET are extracted and displayed in Figure 4a,b, respectively. It is found from Figure 4a that the peak values of the off-state e-BTBT rate for these three EHBTFETs occur in the GUD region and show the following trend: \( V_{P-EHBTFET} > V_{V-EHBTFET} > V_{P_{BP-EHBTFET}} \), which directly reflects that the enhancement of the off-state P-tunneling by the \( P^+ \)-pocket can be suppressed significantly by the In\(_{0.52}\)Al\(_{0.48}\)As-block. The smaller the off-state e-BTBT rate of \( V_{P_{BP-EHBTFET}} \), the better its off-state performance. Figure 4b shows that the peak value of the on-state e-BTBT rate in the GO region of \( V_{P-EHBTFET} \) and \( V_{P_{BP-EHBTFET}} \) is the same, but it is one order of magnitude higher than that of \( V_{V-EHBTFET} \). Thus, it can be confirmed again that the \( P^+ \)-pocket benefits improve the on-state L-tunneling, which makes the proposed \( V_{P_{BP-EHBTFET}} \) have good on-state performance as \( V_{P-EHBTFET} \).

Furthermore, other important performance parameters, such as \( I_{on}/I_{off} \), subthreshold voltage \( (V_{th}) \), average subthreshold swing \( (SS_{avg}) \), point subthreshold swing \( (point\ SS) \), and drain-induced barrier lowering \( (DIBL) \), are calculated based on the \( I_{ds}-V_{gs} \) curves. Due to the high \( I_{on} \) and the minimum \( I_{off} \) in the proposed \( V_{P_{BP-EHBTFET}} \), it obtains the maximum \( I_{on}/I_{off} \) of \( 5.7 \times 10^{14} \). \( V_{th} \) usually refers to the \( V_{gs} \) corresponding to the midpoint of the transition zone, where the drain current \( (I_{ds}) \) changes sharply with the \( V_{gs} \) in the \( I_{ds}-V_{gs} \) curve. Referring to previous publications [2,10], \( V_{gs} \) corresponding to \( I_{ds} = 1 \times 10^{-7} \text{A/\mu m} \) is taken as \( V_{th} \) in this paper. As shown in Figure 2d, the \( V_{th} \) of the proposed \( V_{P_{BP-EHBTFET}} \) is as low as 0.06 V, which is the same as that of \( V_{P-EHBTFET} \). Moreover, the \( V_{th} \) of \( V_{P_{BP-EHBTFET}} \) is...
EHBTFET and VP-EHBTFET are less than that of V-EHBTFET (0.26 V). This is due to the introduction of P'-pocket reducing the λ of the L-tunneling, allowing VP- and VPB-EHBTFETs to be turned on at lower $V_{gs}$. $SS_{avg}$ is expressed as $SS_{avg} = (V_{th} - V_{off})/(\log I_{on} - \log I_{off})$, where $V_{off}$ is the $V_{gs}$ at which the $I_{on}$ begins to increase. In view of the minimum $I_{on}$ (i.e., $I_{off}$) caused by the In$_{As}/Al_{0.52}Ga_{0.48}As$-block, $SS_{avg}$ of 5.5 mV/dec can be obtained in VPB-EHBTFET, which is reduced by 81.8% and 75.1% compared with that in V-EHBTFET and VPB-EHBTFET (30.2 mV/dec and 22.1 mV/dec, respectively), respectively. Figure 5a shows the point $SS$ values of the three EHBTFETs, where the point $SS$ is calculated by $dV_{th}/d(\log I_{on})$. It is found that VPB-EHBTFET possesses steeper point $SS$ at each $I_{on}$; in particular, when $I_{on} < 10^{-6}$ A/μm, the point $SS$ is around 1 mV/dec and basically remains unchanged, guaranteeing the steepest $SS_{avg}$ in VPB-EHBTFET. DIBL can be used to characterize the shift of $V_{th}$ in devices, which is usually defined as $\Delta V_{th}/\Delta I_{on}$. To obtain the DIBL values of the three EHBTFETs, the $I_{on}-V_{gs}$ curves are calculated at $V_{ds} = 0.1$ V and 0.5 V, respectively, and plotted in Figure 5b. Since $V_{ths}$ of the proposed VPB-EHBTFET and VP-EHBTFET change negligibly under different $V_{ds}$, a low DIBL value of 7.5 mV/V can be achieved in both EHBTFETs. This is because the existence of the P'-pocket enhances the built-in electric field in the GO region, thereby reducing the influence of the applied electric field on the L-tunneling. However, the DIBL value cannot be calculated for V-EHBTFET because this device is still turned off at $V_{ds} = 0.1$ V. Thus, it can be seen that the adoption of the P'-pocket can effectively suppress the DIBL effect. For a clear comparison, the parameters discussed above for the three EHBTFETs are summarized in Table 2.

![Figure 5](image-url)  
*Figure 5. (a) The correlation between point $SS$ and drain current of EHBTFETs; and (b) $I_{on}-V_{gs}$ curves of EHBTFETs at $V_{ds} = 0.1$ V and $V_{ds} = 0.5$ V, respectively.*

<table>
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<tr>
<th>Device</th>
<th>$I_{on}$ (A/μm)</th>
<th>$I_{of}$ (A/μm)</th>
<th>$I_{on}/I_{off}$</th>
<th>$V_{th}$ (V)</th>
<th>$SS_{avg}$ (mV/dec)</th>
<th>DIBL (mV/V)</th>
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<tbody>
<tr>
<td>V-EHBTFET</td>
<td>$2.29 \times 10^{-16}$</td>
<td>$1.84 \times 10^{-6}$</td>
<td>$8.0 \times 10^{-10}$</td>
<td>0.26</td>
<td>30.2</td>
<td>N/A</td>
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<tr>
<td>VP-EHBTFET</td>
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<td>$1.04 \times 10^{-4}$</td>
<td>$1.2 \times 10^{-9}$</td>
<td>0.06</td>
<td>22.1</td>
<td>7.5</td>
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<tr>
<td>VPB-EHBTFET</td>
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<td>5.5</td>
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</table>

### 3.2. Effect of P'-Pocket on VPB-EHBTFET

Here, doping concentration and doping width (G and W) in the P'-pocket of the proposed VPB-EHBTFET are investigated for the optimization of device performance. Figure 6a shows $I_{on}$ and $I_{off}$ values under different Crs. It is found from the figure that $I_{on}$ is very low and remains the same order of magnitude when $C_r < 8 \times 10^{19}$ cm$^{-3}$, but it increases sharply with the further increase in $C_r$. $I_{off}$ increases with $C_r$. Both of these trends can be explained by the energy band profiles. Based on the conclusion of device performance comparison between conventional and improved EHBTFETs, it is known that their $I_{on}$ and $I_{off}$ depend on the off-state P-tunneling in the GUD region of the right-side channel and the on-state L-tunneling in the GO region, respectively. Therefore, the off-state energy bands of the P-tunneling in the right-side channel
under different C_ps are calculated first, but results demonstrate that the effect of the change of C_r on the P-tunneling is negligible. This is because the existence of the In_{0.52}Al_{0.48}As-block makes the λ of the P-tunneling possess basically identical lengths (about 50 nm) under different C_ps, thereby preventing the tunneling of electrons in this region. Then, the off-state energy bands of the L-tunneling in the GO region under different C_ps are also calculated and plotted in Figure 6b. With the increase in C_r, the energy band gradually bends upward, and a Δφ can be generated when C_r > 6 × 10^{19} cm^{-3}. The existence of Δφ provides a condition for the off-state L-tunneling, which results in a rapid increase in I_off. Moreover, for the interpretation of the change trend of I_on, the on-state energy bands of the L-tunneling in the GO region are examined and shown in Figure 6c. With the increase in C_r, λ decreases and Δφ increases, so that I_on takes on a monotonically increasing trend according to Equation (1). Figure 6d shows SS_avg and I_on/I_off in VPB-EHBTFET with different C_ps. With the increase in C_r, SS_avg decreases slowly first and then increases rapidly, but I_on/I_off has the opposite change trend compared with SS_avg. When C_r = 6 × 10^{19} cm^{-3}, SS_avg and I_on/I_off can approach the minimum and maximum values, respectively. By compromising performance parameters, it results that 6 × 10^{19} cm^{-3} is the optimal C_r.

Further, the effect of doping width W_P on the device performance is investigated. Figure 7a shows I_off and I_on values under different W_Ps. With the increase in W_P, I_off increases first, then decreases, and finally increases again. To interpret this trend, we extract the e-BTBT rates that can reflect the tunneling ability of the P-tunneling and L-tunneling in the off-state and plot them in Figure 7b. It is observed from the figure that the off-state e-BTBT rates of the P-tunneling and L-tunneling are very low when W_P ≤ 1 nm, which indicates that both kinds of tunneling are suppressed in this condition, so a very small I_off can be obtained. When 1 nm < W_P < 5 nm, the off-state L-tunneling is turned on and dominates,
which makes \( I_{\text{on}} \) have a sharp increase. This is due to the fact that the \( \lambda \) of the L-tunneling reduces with the increase in \( W_B \). With the further increase in \( W_B \), the decrease in electrons in the left side of the GO region lifts the energy band in this region; thus, the \( \Delta \phi \) of the L-tunneling starts to reduce at \( W_B = 4 \) nm and disappears at \( W_B = 5 \) nm, thereby resulting in a decrease in \( I_{\text{on}} \). When \( W_B \geq 5 \) nm, the L-tunneling is turned off, and the P-tunneling is dominant, leading to \( I_{\text{on}} \) increasing with \( W_B \) again. This is because, with the increase in \( W_B \), the P-tunneling junction in the left-side channel becomes steeper, which increases the e-BTBT rate of the P-tunneling. \( I_{\text{on}} \) depends on the on-state L-tunneling in the GO region. Due to the mutual constraint between \( \lambda \) and \( \Delta \phi \), the e-BTBT rate of the L-tunneling exhibits a trend of increasing first and then decreasing with the increase in \( W_B \), which results in the same change trend in \( I_{\text{on}} \) (see Figure 7a). As shown in Figure 7c, the optimal \( SS_{\text{avg}} \) and \( I_{\text{on}}/I_{\text{off}} \) can be obtained at \( W_B = 5 \) nm. Comprehensive analysis shows that the optimal \( W_B \) is 5 nm.

**Figure 7.** (a) The variation of \( I_{\text{on}} \) and \( I_{\text{off}} \) with \( W_B \) for VPB-EHBTFTET; (b) the peak value of the nonlocal e-BTBT rate under different \( W_B \) for the P-tunneling in the left-side channel and the L-tunneling in the GO region, in the off-state; and (c) the variation of \( I_{\text{on}}/I_{\text{off}} \) and \( SS_{\text{avg}} \) with \( W_B \) for VPB-EHBTFTET.

### 3.3. Effect of InAlAs-Block on VPB-EHBTFTET

Here, the width and length (\( W_B \) and \( L_s \)) of the In\(_{0.52}\)Al\(_{0.48}\)As-block in the proposed VPB-EHBTFTET are examined to optimize device performance. Figure 8a shows \( I_{\text{on}} \) and \( I_{\text{off}} \) values under different \( W_B \). \( I_{\text{off}} \) gradually decreases with the increase in \( W_B \) but basically maintains stability when \( W_B > 7 \) nm, which can be explained by the contour plots of the nonlocal e-BTBT rate shown in Figure 8b. It is found that both the distribution range and magnitude of the non-local e-BTBT rate reduce with the increase in \( W_B \), which can demonstrate that the increasing \( W_B \) helps to inhibit the P-tunneling in the right side of the GUD region caused by the P-pocket, thereby lowering the \( I_{\text{off}} \). When \( W_B = 7 \) nm, the non-local e-BTBT rate falls sharply due to complete suppression of this type of P-tunneling, thus resulting in several orders of magnitude reduction in \( I_{\text{off}} \). As \( W_B \) goes beyond 7 nm, the In\(_{0.52}\)Al\(_{0.48}\)As-block begins to suppress the P-tunneling in the left side of the GUD region so as to further reduce the non-local e-BTBT rate. Since the \( \lambda \) of the P-tunneling in the left-side channel is very long, the electron tunneling in this region is insignificant. As a result, \( I_{\text{off}} \) is not sensitive to the change in \( W_B \). Moreover, Figure 8a shows that only when \( W_B > 7 \) nm does \( I_{\text{on}} \) begin to decrease. This is because although the In\(_{0.52}\)Al\(_{0.48}\)As-block does not affect the L-tunneling in the GO region, when \( W_B > 7 \) nm, it prevents the tunneling electrons in the left-side channel from drifting to the drain region. As shown in Figure 8c, with the increase in \( W_B \), \( SS_{\text{avg}} \) and \( I_{\text{on}}/I_{\text{off}} \) decreases and increases, respectively, but both take on the opposite trend when \( W_B > 7 \) nm. Thus, the best choice of \( W_B \) is 7 nm.
Next, the influence of $L_B$ on the device performance is investigated. It should be noted that all research results are obtained with the unchanged channel length. Figure 9a shows the $I_{on}$ and $I_{off}$ values under different $L_B$s. $I_{off}$ decreases first with the increase in $L_B$ but basically keeps stable when $L_B > 25$ nm. Since the off-state $P$-tunneling in the right-side channel is affected by the In$_{0.52}$Al$_{0.48}$As-block, its energy band profiles can be calculated to interpret the trend of $I_{off}$. It is observed from Figure 9b that there are two kinds of $P$-tunneling between the $P$-pocket and the GUD region: (1) electrons tunnel from the valence band of the $P$+-pocket into the conduction band of In$_{0.53}$Ga$_{0.47}$As (CBS) (named PCT-tunneling), and (2) electrons tunnel from the valence band of the $P$+-pocket into the conduction band of In$_{0.52}$Al$_{0.48}$As (CBB) (named PBT-tunneling). Due to the wider $E_g$ in the In$_{0.52}$Al$_{0.48}$As and the longer $\lambda$ in the tunneling junction, the effect of PBT-tunneling on $I_{off}$ is negligible. When $L_B = 0$ nm, only the PCT-tunneling exists in the tunneling junction, and its $\Delta \phi$ is the widest; thus, the maximum $I_{off}$ is generated. With the increase in $L_B$, the $\Delta \phi$ of the PCT-tunneling and the PBT-tunneling (i.e., $\Delta \phi_1$ and $\Delta \phi_2$ in Figure 9b) decreases and increases, respectively, and disappears and saturates, respectively, when $L_B \geq 25$ nm. It follows that the PCT-tunneling is gradually suppressed with the increase in $L_B$ and eventually completely replaced by the PCB-tunneling when $L_B \geq 25$ nm, thereby resulting in the change trend of $I_{off}$ shown in Figure 9a. Furthermore, Figure 9a shows that $I_{on}$ is immune to the change in $L_B$, which is because the L-tunneling dominant in the on-state is not affected by the $L_B$. Figure 9c shows that $SS_{avg}$ and $I_{on}/I_{off}$ have the same and opposite change trend as $I_{off}$, respectively. This is because both parameters mainly depend on $I_{off}$, which is closely related to $L_B$. This research demonstrates that good device performance can be achieved when $L_B$ is not less than 25 nm.
To verify the superiority of the introduction of the In$_{0.52}$Al$_{0.48}$As-block, the device performance of the proposed VPB-EHBTFET under lattice mismatch was investigated, and corresponding simulation results are shown in Figure 10. In simulations, the composition of InGaAs is unchanged, while the Al composition (i.e., x) of the In$_{1-x}$Al$_x$As-block changes from 0.2 to 0.8. Considering the strain caused by the lattice mismatch, a strained two-band zincblende model is included in simulations. As shown in Figure 10a, it is observed that the $I_{on}$ is insensitive to x, but the $I_{off}$ decreases first with the increase in x and then basically remains unchanged when $x \geq 0.48$, both of which can be interpreted by the tunneling mechanism. Based on the previous analyses, the In$_{1-x}$Al$_x$As-block located in the right-side GUD region mainly controls the off-state P-tunneling. With the increase in x, the $E_g$ of In$_{1-x}$Al$_x$As increases. According to Equation (1), the increase in $E_g$ benefits to reducing the $P_{tun}$, eventually reducing the $I_{off}$. When $x \geq 0.48$, electrons are difficult to tunnel into the drain across the In$_{1-x}$Al$_x$As-block due to the long $\lambda$ caused by the $E_g$, which makes the $I_{off}$ basically remain stable. It is found from Figure 10b that when $x < 0.48$, $I_{on}/I_{off}$ and $SS_{avg}$ increases and decreases with the increase in x, respectively. As x increases further, both parameters tend to be saturated. Comprehensive analysis shows that good device performance of VPB-EHBTFET can be achieved when $x \geq 0.48$. However, the epitaxial layers with mismatched lattices are prone to defects during growth, which can affect the performance and lifespan of devices. Therefore, In$_{0.52}$Al$_{0.48}$As with $x = 0.48$ is the optimal choice because it matches the lattice of In$_{0.53}$Ga$_{0.47}$As.

4. Conclusions

To sum up, an In$_{0.53}$Ga$_{0.47}$As vertical EHBTFET with a P-`pocket and an In$_{0.52}$Al$_{0.48}$As-block (VPB-EHBTFET) is introduced and investigated by TCAD simulation. Numerical simulations indicate that the adoption of a P-`pocket and In$_{0.52}$Al$_{0.48}$As-block can make
VPB-EHBTFTET simultaneously possess good on-state and off-state performance. Corresponding indicator parameters are $I_{on}$ of $1.04 \times 10^{4}$ A/µm, $I_{off}$ of $1.83 \times 10^{-19}$ A/µm, $I_{on}/I_{off}$ of $5.7 \times 10^{14}$, $SS_{QV}$ of 5.5 mV/dec, and a DIBL value of 7.5 mV/V. Through examining the influence of the $P$-pocket on VPB-EHBTFTET, it results that $C_T$ controls the device performance by affecting the $L$-tunneling, while $W_p$ can simultaneously regulate the $\lambda$ and $\Delta \phi$ of the point tunneling and line tunneling to obtain the optimal on-state performance. Considering the changes in $W_p$ and $L_S$, it is concluded that both mainly control $I_{on}$ through the suppression of the $P$-tunneling in the right-side channel. Moreover, through investigating the effect of the Al composition of the In$_{0.52}$Al$_{0.48}$As-block on the device performance and considering the potential performance degradation caused by lattice mismatch during device manufacturing, the In$_{0.52}$Al$_{0.48}$As-block that matches the lattice of In$_{0.52}$Ga$_{0.48}$As is the optimal choice.

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