

Article

An Adaptive-Output Operational Amplifier for Electrostatic Closed-Loop MEMS Gyroscope Drive Circuits

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Abstract

To address the challenge that microelectromechanical system (MEMS) gyroscope electrostatic force-modulated closed-loop self-excited driving circuits experience significant dynamic variations in capacitive load and driving demand under different operating conditions, such as start-up, steady-state resonance maintenance, and environmental perturbations, making it difficult to simultaneously achieve strong driving capability, stable oscillation, and low power consumption, this paper proposes a high-energy-efficiency adaptive output operational amplifier architecture. Based on a dynamic load-sensing mechanism, the design introduces a three-threshold decision scheme combining a high threshold, a low threshold, and a mid-supply reference voltage. By coordinating a continuous-time voltage detection circuit with a bidirectional shift register, the proposed approach enables accurate identification of the output state and the load level. A time-division-multiplexed two-stage control strategy is adopted to rapidly compensate for the drive capability under abrupt load changes, while proactively disabling redundant output units under steady-state conditions, thereby achieving power delivery on demand. The output stage employs a Class-AB push-pull structure integrating an improved low-leakage single-pole double-throw (SPDT) switch, which hard shuts off the power transistors in the non-operating state to effectively eliminate the subthreshold leakage current. Circuit simulations in a 0.18 μm CMOS process demonstrate that the proposed operational amplifier can adaptively regulate its output current in real time according to variations in the gyroscope driving demand, ensuring sufficient an electrostatic driving force and oscillation stability during transient conditions while significantly reducing static power consumption during the resonance steady state. The proposed design provides an effective solution for high-performance and high-energy-efficiency interface circuit design in MEMS gyroscope electrostatic force-modulated closed-loop self-excited driving systems.

Keywords: front-end circuits; MEMS gyroscope; continuous-time voltage detection circuit

Academic Editor: Ha Duong Ngo

Received: 3 June 2026

Revised: 24 July 2026

Accepted: 24 July 2026

Published: 27 July 2026

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1. Introduction

With the rapid development of advanced intelligent manufacturing and precision engineering, high-performance sensing and control technologies have become increasingly important for achieving accurate motion control and system reliability [1–8]. It has become important tools for solving complex scientific and engineering problems, providing new opportunities for the design and optimization of integrated circuits and MEMS systems [9–12]. Integrated circuits play a particularly important role in sensor applications, especially in high-performance MEMS interface systems [13–15]. In practical applications, electrostatic force-modulated closed-loop self-excited driving circuits for MEMS gyroscopes operate under highly dynamic driving conditions. During start-up and resonance establishment, the drive loop must provide strong transient electrostatic driving capability to rapidly excite the proof mass into stable oscillation. Under steady-state resonance conditions, however, the drive demand decreases significantly, and excessive power consumption should be avoided to improve energy efficiency and thermal stability. Furthermore, variations in the environmental temperature, mechanical disturbances, quality factor (Q-factor), and structural parameter drift may continuously alter the resonant characteristics of the gyroscope, thereby imposing stringent requirements on the driving capability and power adaptability of the interface circuit.

In particular, in high-precision inertial sensing systems, precision signal acquisition, sensor interface circuits, and closed-loop resonant control systems [16], the performance of the front-end operational amplifier in the electrostatic drive loop is especially critical. However, existing operational amplifier designs often struggle to simultaneously achieve strong transient drive capability, stable resonance maintenance, and low power consumption [17–26]. Conventional static output-stage architectures are typically designed for worst-case transient driving conditions to guarantee start-up reliability and disturbance rejection, which inevitably leads to considerable power redundancy during steady-state oscillation. Although several techniques, such as slew-rate-enhancement structures, adaptive biasing, or programmable-gain amplification, improve the transient response or gain flexibility to some extent, their output stages generally remain fixed and cannot dynamically regulate the number of enabled power devices according to real-time variations in the gyroscope drive demand [27]. This fixed-drive strategy not only degrades energy efficiency, but may also result in an insufficient electrostatic driving force or delayed response under abrupt perturbations and resonance fluctuations. The main contribution of this work is an adaptive-output operational amplifier specifically designed for the electrostatic closed-loop drive path of a MEMS gyroscope. The novelty is not the use of a standalone comparator, shift register, or output switch, but the drive-loop-oriented integration of these blocks into an autonomous output-strength regulation mechanism. Different from adaptive-bias amplifiers, the proposed circuit does not primarily regulate the bias current of the core gain stage. Different from slew-rate-enhancement amplifiers, the adaptive action is not limited to transient current injection for improving the large-signal slew rate. Different from conventional programmable output-stage amplifiers, the output-stage control word is not externally assigned as a static configuration. Instead, the proposed three-threshold voltage-detection circuit monitors the output-voltage state with respect to RefH, RefM, and RefL, and the bidirectional shift register retains and updates the enabled output-array state in finite steps. The adaptive Class-AB output array therefore increases the available drive strength under under-drive conditions and disables redundant output units after load relaxation. In addition, the improved SPDT gate-clamping switch forces the gates of disabled PMOS and NMOS power devices to VDD and GND, respectively, thereby suppressing unnecessary static conduction in idle output units. This work is therefore positioned as a drive-loop operational-amplifier block for electrostatic closed-loop MEMS gyroscopes rather than as a complete MEMS gyroscope readout system. Alt-

though adaptive-bias amplifiers and slew-rate enhancement techniques have been extensively investigated to improve transient performance and power efficiency, these approaches generally adjust the bias current while maintaining a fixed output-stage structure. In contrast, the proposed architecture dynamically reconfigures segmented output units according to the required driving capability, enabling adaptive power reduction during steady-state operation while preserving sufficient output current during start-up and transient conditions.

2. Proposed Structure

The proposed adaptive-output operational amplifier architecture is shown in Figure 1. The structure is straightforward and mainly consists of a main operational amplifier, a voltage-detection circuit, a shift-control circuit, and an adaptive-output array, where the main amplifier and the output array form a negative-feedback loop. When the external load requires the operational amplifier to deliver current, the voltage-detection circuit continuously samples the output-voltage variation at the amplifier output and determines the current operating state through internal continuous-time comparators. It controls the bidirectional shift register in the shift-control circuit to switch the output strategy. By receiving the “0” or “1” signal generated by the voltage-detection circuit, the bidirectional shift register dynamically adjusts the number of enabled PMOS/NMOS units in the output array. The shift register outputs a multi-bit digital control word, where each bit controls the switching of one output unit transistor. In this way, different numbers of unit transistors can be turned on in parallel, thereby adjusting the output-driving capability.

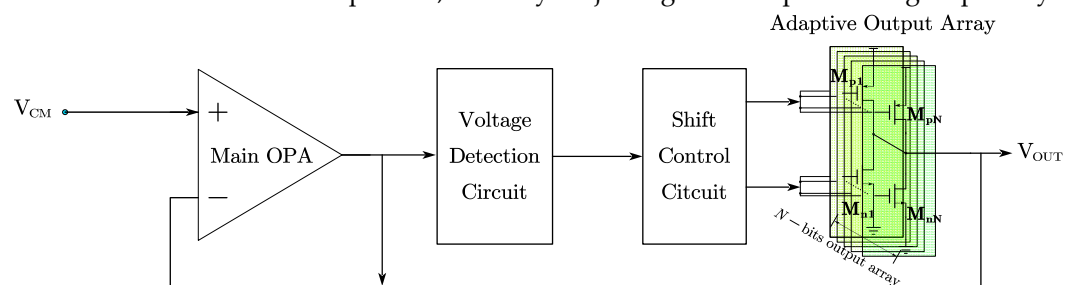


Figure 1. Proposed adaptive output operational amplifier structure.

The proposed regulation scheme should be distinguished from conventional output-current enhancement techniques. In this work, the output stage is treated as a digitally retained, drive-strength-scalable array rather than a fixed-size Class-AB stage assisted by temporary bias boosting. The voltage-detection circuit evaluates the output-voltage deviation relative to three reference levels and converts the analog drive-demand information into discrete control decisions. The bidirectional shift-control circuit then updates the number of enabled output units only when the output voltage leaves the predefined threshold window. Once the output voltage returns to the RefL–RefH window, the current enable state is retained. This finite-step and state-retention behavior is essential for avoiding unnecessary output-stage switching during steady-state resonant operation.

Since conventional detection circuits can only passively increase the drive strength when the output voltage drops under heavy load, yet cannot proactively sense load relaxation and reduce redundant drive current, this design introduces three key reference voltages: the high threshold Ref_H , the low threshold Ref_L , and the mid-supply reference voltage Ref_M . The voltage detection circuit comprises three continuous-time comparators followed by combinational logic. Based on the relationship between V_{out} and these thresholds, the system classifies its operating condition into three regions. The operating states of the proposed system are classified into three distinct regions according to the relationship between the output voltage and the predefined reference thresholds. In the stable region,

where $Ref_L < V_{out} < Ref_H$, the available drive capability is sufficient to maintain loop stability, and no significant adjustment of the output stage is required. When V_{out} falls below Ref_L , the system enters the under-drive region, indicating that the output stage is unable to satisfy the current load demand; in this case, additional transient current must be supplied to restore the output voltage. Furthermore, a load-decision region is defined by introducing a common-mode reference threshold Ref_M . During the subsequent detection period, the comparison between V_{out} and Ref_M enables the system to differentiate between a sustained heavy-load condition and a light-load over-drive condition, thereby providing a quantitative basis for adaptive power regulation and energy-efficiency optimization.

To ensure system stability, this paper proposes a time-division-multiplexed two-stage regulation mechanism. The total number of adaptive array units is defined as N , satisfying $N = 2^j$ ($j > 4$). To balance the response speed and stability, the detection period T_{det} and the shift-control period T_{ctrl} are set to satisfy the following timing constraint:

$$\begin{cases} K = \frac{N}{2} - 1 \\ T_{det} = K \times T_{ctrl} \end{cases} \quad (1)$$

Here, K denotes the maximum number of adjustment steps allowed within a single detection window. This design ensures that, under abrupt load variations, the circuit has a sufficient time window to perform progressive adjustments, thereby avoiding the output oscillations caused by overly aggressive responses. In each operating cycle, the control logic executes in two phases according to the timing sequence. Let $\Delta M[n]$ denote the change in the number of activated units during the n -th control period.

In Phase 1, i.e., during the first detection period, the system primarily checks whether the output voltage deviates excessively, with the goal of quickly pulling the output voltage back to the target range, as follows:

$$\Delta M[n] = \begin{cases} +1, & V_{out} < Ref_L \text{ (Pull Up)} \\ +1, & V_{out} > Ref_H \text{ (Pull Down)} \\ 0, & Ref_L \leq V_{out} \leq Ref_H \end{cases} \quad (2)$$

In this phase, once an out-of-range output voltage is detected, the shift register performs finite stepwise shifting at the control-clock edges for up to K cycles, enabling the output units one by one until the output voltage returns to the safe Ref_L – Ref_H window.

In Phase 2, i.e., during the second detection period, the system compares the output with Ref_M to make a second decision, leading to the following:

$$\Delta M[n] = \begin{cases} +1, & V_{out} \leq Ref_M \text{ (High Load)} \\ -1, & V_{out} > Ref_M \text{ (Low Load/Over Drive)} \\ 0, & \text{Other} \end{cases} \quad (3)$$

This logic indicates that if V_{out} remains higher than Ref_M in the pull-current mode, the available drive capability is excessive relative to the load. In this case, the system performs a reverse shifting operation to progressively turn off redundant power units, thereby achieving power delivery on demand.

The output array adopts a Class-AB push–pull output stage, which offers low power consumption and strong drive capability. Here, M_p/M_n form the static output stage, while P_{out}/N_{out} constitute the adaptive output stage. The drive strength can be controlled by adjusting the number of transistor fingers, and the total output current is jointly provided by the static output stage and N parallel adaptive units, as expressed by the following:

$$I_{Sum_out}(t) = I_n + \sum_{i=1}^{M(t)} I_{out} \quad (4)$$

where I_n denotes the current of a single output unit, and I_{out} represents the total output current formed by the parallel combination of multiple units. To further reduce standby

power consumption, each output unit integrates an improved single-pole double-throw (SPDT) switch module. Unlike conventional approaches that merely disconnect the signal path, this design implements a hard shut-off function using a multiplexer and an inverter. When an output unit is determined to be in the “static” state, the SPDT switch forcibly pulls the gate of the PMOS power transistor to V_{DD} and the gate of the NMOS power transistor to GND. This completely eliminates leakage current of the power devices in the subthreshold region, ensuring that the static power of idle array units under light-load operation approaches zero, thereby significantly improving the overall energy efficiency. The improved SPDT switch is shown in Figure 2.

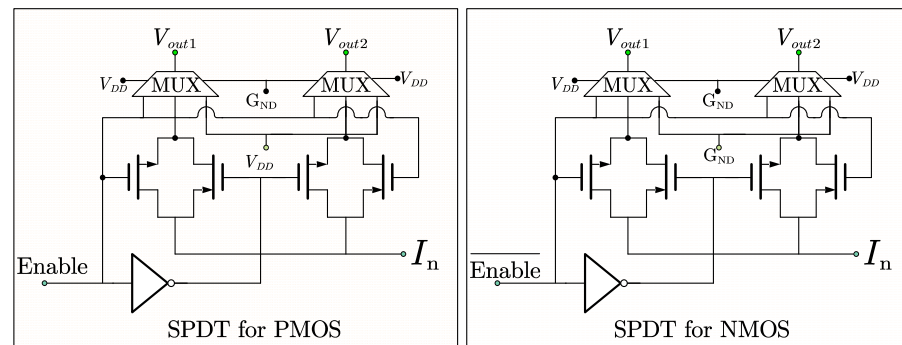


Figure 2. Improved SPDT switch (single-pole double-throw).

3. Design and Implementation of Key Circuit Modules

This work presents the transistor-level implementation of the key modules, including the main amplifier stage, a high-speed low-power continuous-time comparator, and an output array with low-leakage switches. The detailed circuit schematic is shown in Figures 3 and 4. In this design, a commonly used PMOS-input folded-cascode operational amplifier architecture is employed. This module mainly consists of a startup circuit, a current reference circuit, a bias circuit, and a folded-cascode amplifier. Based on small-signal analysis, the gain of this structure can be expressed as follows:

$$\begin{aligned}
 A_{v,total} &= A_{v1} \cdot A_{v2} \\
 A_{v1} &\approx -g_{mp12} [g_{mn14} r_{on14} (r_{op12} \parallel r_{on13}) / (g_{mp14} r_{op14} r_{op13})] \\
 A_{v2} &\approx -m (g_{mpout} + g_{mnout}) \frac{r_{oPout} / r_{oNout}}{m}
 \end{aligned} \quad (5)$$

Here, m represents the number of transistors turned on in the array, g_{mp12} denotes the transconductance of the input differential pair, and r_o is the output resistance. This stage provides the dominant low-frequency gain, ensuring the accuracy of the closed-loop system, and drives the subsequent voltage detection circuit.

To accurately capture small voltage deviations within a nanosecond time scale and effectively suppress kickback noise, an improved three-stage cascaded current-comparator architecture is adopted. This topology mainly consists of an input preamplifier stage, a positive-feedback decision latch stage, and an output buffer stage. The preamplifier as shown in Figure 4 is formed by transistors M_1 – M_7 . Transistors M_5 and M_6 sense the output voltage, which is converted into current through M_2 and M_3 . By leveraging the replication property of the current mirror, the input voltage variation is translated into constant drive currents I_1 and I_2 , which are injected into the subsequent positive-feedback decision latch stage.

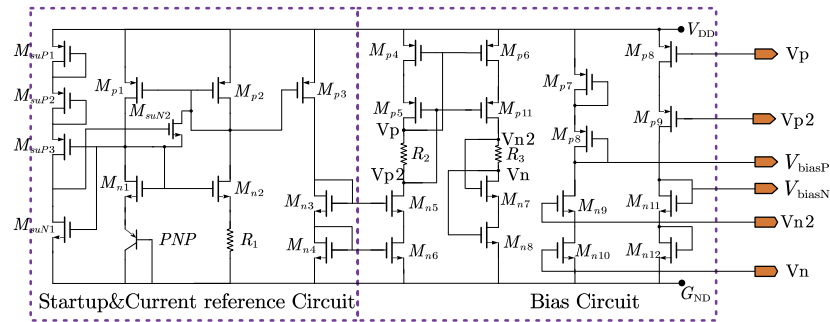


Figure 3. Schematic of bias circuit.

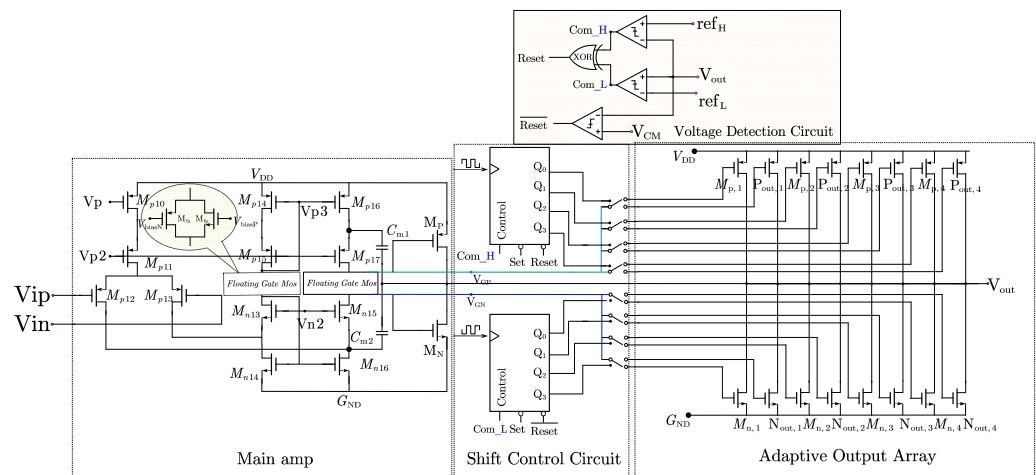


Figure 4. Schematic of the adaptive-output operational amplifier.

As shown in Figure 5 the positive-feedback decision latch stage consists of a positive-feedback loop formed by transistors M8~M12. The circuit exploits the positive-feedback gain provided by the cross-coupled structure to accelerate the voltage transition at the internal nodes. The voltage response at latch nodes C and D depends on the degree of imbalance between the input currents. In the initial state, assuming that the circuit is perfectly symmetric, i.e., $g_{m9} = g_{m12}$ and $g_{m10} = g_{m11}$, Kirchhoff's current law yields the small-signal behavior of the node voltages as follows:

$$\begin{cases} v_C = \frac{g_{m9}}{g_{m9}^2 - g_{m11}^2} \left[I_1 - \frac{g_{m11}}{g_{m9}} I_2 \right] \\ v_D = \frac{-g_{m11}}{g_{m9}^2 - g_{m11}^2} \left[I_1 - \frac{g_{m9}}{g_{m11}} I_2 \right] \end{cases} \quad (6)$$

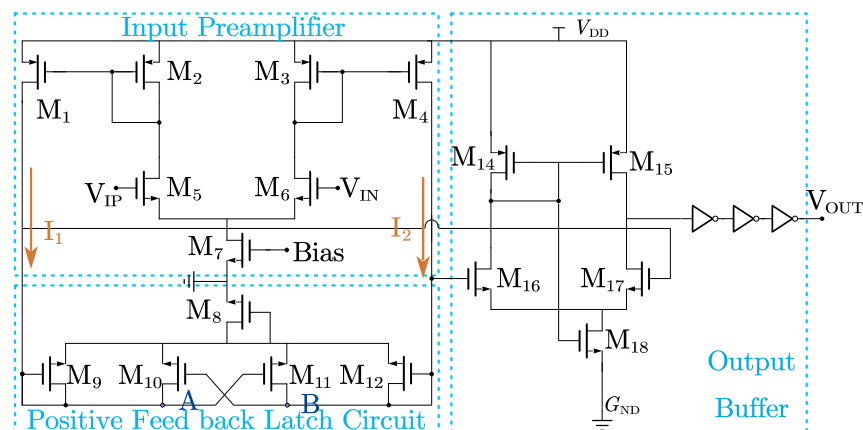


Figure 5. High-speed low-power continuous-time comparator.

Here, g_{m9} and g_{m10} denote the transconductances of the load transistors and the cross-coupled transistors, respectively, while I_1 and I_2 are the injected currents converted from the input voltage. Similarly, the large-signal behavior of this structure can be expressed as follows:

$$\begin{cases} V_A = V_{th} + \sqrt{\frac{K_{n9}}{K_{n9}^2 - K_{n11}^2} \left(I_1 - \frac{K_{n11}}{K_{n9}} I_2 \right)} \\ V_B = V_{th} + \sqrt{\frac{K_{n11}}{K_{n9}^2 - K_{n11}^2} \left(\frac{K_{n9}}{K_{n11}} I_2 - I_1 \right)} \end{cases} \quad (7)$$

where $K_n = \frac{1}{2} \mu C_{ox} \frac{W}{L}$. This expression indicates that the node voltages vary nonlinearly with the input current difference. When $g_{m9} > g_{m11}$, the positive-feedback mechanism of this structure rapidly amplifies the branch current mismatch; this condition can be achieved by adjusting the W/L ratios of $M_9 \sim M_{12}$. The output buffer stage consists of transistors $M_{14} \sim M_{17}$ and a three-stage inverter chain. The self-biased OTA formed by $M_{14} \sim M_{17}$ increases the comparator's conversion gain and effectively suppresses common-mode noise, while the inverters mainly serve as a digital buffer to quantize the OTA's analog output into digital logic levels for controlling the subsequent shift-register logic.

As shown in Figure 6, the adaptive output array consists of N adaptive-output units connected in parallel. Each adaptive unit contains a pair of static output transistors, $M_{p,i}$ and $M_{n,i}$, together with a pair of Class-AB push-pull output transistors, namely the pull-up PMOS power transistor $P_{out,i}$ and the pull-down NMOS power transistor $N_{out,i}$. The drains of these four transistors are directly connected to the output node V_{out} of the operational amplifier. The improved single-pole double-throw (SPDT) switch is placed in the gate-control path of the output-unit transistors and is used to select the connection state of the transistor gates. When the adaptive unit is enabled, the SPDT switch connects the gates of $P_{out,i}$ and $N_{out,i}$ to the PMOS and NMOS gate-drive signals generated by the main output stage, respectively, namely the floating gate voltages V_{GP} and V_{GN} produced by the push-pull stage of the preceding operational amplifier. As a result, the unit participates in Class-AB push-pull amplification. In this operating state, the output current is provided through the source-drain paths of $P_{out,i}$ or $N_{out,i}$, rather than being transmitted through the SPDT switch itself. Specifically, when the output node requires pull-up current, the enabled PMOS output unit supplies the current to V_{out} . Conversely, when the output node requires pull-down current, the enabled NMOS output unit sinks the current from V_{out} . Under light-load or standby conditions, the digital control signal generated by the shift register disables redundant adaptive units. In this case, the SPDT switch clamps the gate of the PMOS power transistor to VDD and the gate of the NMOS power transistor to GND, ensuring that both $P_{out,i}$ and $N_{out,i}$ are strongly turned off. Through this gate-clamping mechanism, the subthreshold leakage current of idle output units is effectively suppressed, while the introduction of additional series switch resistance at the main output node is avoided.

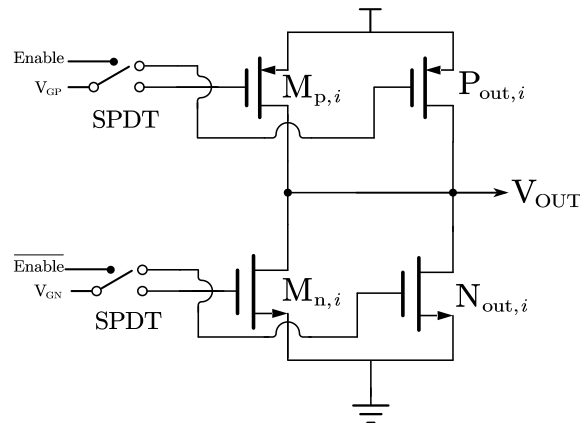


Figure 6. Adaptive output unit.

Conventional Miller compensation realizes dominant-pole compensation through the pole-splitting effect. However, because the compensation capacitor C_C is directly connected between the first-stage high-impedance output node and the second-stage output node, it bypasses the second-stage transconductance path and forms a feedforward path. This feedforward path usually introduces a right-half-plane zero, resulting in additional phase lag, a reduced phase margin, and degraded system stability. To eliminate this right-half-plane zero, the conventional approach typically requires a series zero-nulling resistor. Since this work adopts a cascode structure, cascode compensation is employed to avoid the stability issue caused by the direct feedforward path in conventional Miller compensation, as illustrated in Figure 7. The compensation capacitors are connected from the low-impedance nodes of the PMOS cascode current-source branch and the NMOS cascode current-source branch to the output node, respectively. Because the compensation current is first injected into the low-impedance source node of the cascode device and then affects the output node through the current-buffering action of the cascode branch, this structure can significantly suppress the direct feedforward effect associated with conventional Miller compensation. In addition, the output stage in this work is not a fixed-size structure, but consists of multiple adaptive-output units connected in parallel. As the number of enabled output units m changes, the equivalent transconductance, output resistance, and output parasitic capacitance of the output stage also change, causing the locations of the non-dominant pole and zero to move with the output-stage configuration. Therefore,

$$\begin{aligned} g_{m2,tot} &= m(g_{mPout,i} + g_{mNout,i}) \\ R_{2,tot} &= \frac{r_{oPout,i} // r_{oNout,i}}{m} \\ C_{2,tot} &= m(C_{Pout,i} + C_{Nout,i}) \end{aligned} \quad (8)$$

where m denotes the number of currently enabled adaptive-output units; $g_{mPout,i}$ and $g_{mNout,i}$ represent the small-signal transconductances of the PMOS output transistor and NMOS output transistor in a single adaptive unit, respectively; and $r_{oPout,i}$ and $r_{oNout,i}$ represent their small-signal output resistances, respectively. As m increases, both the equivalent transconductance and the equivalent output conductance of the output stage increase, thereby enhancing the output driving capability.

activating the subsequent control circuitry. All current values reported in this paper refer either to simulated load conditions or measured supply currents, as explicitly indicated.

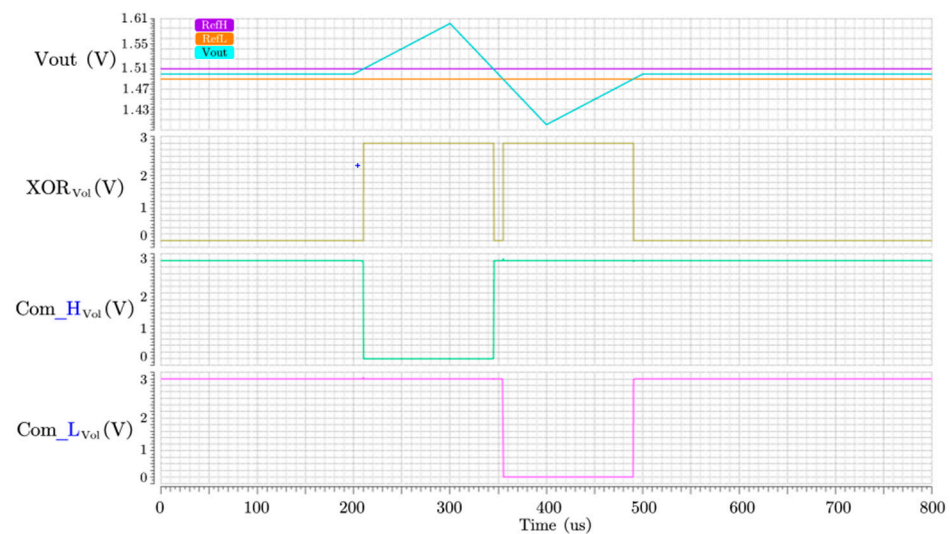


Figure 8. Simulation Results of Voltage Detection Circuit.

The bidirectional shift-register simulation waveform is shown in Figure 9. It can be observed that in the initial stage, when the XOR output is 0, the shift register defaults to output “1”; in this case, the register drives the SPDT switch to turn on the static output transistors. When the XOR output becomes 1, the shift register shifts left or right (P1, P2) under the control of the threshold comparators. During T_1 , an under-drive condition is detected and the shift register performs a right-shift operation driven by the clock, indicating that the system is progressively enabling PMOS power units to increase pull-current capability. During T_2 , an “over-drive” condition after load relaxation (i.e., V_{out} exceeds Ref_M) is emulated; within the decision window, the shift register performs a left-shift operation to progressively disable higher-order outputs. These results demonstrate that the circuit can proactively withdraw redundant drive when the load becomes lighter. To further validate the effectiveness of the two-stage control strategy under complex operating conditions, detailed transient response waveforms of the system from T_3 to T_7 are extracted. These waveforms capture the complete closed-loop process, from large-current establishment to steady-state locking and then to energy-efficiency optimization.

Finally, a full-system simulation is performed. The simulation testbench is shown in Figure 10, where the operational amplifier is configured as a unity-gain buffer, forcing the output to $V_{OUT} \approx V_{CM}$.

Because both ω_{p1} and ω_{p2} are affected by the output-array configuration and parasitic parameters, the worst-case stability condition cannot be accurately determined using only analytical approximations. Therefore, STB simulations under different adaptive output configurations were further performed in Cadence Virtuoso. During the simulations, the shift register was fixed, and different numbers of enabled output units m were set. The simulation results are shown in the Figure 11.

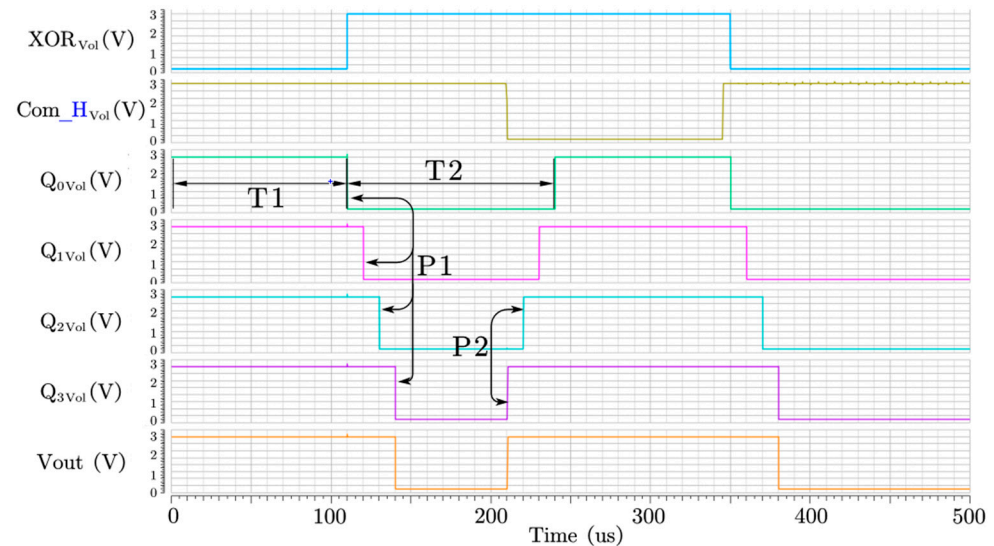


Figure 9. Simulation results of the bidirectional shift register. The blue, yellow, green, magenta, cyan, purple, and orange lines represent XOR_{Vol} , Com_H_{Vol} , Q_{0Vol} , Q_{1Vol} , Q_{2Vol} , Q_{3Vol} , and V_{out} , respectively.

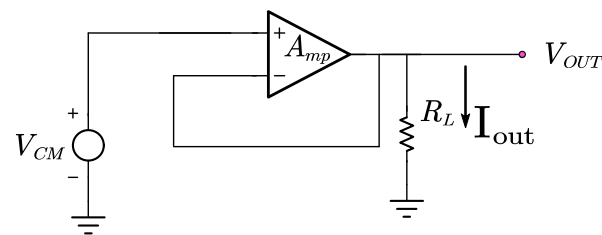


Figure 10. Unity-gain buffer testbench for adaptive-output transient simulation.

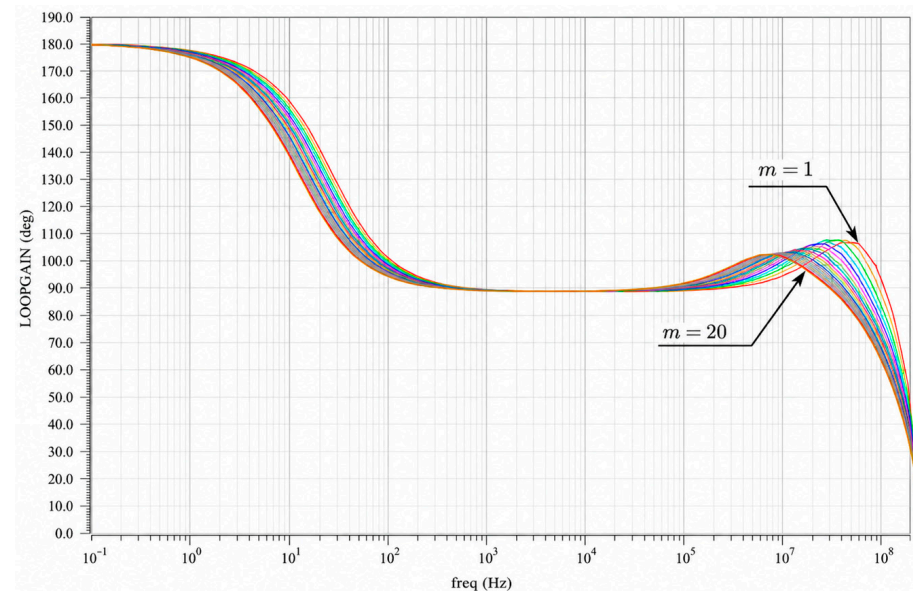


Figure 11. Frequency compensation simulation.

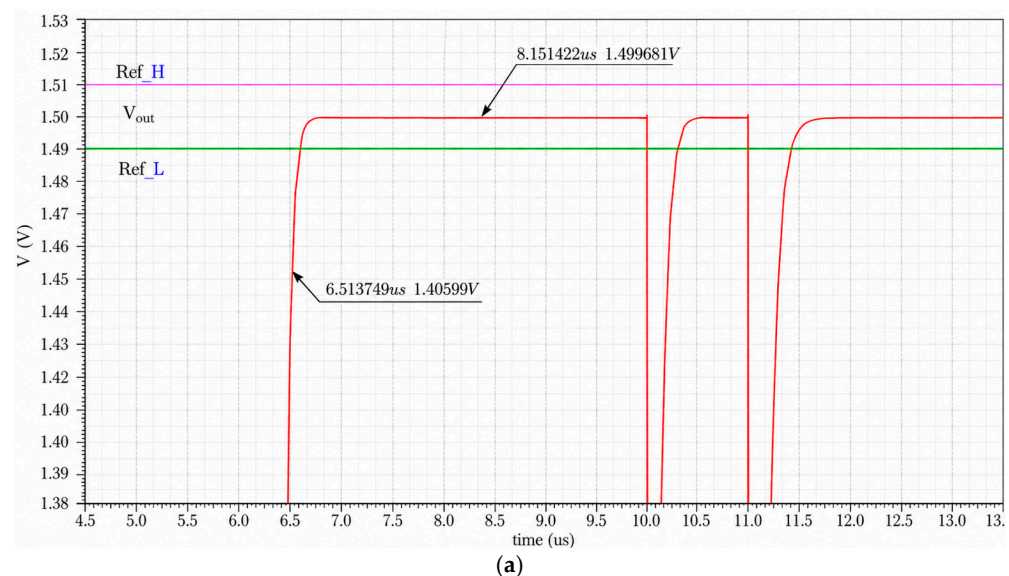
It can be observed that, as the number of enabled output units m increases, the phase-lead behavior in the phase curve appears at a lower frequency, indicating that the zero location or non-dominant pole location of the system shifts with the output-stage configuration. This phenomenon is mainly related to the gate-drain parasitic capacitance of the adaptive output transistors and the equivalent conductance at the output node. On the one hand, enabling more output transistors increases the equivalent gate-drain feedfor-

ward capacitance, which shifts the associated left-half-plane zero to a lower frequency and therefore provides the phase lead earlier. On the other hand, enabling more output transistors also increases the equivalent conductance at the output node, pushing the output-related non-dominant pole to a higher frequency and reducing the phase lag around the unity-gain frequency. These two effects jointly increase the phase margin as m increases.

Although the STB simulation verifies the small-signal stability under fixed output-stage configurations, it does not directly evaluate the nonlinear switching behavior caused by the adaptive enabling and disabling of output cells. Therefore, a transient stability simulation was further performed to examine whether the proposed threshold-based control may introduce repetitive switching or limit-cycle oscillation near the threshold boundaries.

The internal enable states of the adaptive-output array are not directly accessible during the MEMS gyroscope measurement. Therefore, the measured gyroscope oscillation is used only to verify that the proposed drive amplifier can support stable closed-loop resonant operation. The adaptive enable/disable behavior is verified separately through a transistor-level transient simulation, where the voltage-detection output, shift-register states, enabled output units, and output current can be observed. To evaluate the transient stability of the adaptive output regulation under nonlinear switching conditions, a pull-up load transient simulation was performed. The operational amplifier was configured as a unity-gain buffer, and the output node was connected to a time-varying load to emulate a sudden increase in source-current demand. As shown in Figure 12a, the output voltage initially drops below Ref_L , indicating that the available pull-up capability is insufficient. The voltage-detection circuit therefore identifies an under-drive condition and activates the PMOS-side shift-register control.

The corresponding enable states and output current are shown in Figure 12b. During the under-drive interval, the PMOS output units are enabled step by step at the control-clock edges, and I_{out} increases accordingly. As the pull-up current increases, V_{out} gradually recovers toward the threshold window. Once V_{out} returns to the region between Ref_L and Ref_H , the shift register retains the current enable word, and no further PMOS output units are activated. The output current also reaches a stable value corresponding to the applied load condition. These results confirm that the proposed adaptive output regulation completes only finite state transitions during the out-of-range interval. After the output voltage returns to the threshold window, the output-stage configuration is retained rather than repeatedly toggled. Therefore, no persistent current spikes, repetitive enable-state transitions, or sustained limit-cycle oscillation are observed in the nonlinear switching transient.



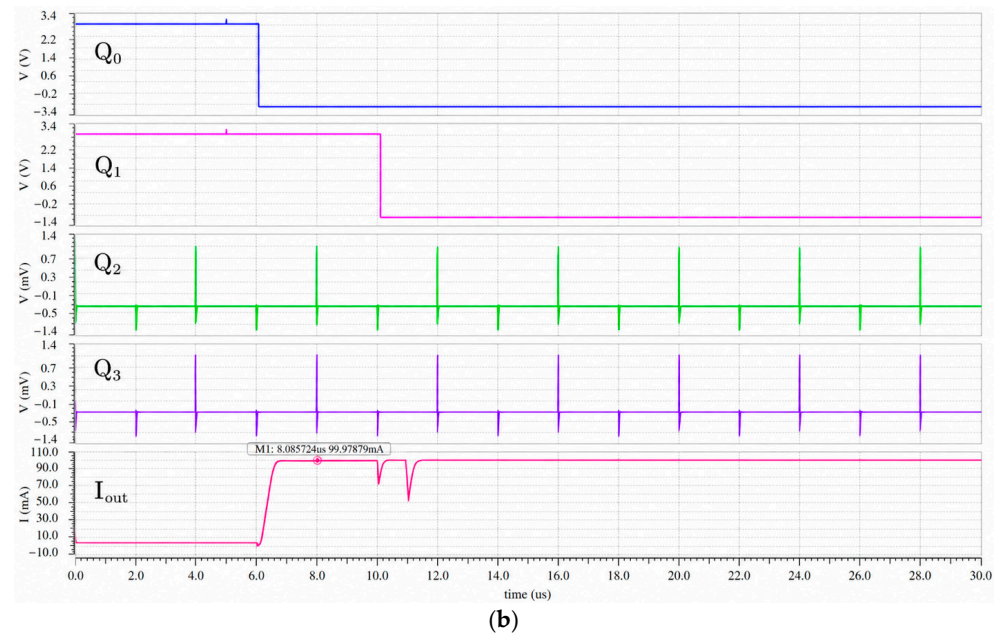


Figure 12. Transistor-level transient simulation of nonlinear adaptive pull-up switching. (a) Output voltage V_{out} and the reference thresholds $RefH$ and $RefL$. (b) Voltage-detection output, simulated shift-register states Q_0 – Q_3 , and simulated output current I_{out} .

In an electrostatic MEMS gyroscope, the drive electrode is primarily a capacitive load rather than a resistive load. The electrical load seen by the drive amplifier can be approximated as the MEMS drive-electrode capacitance together with routing, pad, and interface parasitic capacitances, expressed as follows:

$$C_L = C_{MEMS} + C_{par} \quad (12)$$

The electrostatic drive force is related to the drive voltage by

$$F_{elec} = \frac{1}{2} \frac{dC(x)}{dx} V_{drive}^2 \quad (13)$$

Indicating that the mechanical driving force is nonlinear with respect to the voltage. Therefore, the resistive-load simulation is used only to verify the output-current-regulation mechanism, while the capacitive-load simulation is used to evaluate the stability of the amplifier under a MEMS-equivalent electrode load.

Additional STB simulations were performed by connecting capacitive loads at the amplifier output. The operational amplifier was configured as a unity-gain buffer with $V_{DD} = 3$ V and $V_{CM} = 1.5$ V. The load capacitance was swept from 10 pF to 50 pF to emulate the equivalent MEMS drive-electrode capacitance together with the parasitic capacitance introduced by interconnects, pads, and interface nodes. This capacitive-load condition directly evaluates the additional phase shift introduced at the amplifier output.

The simulated STB results are summarized in Table 1. As C_L increases from 10 pF to 50 pF, the phase margin decreases from 93.582° to 85.062° , indicating that the capacitive load introduces additional phase lag, as expected. Meanwhile, the gain-margin frequency shifts from 90.041 MHz to 39.995 MHz, which is consistent with the movement of the output-related pole caused by the increased capacitive loading. Nevertheless, over the entire simulated capacitance range, the phase margin remains higher than 85° , and the gain margin remains higher than 12.7 dB. These results confirm that the proposed adaptive-output operational amplifier maintains a sufficient stability margin under the simulated MEMS-equivalent capacitive-load conditions.

Table 1. Stability simulation results under capacitive loads.

CL	PM (deg)	PM Frequency	GM (dB)	GM Frequency
10 pF	93.582	8.3889 MHz	14.182	90.041 MHz
20 pF	91.595	8.2707 MHz	13.508	64.078 MHz
30 pF	89.495	8.4847 MHz	13.226	52.078 MHz
40 pF	87.294	8.5966 MHz	12.742	44.423 MHz
50 pF	85.062	8.6341 MHz	12.966	39.995 MHz

To quantitatively evaluate the energy-efficiency improvement provided by the proposed adaptive output regulation, the supply current and average power consumption were compared with those of a fixed-output-stage counterpart. In the fixed-output-stage configuration, all adaptive-output units were kept enabled to provide a constant high-drive capability, while the main amplifier, bias circuit, compensation network, supply voltage, and load conditions were kept unchanged. Therefore, this comparison directly reflects the power reduction achieved by dynamically disabling redundant output units.

The supply current was extracted from the 3 V voltage source in the transient simulation. The output load current was used only to define the load condition, whereas the power consumption was calculated from the supply current. The average power consumption was calculated as

$$P_{\text{avg}} = V_{DD} \cdot \frac{1}{T} \int_0^T I_{DD}(t) dt \quad (14)$$

The light-load condition corresponds to $I_{\text{load}} = 1$ mA, for which the intrinsic Class-AB output stage can maintain V_{out} within the (Ref_L)–(Ref_H) window without enabling additional adaptive output units. The regulated heavy-load condition corresponds to $I_{\text{load}} = 3$ mA, for which additional adaptive output units are enabled and then retained after V_{out} returns to the threshold window. To avoid possible misunderstanding, it should be emphasized that the previously reported 400 mA current does not represent the actual continuous output current delivered by the proposed operational amplifier. Instead, it originated from an intermediate design description and could be misinterpreted without sufficient explanation. Since this value does not correspond to the practical operating condition of the fabricated circuit, the related statement has been removed in the revised manuscript. The adaptive-output mechanism is evaluated using representative load-current conditions that emulate different output driving requirements. Therefore, the proposed architecture should be understood as a dynamically configurable output-stage design for improving power efficiency rather than a high-current output amplifier intended to continuously source hundreds of milliamperes.

The previous description of the 400 mA current has been corrected to avoid ambiguity. Throughout the revised manuscript, the adaptive-output capability is evaluated under representative operating conditions that are consistent with the intended application of electrostatic MEMS gyroscope driving circuits.

The power-comparison results are summarized in Table 2. Under the light-load condition, the proposed adaptive-output design reduces the average power consumption from 4.007 mW to 3.212 mW, corresponding to a (19.84%) reduction compared with the fixed-output-stage counterpart. Under the regulated heavy-load condition, the average power consumption is reduced from 10.92 mW to 10.04 mW, corresponding to an (8.06%) reduction. These results confirm that the proposed adaptive output regulation reduces unnecessary static power consumption under light-load operation while preserving sufficient drive capability when the load demand increases.

Table 2. Power-consumption comparison between the adaptive and fixed-output-stage amplifiers.

Condition	Load Current	$I_{DD,avg}$	P_{avg}	$I_{DD,avg,fixed}$	$P_{avg,fixed}$
Light load	$I_{out} = 1 \text{ mA}$	1.071 mA	3.212 mW	1.336 mA	4.007 mW
Regulated heavy load	$I_{out} = 3 \text{ mA}$	3.347 mA	10.04 mW	3.640 mA	10.92 mW

The statistical results of the key performance metrics are summarized in Table 3. In terms of process-corner verification, PVT simulations were performed, covering three process corners (TT/SS/FF), three supply voltages (2.7/3.0/3.3 V), and three temperatures (−40/27/125 °C), resulting in a total of 27 conditions. The results show that the gain varies from 104.046 to 115.09 dB, the GBW ranges from 11.897 to 22.7 MHz, the phase margin varies from 79.91° to 86.35°, and the slew rate ranges from 11.4 to 24.8 V/μs. The worst-case conditions mainly occur at a low supply voltage, a high temperature, and the SS process corner. Nevertheless, the circuit remains stable under all tested conditions, with the phase margin always greater than 79°, indicating that the design exhibits good robustness against process, voltage, and temperature variations. The detailed parameters are listed in Table 4.

Table 3. Operational Amplifier Performance Parameters.

Performance Parameters	Simulation Results
GBW	17.14 MHz
Phase Margin	85.73 Deg
Gain	109 dB
SR	14.5 V/μs
Output range	0–2.42 V
CMRR	93 dB
PSRR	115 dB

Table 4. Performance of the Operational Amplifier under Different PVT Conditions.

Parameter	Min	Max	Worst Corner
DC Gain (dB)	104.046	115.09	ff, 2.7, 125 °C
GBW (MHz)	11.897	22.7	ss, 2.7, 125
Phase Margin (deg)	79.91	86.35	ss, 2.7, 125
Slew Rate (V/μs)	11.4	24.8	ss, 2.7, 27

The simulated input-referred offset has a mean value of 241.9 μV and a standard deviation of 2.76 mV. Since the nominal threshold window is $RefM \pm 10 \text{ mV}$, the 3σ offset level is approximately 8.28 mV, which remains below the nominal half-window. Therefore, under the simulated mismatch condition, the offset mainly shifts the effective switching boundary rather than eliminating the detection window. However, when V_{out} is very close to $RefH$ or $RefL$, comparator offset and threshold variation may cause early or delayed switching by one or several control-clock cycles. The retained shift-register state helps prevent continuous toggling after V_{out} returns to the $RefL$ – $RefH$ window. This result also indicates that further reduction of the threshold window would require additional offset calibration, hysteresis, or a larger design margin. In addition, Monte Carlo simulations were included to evaluate the impact of device mismatch on the offset voltage, and the statistical results along with the distribution plot have been added to the revised manuscript. Two hundred Monte Carlo runs were performed to assess the input offset voltage of the operational amplifier under process variations and local mismatch conditions as shown in Figure 13. The simulation results indicate that the mean offset voltage is approximately 241.9 μV, with a standard deviation of 2.76 mV. This analysis further illustrates the bias sensitivity and statistical behavior of the circuit under random mismatch conditions. Future work will extend the statistical analysis to the complete adaptive decision

path, including comparator offset, reference mismatch, hysteresis design, and false-switching probability.

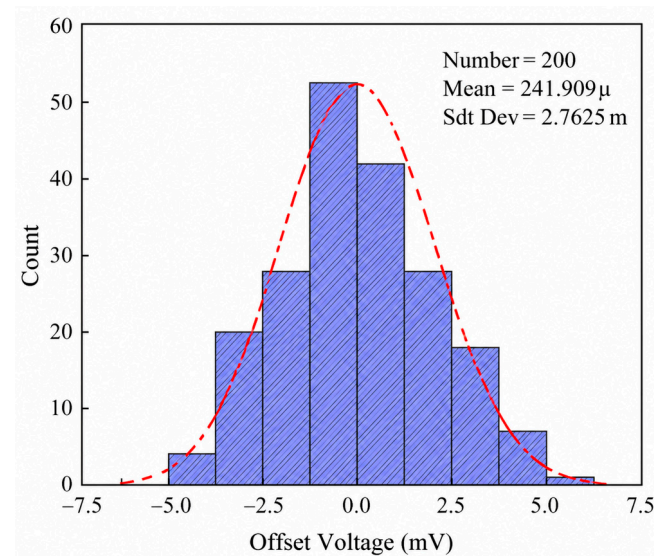


Figure 13. Monte Carlo Simulation of the Operational Amplifier Offset Voltage.

It should be noted that the proposed adaptive-output mechanism is an internal circuit function implemented by the digital control logic and segmented output stage. Since no dedicated observation nodes were reserved in the fabricated prototype, the internal adaptive switching states cannot be directly measured experimentally. Therefore, transistor-level simulations are employed to verify the adaptive operation, whereas the fabricated chip measurements demonstrate the practical applicability of the proposed amplifier in the electrostatic MEMS gyroscope drive loop.

To verify the functionality of the proposed circuit, the adaptive-output operational amplifier for the MEMS gyroscope was fabricated using the SMIC standard 0.18 μm CMOS process. The ASIC chip was mounted on a custom-designed PCB, as shown in Figure 14. The chip area is approximately 0.7 mm $\times$ 0.7 mm. Wire bonding was performed using a wedge bonder to connect the 33 pad points on the ASIC chip to the corresponding pads on the PCB with aluminum–silicon bonding wires. The assembled system was then used for experimental testing.

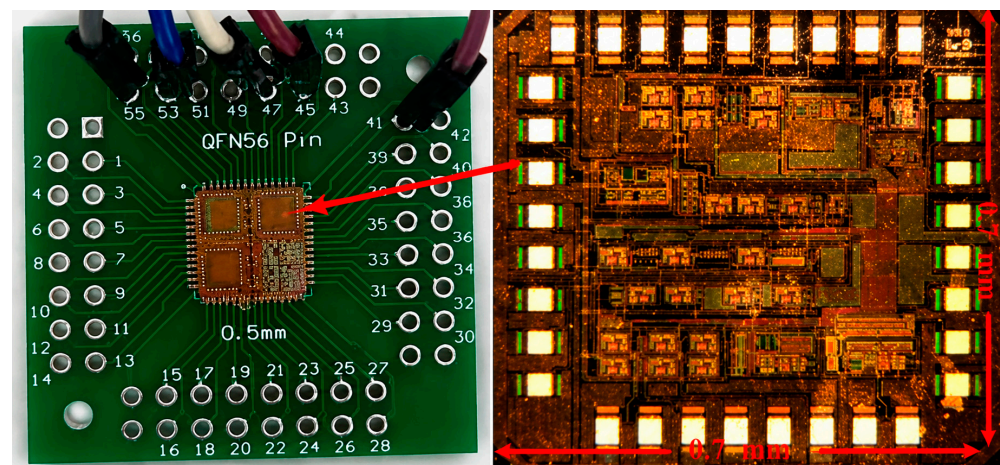


Figure 14. The photograph of the PCB and ASIC chip.

To evaluate the electrostatic force-modulated closed-loop self-excited driving performance of the proposed MEMS gyroscope interface ASIC, experimental measurements

were carried out using a dynamic signal analyzer (HP 35670A, Hewlett-Packard, Palo Alto, CA, USA) and an oscilloscope (TDS2012B, Tektronix, Beaverton, OR, USA). In the proposed driving scheme, a high-frequency square-wave carrier generated by the ASIC was employed to modulate the proof-mass velocity signal, and the modulated driving voltage was subsequently applied to the gyroscope driving comb electrodes to realize electrostatic force excitation. The measured proof-mass velocity signal waveform based on the electrostatic force-modulated closed-loop self-excited driving principle is shown in Figure 15. It can be observed that the gyroscope successfully achieves stable self-excited oscillation under atmospheric pressure conditions. The measured waveform exhibits a highly periodic and continuous resonant signal with no obvious amplitude collapse, waveform distortion, or oscillation interruption, indicating that the proposed interface ASIC can effectively sustain resonant motion through closed-loop electrostatic force compensation. Moreover, the measured resonant frequency is approximately 4.077 kHz, which agrees well with the designed operating condition of the gyroscope resonator. The stable sinusoidal-like waveform and consistent oscillation period further demonstrate that the proposed closed-loop driving circuit is capable of maintaining steady resonant operation and suppressing the resonance instability caused by environmental disturbances or energy dissipation. These results verify the feasibility and effectiveness of the proposed electrostatic force-modulated self-excited drive architecture for MEMS gyroscope applications.

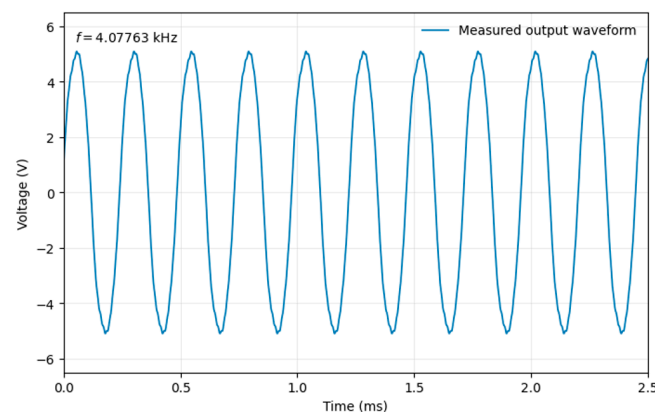


Figure 15. Measured time-domain waveform of the proof-mass velocity signal under electrostatic force-modulated closed-loop self-excited driving.

The frequency-domain response of the proof-mass velocity signal under electrostatic force-modulated closed-loop self-excited driving was further characterized using a dynamic signal analyzer (HP35670A), and the measured spectrum is shown in Figure 16. A distinct and sharp resonance peak can be observed at approximately 4.077 kHz, indicating that the proposed interface ASIC successfully excites and maintains stable resonant oscillation of the MEMS gyroscope under atmospheric pressure conditions. The measured spectrum exhibits strong spectral concentration around the resonant frequency with a relatively low noise floor and no noticeable parasitic oscillation components, demonstrating the effective suppression of resonance disturbances and stable closed-loop operation. To quantitatively evaluate the oscillation stability, the displacement amplitude stability of the proof mass was measured using the voltage mode of an Agilent 34410A digital multimeter. The measured voltage fluctuation was below 0.2 mV relative to an AC driving amplitude of 5.7 V, corresponding to an amplitude stability of approximately 0.005%. In addition, the frequency stability of the velocity signal was evaluated using the frequency measurement mode of the digital multimeter (Agilent 34410A, Agilent Technologies, Santa Clara, CA, USA.) Experimental results show that the resonant frequency remained centered at

4.077 kHz with a fluctuation lower than 0.1 Hz over a 15 min observation period, corresponding to a relative frequency stability of approximately 25 ppm. These results demonstrate that the proposed electrostatic force-modulated closed-loop self-excited driving architecture achieves stable amplitude and frequency control, enabling robust and reliable operation of the MEMS gyroscope under atmospheric conditions.

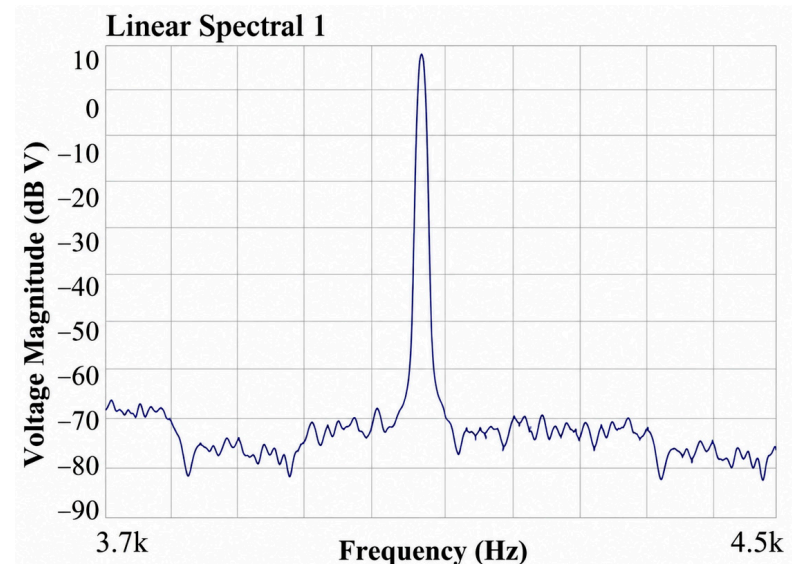


Figure 16. Measured frequency spectrum of the proof-mass velocity signal under electrostatic force-modulated closed-loop self-excited driving.

We have added a comparison table with existing works, as shown in Table 5. The results demonstrate that the proposed design achieves high gain, a large phase margin, and good CMRR/PSRR performance in a 180 nm process, while also providing a certain level of load-driving capability. The present comparison focuses on circuit-level verification rather than complete system-level energy characterization.

Table 5. Comparison with Reported Works.

Parameter	This Work	[28]	[29]	[30]
Supply(V)	3	1.8	1.3–2.5	0.4
CMRR(dB)	93	81	/	76.28
PSRR(dB)	115	94	/	/
DC gain(dB)	109	80	85	70.26
Output range(V)	0.2–2.8	/	0–0.55	/
Phase Margin	85	63	57	61
Gain Bandwidth(MHz)	17.14	0.214	/	1.21
Slew Rate(V/ μ s)	14.5	2.3	/	17.07
Process(nm)	180	180	65	180

5. Conclusions

The proposed adaptive-output operational amplifier was implemented and evaluated as a circuit block for the electrostatic closed-loop drive path of an MEMS gyroscope. Circuit-level simulations verify the adaptive output regulation, capacitive-load stability, nonlinear switching behavior, and supply-power reduction relative to a fixed-output-stage counterpart. The MEMS gyroscope measurement confirms the stable closed-loop resonant operation supported by the proposed drive amplifier, while the internal adaptive enable/disable behavior is verified through a transistor-level simulation. By employing a

three-threshold decision mechanism with $\text{RefH} = 1.51 \text{ V}$, $\text{RefL} = 1.49 \text{ V}$, and $\text{RefM} = 1.50 \text{ V}$, together with a two-stage timing-regulation strategy constrained by the detection period T_{det} and the control period T_{ctrl} , the proposed design achieves both a rapid transient response and stable steady-state operation under dynamically varying electrostatic drive demands. During start-up, resonance establishment, and abrupt disturbance conditions, the bidirectional shift register activates additional output power units step by step within a finite number of control cycles, thereby enhancing electrostatic driving capability and rapidly restoring closed-loop oscillation stability. Once stable resonance is established, redundant output branches are progressively disabled based on the mid-supply reference voltage RefM , effectively suppressing unnecessary static power dissipation while maintaining stable oscillation. Experimental results obtained using the MEMS gyroscope interface ASIC demonstrate that the proposed electrostatic-force-modulated closed-loop self-excited driving scheme successfully achieves stable resonant operation under atmospheric pressure conditions. The measured resonant frequency is centered at 4.077 kHz , with a fluctuation lower than 0.1 Hz over a 15 min observation period, corresponding to a relative frequency stability of approximately 25 ppm. Moreover, the proof-mass displacement amplitude fluctuation remains below 0.2 mV relative to an AC driving amplitude of 5.7 V , corresponding to an amplitude stability of approximately 0.005%. Combined with the hard shut-off isolation of idle power transistors enabled by the improved SPDT switch, the subthreshold leakage current is effectively suppressed, further improving system energy efficiency. These results verify the effectiveness of the proposed design in jointly optimizing electrostatic driving capability, oscillation stability, and power efficiency, thereby providing a practical and reliable solution for high-performance MEMS gyroscope electrostatic-force-modulated closed-loop self-excited driving systems.

One limitation of the present work is that the adaptive output-state transitions were verified through transistor-level simulations rather than direct chip measurements because the fabricated prototype did not include dedicated observation circuitry. Future work will focus on redesigning the prototype to experimentally characterize the internal adaptive regulation mechanism and complete system-level power consumption and include a redesigned prototype incorporating dedicated observation nodes for experimentally monitoring the adaptive output-unit states, shift-register transitions, and dynamic power regulation during practical MEMS operation.

Author Contributions: Writing—review & editing, X.L. and W.R.; Funding acquisition, D.Y. and X.L.; Project administration, S.W. and H.Y.; Investigation, X.H. and W.Z. All authors have read and agreed to the published version of the manuscript.

Funding: This work is supported by the National Natural Science Foundation of China (Grant No. 62571283); the Youth Program of Zhejiang Provincial Natural Science Foundation of China (Grant No. LQN26F040018); the General Scientific Research Project of the Department of Education of Zhejiang Province (Grant No. Y202559671); the Natural Science Foundation of Huzhou Science and Technology Plan Project (Grant No. 2025YZ08); the Scientific Research Project of Huzhou College (Grant No. 2024HXKM04); the 2025 Education and Teaching Reform Research Project of Huzhou College (Grant No. hyjg202503); the 2025 First-Class Undergraduate Course Construction Project of Huzhou College. and in part by the Natural Science Foundation of Ningbo under Grant 2024J026; in part by 2025 Domestic Visiting Scholar Program for University Teachers (FX2025111).

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding authors.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Zhong, L.; Yang, J.; Xu, D.; Lai, X. Bandwidth-enhanced oversampling successive approximation readout technique for low noise power-efficient MEMS capacitive accelerometer. *IEEE J. Solid-State Circuits* **2020**, *55*, 2529–2538. <https://doi.org/10.1109/JSSC.2020.3005811>.
2. Zhang, W.; Di, X.; Wang, S.; Gu, H.; Sha, X.; Fu, Q.; Li, X. Design of High-Precision Interface ASIC for Quartz Gyroscopes with $0.022^\circ/\sqrt{\text{hr}}$ Angle Random Walk. *IEEE Sens. J.* **2025**, *25*, 36423–36433. <https://doi.org/10.1109/JSEN.2025.3600292>.
3. Yu, G.; Liu, J.; Hu, L.; Jiang, A.; Wang, L. Motion system modeling and acceleration analysis of five-axis hybrid machine tool. *Adv. Eng. Inform.* **2026**, *71*, 104368.
4. Zhang, W.; Yu, X.; Wang, Y.; Zhang, H.; Sha, X.; Liu, X.; Yin, L.; Fu, Q.; Li, X. An interface ASIC for MEMS disk resonator gyroscope with $0.018^\circ/\text{h}$ bias instability and 108 Ppm scale factor nonlinearity. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2025**, *73*, 113–125.
5. Zhai, G.; Li, S. MESPBO: Multi-Strategy-Enhanced Student Psychology-Based Optimization Algorithm for Global Optimization Problems and Feature Selection Problems. *Biomimetics* **2026**, *11*, 37.
6. Xu, K.; Liu, J.; Huang, H.; Wang, C.; Zhao, W.; Ge, S.S. Multi-agent dynamic surface consensus control of dual-motor steer-by-wire system under communication faults. *IEEE Trans. Ind. Electron.* Early Access, 1–12, **2026**. DOI: <https://doi.org/10.1109/TIE.2026.3695241>
7. Chen, L. Beyond External Constraints: The Missing Dimension of AI Governance. 2026. Available online: https://papers.ssrn.com/sol3/papers.cfm?abstract_id=6449738.
8. Zhang, W.; Yu, X.; Wang, Y.; Zhan, X.; Zhang, H.; Di, X.; Chen, L.; Zhang, H.; Fu, Q.; Yin, L.; et al. A Low noise readout circuit with input-common-mode-feedback charge sensitive amplifier using differential pseudo resistors for MEMS gyroscopes. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2025**, *72*, 6436–6448.
9. Yu, G.; Hu, L.; Qu, Y. Fretting slip Wear mechanism of AlCrN coated cemented carbide tool on titanium alloy TC4 under ultimate continuous cutting. *Int. J. Refract. Met. Hard Mater.* **2026**, *140*, 107859.
10. Wang, S.; Zhang, X.; Wang, P.; Li, X. Design of Magnetic Sensor Array-Based PUFs for IoT Security. *IEEE Trans. Instrum. Meas.* **2026**, Early access. <https://doi.org/10.1109/TIM.2026.3679077>.
11. Han, X.; Wang, S.; Yu, J.; Wang, P.; Li, X. Design of PUF based on a Cr₂O₃-SnO₂ gas sensor for Internet of Things security. *Measurement* **2026**, *276*, 121395.
12. Wang, S.; Yang, H.; Jiao, G.; Ren, M.; Li, X. ECG analog front end circuit-A review. *Measurement* **2026**, *267*, 120566.
13. Li, X.; Wang, P.; Li, G.; Ni, L.; Zhang, Y. Design of interface circuits and lightweight PUF for TMR sensors. *IEEE Sens. J.* **2023**, *23*, 11754–11761.
14. Cui, R.; Li, K.; Xu, X.; Rihui; Xue; Shen, C.; Shi, Y.; Cao, H.; Xue, R. Design and experiment of MEMS solid-state wave gyroscope quadrature error correction system. *IEEE Sens. J.* **2023**, *23*, 16645–16655.
15. Jin, J.; Xu, M.; Guo, Y.; Liu, X.; Sun, N.; Zhou, J. A 470 μW 20 kHz-BW 107.3 dB-SNDR Nested CT DSM Using Negative-R-Based Cross-RC Integrator and Weighted Multi-Threshold MSB-Pass Quantizer. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2025**, *72*, 6807–6819.
16. Li, X.; Wang, P.; Li, G.; Zhang, Y. Design of a novel self-test-on-chip interface ASIC for capacitive accelerometers. *IEEE Trans. Circuits Syst. I* **2023**, *70*, 2834–2843.
17. Guo, Y.; Jin, J.; Liu, X.; Zhou, J. A 60-MS/s 5-MHz BW noise-shaping SAR ADC with integrated input buffer achieving 84.2-dB SNDR and 97.3-dB SFDR using dynamic level-shifting and ISI-error correction. *IEEE J. Solid-State Circuits* **2022**, *58*, 474–485.
18. Vujadinović, M.; Hiller, T.; Blocher, L.; Northemann, T.; Choubey, B. Impact of phase noise on bias instability in mode-split open-loop MEMS gyroscopes. *IEEE Sens. J.* **2024**, *24*, 17772–17780.
19. Kant, K.; Paswan, R.K.; Ahmad, I.; Sinha, A.P. Digital control and readout of MEMS gyroscope using second-order sliding mode control. *IEEE Sens. J.* **2022**, *22*, 20567–20574.
20. Zhang, H.; Chen, W.; Yin, L.; Fu, Q.; Zhang, Y. Design of the digital interface circuit system for MEMS gyroscope. *Mod. Phys. Lett. B* **2022**, *36*, 2250127.
21. Guo, Y.; Jin, J.; Liu, X.; Zhou, J. A 372 μW 10 kHz-BW 109.2 dB-SNDR nested delta-sigma modulator using hysteresis-comparison MSB-pass quantization. *IEEE J. Solid-State Circuits* **2023**, *58*, 2554–2563.
22. Li, Y.; Jin, J.; Guo, Y.; Zhou, J.; Jiang, J. A 3–5 V to Sub-1 V DLDO-SC-Sigma Converter With Auxiliary Loop for Efficiency Improvement in High-Density Power Delivery. *IEEE J. Solid-State Circuits* **2025**, *61*, 641–650.
23. Zhang, H.; Liu, X.; Zhang, J.; Zhang, H.; Li, J.; Zhang, R. A Nano-Watt MOS-Only Voltage Reference With High-Slope PTAT Voltage Generators. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *65*, 1–5.

24. Guo, Y.; Jin, J.; Liu, X.; Zhou, J. An inverter-based continuous time sigma delta ADC with latency-free DAC calibration. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 3630–3642.
25. Yang, C.; Liu, X.; Jin, J.; Guo, Y.; Zhou, J. A fast-settling phase-locked loop utilizing cycle-slipping-elimination PFDCP. *IEEE Trans. Circuits Syst. II Express Briefs* **2022**, *69*, 3998–4002.
26. Sawigun, C.; Demosthenous, A.; Liu, X.; Serdijn, W.A. A Compact Rail-to-Rail Class-AB CMOS Buffer With Slew-Rate Enhancement. *IEEE Trans. Circuits Syst. II Express Briefs* **2012**, *59*, 486–490.
27. Khorami, A.; Sharifkhani, M. A Low-Power High-Speed Comparator for Precise Applications. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2018**, *26*, 2038–2049. DOI: <https://doi.org/10.1109/TVLSI.2018.2833037>
28. Beheshti, M.M.; Koolivand, Y.; Rezaeiyan, Y.; Zamani, M. A Power-Efficient Adaptively-Biased Class-AB OTA with Improved Gain, Slew Rate, and Reduced Systematic Mismatch. In Proceedings of the 2025 IEEE Biomedical Circuits and Systems Conference (BioCAS), Abu Dhabi, United Arab Emirates, 16–18 October 2025; pp. 492–496. <https://doi.org/10.1109/BioCAS67066.2025.00111>.
29. Feng, X.; Ma, S.; Zou, M.; Wu, T. A High Gain and Wide Bandwidth Dual-Power CMOS Op-amp for High-Speed ADCs Application. In Proceedings of the 2023 IEEE 15th International Conference on ASIC (ASICON), Nanjing, China, 24–27 October 2023; pp. 1–4. <https://doi.org/10.1109/ASICON58565.2023.10396342>.
30. Mahendra, M.; Kumari, S.; Gupta, M. Low Voltage Adaptive Biased OTA with Enhanced Slew Rate and its application in Universal Filter. In Proceedings of the 2021 5th International Conference on Electrical, Electronics, Communication, Computer Technologies and Optimization Techniques (ICEECCOT), Mysuru, India, 10–11 December 2021; pp. 460–465. <https://doi.org/10.1109/ICEECCOT52851.2021.9708040>.

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