



Silicon-Based Optoelectronics Enhanced by Hybrid Plasmon Polaritons: Bridging Dielectric Photonics and Nanoplasmonics

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Abstract: Silicon-based optoelectronics large-scale integrated circuits have been of interest to the world in recent decades due to the need for higher complexity, larger link capacity, and lower cost. Surface plasmons are electromagnetic waves that propagate along the interface between a conductor and a dielectric, which can be confined several orders smaller than the wavelength in a vacuum and offers the potential for minimizing photonic circuits to the nanoscale. However, plasmonic waveguides are usually accompanied by substantial propagation loss because metals always exhibit significant resistive heating losses when interacting with light. Therefore, it is better to couple silicon-based optoelectronics and plasmonics and bridge the gap between micro-photonics and nanodevices, especially some nano-electronic devices. In this review, we discuss methods to enhance silicon-based optoelectronics by hybrid plasmon polaritons and summarize some recently reported designs. It is believed that by utilizing the strong light confinement of plasmonics, we can overcome the conventional diffraction limit of light and further improve the integration of optoelectronic circuits.

Keywords: silicon photonics; silicon-based optoelectronics; hybrid plasmon polaritons; large-scale optoelectronic integrated circuits

1. Introduction

1.1. Silicon-Based Optoelectronics

The development of optoelectronic devices has affected many aspects of society, from simple household appliances and multimedia systems to communications, computers, and medical equipment. The main characteristics of the next-generation optical communication system will be intelligence, integration, low cost, and high reliability. At the same time, with the rapid development of high-performance computers, the central processing unit (CPU) speed will be faster, and the memory storage space will be larger. Therefore, high-density data communication in the computer system has become the main bottleneck restricting its development. Currently, optical interconnection is recognized as an important development direction for realizing high-speed communication between computers and even chips. Due to the above-mentioned requirements for the development of optical communications and computers, people have a keen interest in the development of micronano-sized devices that can provide more functions and better performance.

However, the materials used in optoelectronic devices are diverse, such as III–V group compounds (InP, GaAs) and group IV materials (Si, Ge). The fabrication processes of various material platforms are different from each other. Therefore, it is hard to integrate them together. Fortunately, the price of silicon materials is very low, and silicon-based micro-nano processing technology developed by the integrated circuit industry is very mature. This gives people hope to make silicon-based micro-nano photonic devices. Then,



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). silicon photonic devices and logic circuits can be integrated on the same chip. In this way, the high-density data communication capability of the computer system can be greatly improved, while the size, power consumption, and cost of the system will be significantly reduced.

Silicon-based optoelectronics is a chip-size solution based on the interaction between photons and electrons, developed on the traditional microelectronics platform. Since Richard A. Soref's early work about the electro-optic effect of silicon in 1985, silicon-based optoelectronics have been on a rapid development track. Many breakthroughs have been made on the fundamental components of the silicon-based optoelectronics platform, such as on-chip light sources [1], modulators [2,3], multiplexing technologies [4,5], light coupling [6,7], polarization handling [8], and light detection [9,10]. Several important works of silicon-based optoelectronics in the past few decades are shown in Figure 1.



Figure 1. The development trend of silicon-based optoelectronics and some significant works in the past few decades. Figures reproduced from [11–16].

In 2004, Yurii et al. designed and fabricated low loss CMOS-compatible silicon strip waveguides [13], which are most commonly used for light guiding. In 2006, 2007, and 2009, on-chip lasers [14], optical modulators [17], and photon detectors [18] for silicon-based optoelectronics were reported by Intel. These basic devices are indispensable for researches on modules. After 2010, some research institutions (Intel, IBM, etc.) [12,15,16,19] manufactured high-speed and broadband optical transceivers, which are greatly demanded in date center short-reach interconnection nowadays [20]. According to the 'More than Moore' roadmap [21], integrating processing units and optical transceivers on a monolithic chip is the future trend after Moore's Law. In 2015, a single-chip microprocessor communicating directly using light was reported [11], which realized CMOS-compatible chip-scale electronic-photonic systems for the first time.

1.2. Plasmonics

Plasmonics has become a promising technology that can overcome the diffraction limits of dielectric photonics [22–27]. Propagating along the interface between a conductor

and a dielectric material, surface plasmons are mixing of photons and plasmons (in the conductor) [28,29]. The term 'surface plasmons' (SPs) was first used by Ritchie in 1957 when he extended the work of Pines and Bohm [30]. Since then, surface plasmons have gone by several names in the literature. The term 'surface plasmon polaritons' (SPPs) is also frequently used in many areas. The word 'polaritons' means the polar excitation in material mixing with the photon, emphasizing that the electromagnetic field is connected to the electronic excitation in the metal.

Figure 2a illustrates the surface plasmons waves propagating along the interface of silver and air. The electromagnetic field is localized on the surface of silver, and the free electrons in the silver oscillate in resonance with the optical field in the air. These optical waves are trapped on the surface and help us to channel and manipulate on a subwavelength scale. It could lead to photonic circuits with footprints much smaller than those traditional dielectric ones. The relationship of semiconductor electronics, dielectric photonics, and plasmonics is illustrated in Figure 2b, in which the dashed lines indicate the limitations of these technologies. Semiconductor electronics are limited by interconnect delay time and heat generation issues with an operating speed of about 10 GHz. The diffraction limit prohibits dielectric photonics from achieving critical dimensions comparable with microelectronics. Plasmonics can be guided beyond the diffraction limit and serve as a bridge between semiconductor nanoelectronics and photonics [31].



Figure 2. (a) Optical field profile (E_z) of surface plasmons on the air–Ag interface. (b) The operating speed and device sizes of semiconductor electronics, dielectric photonics, and plasmonics. Plasmonics can bridge the gap between nanoelectronics and photonics.

1.2.1. Fundamental Principles of Plasmonics

Plasma is hot ionized gas with free charges and is usually named the fourth state of matter. Actually, plasma exists in our daily lives [32–35] but often needs high temperature and pressure. At room temperature, it is too cold and dense for classical plasma to exist. However, in metal, electrons are delocalized from ions. This means that we can treat metal as a material with plasmons inside. According to the electromagnetic field theory, the relative permittivity of metal can be described approximately by the Drude model [36]:

$$\varepsilon(\omega) = 1 - \frac{\omega_p^2}{\omega^2 + i\gamma\omega}, \omega_p = \sqrt{\frac{Ne^2}{\varepsilon_0 m}}$$
(1)

where γ is the damping frequency, ω_p is the plasma frequency, N is the density of electrons, and m is the mass of electron. The damping frequency is usually about 100 THz. At optical frequency $\omega \gg \gamma$, the relative permittivity of metal $\varepsilon(\omega)$ can be simplified as:

$$\varepsilon(\omega) \approx 1 - \frac{\omega_p^2}{\omega^2}$$
(2)

For different frequencies ω , the relative permittivity of the metal $\varepsilon(\omega)$ varies, and the metal appears to have different properties (summarized in Table 1).

	Very high frequency	Optical frequency	Very low frequency	At plasma frequency	
Frequency region	$ \begin{array}{c} & & & \\ & &$	$\mathcal{E} \longrightarrow \mathcal{E} \longrightarrow $	$\varepsilon(\omega) = 1 - \frac{\omega_p^2}{\omega^2 + i\gamma\omega}$ is complex	$ \begin{array}{c} $	
	$\omega > \omega_p$	$\gamma \ll \omega < \omega_p$	$\omega \ll \gamma$	$\omega = \omega_p$	
Relative permittivity	$\varepsilon'>0,\ \varepsilon''pprox 0$	$arepsilon' < 0, \ arepsilon'' pprox 0$	$arepsilon'' \gg arepsilon'$	arepsilonpprox 0	
Refractive index	$n' > 0, n'' \approx 0$ <i>n</i> is real	$n' \approx 0, n'' > 0$ <i>n</i> is complex	$n' \approx n'' \approx \sqrt{\varepsilon''/2}$	$n \approx 0$	
Properties of Metal	Air Metal	Air Metal	Air Metal	Only collective longitudinal oscillations of free electrons	
	Metal is like dielectric	Fields decay exponentially	Fields decay rapidly	exist (called volume plasmons)	

Table 1. The properties of metal for different frequency of light.

For surface plasmons $\gamma \ll \omega < \omega_p$, the real part of permittivity ε' is less than zero, and the imaginary part of permittivity ε'' is approximately equal to zero. This means the refractive index *n* of metal is imaginary, and fields decay exponentially in the metal. A variety of theories for surface plasmons have been developed in the literature. Someone might define surface plasmons with quantum mechanics as particles with quantized energy and momentum [37]. However, the classical Maxwell's equation and electromagnetic model can describe most of the properties of surface plasmons satisfactorily. Though quantum mechanics potentially exist in the background, we can roll it up to the dielectric function in most cases. Practically, it is found that in the surface plasmons system, the bulk dielectric constant can describe the object down to ~10 nm accurately [38]. For most photonic devices on chip, typically, the footprints are much larger. Usually, the classical electromagnetic theory can fully explain the function of the devices, and some numerical calculation methods, such as the finite element method (FEM) and finite difference time domain method (FDTD), are applied to simulate the field profile of surface plasmons.

1.2.2. Surface Plasmon Subwavelength Optics

Solving Maxwell's equations under the boundary conditions, we can derive the dispersion relation of surface plasmons [39]:

$$k_{\rm sp} = k_0 \sqrt{\frac{\varepsilon_d \varepsilon_m(\omega)}{\varepsilon_d + \varepsilon_m(\omega)}}$$
(3)

where k_0 is the free-space wave vector, ε_d is the relative permittivities of dielectric, and ε_m is the frequency-dependent permittivity of the metal. According to the boundary conditions [28], if the interface is able to support propagation of surface plasmons, the permittivity of the medium on the different side of the interface necessarily have opposite signs. As shown in Table 1, metals can satisfy this condition because ε_m is approximately a negative number for optical frequency. Based on Equation (3), the dispersion curve for surface plasmons mode is depicted in Figure 3. At very low frequency, the dispersion curve tends to the light line in the dielectric. As the frequency increases, the wave vector

of surface plasmons approaches infinity. The frequency limit is called the characteristic surface plasmons frequency:

We

$$p = \frac{\omega_p}{\sqrt{1 + \varepsilon_d}} \tag{4}$$



Figure 3. The unique dispersion curve of surface plasmons mode illustrates the momentum mismatch, with the surface plasmons mode lying on the right side of the light line. This yields extraordinary high wave vectors k_{sp} capable of overcoming the diffraction limit of light.

The high wave vector k_{sp} means that the wavelength of surface plasmons λ_{sp} is smaller than light in the dielectric. This reveals the subwavelength characteristic of surface plasmons, which provides a method to overcoming the Abbe's diffraction limit [40], and spawns a variety of new technologies to deliver, control, and manipulate electromagnetic radiation on the nanoscale.

The use of surface plasmons has led to the development of abundant nano-optical techniques [41,42], such as surface-enhanced Raman scattering (SERS) [43] for optical sensing of individual molecules [44–46], optical nanoscopy, and spectroscopy to achieve super-resolution and unravel the structure–function of materials as tiny as a few nanometers [47–49].

In this process, the plasmonic light concentrators that can focus electromagnetic radiation and optical energy to a localized tiny area have attracted the attention of many researchers [50]. Some researchers have reported nanofocusing structures that can squeeze light into a focal spot as small as possible [51]. By using chirped surface gratings [52], plasmonic Fresnel zone plate [53,54], nano-slit arrays [55,56], or other similar periodic optical elements [57,58], the light beam can be concentrated to a little spot in space. These configurations are able to enhance light intensity out-of-plane in free space by tens of thousands of times [41], which shows the superiority of surface plasmons to concentrate light far beyond the diffraction limit. However, in most circumstances, we need to focus light in-plane for practical use [33,59]. One way is to modulate the phase of optical waves and generate a focused spot at some distance. This principle is similar to that used to concentrate light in free space. For example, by arranging holes [60], condensers [61], or slits [62] in curved shapes, the phase fronts of surface plasmon waves will be concaved. As a result, the light is focused in-plane on the metal surface. Another way is to use tapered structures that support surface plasmons. The taper gradually concentrates the field and enhances the intensity of surface plasmons as the light propagates to the apex of the taper. Various types of tapered nanofocusing structures have been reported, such as a conical metal rod with a tiny tip [63-66], a metal wedge on a dielectric substrate [67-70], a dielectric wedge on a metal substrate [71,72], etc. Typically, these tapered structures are

based on metal–insulator–metal (MIM) or insulator–metal–insulator (IMI) configurations. The MIM structures usually have better optical confinement and a smaller mode area, whereas the IMI structures often have a lower loss and larger propagation length [22,24]. Besides the structures of the taper, the taper angles also influence the physical processes. If the taper angles are sufficiently small, the propagating electromagnetic waves do not 'feel' the variation of the taper. Therefore, the reflection and scattering of light are negligible. This is the so-called adiabatic condition [63,73]. Generally speaking, if the variation of the light wavelength is slow enough relative to its wavelength [74–76], we can treat the taper as an adiabatic one, by which the energy losses can be significantly reduced during the nanofocusing processes. Some representative functional plasmonic subwavelength waveguide components reported are shown in Figure 4.



Figure 4. Topographical (**a**,**c**,**e**,**g**,**i**,**l**) and near-field optical (**b**,**d**,**f**,**h**,**j**,**k**,**m**) images of plasmonic subwavelength waveguide components. (**a**,**b**) S-bend [77]. (**c**,**d**) Y-splitter [77]. (**e**,**f**) Mach–Zehnder (M.Z.) interferometer [78]. (**g**,**h**) Waveguide–ring (WR) resonator [78]. (**i**–**k**) WR-resonator-based add-drop multiplexer [79]. (**l**,**m**) Bragg grating filter (BGF) [79]. Figures reproduced from (**a**–**d**) [77]; (**e**–**h**) [78]; (**i**–**m**) [79].

Besides the plasmonic light concentrators illustrated above, the plasmonic waveguide components that can find their very practical use in large-scale integrated optical circuits have also generated tremendous interest [80–83]. Unlike light concentrators, these plasmonic waveguide components support the propagation of electromagnetic waves for a long distance while the light field is bound in a small area. These ultracompact functional plasmonic components utilize channel plasmon polaritons (CPPs), where the electromagnetic waves are confined on the bottom of V-shaped grooves cut into a metal [84–86]. At telecom wavelengths, the CPPs can propagate about tens of micrometers while showing

relatively strong confinement. Therefore, CPP-based extremely sharp bends and even more sophisticated components (such as waveguide–ring resonator-based add-drop multiplexer and Bragg grating filter shown in Figure 4i,l) have been realized in experiments [77–79].

2. Hybrid Plasmon Polaritons (HPPs)

The use of surface plasmons opens up the prospect of extreme light concentration and manipulation. The unprecedented ability of plasmonic devices paves the way for generating [83,87], guiding, modulating [88–93], and detecting [94–96] light similar in size to semiconductor electronic devices. However, if photonic integrated circuits based on surface plasmons are to be developed, the attenuation owing to the absorption of the metal cannot be ignored. The significant resistive heating losses of metal make it impossible for surface plasmons to travel a long distance. The propagation length δ_{sp} of surface plasmons depends on the relative permittivity of metal and dielectric at the oscillation frequency [97]:

$$\delta_{\rm sp} = \frac{c}{\omega} \left(\frac{\varepsilon'_m + \varepsilon_d}{\varepsilon'_m \varepsilon_d} \right)^{\frac{2}{2}} \frac{\left(\varepsilon'_m\right)^2}{\varepsilon''_m} \tag{5}$$

where ε'_m and ε''_m are the real and imaginary parts of the relative permittivity function of the metal. Generally, the propagation length is on the order of micrometers [23]. For example, the propagation length of aluminum is about 2 µm at a wavelength of 500 nm. Silver is a low-loss metal with a propagation of about 20 µm at the same wavelength and towards 1 mm at the 1.55 µm near-infrared communication band. This means plasmonic components must be smaller than the propagation length, which enables light waves to travel through the structure before suffering from significant propagation losses.

Table 2 provides the attenuation of several typical plasmonic waveguides, which have been reported in the literature by experiments. Due to the limitation of fabrication resolution, misalignments between different layers, roughness of the sidewall of metal, and other defects in fabrication processes, those fabricated plasmonic waveguides showed fairly high losses in experiments [98–101]. The intrinsic optical properties of metals enable plasmonic waveguides to guide electromagnetic waves with smaller mode areas than dielectric waveguides, while the absorption of metals makes the propagation length of surface plasmons much shorter. This fact reveals that for plasmonic waveguides, the maximum light confinement and the maximum propagation length are in opposition to each other. Stronger field confinement pushes the surface plasmon waves closer to the surface of the metal, which leads to higher absorption and thus shorter propagation length.

Table 2. Attenuation of several types of plasmonic waveguides reported in literature by experiments.

Waveguide Type	Schematics ¹	Free Space Wavelength λ (nm)	$\frac{Mode\ Area}{\left(\lambda/2\right)^2}$	Propagation Length L_m/λ	
Metal-insulator-metal (MIM) [98]		685	10%	5	
Insulator-metal-insulator (IMI) [99]	-	1550	14%	14	
Triangular metal wedge [100]		633	-	2	
Dielectric stripe on metal [101]		800	-	10	

¹ The schematics show the plasmonic waveguide cross-sections, with the optical field propagating in the third dimension. The yellow color marks metal, blue—dielectric, pink—mode intensity distributions.

Therefore, a compromise between propagation length and field confinement should be reached if we want to integrate plasmonic components into optoelectronic circuits in practical applications. A variety of strategies have been demonstrated and tested in the past few decades. Among them, hybrid plasmon polaritons (HPPs) that combine dielectric and plasmonic principles together probably attract the most attention from researchers [102–113]. The hybridization model for the HPPs is shown in Figure 5. A typical hybrid plasmonic waveguide consists of a dielectric core and a metal layer separated by a low-index dielectric gap. The resulting HPP mode 'stores' most of its optical energy in the 'capacitor-like' low-index dielectric gap and only a small amount in the metal. In this way, the HPPs can feature a subwavelength mode area and a large propagation length.



Figure 5. Schematics (**a**,**c**) and field distributions (**b**,**d**) of two types of hybrid plasmonic waveguides reported in literature. (**a**,**b**) A dielectric cylinder above a metal surface [106]. (**c**,**d**) A metal cap on an SOI slab with a low-index nano-layer between them [104]. This type of hybrid plasmonic waveguide is compatible with standard processes for SOI wafers and is thus easily fabricated. Figures reproduced from (**b**) [106]; (**d**) [104].

According to the coupled-mode theory (CMT) [106,114–116], the HPPs can be described as a combination of plasmonic modes and dielectric modes (as shown in Figure 5), which is also the origin of its name. Therefore, the field distributions of the hybrid plasmonic waveguide (HPW) can be expressed as:

$$\psi_{\text{HPW}}(d,h) = a(d,h)\psi_{\text{plasmonic}} + b(d,h)\psi_{\text{dielectric}}(d)$$
(6)

where $\psi_{\text{plasmonic}}$ and $\psi_{\text{dielectric}}(d)$ are the uncoupled plasmonic and dielectric modes, a(d, h) and b(d, h) are the amplitudes of the plasmonic and dielectric modes, respectively. In Figure 5a, the parameters d and h are the diameter of the dielectric cylinder and the thickness of the low-index dielectric gap. In Figure 5c, the parameters d and h are the heights of the dielectric waveguide and low-index gap layer. The coupled modes of the HPW satisfy equations [106]:

$$\begin{pmatrix} n_{\text{dielectric}}(d) & \kappa(d,h) \\ \kappa(d,h) & n_{\text{plasmonic}} \end{pmatrix} \begin{pmatrix} a(d,h) \\ b(d,h) \end{pmatrix} = n_{\text{HPW}}(d,h) \begin{pmatrix} a(d,h) \\ b(d,h) \end{pmatrix}$$
(7)

Here, $n_{\text{plasmonic}}$, $n_{\text{dielectric}}(d)$ and $n_{\text{HPW}}(d,h)$ are the effective refractive indices of the plasmonic, dielectric, and coupled HPW modes and $\kappa(d,h)$ is the coupling strength between plasmonic and dielectric modes. The solutions for Equation (7) are:

$$n_{\rm HPW\pm}(d,h) = \frac{n_{\rm plasmonic} + n_{\rm dielectric}(d)}{2} \pm \sqrt{\frac{\left(n_{\rm plasmonic} - n_{\rm dielectric}(d)\right)^2}{4} + \kappa(d,h)^2}$$
(8)

which reveals the typical behavior of a coupled system with two possible modes. Usually, the lower index (antisymmetric) mode is cut off, and the higher index (symmetric) mode is the only bound mode in the HPW system.

Although the CMT is approximate, it provides a good physical insight and helps us to gain a deep understanding of the HPPs. Actually, we can obtain accurate information from the dispersion relation of HPPs directly. Using the transfer matrix method [117], the dispersion relation for one-dimensional multilayer HPPs (as shown in Figure 5c) can be obtained as [110,118]:

$$\frac{k_m}{\varepsilon_m}m_{11} + \frac{k_s}{\varepsilon_{\rm SiO_2}}m_{22} - m_{21} - \frac{k_mk_s}{\varepsilon_m\varepsilon_{\rm SiO_2}}m_{12} = 0$$
(9)

where the coefficients m_{ij} (i = 1, 2; j = 1, 2) are given by:

$$\begin{pmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{pmatrix} = \begin{pmatrix} \cos(k_1h) & -\frac{\varepsilon_{\mathrm{SiO}_2}}{k_1}\sin(k_1h) \\ \frac{k_1}{\varepsilon_{\mathrm{SiO}_2}}\sin(k_1h) & \cos(k_1h) \end{pmatrix} \times \begin{pmatrix} \cos(k_2d) & -\frac{\varepsilon_{\mathrm{Si}}}{k_2}\sin(k_2d) \\ \frac{k_2}{\varepsilon_{\mathrm{Si}}}\sin(k_2d) & \cos(k_2d) \end{pmatrix}$$
(10)

where $k_m = (\gamma^2 - \varepsilon_m k_0^2)^{1/2}$ and $k_s = (\gamma^2 - \varepsilon_{SiO_2} k_0^2)^{1/2}$ are the rate of attenuation in the metal and substrate and $k_1 = (\varepsilon_{SiO_2} k_0^2 - \gamma^2)^{1/2}$ and $k_2 = (\varepsilon_{Si} k_0^2 - \gamma^2)^{1/2}$ are the transverse wavevectors in the silica gap layer and silicon core layer. $\gamma = k_0 (N_{\text{eff}} + iK_{\text{eff}})$ is the complex propagation constant of the HPP mode and $k_0 = 2\pi/\lambda_0$ is the free space wavevector. By solving the dispersion relation Equation (9), we can find the exact guided modes of HPPs.

3. HPPs Enhancing the Silicon Photonic Circuits

As described above, the development of silicon-based optoelectronics over the past several decades has introduced silicon as one of the most promising platforms for largescale integrated optoelectronic circuits due to its CMOS compatibility. Yet, silicon photonic devices, like other dielectric optical components, are blocked from being scaled down to the nanoscale by the diffraction limit. To enhance light confinement, researchers pay attention to hybridizing surface plasmons with silicon-based optoelectronics. Figure 6 compares the light confinement characteristics of silicon photonic and plasmonic structures. Figure 6a demonstrates the field profiles of the commonly used silicon strip waveguides for different widths. As the width of waveguides d is decreased, the light field penetrates deeper into the surrounding cladding. When *d* approaches zero, the guided mode eventually turns into a plane wave in the cladding medium. In other words, the mode size decreases to a minimum limit and then increases to infinity when the waveguide width d is reduced further. Therefore, reducing the cross-section area of the silicon waveguides to zero cannot enhance the light confinement further. This is what we call the diffraction limit of dielectric waveguides, which is the main hurdle to realizing smaller physical device sizes. For plasmonic structures, the situation is different. Since surface plasmons are kinds of surface modes on the metal interface, the light field can still be bounded on the metal wires even when the width d decreases to just a few nanometers (shown in Figure 6b). This enables the plasmonic structures to overcome the diffraction limit and concentrate light in a nanoscale area, which can enhance the light confinement far beyond those dielectric ones.



Figure 6. Schematics illustrating the light confinement of (**a**) dielectric versus (**b**) plasmonic waveguides for various core diameters. The dotted lines approximately indicate the *1/e* level of the field.

Therefore, hybridizing surface plasmons on silicon-based optoelectronics is a good way to enhance the light confinement of conventional dielectric optical components. On the other hand, plasmonic structures often suffer from relatively high propagation losses, while silicon dielectric structures can guide the light losslessly at a very large distance. Consequently, the strengths and weaknesses of silicon-based optoelectronics and plasmonics are complementary to each other. For most photonic components in the optoelectronic integrated circuits, silicon photonic structures are suitable due to their low losses and high compatibility with CMOS fabrication processes. For parts requiring higher light confinement, we can apply plasmonic structures to enhance light–matter interaction.

Generally, there are two methods to integrate silicon photonic and plasmonic waveguides together. One is utilizing tapered regions to connect these two kinds of waveguides directly, and another is coupling the light between the two kinds of waveguides by evanescent fields, just like the directional couplers.

3.1. Tapered Coupling Design

Early works about the seamless transition between silicon photonic waveguides and plasmonic waveguides date back to decades ago. In 2006, Ginzburg et al. [119] theoretically demonstrated a nonadiabatic taper connecting a microscale dielectric waveguide and a nanoscale plasmonic waveguide (shown in Figure 7a). The input is a 1.25 μ m-wide silica waveguide with air cladding, and the output is a 50 nm-wide gold slot with silica as the core. A 6 μ m-long linear plasmonic gap taper acts as the coupler to realize mode conversion between these two types of waveguides, and a coupling loss of less than 2 dB can be achieved in theory. The field profiles simulated by FDTD are shown in Figure 7b,c. For TM excitation, the light field propagates through the taper with about 70% transmission, while for TE excitation, no plasmon mode can exist. In [120], Chen et al. fabricated metal tapers and slots on silicon-on-insulator wafers by electron-beam lithography patterning, reactive ion etching, metal evaporation, and the liftoff process. The microscope image of the fabricated sample is shown in Figure 7d, and the schematic structure is shown in Figure 7e,f. The silicon waveguide and the metal slot are both 250 nm thick, and the widths are 450 nm

and 150–450 nm, respectively. The taper for coupling is about 4 μ m long. Results of the experiment are shown in Figure 7h,i. From the linear fit of the normalized power versus the length of the metal slot waveguide (Figure 7h), the coupling and propagation loss for 150 nm wide metal slot can be found to be about 2.5 dB and 0.8 dB/ μ m, respectively.



Figure 7. Tapered coupling design with reduction in width. Schematic configuration of the proposed taper for coupling a 1.25 µm-wide dielectric strip waveguide with a 50 nm-wide metal slot waveguide (**a**) and its field profile (**b**,**c**) [119]. Microscope image (**d**), schematic structure (**e**,**f**), and field distribution (**g**) of the fabricated tapered coupler between a standard silicon strip waveguide and a metal slot waveguide. (**h**,**i**) The transmitted power as a function of the length of metal slot *L*_t and the propagation losses as a function of the metal slot width, respectively [120]. The wavelength λ = 1550 nm. Figures reproduced from (**a**–**c**) [119]; (**d**–**i**) [120].

However, if we demand stronger light confinement and higher focusing efficiency, the tapers should not only have a reduction in width but also in thickness. Figure 8 shows the reported tapered structure with a reduction in both width and thickness. Figure 8a illustrates a tapered mode converter between the Si-strip waveguide and plasmonic slot waveguide. The core size of the Si-strip waveguide is 400 nm \times 200 nm, and the air-core size of the plasmonic slot waveguide is 50 nm \times 20 nm. Thus, there is a large thickness mismatch between the silicon and plasmon waveguide, which should have resulted in considerable coupling loss. However, in this work [121], the authors note that the optical field in the Si-strip waveguide has two side lobes outside the core. These side lobes are similar to the mode profiles in the plasmonic slot waveguide and gradually increase in size while the light propagates to the apex of the silicon taper. Finally, they are coupled to the mode of the plasmonic slot waveguide. Due to the existence of the side lobes, a 600 nm-long tapered mode converter achieves a coupling loss of only 1.7 dB even with discontinuity in thickness. The core size of the plasmonic slot waveguide is as small as $\langle \lambda/n \rangle^2/2000$, which realizes a relatively high field intensity enhancement of 41. Furthermore, Choo et al. [122] demonstrated a three-dimensional linear taper for focusing light into an 80 nm \times 14 nm MIM plasmonic waveguide (as shown in Figure 8d-f). They fabricated the 3D taper using e-beam-induced deposition (EBID), focused ion-beam (FIB) milling, and electron-beam evaporation. Without discontinuity, the 3D taper can enable the optical field to undergo a gradual conversion and achieve a field intensity enhancement of 400. Table 3 summarizes some other tapered coupling design reported in the literature.



Figure 8. Tapered coupling design with reduction in both width and thickness. (**a**–**c**) A taper with large reduction in thickness for Si-strip waveguide to plasmonic slot waveguide mode conversion [121]. (**d**–**f**) A three-dimensional linear taper for highly efficient nanofocusing in MIM plasmonic waveguide [122]. (**a**,**d**) Schematics of the proposed tapers. (**b**,**e**) Field distributions. (**c**,**f**) SEM images of the fabricated tapers. Figures reproduced from (**a**–**c**) [121]; (**d**–**f**) [122].

Ref.	Dielectric Waveguide Type and Core Size	Plasmonic Waveguide Type and Core Size	Taper Length /nm	λ/nm	Coupling Loss/dB	Propagation Loss /(dB \times μm $^{-1}$)	Field Enhancement
[123]	Si-strip 400 nm \times 220 nm	HPW 60 nm \times 20 nm	1080	1550	< 0.8	-	135.5
[124]	Si-strip 400 nm \times 220 nm	HPW 20 nm \times 40 nm	-	1550	< 0.7	-	75
102	Si-strip 450 nm \times 250 nm	HPW 200 nm \times 250 nm	400	1550	1.5	-	-
[121]*	Si-strip 400 nm \times 200 nm	Au-air-Au 50 nm $ imes$ 20 nm	600	1500-1600	1.7	1.8	41
[125] *	Si-strip 450 nm \times 250 nm	Au-air-Au 200 nm $ imes$ 250 nm	958.9	1460-1540	4.5	2.5	-
[122] *	SiO_2 -strip 500 nm \times 200 nm	Au-SiO ₂ -Au 80 nm \times 14 nm	1500	830	1.3	4.9	400
[126] *	$\dot{\text{Si-strip}}$ 300 nm \times 340 nm	Au-PMMĀ-Au 200 nm $ imes$ 200 nm	>2500	1550	5.2	0.78	-
[119]	SiO ₂ -strip 1250 nm in width	Au-SiO2-Au 50 nm in width	6000	1550	1.5	-	-
[127]	Si-strip 300 nm in width	Ag-air-Ag 50 nm in width	400	1550	0.3	-	-
[128]*	Si-ridge 740 nm \times 220 nm	Dielectric-loaded 500 nm $ imes$ 560 nm	~2000	1550	1	0.09	-
[129]	SiO ₂ -slab 50 nm in thickness	Ag-SiO ₂ -Ag 1 nm in thickness	~428	476	~2	~109	~350
[130]	Si-slot 650 nm in width	HPW 300 nm in width	50	1550	~0.5	-	-
[131]	Si-strip 450 nm $ imes$ 250 nm	Au-SU8-Au 250 nm × 250 nm	1700	1550	0.3	0.32	-
[132]*	Si-strip 450 nm \times 230 nm	Au-PMMA-Au 80 nm $ imes$ 180 nm	5400	1640	4	1.8	-
[133]	Si-strip 450 nm $ imes$ 300 nm	HPW 350 nm $ imes$ 300 nm	500	1400-1700	< 0.1	0.1	16
[120] *	Si-strip 450 nm $ imes$ 250 nm	Au-Si-Au 150 nm $ imes$ 250 nm	4000	1550	2.5	0.8	-
[134] *	Si-strip 500 nm \times 340 nm	HPW 45 nm $ imes$ 340 nm	1000	1550	0.4	0.63	-
[135]	SiO ₂ -strip 1250 nm in width	Au-SiO ₂ -Au 50 nm in width	2500	1550	1.5	-	-
[136]	SiO ₂ -strip 1250 nm in width	Au-SiO ₂ -Au 50 nm in width	6000	1550	<2	-	-
[137] *	Si-slot $460 \text{ nm} \times 260 \text{ nm}$	Au-air-Au 80 nm $ imes$ 260 nm	-	1550	3.7	2	-
[138] *	Si-strip 1000 nm \times 340 nm	HPW 200 nm $ imes$ 440 nm	1000	1550	0.97	0.1	-
[139] *	Si-strip 400 nm \times 340 nm	Ag-air-Ag 50 nm $ imes$ 340 nm	-	1530-1590	~1.5	~3.6	-
[140]	Si-strip with SiN 400 nm $ imes$ 390 nm	HPW 200 nm $ imes$ 460 nm	300	1300-1650	< 0.5	~0.2	-
[141]	Si-strip 1000 nm \times 370 nm	Ag-SiO ₂ -Ag 1000 nm \times 100 nm	540	1550	~0.6	-	-
[142]	Si-slab 300 nm in width	Ag-air-Ag 63 nm in width	-	1550	1.2	-	-
[143]	Si-slab 1250 nm in width	Ag-Si-Ag 50 nm in width	1500	1550	0.3	-	-
[144]*	Si-strip 2500 nm $ imes$ 900 nm	\tilde{HPW} 500 nm $ imes$ 900 nm	4000	1550	1.1	0.083	-
[145] *	Si-strip 900 nm $ imes$ 250 nm	Au-Si-Au 50 nm $ imes$ 200 nm	2000	1552	~1.2	-	~10
[146] *	Si-strip 460 nm \times 250 nm	Au-air-Au 80 nm $ imes$ 250 nm	50	1260-1620	~2.8	~2	-

Table 3. Summary of reported taper design for coupling silicon waveguides with plasmonic waveguides.

* Experimental results.

In theory, some more complicated structures can achieve higher coupling efficiencies. For example, Veronis et al. [127] investigated a multisection tapered coupler between a 300 nm-wide Si-slab waveguide and a 50 nm-wide metal-insulator-metal plasmonic waveguides. As shown in Figure 9a, the taper consists of four silicon waveguide sections and four MIM plasmonic waveguide sections. The lengths of the eight waveguide sections are all 50 nm, and the widths of them are optimized by the microgenetic algorithm. With the optimal value of $w_1 = 420$ nm, $w_2 = 440$ nm, $w_3 = 440$ nm, $w_4 = 340$ nm, $w_5 = 330$ nm,

 $w_6 = 40 \text{ nm}, w_7 = 40 \text{ nm}, w_8 = 120 \text{ nm}$, the multisection taper reaches a coupling efficiency of 93%. Similarly, a partially corrugated taper [143] (shown in Figure 9b) was demonstrated by Y. Liu. et al. The dispersion relationship of corrugated waveguides can be engineered to extend across the light line [147,148]. In the coupler design, they utilized this principle to convert the silicon-waveguide-guided mode across the light line to match the plasmonic gap waveguide mode. As a result, a coupling efficiency of 93% was also realized between a 1.25 µm-wide Si-slab waveguide and a 50 nm-wide plasmonic gap waveguide. Figure 9c illustrates a coupler structure for silicon slot waveguides and hybrid plasmonic waveguides. The coupling region consists of a small air gap with a length of $H_{gap} = 50$ nm. Compared with direct coupling, the insertion of the intermediate section improves the coupling efficiency from 75% to 90%. By taking more parameters into account, these more complicated taper structures can be designed to significantly reduce the coupling loss. However, the complexity of structures can be challenging in fabrication. In [132], a slot-funnel (SF) structure (shown in Figure 9d) for mode conversion was designed and fabricated. An additional silicon strip-slot mode converter was added before the conventional taper structure. According to the slot-slot coupling scheme, the mode and effective refractive index matching are improved, and only a small loss due to the gaps between silicon and metal is introduced. In the experiment, the coupling loss of the slot-funnel mode converter was measured to be 4 dB, which is above expectations and can be attributed to the fabrication roughness and misalignment.



Figure 9. Some more complicated tapered coupling designs with simulated coupling efficiencies of (a) 93% [127], (b) 93% [143], (c) 90% [130], and experimentally measured coupling loss of (d) 4 dB [132]. Figures reproduced from (a) [127]; (b) [143]; (c) [130]; (d) [132].

3.2. Directional Coupling Design

As opposed to tapered coupling, the silicon and plasmonic waveguides should be parallel to each other in the directional coupling design for overlapping the evanescent fields. In 2004, Hochberg et al. [149] demonstrated the directional coupling between a 500 nm \times 120 nm silicon waveguide and a 100 nm-thick layer of silver. As shown in

Figure 10, the silicon waveguide is placed beside the silver layer with a separation of 150 nm and a coupling length of 1.8 μ m. Since the plasmonic waveguide is just a simple single interface one, the light field tends to escape into free space. The coupling loss was measured to be 4.2 \pm 1.6 dB at the wavelength range of 1510–1520 nm in the experiment.



Figure 10. Directional coupling between silicon waveguides and a single interface plasmonic waveguide. (a) A rendering of simulated field profile of the coupler. (b) An SEM image of the fabricated coupler. Figures reproduced from [149].

Compared with the single interface metal, the directional coupling into metal-insulatormetal multilayer plasmonic waveguides usually have better light confinement and lower coupling loss. Figure 11 shows two reported directional couplers between silicon waveguides and MIM plasmonic waveguides with horizontal and vertical space, respectively. Figure 11a,b is the cross-section and top views of a horizontally spaced directional coupler [150]. For overlapping with the evanescent fields in the silicon waveguide, the MIM plasmonic waveguide should also be a horizontally oriented one in the horizontally spaced directional coupler (as shown in Figure 11a). According to the coupled-mode theory, the TM mode couples between the silicon and plasmonic waveguides and oscillates as a function of the length. The characterization of directional coupling is illustrated in Figure 11c, in which the different coupling lengths L_1 and L_2 correspond to two different distances of 20 nm and 60 nm between the silicon and plasmonic waveguides. The electric field distribution is shown in Figure 11d, which also reveals the nature of field oscillating in directional coupling. In [151], Delacour et al. designed and fabricated a directional coupler with the silicon and plasmonic waveguides vertically spaced (shown in Figure 11e–i), of which the principle is the same as the previous one in [150]. In the experiment, they measured at least 70% coupling efficiency around the wavelength of 1550 nm from a 400 nm imes 220 nm silicon strip waveguide to a 25 nm \times 50 nm silver slot waveguide with a metal-silicon gap of 30 nm and coupling length of 0.9 μ m.

The directional coupler for silicon waveguide and hybrid plasmonic waveguide was designed and fabricated by Chelladurai et al. [112] in 2019. The schematic and SEM image of the hybrid plasmonic coupler are presented in Figure 12a,b. The authors fabricated the device in three steps: first, they created the silicon by electron beam lithography and dry etching, then deposited the silica spacer layer using PECVD, and, finally, used a lift-off process to evaporate the titanium adhesion layer and the gold layer. Figure 12c shows the schematic of the structure used to measure the coupling loss and propagation loss of the coupler. By linear-fitting the measured transmission of the through and cross ports for the varying hybrid length L, the coupling loss and propagation loss could be found to be 0.16 dB/ μ m and 0.27 dB with the optimal structure. Compared with tapered coupling designs, the hybrid plasmonic directional coupler can achieve much higher coupling efficiency, which could be attributed to the physical principle of the directional coupling and larger fabrication tolerance of the directional coupler structure design. However, the input and output waveguides are non-collinear in the directional coupler, while the tapered coupler can simply connect the input and output waveguides together on one straight line. For these reasons, it is better to choose the coupling methods based on practical usage.



Figure 11. Directional coupling between silicon waveguides and metal–insulator–metal plasmonic waveguides. (**a**) Cross-section and (**b**) top views of a horizontally spaced directional coupler, of which the coupling efficiency and field distribution are shown in (**c**,**d**), respectively. (**e**) Perspective and (**f**) side views of a vertically spaced directional coupler, of which the SEM cross-section view, top view, and normalized transmission are shown in (**g**,**h**,**i**), respectively. Figures reproduced from (**a**–**d**) [150]; (**e**–**i**) [151].



Figure 12. Directional coupling between silicon waveguides and hybrid plasmonic waveguides. (a) Schematic structure and (b) SEM image of the proposed coupler. (c) Schematic structure used to measure the coupling efficiency in the experiment. (d) Measured (dots) and simulated (solid lines) coupling efficiencies as functions of the gap width. Figures reproduced from [112].

4. Prospects and Challenges of HPPs

Silicon-based hybrid plasmonic devices and circuits have attracted the interest of researchers for some time. This is due to the unique characteristics of plasmonics that can realize stronger light confinement and improve the performance and integration of silicon-based optoelectronics. Figure 13 shows some recent representative works of silicon-based hybrid plasmonics that also concern the coupling designs of plasmonic waveguides. In 2018, an outcome of a plasmonic electro-optic modulator was reported by Haffner et al. [91]. As shown in Figure 13a, the plasmonic ring resonator couples to the silicon waveguide by directional coupling methods with a coupling loss of about 1 dB. In the off state, light is coupled to the plasmonic ring resonator. While in the on state, the plasmonic ring is out of resonance to prevent coupling loss. The fabricated compact plasmonic

electro-optic ring modulator can be operated at over 100 GHz with great energy efficiency. This result reveals the potential of silicon-based hybrid plasmonics to realize fast and compact communications technologies. Similarly, Ding et al. and Ono et al. demonstrated a graphene plasmonic photodetector (Figure 13b) and switch (Figure 13c), respectively, in 2020. These structures use tapered couplers to connect to silicon waveguides. Taking advantage of higher carrier mobility, unique electronic band structure, and ultra-broadband nonlinear absorption, these graphene-based devices realize ultra-compact footprints, high speed, and efficient energy consumption at the same time.



Figure 13. Some latest works of HPPs based on SOI platform. (**a**) A plasmonic electro-optic modulator. (**b**) An integrated graphene plasmonic photodetector. (**c**) A graphene-loaded plasmonic all-optical switch. Figures reproduced from (**a**) [91]; (**b**) [152]; (**c**) [153].

Obviously, silicon hybrid plasmonics is still in its infancy. The great dream of making hybrid plasmonic circuits on a silicon-on-insulator platform will require much further research. By using an efficient coupling design, some hybrid plasmonic components may find their way into silicon-based optoelectronics as discrete elements. However, one of the major blocks in the way is its non-compatibility with conventional CMOS fabrication processes. Involving metals or low-dimensional materials (e.g., graphene), these hybrid plasmonic components must be fabricated with film liftoff and transfer technology, which requires additional processing steps. Since silicon photonic devices are almost fully CMOS-compatible, it is our hope that some supplementary processes will be developed in the future.

5. Conclusions

In this review, we present the development trends of silicon-based optoelectronics and the challenges that can be overcome by hybrid plasmon polaritons. Silicon photonic devices and systems dissipate much less power and have greater bandwidth than electronic ones. Compatibility with the mature CMOS technology also makes silicon-based optoelectronics the best candidate for large-scale optoelectronic integration. One of the major challenges in the development of silicon-based optoelectronics is the diffraction limit, which impedes the further improvement of chip integration. Plasmonics has unique prospects for designing highly integrated optoelectronic circuits due to its significantly strong light confinement. However, metals exhibit substantial heating losses in the interaction with light. Hence, hybrid plasmon polaritons can enhance silicon-based optoelectronics in light confinement while keeping a low propagation loss. Two coupling designs for silicon and plasmonic waveguides have been reported in the literature. The tapered coupling design can achieve a higher field intensity enhancement, while the directional coupling design has a lower coupling loss. With enhancement by hybrid plasmon polaritons, it is expected that siliconbased optoelectronics will obtain further development to a higher integration scale.

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