Design of Compact, Broadband, and Low-Loss Silicon Waveguide Bends with Radius under 500 nm

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Abstract: Waveguide bend is an indispensable component in the on-chip compact photonic integrated circuits (PICs) and the minimum bend size greatly limits the increase of integration density of PICs. Here, we propose broadband and low-loss silicon waveguide bend schemes using air trenches on both sides and embedded germanium arc in the inner side of waveguide bend. Using these ways, the silicon waveguide bending radius can be greatly reduced to less than 500 nm and the obtained insertion loss (IL) can be as low as 0.12 dB compared with IL = 1.73 dB obtained by direct silicon waveguide bend under the same bending radius. Meanwhile, the working bandwidth can be extended over 500 nm covering the whole optical communication band by keeping IL < 0.5 dB. Therefore, the proposed device schemes could push the development of on-chip PICs toward higher integration density.

Keywords: silicon photonic integrated components; waveguide bend; ultracompact size

1. Introduction

Silicon-on-insulator (SOI), a promising platform for silicon photonics, has attracted tremendous interest to realize compact, high-yield, and energy-efficient photonic integrated circuits (PICs) due to its high refractive-index-contrast and complementary metal-oxide-semiconductor (CMOS) processing [1,2]. To make an on-chip compact integration, waveguide bends become inevitable which can efficiently connect different photonic components on the same chip within a specified range [3]. For the waveguide bend, bending loss is a vital important parameter which is directly determined by the bending radius and waveguide width [4–7]. To reduce the on-chip bending loss, various waveguide structures and design methods have been reported, e.g., free-form curves [8], waveguide lateral offsets [9], etching slots [10,11], corner mirrors [12,13], subwavelength grating bendings [14,15], and boundary-shape optimizations [16–18]. Note that these waveguide bend schemes are mainly working at the bending radius larger than 1 µm and the waveguide width has been increased even up to the multimode waveguide width in order to reduce the bending loss. However, these bending size requirements greatly limit the further development of silicon photonics toward ultrasmall size and on-chip high density integration.

To break the bending radius limitation of silicon waveguide and reduce this limitation (1 µm) to less than 500 nm, abovementioned schemes are almost not suitable. Fortunately, surface plasmon polariton waveguide and hybrid plasmonic waveguide were proposed and became efficient structures to realize submicron waveguide bend due to their strong light field interactions [19,20]. However, the main issue of these waveguide structures is the metal absorption loss, and the lowest bending loss is higher than 1 dB for a 90° bend with a bending radius of 500 nm, which is relatively high for an ultrasmall waveguide bend [19]. Recently, inverse design method based on numerous optimization algorithms have been applied to design the silicon waveguide bend and the minimum bending radius can be reduced to less than 500 nm [21,22]. However, these optimization methods require...
large numbers of iterative calculations which are quite time-consuming, and the generated device patterns might pose huge challenges for the device fabrications since there are some tiny structures that are difficult to be fabricated accurately [21–25]. Meanwhile, the obtained bending loss is ~1 dB for a typical 90° waveguide bend as well as small working bandwidth [21–24]. Therefore, low-loss and broadband silicon waveguide bend with a bending radius of less than 500 nm is our pursuit goal.

In this paper, we propose a compact silicon waveguide bend, where two optimized air trenches are applied on both sides of the bending part. By introducing these two air trenches, the refractive index difference between silicon waveguide and cladding is increased for the TE polarization, and then the TE mode can be more confined by the silicon waveguide, thus reducing its bending loss [26]. From results, the obtained insertion loss (IL) of TE mode is only 0.28 dB for the proposed waveguide bend with bending radius of 480 nm at the wavelength of 1.55 µm, which is clearly lower than previous reports [10–19,21–24], and the working bandwidth is 500 nm (IL < 0.5 dB). To further reduce bending loss, we introduce a high refractive index material of germanium (Ge) and embed it into the inner side of the silicon waveguide bend to further enhance the mode confinement ability. Note that IL is reduced to only 0.12 dB for a 90° bend and the working bandwidth can be further extended over 650 nm by keeping IL < 0.5 dB, which could well support the broadband operation of on-chip photonic devices with high integration density. We believe the proposed compact, broadband, and low-loss silicon waveguide bend schemes would be very beneficial and promising for the current and future on-chip high density PICs [1,2].

2. Device Structure and Principle

Figure 1a illustrates the three-dimensional (3D) schematic of a conventional direct silicon waveguide bend with a radius \( R = 480 \) nm which is defined as the distance between the center of 90° bend and the center of silicon waveguide. The input and output waveguides are typical silicon waveguides with a width of \( W = 500 \) nm and a thickness of \( h = 220 \) nm, respectively, and the whole waveguide bend is covered by silicon dioxide as the upper cladding. To get the light transmission performance through such silicon waveguide bend, the 3D finite-difference time-domain (FDTD) method is used [27,28]. Figure 1b shows the calculated electric field evolution through such device for the input fundamental TE\(_0\) mode at a wavelength of 1.55 µm. After input mode passing through the direct waveguide bend, obvious mode interference phenomenon can be observed, generating a periodic mode interference pattern, and the obtained IL is 1.73 dB which is quite large for the on-chip compact light transmission. Moreover, wavelength spectrum analyses have been conducted for the direct silicon waveguide bend in a broad range from 1.2 µm to 1.9 µm, as shown in Figure 1c, where the material dispersions have been considered [29]. Note that the direct waveguide bend almost has larger IL working at long wavelength compared to at a short one and the largest IL is even higher than 3.5 dB. Therefore, we should consider effective ways to reduce such loss.

Before we perform the waveguide bend design, the main source of the bending loss needs to be analyzed at first. From our calculations, the bending loss is mainly coming from two parts, mode mismatching loss between strip waveguide and bend waveguide and transmission loss within the bending region. As the bending radius goes down to less than 1 µm (or even 500 nm) for the silicon waveguide, the bending waveguide mode will leak and tend to the bending outside within the cladding region, thus leading to the clear increase of mode mismatching loss and transmission loss for the input TE\(_0\) mode, as shown in Figure 1b. To reduce bending loss, the waveguide mode should be more confined in the waveguide core especially in the bending region [19]. So, we need to create larger refractive index difference of silicon waveguide compared to direct silicon waveguide bend illustrated in Figure 1a. Based on such mechanism, two ways can be employed, one is reducing the cladding refractive index and other one is increasing the core refractive index.
Therefore, we will use these ways to effectively reduce the bending loss for the compact silicon waveguide bend with a bending radius less than 500 nm.

Figure 1. 90° direct silicon waveguide bend. (a) Device schematic. (b) Electric field evolution (|E|) through the direct waveguide bend with a radius of $R = 0.48 \mu m$, where $|E|$ stands for the norm of electric field. (c) Wavelength spectrum of IL for the device in a wavelength range from 1.2 $\mu m$ to 1.9 $\mu m$.

3. Results and Discussion

Figure 2a shows the silicon waveguide bend with two air trenches on both sides of the bending region, where the air trench is formed by deep etching from upper cladding to the silicon substrate. Using this structure, the refractive index difference between waveguide core and cladding for the TE polarization reaches the largest if no other materials are added. Two air trenches are located at the inside and outside of the waveguide bend region respectively, and their shapes are different. The outside trench is an arc shape with a radian angle of 90° and a trench width of $W_{TO}$, and the inside trench is an equilateral right triangle shape with a rounded corner of 90° and a width of $W_{TI}$, respectively, as illustrated in Figure 2a. To find the optimum air trench sizes, we analyze the air trench widths ($W_{TI}$, $W_{TO}$) affecting the device IL shown in Figure 2b. Note that the device IL first decreases as air trench widths increase from 0 and gradually becomes saturated when both $W_{TI}$ and $W_{TO}$ are larger than 0.6 $\mu m$. Moreover, we also plot an enlarged view as $W_{TO}$ varies from 0.6 to 1.0 $\mu m$, and we can clearly find that $W_{TI} = 0.8 \mu m$ corresponds to the lowest IL. For the chosen $W_{TO}$, we analyze the IL curve versus $W_{TO}$ when $W_{TI}$ equals to 0.8 $\mu m$, which is shown as a red curve in Figure 2b. By analyzing the curve, we can find that the change rate of IL is even lower than 5% when $W_{TI}$ is larger than 0.6 $\mu m$, which is relatively stable. Under such a condition, we set $W_{TI}$ to 0.7 $\mu m$ where the obtained IL is relatively low and stable. The corresponding IL clearly decreases from 1.73 dB to 0.28 dB with reflection loss lower than −30 dB. From electric field evolution shown in Figure 2c, we can observe that the mode interference phenomenon at the output waveguide has been effectively suppressed and the output field is more steady together with higher power than the result shown in Figure 1b. Moreover, we also calculate the wavelength spectrum of IL for such a device, as shown in Figure 2d. By comparison, the obtained ILs reveal an overall decrease within the whole calculation range and the allowable working band is over 500 nm by keeping IL less than 0.5 dB. From Figure 2c, however, slight mode interference at the output waveguide can be observed. Next, we will use new ways to address this issue and further reduce the device IL.
waveguide bend with air trenches are also plotted for comparison. From Figure 3d, the waveguide bend and the mode field transmission reveals a quite stable behavior when passing through the designed bend. We further study the wavelength spectrum of IL for the proposed device, where $|E|$ stands for the norm of electric field.

Based on the device structure shown in Figure 2a, we further embed a high refractive index material of Ge with a shape of $90^\circ$ arc in the inner side of the silicon waveguide bend, as shown in Figure 3a, where the Ge arc width is $W_G$. By embedding Ge into the waveguide bend, the refractive index of waveguide can be increased since the refractive index of Ge is larger than that of silicon, thus increasing the mode confinement. Figure 3b plots the device IL as functions of Ge arc width $W_G$ and outside air trench width $W_{TO}$, where the inside air trench width is still fixed as $W_{TI} = 0.8 \mu m$. Note that the device IL reaches to the minimum value as $W_G$ equals to 0.18 $\mu m$ since the influence of Ge on the waveguide mode is weak as $W_G$ gets smaller (<0.18 $\mu m$) while the mode mismatching loss increases quickly as $W_G$ gets larger (>0.18 $\mu m$). So, the balance point is just located at $W_G = 0.18 \mu m$, corresponding to the lowest IL. As $W_{TO}$ is still set as 0.7 $\mu m$, the obtained IL can be further decreased from 0.28 dB to 0.15 dB, which is quite promising for the on-chip low-loss transmission in an ultracompact size. Figure 3c illustrates the electric field evolution through the proposed waveguide bend and the mode field transmission reveals a quite stable behavior when passing through the designed bend. We further study the wavelength spectrum of IL for the proposed waveguide bend shown in Figure 3d, where the material dispersions have been considered [29]. Note that the wavelength spectra of direct waveguide bend and waveguide bend with air trenches are also plotted for comparison. From Figure 3d, the scheme shown in Figure 3a has the lowest IL and largest bandwidth. If IL still needs to be less than 0.5 dB, the available working bandwidth can be further extended from 500 nm to 650 nm, covering the whole optical communication band.
By virtue of the low-loss advantage of embedded Ge arc in the waveguide bend, we further study the structure extension of Ge on the bending performance. Figure 4a shows the waveguide bend structure, where the embedded Ge arc is extended toward the inside ($W_{GI}$) and outside ($W_{GO}$) refers to the inside wall of the silicon waveguide bend as the baseline. Detailed parameter analyses of these extension widths ($W_{GI}$, $W_{GO}$) on the device performance (IL) are shown in Figure 4b. From Figure 4b, we can clearly find two minimum regions of IL, one corresponds to $W_{GI} = 0.17 \mu m$, $W_{GO} = 0.18 \mu m$ and the other one corresponds to $W_{GI} = 0.07 \mu m$, $W_{GO} = 0.16 \mu m$, respectively. These two regions are marked as Ge I and Ge II and the obtained IL of these two regions are very close, ~0.12 dB. Their electric field evolutions through the designed bends are plotted in Figure 4c, where the mode field transmission is quite stable without any clear wave fluctuations and the achieved ultralow loss of only 0.12 dB is quite difficult to obtain using previous reports under a bending radius of less than 500 nm [8–19,21–24]. Meanwhile, the device reflection losses are lower than −28 dB. Wavelength spectra of these embedded Ge arc schemes in the waveguide bend are analyzed in Figure 4d, where the material dispersions have been considered [29]. Note that their wavelength dependences of IL are similar and the allowable working bandwidth can be over 650 nm (IL < 0.5 dB). Moreover, Ge II type has the best performance in the short wavelength ($\lambda < 1.5 \mu m$).

Figure 3. (a) Schematic of the silicon waveguide bend with two air trenches on both sides and embedded with a 90° arc made of Ge in the inner side. Insets show the enlarged views of the designed bend. (b) Device IL dependent on the Ge arc width $W_G$ and outside air trench width $W_{TO}$. (c) Electric field evolution ($|E|$) through the proposed waveguide bend, where $|E|$ stands for the norm of electric field. (d) Wavelength spectrum of IL for the proposed waveguide bend together with that for the direct waveguide bend and waveguide bend with air trenches. AT: Air Trench.
For the device fabrication, we employ the proposed silicon waveguide bend with air trenches and embedded Ge arc as an example, and four main fabrication steps will be required [1,30]. First, the silicon waveguide 90° bend is fabricated using E-beam lithography and etching process on a standard SOI wafer (220 nm-thick top silicon layer and 2 μm-thick buried oxide layer), where the input/output waveguide width is 500 nm and the inner side of 90° bend should also be etched to leave space for the embedded Ge arc. Second, a 220 nm-thick Ge layer is grown on the silicon waveguide bend by chemical vapor deposition and then etched to form the Ge arc in the inner side of 90° bend, where other parts need to be removed [31]. Third, a 2 μm-thick upper cladding is deposited using plasma enhanced chemical vapor deposition to protect the waveguide bend. Finally, deep etching method is used to generate the designed inner and outside trenches of silicon waveguide bend, where the etching depth is from upper cladding down to the silicon substrate (total etching depth: 4 μm) [30].

Finally, in Table 1 we compare our proposed waveguide bends with previous reports under a bending radius of 1 μm, where the employed device structure, bending radius, waveguide width, footprint, IL, and bandwidth have been considered for the TE polarization [18,19,21,23]. By comparison, the proposed device has the lowest IL, largest bandwidth, and compact size. In addition, we also consider if such bending structure can be applied in the racetrack resonator [32,33], where the proposed low-loss and broadband 90° bend is used which could help greatly reduce the footprint of micro-resonator with relatively low loss. As we mentioned in the device fabrication process, the proposed silicon waveguide bend requires several extra fabrication steps compared with conventionally used silicon waveguide micro-resonator. The fabrication impression during the embedded Ge arc formation will clearly affect the bending loss. So, the key Q factor will be determined by the practical device fabrication though the proposed waveguide bend could support the
compact racetrack resonator. The reduced resonator size is very beneficial to the increment of free spectral range (FSR), which contributes to some applications requiring large FSR, e.g., wavelength division multiplexing systems [34]. Therefore, we hope the proposed waveguide bend schemes could find important applications in the current and future on-chip high density PICs.

Table 1. Device comparisons between various silicon waveguide bends (bending radius < 1 µm).

<table>
<thead>
<tr>
<th>Reference</th>
<th>Structure</th>
<th>Bending Angle</th>
<th>Radius (µm)</th>
<th>Width (µm)</th>
<th>Footprint (µm²)</th>
<th>IL (dB)</th>
<th>BW (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[18] [E]</td>
<td>BSO</td>
<td>90°</td>
<td>1</td>
<td>0.645</td>
<td>1.6 × 1.6</td>
<td>0.35 ± 0.05</td>
<td>&lt;100   (IL &lt; 0.5 dB)</td>
</tr>
<tr>
<td>[19] [S]</td>
<td>SPP</td>
<td>90°</td>
<td>0.5</td>
<td>0.5</td>
<td>~1 × 1</td>
<td>&gt;1</td>
<td>-</td>
</tr>
<tr>
<td>[21] [S]</td>
<td>ID</td>
<td>180°</td>
<td>0.38</td>
<td>0.44</td>
<td>1.2 × 1.2</td>
<td>1.73</td>
<td>25      (IL &lt; 1.2 dB)</td>
</tr>
<tr>
<td>[23] [E]</td>
<td>ID</td>
<td>180°</td>
<td>-0.5</td>
<td>0.44</td>
<td>1.2 × 1.2</td>
<td>1.07</td>
<td>100     (IL &lt; 2 dB)</td>
</tr>
<tr>
<td>This work</td>
<td>AT &amp; Ge</td>
<td>90°</td>
<td>0.48</td>
<td>0.5</td>
<td>2.2 × 2.2</td>
<td>0.15</td>
<td>650     (IL &lt; 0.5 dB)</td>
</tr>
<tr>
<td></td>
<td>Ge I/Ge II</td>
<td></td>
<td>0.12</td>
<td></td>
<td></td>
<td>0.12</td>
<td>&gt;650    (IL &lt; 0.5 dB)</td>
</tr>
</tbody>
</table>

BSO: boundary-shape optimization; SPP: surface plasmon polariton; ID: inverse design; AT: air trench; IL: insertion loss; BW: bandwidth for TE polarization; E: experiment; S: simulation; “-”: not mentioned.

4. Conclusions

In summary, utilizing air trenches and embedded Ge arc structures, we have proposed broadband and low-loss silicon waveguide bend schemes, which can realize the compact silicon waveguide bend with a bending radius less than 500 nm. The key bending region is formed by etching two air trenches on both sides of the silicon waveguide 90° bend and embedding a high refractive-index Ge arc in the inner side. Using these ways, the waveguide bending loss is greatly reduced from 1.73 dB (direct silicon waveguide bend) to 0.28 dB (with two air trenches), 0.15 dB (with air trenches and embedded Ge arc), and 0.12 dB (with air trenches and embedded Ge arc extension). Moreover, these device working bandwidths can be over 500 nm covering the whole optical communication band (IL < 0.5 dB). With these advantages, the proposed device schemes could become good candidates to realize on-chip broadband and low-loss optical circuits with high integration density.

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References


