All-Monolithically Integrated Self-Scanning Addressable VCSEL Array for 3D Sensing

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Abstract: We propose an all-monolithically integrated self-scanning addressable vertical-cavity surface-emitting laser array for time-of-flight measurement. Some advantages of addressable VCSELs for ToF measurement applications include large reductions in power consumption, heat generation, multi-pass noise, and flare noise. In this paper, we discuss the characteristics of the proposed self-scanning addressable VCSEL array. All layers in the epilayer structure of the proposed VCSEL array were formed at once by metal-organic chemical vapor deposition. The device consists of an (Al)GaAs-based thyristor and a conventional top-emitting 940-nm oxide-confined VCSEL on an n-type GaAs substrate. The array contained 12 blocks ($4 \times 3$) that have more than 40 emitters each. The device required only four signals from a field-programmable gate array to select the emitting blocks and one emission signal from a conventional VCSEL driver, even for arrays containing hundreds of blocks. The proposed module is capable of one-block sequential emission, parallel emission from several blocks, and emission from all blocks. The rise and fall times of the fabricated VCSEL array were observed to be 200 and 400 ps, respectively, for each emission mode. The influence of flare noise from an obstacle in front of the camera was dramatically reduced by avoiding emission to the obstacle.

Keywords: addressable VCSEL; self-scan; 3D sensing; time of flight; thyristor

1. Introduction

Vertical-cavity surface-emitting lasers (VCSELs) are commonly used as light sources for optical communication, printers, heating, illumination, and sensor applications for cell phones, robots, and vehicles [1–7]. In particular, VCSELs are highly promising as a light source for 3D sensing owing to their high-power conversion efficiency, small wavelength drift against temperature, and low cost. Furthermore, the market for VCSELs in 3D sensing applications is growing dramatically.

A well-known technique for 3D sensing is time-of-flight (ToF) measurement, which is commonly used in the measurement range of 1 m to several hundred meters [6–11]. VCSEL technology is mainly applied to ToF measurements from below 1 m to several meters. However, this technique has limitations, as shown in Figure 1: (1) measurement error due to flare noise or multi-pass noise from floors, walls, and ceilings [12–14]; (2) poor distance measurement performance for low-reflective objects or those at long distances or in high-noise environments under the sun [15]; and (3) large power consumption and heat generation. These issues have prevented the widespread adoption of ToF systems. Addressable VCSEL is a key technology to overcome these limitations by avoiding emission obstacles. All the power is injected into one area of the VCSEL array, thereby increasing optical power density. Specific emission areas are selected to optimize power consumption and heat generation.
In this study, we developed an all-monolithically integrated self-scanning addressable VCSEL (SS-VCSEL) that has small circuits based on self-scanning light emitting device (SLED) technology composed of thyristors [16,17]. The thyristor has many advantages. For example, applying a small gate current can change the thyristor to the on-state, which can be maintained regardless of the gate voltage after switching. The thyristor is also highly tolerant against high currents and voltages, and exhibits high-speed switching below 10 ns [18]. An emitting diode, such as a VCSEL, of a device that has a diode-on-thyristor (DoT) structure is electrically connected to a switching thyristor in series through a tunnel junction.

2. Materials and Methods

Figure 2 shows a cross-sectional view of a conventional top-emitting 940-nm oxide-confined VCSEL with a single junction-emission region on a thyristor fabricated by us. There are 22 pairs p-Al_{0.15}Ga_{0.9}As/Al_{0.9}GaAs DBRs, 45 pairs n-Al_{0.15}Ga_{0.9}As/Al_{0.95}GaAs DBRs, and 3 InGaAs/AlGaAs quantum wells as an active layer. The thyristor is made of pnpn (Al)GaAs layers on an n-GaAs substrate. The VCSEL is connected in series to the thyristor through a GaAs-based tunnel junction. All layers in the epilayer structure are formed at once by metal-organic chemical vapor deposition. The VCSEL emits light if the voltage of the n-gate is changed to the on-level, and the n and p electrodes are supplied with a forward voltage that is larger than the threshold voltages of the VCSEL and the thyristor. Figure 3 shows an equivalent circuit of the proposed SS-VCSEL. The transmission region comprises transmission thyristors, diodes, and resistances. The on-state of the transmission thyristor is shifted to the next transmission thyristor sequentially by applying transmission signals 1 and 2 in order. The VCSEL that is connected to a transmission thyristor in the on-state emits light by adding an emission signal.
Figure 2. Cross-sectional view of a conventional top-emitting 940-nm oxide-confined VCSEL.

Figure 3. Equivalent circuit of the proposed SS-VCSEL.

Figure 4 shows the top view of the proposed SS-VCSEL for ToF measurement. The array is composed of a transmission region (right side of the chip), an emission region (left side of the chip), five bonding pads on the top, and one electrode on the bottom of the substrate. The emission region comprises a $4 \times 3$ array of blocks. Each block includes 41 emitters. The device size is 1.2 mm $\times$ 1.1 mm. The anode and cathode metals are the same as those of a conventional VCSEL array. The bonding pads are for the two transmission signals, a constant voltage, and emission signals.
Figure 2. Cross-sectional view of a conventional top-emitting 940-nm oxide-confined VCSEL.

Figure 3. Equivalent circuit of the proposed SS-VCSEL.

Figure 4. Schematic drawing of the proposed all-monolithically integrated self-scanning addressable VCSEL array for ToF measurement.

Figure 5 shows a top view of the transmission module containing the proposed SS-VCSEL. The field-programmable gate array (FPGA) on the left side of the module provides a minimum pulse width of 2.5 ns to control transmission and emission signals. The high voltage of the FPGA is 3.3 V. The SS-VCSEL, optical device, and commercial low-side laser diode driver (LDD) are situated on the right side of the module. The LDD can apply a maximum current of 3.6 A to the VCSEL by inputting the emission signal from the FPGA. The anode voltage of the SS-VCSEL can be changed up to 12 V, as shown in Figure 6.

Figure 6. Block diagram of the Tx module.

3. Results

Figure 7 shows the emission pattern of the SS-VCSEL generated by applying the transmission and emission signals. One-block sequential emission, parallel emission from several blocks, and emission from all blocks are possible by changing the input signals. The current–light and current–voltage characteristics of the VCSEL on the thyristor in the all-blocks emission mode are shown in Figure 8. The device was operated using a pulse width and duty cycle of 1 ms and 1%, respectively. The $I–L$ characteristics of the SS-VCSEL are identical to those of conventional VCSELs. Additionally, the threshold voltage of the SS-VCSEL is higher than that of conventional VCSELs because the thyristor is connected to the VCSEL in series.

Figure 9a,b show the $I–L$ characteristics of the fabricated SS-VCSEL on the Tx module at different temperatures corresponding to one-block and all-blocks emissions, respectively. In Figure 9b, the vertical axis is the output power per block of the all-blocks emission mode.
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Figure 8. (a) I–L and (b) I–V characteristics of the SS-VCSEL during all-blocks emission at different temperatures.

Figure 9a,b show the I–L characteristics of the fabricated SS-VCSEL on the Tx module at different temperatures corresponding to one-block and all-blocks emissions, respectively.
In Figure 9b, the vertical axis is the output power per block of the all-blocks emission mode. The module was operated using a pulse width and duty cycle of 10 ns and 5%, respectively. An optical output power of over 1 W was achieved during one-block emission at 75 °C. This result was 19 times higher than that of a single block in the all-blocks emission mode at a current of 2 A. The overall output power was 1.1 W/block × 12 blocks or 13 W at a temperature of 75 °C.

![Figure 8. (a) I–L and (b) I–V characteristics of the SS-VCSEL during all-blocks emission at different temperatures.](image1)

![Figure 9. I–L characteristics of the SS-VCSEL on the Tx module at different temperatures under (a) one-block and (b) all-blocks emissions; the vertical axis in (b) is the output power per block.](image2)

The SS-VCSEL output spectra of the Tx module at different temperatures obtained in the one-block and all-blocks emission modes are shown in Figure 10a,b, respectively. The current in the one-block and all-blocks emission modes were 2 A (49 mA/emitter) and 3.5 A (7 mA/emitter), respectively. The module was operated using a pulse width and duty cycle of 10 ns and 5%, respectively. The peak wavelengths during one-block emission and all-blocks emission at 25 °C were 943.0 and 941.8 nm, respectively. Narrow spectrum widths of 0.6 and 0.27 nm were achieved in the one-block and all-blocks emission modes, respectively. The spectrum width of one-block emission modes is wider than that of all-blocks emission modes due to the number of transverse modes with higher injected current density. The wavelength shift owing to changes in temperature was 0.06 nm.

![Figure 10. Output spectra of the SS-VCSEL on the Tx module at different temperatures under (a) one-block and (b) all-blocks emissions.](image3)
Figure 11a,b shows the far-field patterns of the SS-VCSEL on the Tx module at different temperatures in the one-block and all-blocks emission modes, respectively. The current during one-block and all-blocks emission were 2 A (49 mA/emitter) and 3.5 A (7 mA/emitter), respectively. The module was operated using a pulse width and duty cycle of 10 ns and 5%, respectively. The divergence angles corresponding to one-block and all-blocks emissions at 25 °C were 18.9° and 13.5°, respectively. The divergence angles of one-block emission modes is wider than that of all-blocks emission modes due to the number of transverse modes with higher injected current density. The profiles and divergence angles were stable in the temperature range of 25–75 °C.

Figure 12a,b show the pulse operation in the one-block and all-blocks emissions modes, respectively. The module was operated using a pulse width and duty cycle of 10 ns and 5%, respectively. The rise times during all-blocks and one-block emissions were 243 and 282 ps, respectively. Therefore, a good rise time was achieved for application in the direct ToF system. The overshot in Figure 12a is a conventional relaxation oscillation of the lasing. The fall times during one-block and all-blocks emissions were less than 500 ps. The shape of the optical pulse from a single block can be optimized by changing the parameters of the VCSEL driver for indirect ToF systems. The pulse width can be shortened up to 2.5 ns by keeping rise time and fall time the same for one-block and all-blocks emissions.
4. Discussion

Figure 13 shows a comparison between the current–optical power density characteristics of a conventional three-junction VCSEL array with approximately 500 emitters and one-block and all-blocks emission of an SS-VCSEL with a single-junction active layer. Even though the optical power density of the all-blocks SS-VCSEL emission is lower than that of the conventional multi-junction VCSEL because of the number of junctions of active layers, the power density of one-block emission is higher than that of the multi-junction VCSEL. This result shows that the signal-to-noise (S/N) ratio is higher, the measurement distance is longer, and the power consumption and heat generation are lower when using the SS-VCSEL in comparison with those of the conventional multi-junction VCSEL. Moreover, the SS-VCSEL optical power density can be increased further by applying a multi-junction active layer.

![Figure 13.](image)

(a) Comparison between current–optical power density characteristics of a conventional three-junction VCSEL array with approximately 500 emitters and an SS-VCSEL with a single-junction active layer under one-block and all-blocks emissions. (b) Schematic of the measurement distances of the devices.

The advantages of the proposed SS-VCSEL over conventional addressable VCSELs are the following in Figure 14. The SS-VCSEL has a common anode and cathode metal that enables the uniform injection of current into each emitter in the block and the realization of simple circuits to minimize inductance. Moreover, the SS-VCSEL requires only a one-channel driver, even if the number of blocks exceed 100. No electrical skew occurs from the driver, and all currents can be injected into a single block.

<table>
<thead>
<tr>
<th>Point</th>
<th>Advantage</th>
<th>Self-scanning VCSEL</th>
<th>Conventional VCSEL</th>
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<tbody>
<tr>
<td>Common anode and cathode</td>
<td>Uniform current injection</td>
<td>Uniform optical output power</td>
<td>Uniform</td>
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<td>Simple circuits</td>
<td>Low inductance</td>
<td>Good electrical pulse shape</td>
<td>High inductance, bad pulse shape</td>
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<tr>
<td>Only 1th VCSEL Driver</td>
<td>Driver (Current 4A)</td>
<td>VCSEL</td>
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</tr>
<tr>
<td>No electrical skew from the Driver</td>
<td>Small optical skew for each block</td>
<td></td>
<td></td>
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<tr>
<td>Inject whole current into 1 block</td>
<td>Higher optical output power density</td>
<td></td>
<td>Need same size drivers for each block</td>
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![Figure 14.](image)

Advantages of the SS-VCSEL over conventional VCSELs.
5. Conclusions

We successfully designed, fabricated, and evaluated an all-monolithically integrated SS-VCSEL array that contains 12 blocks with 41 top-emitting VCSELs in each block for application to ToF systems. Any block emission mode can be realized. The optical power density of the proposed SS-VCSEL can exceed that of a conventional three-junction VCSEL owing to the concentration of the current on one block without lethal heating, despite the SS-VCSEL having a single-junction active layer. Further increases in optical power density can be realized by applying a multi-junction active layer. The rise time of the proposed SS-VCSEL was below 500 ps, and a good optical pulse shape was achieved. The number of blocks can be increased up to 100 without increasing the number of pads on the chip, resulting in much smaller chip and module sizes compared with other addressable VCSEL arrays. The SS-VCSEL is a highly promising light source for ToF systems.

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