Minimisation of Parasitic Capacitance in Lumped-Element Electro-Absorption Modulators for High-Speed Optical Components

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Abstract: This paper presents an investigation into the parasitic capacitance of an RF contact scheme for lumped-element EAMs. Test structures are fabricated to analyse this parasitic capacitance via $S_{11}$ characterisation using a vector network analyser (VNA). Optimisations of the contact scheme lead to the parasitic capacitance being reduced to <10 fF. EAMs using this contact scheme are fabricated and characterised using $S_{11}$ measurements. These $S_{11}$ measurements are used to simulate $S_{21}$ measurements, which predict a $f_{3dB}$ bandwidth of near 80 GHz using an equivalent circuit model.

Keywords: lumped-element electro-absorption modulators; radio-frequency modulation; parasitic capacitance; contact scheme

1. Introduction

Heavy increases in internet traffic have spurred renewed interest in low-cost, low-power-consumption, cost-effective optical transceivers for usage in data centres. This growth in demand has sparked active discussions and standardisation efforts for 800 Gigabit Ethernet (800 GbE) and 1.6 Terabit Ethernet (1.6 Tbe) [1,2]. These networks require optical transceivers constructed from densely packed parallel channels that can run at high bitrates (>50 G/s) while consuming very little power. External modulation is a good choice at these speeds to enable data transfer with a high enough level of quality.

Electro-absorption modulators (EAMs) offer a solution to this need, requiring relatively simple fabrication consisting of reverse-biased p-i-n waveguides whose electrical contacts do not require overly specific design restrictions. EAMs monolithically integrated with distributed feedback lasers (DFBs) have shown major progress in terms of operational speed. In 2017, Ozolins et al. reported a 116 Gb/s on-off keying (OOK), four pulse amplitude modulation (PAM) and 105-Gb/s 8-PAM optical transmitter using an InP-based modulated laser integrated and packaged externally [3].

In 2019, Nakai et al. showed a high-bandwidth 1.3 µm uncooled electro-absorption modulator-integrated distributed-feedback laser and demonstrated uncooled 53 GBd four-level pulse amplitude modulation (PAM4) operation with low drive voltage [4]. The simplicity of EAM operation through reverse-biased light absorption has also made them prime candidates for usage on the silicon platform [5]. EAMs using InP have also been shown to be successfully integrated onto the silicon platform using die-bonding [6,7] and micro-transfer printing to much success [8].

Lumped-element EAMs enable the realisation of highly efficient, small-footprint, high-modulation efficiency and low-drive voltage and on the InP platform EAMs benefit from a strong electro-absorption effect, especially the quantum-confined Stark effect [9], and consequently an EAM can be as short as 50 µm but the modulation bandwidth of a
lumped-element EAM depends on the capacitance of the device, which consists of the waveguide and the electrical contacts used to reverse-bias it to facilitate absorption.

The capacitance of the electrical contacts is known as parasitic, which we seek to minimise in order to maximise the speed of our devices. The minimisation of parasitic capacitance in lumped-element EAMs is a critical aspect in the design of high-performance optical transmitters. This article discusses the challenges associated with minimising parasitic capacitance in lumped-element EAMs to reduce losses while achieving wide bandwidth at high-speed operation with low power consumption. By presenting an easily replicated technique it is hoped that a simple improvement in RF contact pad design for lumped-element EAMs will facilitate the increase in speed necessary to facilitate growing network demands.

2. Device Design

Figure 1 shows a schematic of the lumped-element EAM device design used for this research. The design consists of a p-i-n InP waveguide and three p-i-n InP pillars upon which the ground, signal and ground (GSG) contacts sit in order to be planar with the EAM waveguide. The signal pillar and the waveguide are connected by a metal bridge which sits atop patterned benzocyclobutene (BCB). The EAM is formed from a central electrically isolated section of the main waveguide, as can be seen in the SEM image on the right of Figure 1. This divides the waveguide into three sections. From left to right, these sections are a passive section for input, the EAM waveguide, and a passive section for output. The passivation of these sections is achieved through forward-bias. This design minimises the difficulty in manually scribing and cleaving EAMs as short as 50 µm by ensuring the overall chip size is ≥400 µm.

The lumped-element EAM device was fabricated on two different in-house-grown InP-based materials on a semi-insulating substrate. The quantum wells for these epitaxies were placed asymmetrically in the intrinsic region to minimise the material’s capacitance as in Daunt et al. [10]. These materials were designed to modulate wavelengths surrounding 1310 nm. The first material consisted of six compressively strained quantum wells, denoted 6 QW. The second consisted of twelve compressively strained quantum wells, denoted 12 QW. Standard lithographic techniques were used to define the ridge, with a ridge width of 2.5 µm, and height of 1.7 µm. The modulating section of the EAM is electrically isolated from surrounding pseudo-passive sections by etching away the contact layers, resulting in a measured isolation resistance of >10 kΩ. A separate etch through the quantum wells was performed so as to provide access to the n region to form a ground-signal-ground contact.

3. Equivalent Circuit Modelling

As seen in Figure 2, the EAM can be separated into three distinct electrical sections; the GSG contacts, the metal bridge suspended on a polymer connecting the signal contact to the EAM, and the EAM itself. The contact pads and the bridge are part of the electrical
contact scheme to deliver the RF signal to the EAM. The bandwidth of the EAM, $f_{3\text{dB}}$, is inversely related to the impedance of the entire circuit, thus minimising these parasitic impedances maximises the EAM’s speed.

In order to model the device, we calculate the impedance of each section of our circuit of resistors, $Z_R$, inductors, $Z_L$, and capacitors, $Z_C$, to form an equivalent Thevenin circuit of the entire structure. This is done by adding the impedance in series and parallel until only one remains, $Z_T$. For radio frequency (RF) signals, we have

$$Z_R = R \quad Z_L = i\omega L \quad Z_C = \frac{1}{i\omega C}$$

(1)

Using complex variables, the mathematics proceeds as if these quantities were simple resistors. Thus, by finding the frequency-dependent equivalent-impedance circuit for the EAM, we can find the reflection coefficient, $S_{11}(\omega)$.

$$S_{11}(\omega) = \frac{Z_T(\omega) - Z_0}{Z_T(\omega) + Z_0}$$

(2)

where $Z_0$ is our impedance match. With a method of calculating $S_{11}(\omega)$ based on our equivalent circuit, we can now recursively solve the equation to match the simulated $S_{11}(\omega)$ to an experimental $S_{11}(\omega)$ measurement. This allows us to solve for the parasitic capacitance present in each of our components by creating individual test structures which can isolate the constituent components of our EAM, the contact pads, the metal bridge, and finally the EAM itself.

![Figure 2.](image)

Electrically, the EAM device can be broken down into 3 distinct sections: the contact pad, the metal bridge connecting the contact pad to the EAM, and the EAM itself.

**4. Contact Scheme Optimisation**

**4.1. Contact Pad Optimisation**

In the fabrication of DC devices (<10 GHz operation), an n-doped substrate is often used, as shown on the left in Figure 3. This is often unsuitable for high-speed performance as the signal contact pillar’s parasitic capacitance is large, which can limit the device’s overall speed. The contact pillars are formed from the same p-i-n structure as the EAM waveguide, wherein the p-doped layers of the semiconductor and the n-doped layers may act as parallel plate capacitors with capacitance >400 fF. Further capacitance can be caused by the interaction of the metal bridge with the doped semiconductor layers. In the structure optimised for these devices for high-speed performance, a semi-insulating substrate is used and the contact pillars are isolated via a deep etch into the semi-insulating substrate, as shown in the centre of Figure 3. An alternate method of achieving high speed is through the use of a high-mesa semi-insulating buried heterostructure (SI-BH) [11].

This isolation prevents charge build-up below the signal contact, eliminating the capacitance between the signal contact and the n-doped layers. A test structure shown on the right of Figure 3 was characterised by measuring the $S_{11}$ scattering matrix from 0–40 GHz using an Anritsu vector network analyser (VNA). The measured complex impedance values were then fitted to an inductor–resistor–capacitor (LRC) circuit as described in the previous section with the extracted capacitance being ≈5 fF for the device. Figure 4a shows the $S_{11}$ measurements from the test structure as a Smith chart and Figure 4b shows the magnitude vs. frequency for the test structure.
Figure 3. On the left is a DC device with GSG contacts on an n-doped substrate. In the centre is a modified contact scheme designed to minimise the effect of the signal pad’s capacitance. On the right is the test structure fabricated to perform a measurement of the capacitance of the pads.

Figure 4. Experimental measurements from the pad test device. (a) Smith chart for the $S_{11}$ data from the pad test structure shown in Figure 3. (b) Magnitude vs. frequency for the $S_{11}$ data from the pad test structure shown in Figure 3.

Additional test structures were fabricated which varied the width of the deep-etch isolation as shown on the left of Figure 5. The numeric value of the isolation separation was taken to be the width of the isolation between the signal contact pillar and the area occupied by the waveguide. These devices were measured using the VNA and the capacitance was extracted. Two different fabrication runs were used to collect data for this measurement; in the first run, the isolation was etched 200 nm into the SI substrate. In the second run, the isolation etch was >500 nm into the SI substrate. Overall, not much variation was found due to the decrease in isolation width. The results on the right of Figure 5 show that 10 µm of isolation is sufficient to reduce the parasitic capacitance to acceptable levels. The variation between run 1 and run 2 can be attributed to the increased isolation depth.

Figure 5. On the left is a closer look at the test structure used to measure the pad capacitance. The isolation separation is highlighted. On the right is the collated result of the pad’s capacitance with varying isolation separation.
4.2. Metal Bridge Optimisation

The impedance of the pillars to the ridge waveguide was quantified using a test structure as shown in Figure 6 wherein the metal bridge sits atop a pillar of BCB. Using the equivalent circuit model fitted to the already-measured data of the contact pads shown previously, measurements of this test structure were able to isolate the parasitic capacitance exclusive to the metal bridge. The metal bridge forms a pair of capacitor plates with the lower n region remaining following the deep isolation etch as shown in the figure below. Figure 7a shows the $S_{11}$ measurements from the test structure as a Smith chart and Figure 7b shows the magnitude vs. frequency for the test structure. The parasitic capacitance of the bridge was experimentally verified via $S_{11}$ analysis to be $\approx 10\, \text{fF}$.

![Figure 6](image)

**Figure 6.** On the left is the test structure used to determine the metal bridge’s contribution to the EAM’s parasitic capacitance. In the centre is a cross-section schematic of the source of the bridge’s capacitance. On the right is the fitted model of the experimental data measured.

![Figure 7](image)

(a) (b)

**Figure 7.** Experimental measurements from the bridge test device. (a) Smith chart for the $S_{11}$ data from the pad test structure shown in Figure 6. (b) Magnitude vs. frequency for the $S_{11}$ data from the pad test structure shown in Figure 6.

These measurements offered a chance to further improve the bridge contribution to the parasitic capacitance of the overall device. Recognising that the capacitance of the metal air bridge depends on the surface area of the bridge as $C \propto A$, decreasing the area of the bridge overlapping with the remaining n-doped semiconductor linearly reduces the bridge’s parasitic capacitance. To measure this effect, test structures were fabricated which varied the width of the metal bridge as shown on the left of Figure 8. These test structures were measured and characterised in order to isolate the capacitance of each bridge width, with the results being shown on the right of Figure 8.

These results show a bridge with $\approx 3\, \text{fF}$, which brings the total parasitic capacitance of the contact scheme down to below 10 fF. Full EAM structures were fabricated using the contact scheme proposed in the previous sections with varying bridge widths with no notable relationship between bridge width and device inductance or resistance being noted.
5. EAM Measurements

Full EAM structures were fabricated using the contact scheme proposed in the previous sections. $S_{11}$ measurements were taken of these devices. These data were then inserted into the equivalent circuit model shown in Figure 2. With the values of the contact pad and bridge elements of the circuit already measured using the aforementioned test structures, the full equivalent circuit of the EAM alone was able to be isolated through fitting the measured data as described in Section 3. This process was applied to EAMs of lengths varying from 50 to 175 µm. With the equivalent circuit of the contact pads, the bridge and the EAMs, a simulated $S_{21}$ of the proposed EAM device could be calculated.

This is done by calculating an equivalent impedance for the entire structure. We then form a simplified circuit with an idealised voltage source with a series impedance of $Z_0$, which is connected to the circuit with a total impedance of $Z$. In this case, the voltage across the circuit is

$$V_{\text{temp}} = \frac{V_{\text{source}}Z}{Z + Z_0} \quad (3)$$

Taking $V_{\text{source}} = 1$ for an idealised case and using Ohm’s law, we can then write

$$I = \frac{V_{\text{source}}}{Z + Z_0} \quad \rightarrow \quad V_{\text{temp}} = IZ = \frac{V_{\text{source}}Z}{Z + Z_0} \quad (4)$$

With our branch being made up of the inductor, $Z_L$, plus the remainder, $Z_m$, the voltage on the other side of the inductor will be

$$V_{\text{branch}} = \frac{V_{\text{temp}}}{Z} (Z - Z_L) \quad (5)$$

which is the value of the voltage at the first stage to the right of the inductor. Calculating this value for each stage will eventually yield

$$V_{\text{final}} = S_{21} = \frac{V_{\text{branch}}}{Z_m} \left( \frac{R_s}{1 + i\omega R_s C} \right) \quad (6)$$

where $R_s$ is the shunt resistance.

EAMs were fabricated with various lengths on two different materials, one with twelve quantum wells, and one with six quantum wells and a widened separate confinement hetero-structure layer. $S_{11}$ measurements were then made on these devices. Using the test structures present in the previous sections, the parasitic capacitance of the EAM device was able to be isolated from the capacitance of the EAM itself. Using Equation (6), $S_{21}$ values were calculated with inputs from over sixty different $S_{11}$ EAM measurements. $S_{21}$s were calculated for over 60 EAM devices of varied lengths for both materials. Experimental $S_{21}$s were not obtained due to a lack of input and output facets on the test devices. Figure 9 shows the result of one of these simulated $S_{21}$s calculated using data from an EAM made.
from the material with six quantum wells. This EAM had a length of 50 µm and a width of 2.5 µm. Figure 10 shows the averaged result of these calculations which predicts a $f_{3dB}$ bandwidth of near 80 GHz for a 25 Ω impedance-matched EAM of length 50 µm. The simulated values presented for the $S_{21}$ do not take into account the wavelength and injected power dependence of the $f_{3dB}$ of an EAM; however, the results confirm that an improvement in the $f_{3dB}$ can be achieved through the optimisation of the electrical contact scheme used for the EAM.

Figure 9. A simulated magnitude of an $S_{21}$ measurement based off experimental $S_{11}$ data taken from an EAM with length of 50 µm. The simulation is made for an impedance match of 50 Ω (black) and 25 Ω (red).

Figure 10. Experimental $S_{11}$ measurements were made on over 60 devices. By isolating the parasitic capacitance measured before, simulated $S_{21}$s were generated and $f_{3dB}$ values were extracted for devices of varying length. The average value for each material is presented above for impedances of 25 Ω and 50 Ω.

6. Conclusions

The parasitic capacitance of an RF contact scheme for lumped-element EAMs was investigated. Test structures to analyse this parasitic capacitance were fabricated and characterised via $S_{11}$ measurement using a VNA. The characterisation of these structures allowed further improvements to be made to the contact scheme, which reduced the total parasitic capacitance to $<10 fF$. EAMs using this contact scheme were fabricated and characterised using $S_{11}$ measurements. These $S_{11}$ measurements were used to simulate $S_{21}$ measurements, which predict a $f_{3dB}$ bandwidth $\geq 80$ GHz for an EAM of length 50 µm.

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