

Article

In-Pixel Time-to-Digital Converter with 156 ps Accuracy in dToF Image Sensors

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Abstract

As the mainstream technology solution for deep imaging LiDAR, dToF measurement has been widely applied in emerging fields such as environmental perception and obstacle recognition, 3D terrain reconstruction, real-time motion capture, and drone obstacle avoidance navigation due to its advantages of high resolution, long-range detection capability, and high sensitivity. In order to adapt to functional applications in different scenarios, the resolution of TDC needs to be adjustable and can work normally in different environments. In view of this, this article studies the pixel array and TDC circuit in the chip and locks a voltage-controlled ring oscillator (VCRO) with the same structure as the pixel to a fixed frequency through a PLL structure. Then copy the control voltage of the locked VCRO to the control terminal of the TDC in each pixel. In an ideal situation, this control voltage can make the oscillation frequency of VCRO within the pixel consistent with the locking frequency of VCRO within the PLL, and insensitive to changes in PVT. This study developed a module expandable 16×16 -pixel array dToF sensor chip based on TDC architecture using CMOS technology. Finally, six configurable 16×16 -pixel subarrays were integrated and constructed into a 32×48 large-scale dToF sensor chip through modular splicing. The top-level layout design was completed using SMIC 180 nm technology, with a layout area of $5285 \mu\text{m} \times 3669 \mu\text{m}$. Post-simulation verification showed that, under the testing conditions of a 400 MHz system clock and a 33.3 kHz frame rate, the dToF chip system performance indicators were: time measurement resolution of 156 ps, DNL < 1 LSB, INL < 0.85 LSB, and absolute ranging accuracy better than 2.5 cm.

Keywords: time of flight; ToF; resolution; PLL; VCRO Linearity; time to digital converter; TDC



Received: 21 December 2025

Revised: 3 February 2026

Accepted: 4 February 2026

Published: 6 February 2026

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1. Introduction

Demand for the acquisition of depth images is increasing in automated driving technology, industrial automation, robotics, and 3D modeling fields. The direct time-of-flight (dToF) measurement technique is a prevalent light detection and ranging (LiDAR) sensor method, largely due to its system simplicity, ease of integration, and extensive detection range [1]. Time of flight LiDAR determines the distance to a target object or scene depth by measuring the time difference between the reflected light signal and the reference time. Its ranging technology is mainly divided into two categories: dToF achieves ranging by detecting the time delay between the emitted light pulse and the received echo; iToF (indirect time of flight) measures distance by analyzing the phase difference between modulated continuous light waves and reflected waves [2]. Although both technologies have millimeter-level

spatial resolution, dToF technology is more suitable for applications such as autonomous driving that require real-time environmental perception due to its high-speed response characteristics [3].

As a core component of dToF LiDAR, the time-to-digital converter (TDC) directly determines ranging precision by converting time intervals into digital codes, with its resolution and quantization behavior imposing fundamental limits on system performance [4]. Comprehensive overviews of LiDAR system architectures, performance trade-offs, and key design considerations have been established, covering ranging principles, resolution definitions, and practical implementation constraints across flash and scanning architectures [5]. To address cost and dynamic range challenges in LiDAR-oriented time measurement, recent work has combined time-to-amplitude conversion with FPGA-based TDC implementations, achieving balanced resource usage and timing linearity for real-world LiDAR frontends [6]. However, TDC-induced quantization effects remain a critical source of ranging error, directly degrading axial resolution and distorting point cloud integrity; formal methods have been developed to quantify object detection probability, lateral resolution, and systematic error contributions from quantization and sampling non-idealities [7]. Despite these advances, integrated dToF sensor arrays with robust TDC performance, stable resolution under process-voltage-temperature (PVT) variations, and scalable pixel-level timing control remain essential for next-generation compact, high-frame-rate 3D depth sensing.

Figure 1 shows a schematic diagram of the dToF LiDAR system architecture. The system scans the target scene by periodically emitting light pulses. When the pulse is triggered, TDC is activated and terminated when the echo signal reaches the corresponding pixel unit. The recorded time delay corresponds to the propagation time of the light wave back and forth between the light source and the target object. In a LiDAR system, time-of-flight measurement accurately characterizes the time interval between the transmit pulse (START) and the echo pulse (STOP) through TDC. Based on the flight time and the constant of light speed $c = 3 \times 10^8$ m/s, the target distance can be calculated using Formula (1). The parameters D_{obj} : The actual distance between the target object and the dToF sensor (unit: m); ToF: The round-trip flight time (unit: s) of a laser pulse emitted from the sensor and received after being reflected by the target object.

$$D_{obj} = \frac{1}{2} c \times \text{ToF} \quad (1)$$

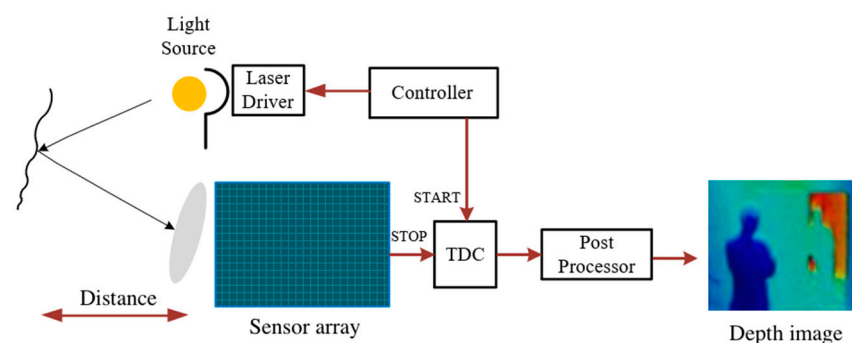


Figure 1. Photon detection system.

The dToF LiDAR system architecture in Figure 1 includes core modules such as a main controller, laser emission unit, narrowband filter, single photon avalanche diode (SPAD) array, TDC, and point cloud processor. The main controller performs dual functions: dynamically adjusting the laser power to balance human eye safety standards and signal-to-noise ratio optimization while synchronizing the timing logic between the laser drive module and the image sensor through a common clock. After the reflected light pulse

is focused by the receiving lens, background light suppression is achieved through a wavelength-matched narrowband filter and finally projected onto the SPAD sensor array. Each pixel unit of the array is integrated with a single photon detector, which transmits the pulse trigger signal generated by avalanche current to the TDC module for time-of-flight quantification and time-to-digital conversion processing. The point cloud processor reconstructs a three-dimensional point cloud model based on pixel spatial coordinates and delay parameters using the (1) calculation formula algorithm [8].

The TDC plays a pivotal role in the functionality of a dToF image sensor. The resolution and dynamic range of the TDC directly influence the precision and depth of the imaging. Typically, SPADs have a sensing range of 100 m, necessitating the use of more sensitive photodetectors to detect objects at longer distances [9]. LIDAR systems operate on the fundamental principle that a laser emits infrared photons and receives the returned photons through a SPAD. The SPAD then undergoes an active quenching recharge circuit, which generates a signal pulse to indicate the arrival of the photons [10]. The measurement of photon time of flight is employed to indicate the distance to an object. The time of flight is quantified by the TDC and converted into a digital signal that can represent the distance to the object. In the field of three-dimensional measurement, time-of-flight image sensors have emerged as a prominent area of development for three-dimensional depth perception technology, largely due to their straightforward structure, straightforward integration, high degree of accuracy (at the centimeter or even millimeter level), and capacity for long-range operation. The resolution of the TDC directly influences the accuracy of the distance measurements produced by the sensor. In order to obtain higher resolution, the pixel array in LiDAR sensors is increasing [11]. The TDC in the sensor is the key component in each pixel, so higher accuracy, smaller area and lower power consumption are required for the TDC. The ring oscillator-type TDC is an optimal choice for integration into large array sensor chips, offering a compact structure, minimal area requirements, and the capacity to attain resolutions of less than 10 ps in advanced processing [12].

2. Comparative Analysis of Typical Structures of TDC

From the perspective of technological iteration, TDC architectures can be categorized into four generations with the following core characteristics: (1) Analog TDC, based on current integration/voltage ramping, is significantly affected by RC time constants and PVT variations (typical error > 1 ns). (2) Digital TDC, employing a coarse-fine quantization architecture composed of CMOS delay chains and counters, achieves a resolution of hundreds of picoseconds. (3) Sub-gate delay TDC, based on DLL phase interpolation and a dual-clock vernier structure, realizes a resolution of <10 ps. (4) Sub-picosecond TDC, through multi-layer interpolation and hybrid architecture collaboration, improves measurement precision from the nanosecond to the femtosecond level. The core mechanisms and inherent drawbacks of various mainstream TDC architectures are summarized as follows:

- (1) Current-integrating TDC and its typical structure are shown in Figure 2: Maps the time interval to a voltage via a charge pump and integrating capacitor, followed by quantization using an ADC. Its limitation is that the precision relies on the RC time constant, making it sensitive to temperature and process drifts, with restricted dynamic response speed [9].
- (2) Countertype TDC: Achieves time quantization by counting reference clock cycles, featuring a simple structure. Its limitation is that the resolution is constrained by the clock frequency, with an inherent trade-off between dynamic range and precision; the asynchronous operation mode is prone to introducing metastability risks.
- (3) Delay-line TDC as shown in Figure 3: Maps the time interval to delay stages through cascaded delay units, outputting digital codes via decoding. Its limitation is that PVT

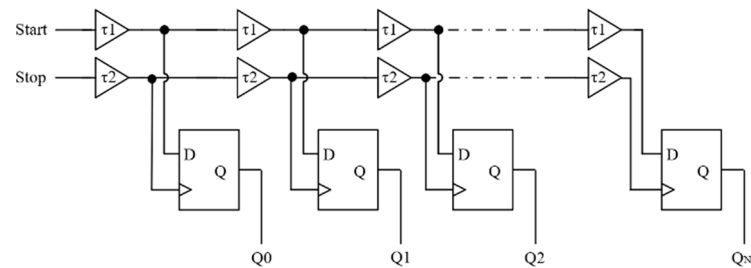


Figure 5. TDC based on cursor delay line type.

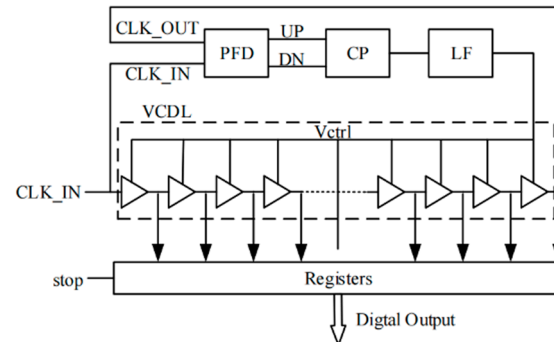


Figure 6. DLL-based TDC.

Among the above architectures, the ring oscillator TDC features a compact structure and outstanding precision advantages, making it more suitable for pixel-integrated dToF systems [15]. The ring oscillator TDC adopted in this work is shown in Figure 7, mainly consisting of Start/Stop logic, a counter, a voltage-controlled ring oscillator (VCRO), and an encoder. The Start/Stop logic defines the time interval to be measured and controls the start and stop of downstream circuits; the VCRO oscillates only when the EN signal is high, which helps reduce power consumption. A two-level quantization architecture is adopted for time measurement: the counter performs coarse quantization at the oscillation period level, while the encoder carries out fine quantization of multi-phase clocks. The final-stage phase of the VCRO drives the counter to count the number of full cycles, and the encoder analyzes the states of multi-phase nodes to obtain the fine time margin; the combination of the two enables high-precision measurement.

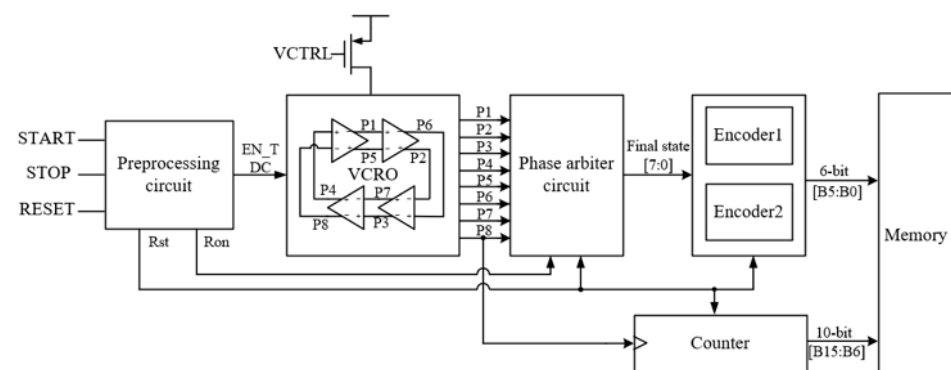


Figure 7. TDC based on ring oscillator type.

Traditional ring oscillator TDCs present an inherent trade-off among resolution, area, and power consumption: improving resolution generally requires increasing the number of VCRO phases, which in turn leads to larger area and higher power consumption. The proposed TDC in this work retains the compactness advantage of the ring oscillator structure

while introducing a phase arbiter circuit and a PLL-based PVT compensation mechanism. The phase arbiter can detect phase differences smaller than 1 ps, effectively suppressing sampling errors caused by metastability; the PLL replicates the locked control voltage to each pixel TDC, ensuring stable resolution across the array under PVT variations.

In terms of pixel integration, conventional structures struggle to balance area and performance. The TDC in this work has a layout area of only $70\ \mu\text{m} \times 88\ \mu\text{m}$ and a power consumption of 1.512 mW, meeting the integration requirements of large-scale pixel arrays for dToF sensors in both size and power. The comprehensive comparison demonstrates that the optimized ring oscillator architecture achieves a favorable balance among resolution, area, power consumption, and PVT robustness, making it more suitable for the dToF pixel-level application scenario targeted in this work.

The simulation results for DNL and INL are shown in Figures 8a and 8b, respectively. The values $\text{DNL}_{\text{p-p}} < 1\ \text{LSB}$ and $\text{INL}_{\text{p-p}} < 0.85\ \text{LSB}$ indicate that the TDC exhibits good linearity.

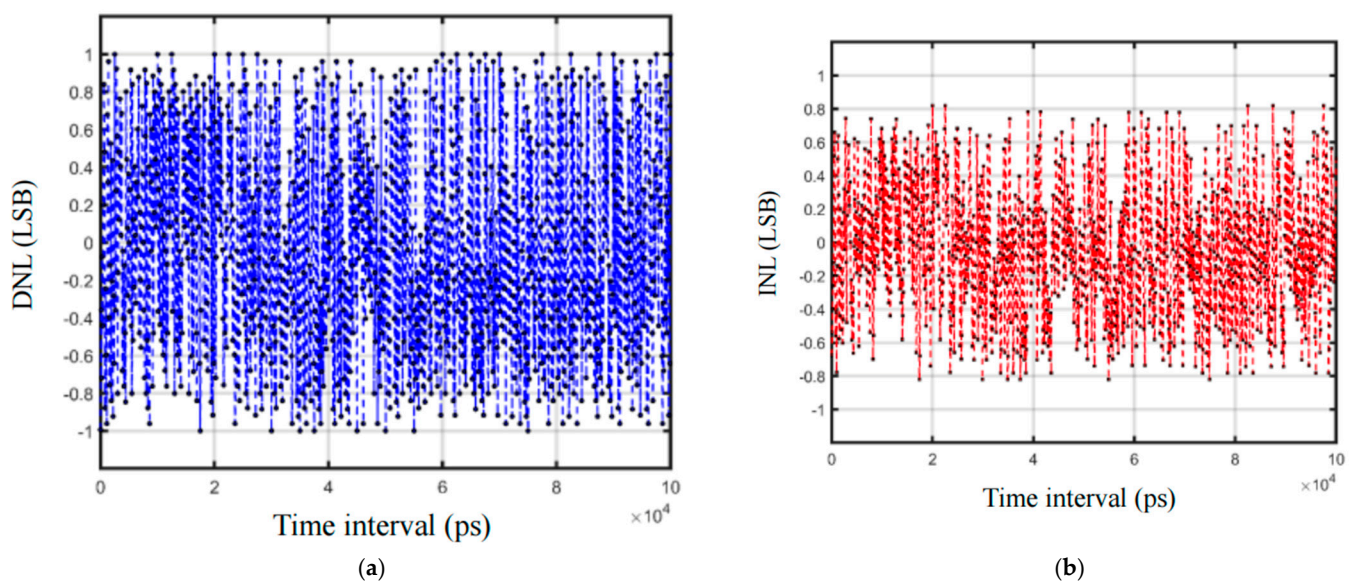


Figure 8. The simulation results of DNL and INL are shown in (a) and (b), respectively.

3. The Design of TDC in dToF Image Sensors

The dToF image sensor proposed in this paper is shown in Figure 9. It incorporates an array of 32×48 smart pixels, PLL, Analog buffer, Start/Stop distribution tree, ROW Control Logic, Column Control Logic and Data Serialization. Each pixel contains two SPADs that improve photon detection efficiency, an active quenching recharge circuit (AQR) and a TDC. The 32×48 -pixel array necessitates the utilization of an analog buffer to regulate the oscillation frequency of the ring oscillator within each pixel. The Vctrl is provided by the PLL [16]. Consequently, the TDC is capable of compensating for the effects of process variations and ambient temperature fluctuations [17]. Furthermore, a start/stop distribution tree is necessary to provide consistent start and reset signals for the pixel array. Additionally, the pixel array employs row and column selection techniques to facilitate data transfer through the pixel cells, culminating in parallel-to-serial conversion.

3.1. Principle of Phase-Locked Loop Adjusting TDC Resolution

The pixel-level TDC adopts a PLL global closed-loop calibration architecture and adjusts the VCRO oscillation frequency through a voltage-controlled oscillator tuning voltage VCTRL closed-loop to establish a TDC quantization accuracy benchmark. The minimum distinguishable time is set by the maximum oscillation frequency of VCRO, and

the global matching transmission of locked voltage is achieved through a unit gain buffer array, ensuring the consistency of VCRO frequency tuning for each pixel unit and achieving uniform control of system-level time to digital conversion accuracy.

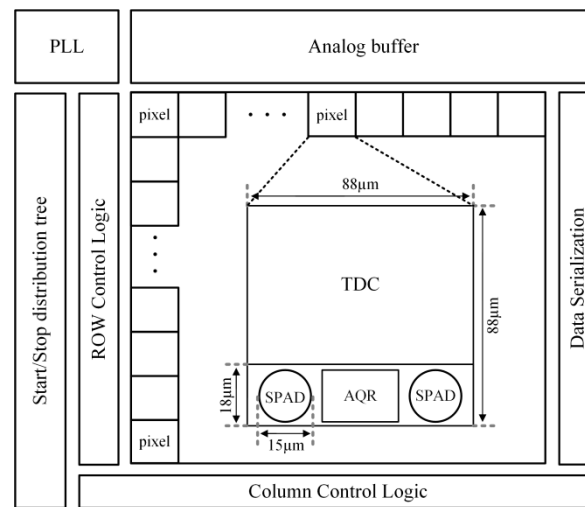


Figure 9. 32×48 dToF image sensor.

Figure 10 shows a global VCRO frequency calibration architecture based on a PLL, whose core consists of a main VCRO reference unit embedded in the PLL, which can achieve programmable tuning over a wide frequency range. Synchronize the DC tuning voltage of the filter to all VCRO units in the array through a shared voltage distribution network. Given the characteristics of this architecture, the output voltage ripple suppression capability of the loop filter becomes a key design element, and the TDC time error introduced by its ripple can be quantified as:

$$V_{\infty} = \frac{8KT_{\infty}V_{ref}^2}{1 + 8KT_{\infty}V_{ref}} \quad (2)$$

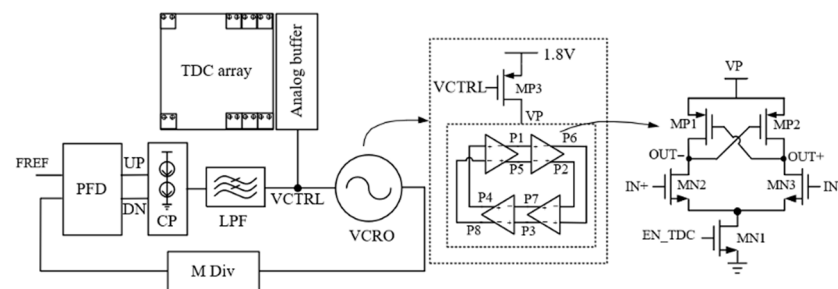


Figure 10. PLL global calibration TDC resolution architecture.

Among them, V_{ϵ} is the ripple output of the loop filter, T_{ϵ} is the error of the TDC time interval, K is the gain of VCRO, and V_{ref} is the output of the loop filter.

The design and post-simulation results of this paper show that the loop bandwidth of the phase-locked loop has been optimized to 275 KHz, achieving a balance between noise suppression and dynamic response speed to meet the real-time PVT compensation requirements of the dToF sensor. The phase margin is set to 65° , ensuring stable operation without oscillation across the entire process, voltage, and temperature (PVT) range. The lock time, as indicated by the simulation results, is less than 6 microseconds, supporting a 33.3 kHz frame rate for a 32×48 array dToF sensor. The period jitter of the output clock is

2.64 picoseconds, meeting the requirements of high-precision time-of-flight (dToF) systems for clock reference sources.

The proposed TDC employs a ring-type voltage-controlled oscillator (VCRO) structure. The TDC and the phase-locked loop (PLL) in this work share an identical core VCRO architecture, both of which exhibit excellent linearity of more than 99% in oscillation frequency versus control voltage [14]. The block diagram is illustrated in Figure 10. This VCRO design is integrated into all 32×48 TDC units across the pixel array.

The control voltage VCTRL generated by the PLL is distributed to regulate the oscillation frequency of the VCROs in the pixel array, which in turn adjusts the time resolution of the TDCs. To ensure stable and accurate delivery of the analog control signal, the VCTRL voltage drives all VCROs in the array through analog buffers [15].

Since the TDC VCROs and the PLL VCROs are identical in topology and device sizing, they exhibit nearly identical sensitivity to process, voltage, and temperature (PVT) variations. By locking the PLL VCRO to a stable reference clock and replicating the resulting VCTRL to all pixel TDCs, the oscillation frequency—and thus the TDC resolution—of every pixel VCRO is dynamically calibrated to track the target value. In this way, the proposed closed-loop adjustment mechanism effectively mitigates the impact of PVT variations on TDC resolution, ensuring consistent performance across the entire array.

3.2. Pixel Circuit Layout

In response to the signal integrity improvement requirements of high-frequency multi-phase clock systems, a design strategy for minimizing interconnect paths is implemented to effectively suppress parasitic capacitance, resistance, and mutual coupling effects of adjacent interconnect structures. This article proposes a pixel built-in clock scheme, which integrates VCRO to generate clock signals in each pixel and combines an on-chip PLL to construct a global frequency regulation mechanism to adjust the oscillation frequency of pixel VCRO. This scheme extends the VCRO control voltage network in the PLL to the pixel array to form a closed-loop frequency calibration system. To ensure phase consistency of multi-node oscillators, PLL and pixel built-in VCRO achieve precise parameter replication from circuit architecture to physical implementation. This design transmits voltage signals through a single voltage line, avoiding parallel transmission of high-frequency clock signals, completely eliminating synchronization deviation and buffer mismatch noise in multi-phase clock domains, and achieving phase uniformity across arrays. In addition, based on the master-slave voltage control synchronization mechanism, the control voltage of the VCRO in the PLL main loop is mirrored to the pixel-level slave VCRO array to construct a global PVT compensation system. To address the RC attenuation effect in voltage transmission networks under large-scale arrays, a low clock skew analog buffer chain distributed drive is adopted to enhance the voltage driving capability and effectively solve the signal attenuation problem.

To ensure timing matching and reduce clock jitter, key signals such as START, RESET, and Load are transmitted to each pixel unit in the array through a nested H-tree network. The pixel array based on the above design rules is shown in Figure 11. This structure minimizes clock skew between pixels by accurately matching different signal delay paths. Due to the consistent system delay clock skew of all pixels, manifested as common mode deviation, its impact on the relative resolution between pixels can be ignored, effectively ensuring that the quality of 3D imaging is not affected.

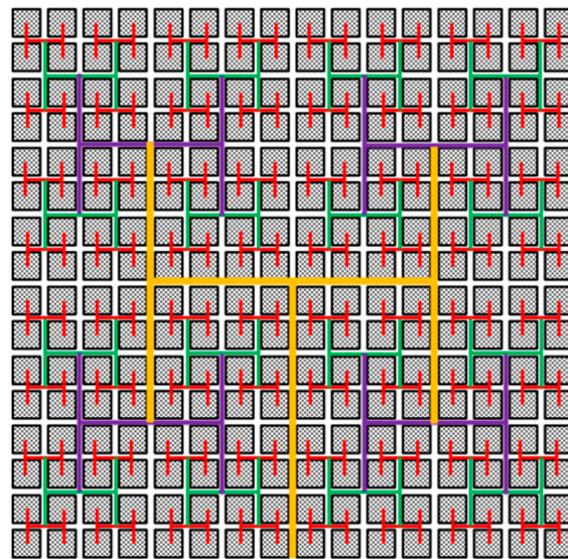


Figure 11. H-tree structure pixel array.

First, the LOAD signal (first introduced herein) is defined as the register latch enable signal for TDC quantization results: its rising edge triggers the on-pixel register to store the TDC quantization code, coordinating with the START and RESET signals to ensure global timing synchronization across the 32×48 pixel array. To achieve synchronous transmission of the LOAD signal, clock, and other critical signals, a nested H-tree global interconnect structure is adopted, combined with a segmented buffer insertion strategy to enhance signal integrity.

The nested H-tree interconnect structure features a hierarchical topology of “main trunk—branches—sub-nodes”, with the geometric center of the chip as the origin. The main trunk extends outward, and each branch splits at a 1:2 ratio, with the final sub-nodes accurately connected to each 16×16 sub-array and individual pixel units. This design ensures identical transmission path lengths for critical signals to all pixels in the array, controlling the transmission delay skew of the LOAD signal and clock within 10 ps to avoid TDC quantization errors caused by inter-pixel timing mismatch. Additionally, equal-width and equal-spacing metal routing, along with rounded branch nodes, are used to reduce signal reflection and crosstalk, adapting to the signal synchronization requirements of large-scale pixel arrays.

To suppress the accumulation of parasitic capacitance on transmission lines and optimize signal timing, a segmented buffer insertion strategy is implemented based on explicit signal integrity rules: for the SMIC 180 nm BCD process adopted in this design, the critical transmission line length is set to 200 μm (determined by the process’s parasitic parameters and signal frequency). Buffers are inserted in segments when the transmission line length exceeds this critical value, with an insertion interval of 100 μm (half the critical length) to decompose the global interconnect into shorter segments. The buffers adopt a two-stage inverter structure, and the aspect ratio of the driver-stage transistors is optimized to 1.2 times the total load capacitance (including wiring parasitic capacitance and on-pixel load capacitance), achieving precise matching between driving capability and load capacitance. These buffers perform dual functions of signal level recovery and waveform shaping, significantly reducing signal rise/fall time and transmission delay, and strictly meeting the signal integrity criterion that “signal rise/fall time $\leq 10\%$ of the signal cycle”.

As shown in Figure 12, the transmission line lengths of the clock interconnect topology for 16×16 , 8×8 , 4×4 , and 2×2 sub-array sizes are 1.6 mm, 0.4 mm, 0.2 mm, and 0.1 mm, respectively. Based on RC transmission line delay model analysis, when the

total interconnect length of the global clock tree reaches 2.3 mm, a five-level distributed buffer insertion scheme is required to achieve high-fidelity signal transmission, ensuring consistent timing performance of TDC units across the entire array.

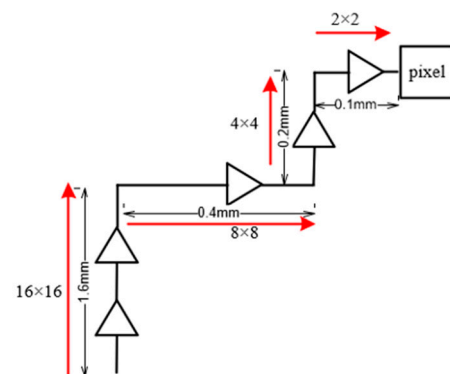


Figure 12. Signal transmission path.

4. The Simulation Result and Discussion

This chapter proposes a design scheme for an array-based dToF sensor chip based on SMIC 180 nm BCD technology. This chip constructs a 32×48 micropixel array through 6 independent and scalable 16×16 arrays, integrating 1536 TDC units. The chip layout size is $5285 \mu\text{m} \times 3669 \mu\text{m}$, as shown in Figure 13. The pixel center spacing is $100 \mu\text{m} \times 88 \mu\text{m}$, achieving a filling rate of 11.15%. The chip integrates a total of 224 I/O PADs, most of which are dedicated to testing PADs. When packaging the pins, the same source test signals can be connected to the same PAD to reduce packaging costs. The chip is equipped with a grounded Sealing protective ring structure on the periphery, which meets the requirements of the wafer packaging process.

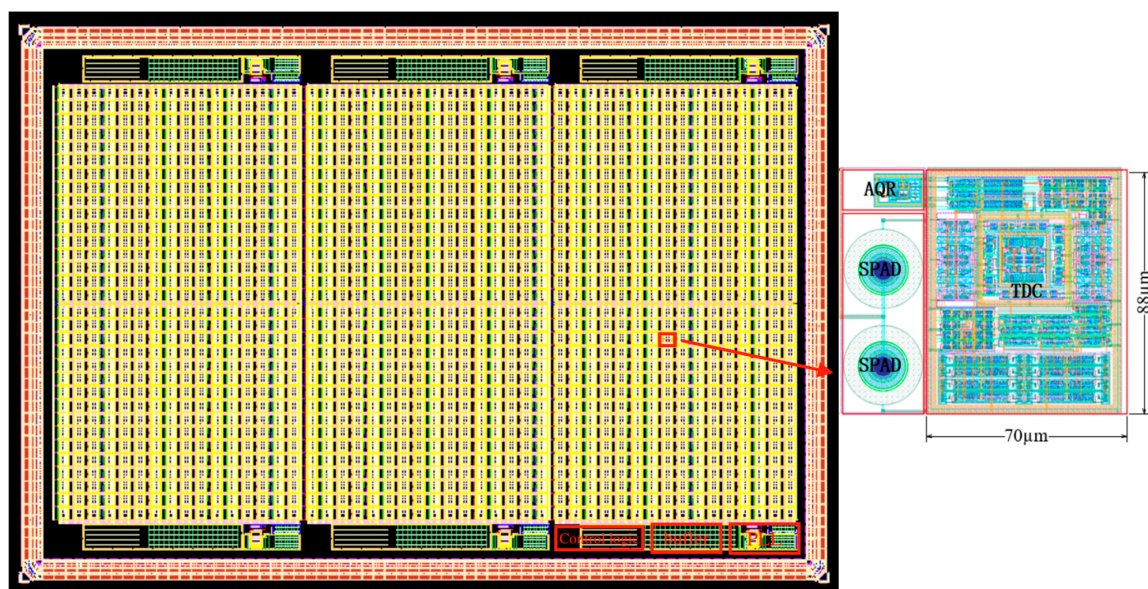


Figure 13. Layout of 32×48 array dToF sensor chip.

The chip adopts a modular and scalable subarray architecture, and one of its core design goals is to support the expansion to a larger array scale to meet the needs of applications such as automotive lidar for the number of pixels. From the perspective of architecture, its scalability is guaranteed by the following design features:

1. Independent design of 16×16 subarrays adopts independent timing control, power domain and data readout path. When expanding, only the number of subarrays is required, and there is no need to reconstruct the core circuit to ensure the consistency of performance of each TDC unit.
2. The signal synchronization and transmission optimization chip adopts hierarchical timing allocation and an equal-length routing strategy to control the transmission delay deviation of key signals (START, RESET, LOAD, etc.), laying the foundation for timing synchronization in large-scale arrays.
3. Power Distribution and Noise Isolation Subarray-level independent power domain design can suppress crosstalk and noise coupling after large-scale integration and ensure that the core performance such as resolution and linearity of each pixel TDC after expansion will not be significantly affected.
4. The scalable subarray of data readout architecture has a built-in parallel readout structure. After expansion, the overall data throughput can be improved through the parallel readout channel to ensure the frame rate index under the large array.
5. Packaging and I/O architecture compatible expansion chip adopts the strategy of multiplexing PAD with the same source test signal. When expanding the array size, it can optimize the PAD allocation and pin definition to achieve a large array test and function without significantly increasing the packaging cost pin requirements while retaining the Sealring protection structure to be compatible with the standard wafer packaging process.

To sum up, the dToF sensor chip proposed in this paper relies on modular sub-arrays, hierarchical timing control, sub-domain power management and scalable readout architecture, and it has the ability to expand to larger pixel arrays without changing the core TDC and array basic architecture. The engineering feasibility can maintain core performance indicators by optimizing signal transmission delay, power distribution and data readout bandwidth, and the application requirements for large-area array dToF sensors in automotive and other fields.

This design proposes an innovative solution to the core challenges of 3D depth sensing dToF sensors, focusing on breaking through how TDC circuits can improve anti-interference performance, enhance linearity, reduce area, and integrate into pixel arrays. The sensor adopts multiple innovative architectures: an integrated PLL circuit generates a globally synchronized clock, and the VCRO frequency of the TDC within the pixel is precisely controlled through voltage calibration technology, thereby achieving calibration of TDC resolution. A unit gain buffer with a bandwidth of 80 MHz is used, which is higher than the input reference frequency of 40 MHz. Its conversion rate can correct the phase difference in the phase-separated clock in real time. An independent submodule with 256-pixel units sharing a Parallel-In-Serial-Out (PISO) is used to transmit data through a row-column timing control circuit, maximizing the amount of data transmitted while minimizing the circuit area. The dToF sensor uses a single external clock source, which is approximately 400 MHz after PLL multiplication, to control the transmission of IO data to the synchronous receiver.

The simulation results within one frame of the chip system are shown in Figure 14. From the figure, it can be seen that, after the chip is powered on and initialized, waiting for $6 \mu\text{s}$ PLL lock, the lock voltage is 623.88 mV, which is the same as the simulation results of the PLL module alone. From Figure 15, it can be seen that, when the RESET signal is high, the pixel circuit is reset and waits for the START signal to arrive. The arrival time of photons is random, and it is necessary to simulate the arrival time of photons to set the STOP signal. The row select column select timing control circuit opens the control switch in the pixel when X and Y are high and transmits the time-of-flight data of a pixel

unit through the PISO circuit. At this time, the input flight time interval is 99 ns, and the quantized digital code is 00010011111100010. According to the formula in (1), the calculated result is 99.063 ns, with an error of less than 156 ps, which meets the requirements. From Figures 14 and 15, it can be seen that the chip system needs to sequentially gate and read out each pixel unit until 16×16 -pixel units are read out. After TDC quantizes the flight time, the load signal encodes and saves the quantized data into memory, waiting for the row and column selection timing control circuit to read the data. It can be seen that, at this time, the column signal $Y<6>$ is at a high level, and the row selection signals $X<4>$, $X<5>$, $X<6>$, $X<7>$ – $X<15>$ pulse signals are sequentially turned on. After 16 cycles of the row selection signal, the column selection signal is flipped once, and then the data in the pixel unit is read out column by column from $Y<0>$, $Y<1>$ – $Y<15>$. At this time, the flight time of the test input is 146 ns, where LO is the symbol of the pixel output signal. The output result of DATAOUT is $D<0:15> = 0001110101010011$, and the calculated result is 145.86 ns with an error of 140 ps. The frequency of the clock signal CLK in PISO is 400 MHz, and it takes 80 ns to complete the data transmission of one pixel, with a total readout time of 20.480 μ s. The chip completes one frame of measurement work, including reset, quantization, and readout stages, with a total time of about 30 μ s.

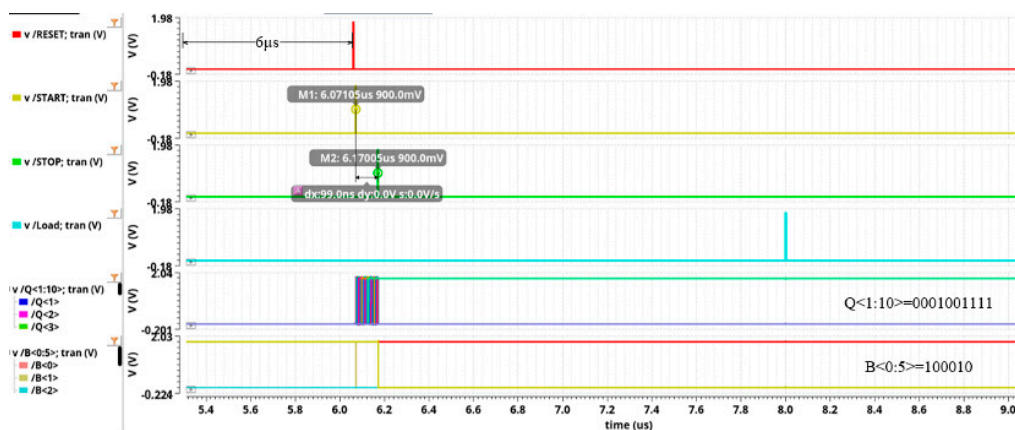


Figure 14. The simulation timing results of the chip after reading out single-pixel data.

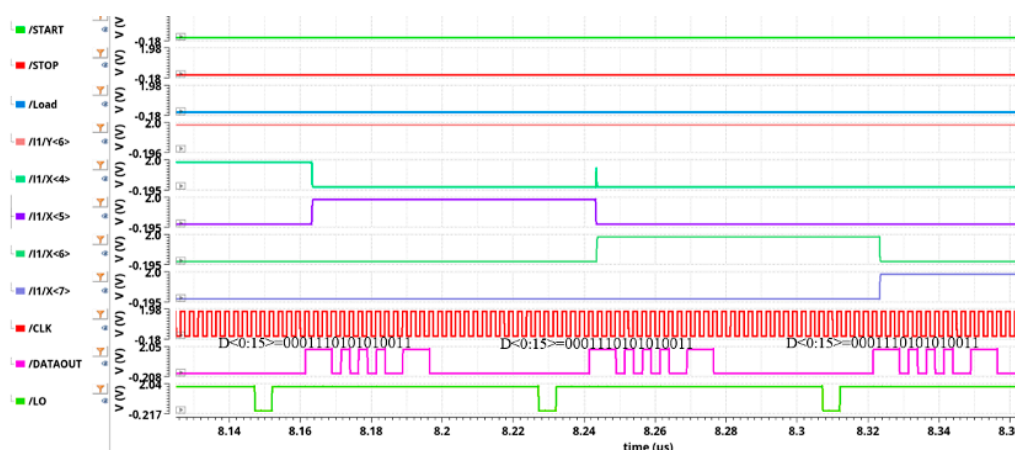


Figure 15. Partial enlarged view of the simulation timing results after reading one frame of data from the chip.

Due to the fact that the row select column select timing control circuit and PISO circuit only implement data gating and readout functions and do not participate in the time digital quantization process, they are reasonably simplified in the system-level error analysis. The TDC array and PLL circuit are the core modules for time-of-flight measurement,

and simulation verification will focus on this subsystem. By injecting ideal time interval signals into the TDC in dToF sensor systems and comparing the measured output data, key performance indicators such as system time resolution and measurement linearity can be effectively evaluated. The chip is paired with pixel units, and a total of 99,890 sets of values are randomly selected from the middle segment between 10 ps and 99.9 ns in increments of 1 ps. Perform post-simulation verification on the layout of the 32×48 array dToF sensor chip, as shown in Table 1. Due to limited space, Table 1 only displays 20 sets of data. To quantify the time measurement accuracy of the analysis system, this study uses visual statistical methods to characterize the measurement data errors. The comparison curve between the ideal input time interval value and the actual measurement output time interval value shown in Figure 16 can intuitively reflect the linearity of the system measurement.

Table 1. Simulation results of chip system (excerpt).

Number	Input Time Interval (ps)	TDC Quantization Coding D<15:0>		Output Time Interval (ps)	Nonlinear Error (ps)
		D<15:6>	D<5:0>		
1	10	0000000000	001000	156	−146
2	100	0000000000	001000	156	−56
3	200	0000000000	010000	312	−112
4	300	0000000000	011001	312	−12
5	400	0000000001	000101	469	−69
68	37,900	0000011111	010111	37,969	−69
69	38,000	0000011111	000100	38,125	−125
70	38,100	0000011110	110011	37,969	131
98	40,900	0000100001	000011	40,782	118
99	41,000	0000100001	001011	40,938	62
100	41,100	0000100001	010010	41,250	−150
128	43,900	0000100011	111111	43,750	150
129	44,000	0000100011	011001	44,062	−62
130	44,100	0000100100	000110	44,063	37
168	63,400	0000110011	001100	63,281	119
169	63,500	0000110011	001010	63,594	−94
170	63,600	0000110011	011100	63,593	7
196	99,500	0001001111	111010	99,531	−31
197	99,600	0001001111	110001	99,531	69
198	99,700	0001001111	111000	99,843	−143
199	99,800	0001001111	110000	99,687	113
200	99,900	0001010000	000000	100,000	−100

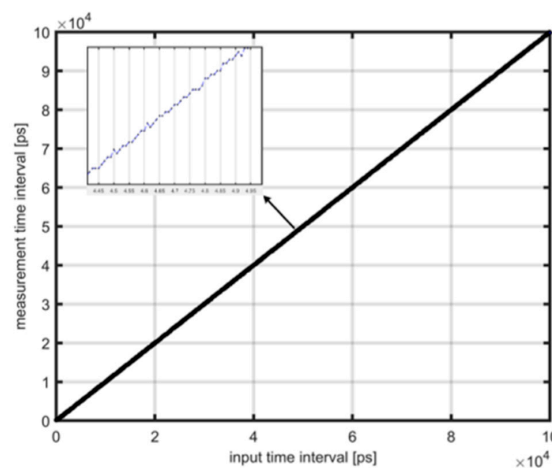


Figure 16. TDC linearity simulation.

5. Conclusions

The single-frame working time of the 32×48 array dToF sensor chip designed in this article is 30 μ s, corresponding to a system frame rate of 33.3 kHz. Through system analysis, it is known that the frame rate is constrained by the following key parameters: (1) measuring dynamic range, the maximum range of TDC (corresponding to the upper limit of photon flight time) is positively correlated with the frame period, and the extension of the photon reception window during long-distance detection directly leads to a decrease in frame rate. (2) Quantization accuracy: The larger the number of TDC conversion bits, the longer the data readout time will be. (3) When using a parallel IO interface for data transmission architecture, the read time can be shortened compared to a single-channel serial transmission scheme. (4) Clock synchronization mechanism: The faster the chip reads data, the less time is required for reading, and the higher the frame rate. To objectively evaluate the technical competitiveness of this design in the field of dToF sensors, Table 2 compares the core parameters of the chip horizontally with mainstream TDC architecture dToF sensors at home and abroad. Among them, by comparing with references [8,18–21], the dToF sensor chip designed in this paper has significant advantages in core parameters such as TDC resolution, linearity, and maximum detection distance. In addition, an innovative design of pixel array based on modular architecture, using expandable 16×16 array modules to form a 32×48 array, makes it easy to expand the number of pixels.

Table 2. Summary of dToF sensor chips based on TDC.

Parameter	This Paper	[18]	[19]	[8]	[20]	[21]
Process node (nm)	180	180	180	110	150	180
Array size	32×48	1×16	8×8	80×60	32×32	32×32
Pixel pitch (μ m)	88	100	-	75	44.64	60
Fill rate	11.15%	-	11.5%	10.4%	19.48%	7.2%
TDC depth (bit)	13	11	16	12	8	13
TDC number	1536	16	64	4800	-	1024
TDC resolution (ps)	156	100	208.3	100	210	200
TDC area (μ m ²)	6160	1310	19,000	-	402.7	-
TDC DNL (LSB)	+1/−1	+0.4/−0.4	+0.5/−0.5	-	+0.86/−0.68	+0.24/−0.29
TDC INL (LSB)	+0.83/−0.85	+1.4/−0.14	+1.02/−2.53	-	+0.51/−2.4	+1.02/−2.53
Maximum measurement (m)	421	33	396	45	17	20
Frame rate (Hz)	33.3 K	200 K	-	30	-	270 K
Accuracy (cm)	2.5	1.5	3.4	1.5	-	3.3
dToF area (mm ²)	5.285×3.669	2.645×1.552	1.279×0.884	7.03×5.9	1.69×1.88	2.9×2.9

Author Contributions: Conceptualization, B.L. and L.C.; methodology, B.L.; software, B.L.; validation, B.L., L.C. and C.C.; formal analysis, B.L.; investigation, B.L.; resources, L.C. and C.C.; data curation, B.L.; writing—original draft preparation, B.L.; writing—review and editing, B.L., L.C. and C.C.; visualization, B.L.; supervision, L.C.; project administration, L.C.; funding acquisition, L.C. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: The original research data supporting the conclusions of this article are included within the article. All key data related to the design, simulation, and performance characterization of the array-based dToF sensor chip (e.g., TDC resolution metrics, array layout parameters, signal transmission delay data, and PVT variation test results) are presented in the corresponding figures, tables, and text descriptions of the manuscript. Further inquiries regarding the data can be directed to the corresponding author.

Acknowledgments: The authors would like to express their sincere gratitude to all individuals and institutions that contributed to the completion of this work. Bangtian Li acknowledges the valuable technical discussions with colleagues in the research team during the chip design and simulation phase, which provided critical insights for optimizing the TDC architecture and array synchronization strategy. Liying Chen appreciates the administrative support from the department office for facilitating manuscript preparation, submission procedures, and communication with the editorial team. Chuantong Cheng extends thanks to the laboratory technical staff for their assistance in equipment operation and performance testing of the dToF sensor prototype, ensuring the reliability of experimental data. The authors also sincerely thank the anonymous reviewers for their constructive comments and thoughtful suggestions, which have significantly enhanced the technical rigor and clarity of this manuscript. Additionally, the team acknowledges the use of standard academic writing tools for language polishing and formatting optimization during manuscript preparation. All authors have reviewed and edited the content thoroughly, taking full responsibility for the accuracy and integrity of the publication.

Conflicts of Interest: The authors declare no conflict of interest.

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