

## Article

# 65% Efficient Multijunction Photovoltaic Laser Power Converters Operating over 150 W/cm<sup>2</sup>

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## Abstract

Multijunction laser power converters are demonstrated for the first time with high efficiencies for average optical irradiances exceeding 150 W/cm<sup>2</sup>. The GaAs-based photovoltaic power converting III-V heterostructures are designed with six GaAs subcells having an area of 0.14 cm<sup>2</sup>, receiving up to 22 W of input power at ~811 nm, delivering over 14 W of output power. The maximum efficiencies are obtained in the range of 30 to 75 W/cm<sup>2</sup>, and efficiencies > 64% are still obtained at 160 W/cm<sup>2</sup>. The efficiency reduction for higher irradiance values originates predominantly from residual heat generated in the active layers. For example, in 100% duty factor measurements, the bandgap voltage offset saturates to  $W_{oc} \sim 170$  mV. However, in pulsed mode,  $W_{oc}$  values as low as 150 mV have been obtained for a device base temperature of 20 °C. For smaller 0.029 cm<sup>2</sup> devices,  $W_{oc}$  values around 137 mV are obtained at 240 W/cm<sup>2</sup>.

**Keywords:** optical power converters; laser power converters; power-over-fiber; power beam-ing; photovoltaic; galvanic isolation; GaAs; multijunction semiconductor heterostructures

## 1. Introduction

The key attributes for photovoltaic laser power converter (LPC) devices are obviously their conversion efficiencies [1–5], but also their ability to reliably deliver an adequate amount of output power at a prescribed voltage. To that effect, GaAs-based LPCs (often also called optical power converters or OPCs) have been developed first for the wavelength ranges of 800–850 nm [6–36] and 940–990 nm [37,38]. In the past few years, InP-based OPCs have also been developed for the wavelength ranges of 1050–1080 [2,39–48] and 1450–1550 nm [49–56]. There is also potential for other wavelengths [57–70] and continued research related to the field of photovoltaics [71–104].

Importantly, advancements in optical wireless power transmission (OWPT) and power-over-fiber (PoF) applications [105–139] often demand additional output power capabilities. For example, Broadcom has been manufacturing regular power OPCs for about 10 years now, such as the AFBR-POC2xx series capable of up to 1 W of galvanically isolated outputs. Broadcom has also been manufacturing multijunction medium-power OPCs for over 5 years, such as the AFBR-POC306A1 and -A5 series, both capable of up to 3 W outputs with a laser input at ~808 nm and ~975 nm respectively. These products serve PoF applications. Broadcom is currently also releasing high-power OPCs for power beaming applications, with up to 20 W of output power from individual chips (AFBR-POC506A6) [2]. However, PoF applications sometimes also require more than 3 W to drive more power-hungry solutions. Utilizing multiple medium-power OPCs is a good approach for achieving higher



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power outputs [37], but the alternative of deploying a smaller number of higher power OPCs and laser sources remains an interesting perspective.

It is therefore the goal of this study to explore the OPC chip capabilities and constraints to address PoF applications requiring up to 10 W of electrical output power while using a single laser source. The GaAs-based multijunction OPCs are the most mature and best suited for reliably reaching 10 W of output power with high efficiencies [29,37]. This study will focus on the well-proven six-junction (6J) GaAs OPCs intended for an optical input around 808 nm. A key purpose of this study is to lay the foundation for the chip-level properties and the key characterization related to the working distance, input/output power capabilities, output voltage properties, conversion power/efficiencies, and the related thermal properties and requirements.

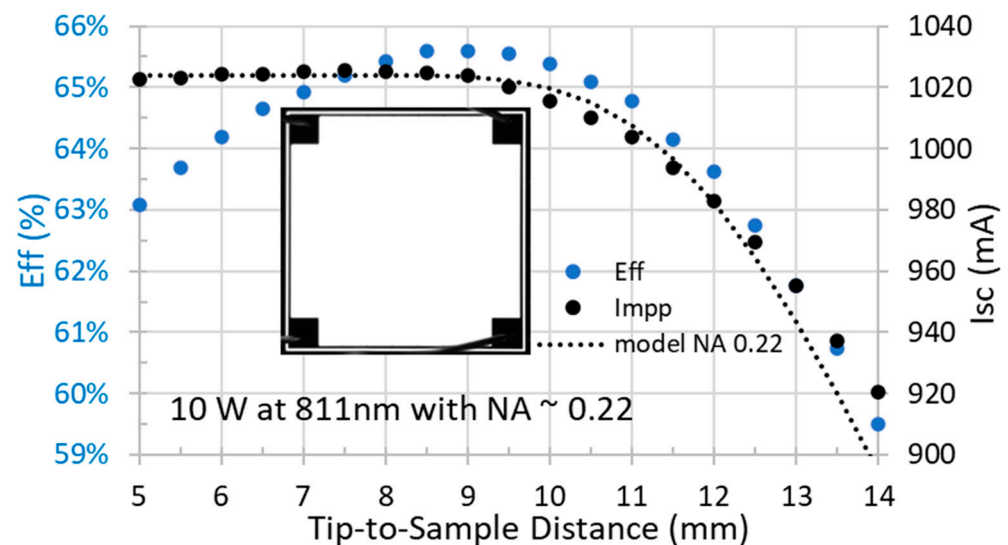
Subsequently, Broadcom intends to package this chip into a suitable housing with adequate thermal properties and with an input ST optical connector. In the current work, we therefore reveal the properties of such a new chip candidate, using a laser input with a wavelength around 808 nm (here 809 nm or 811 nm for many of the measurements, due to the available lasers).

The selected active area for the 10 W chip in this study is 0.14 cm<sup>2</sup>. The OPC chip geometry includes four corner pads connected to a contour busbar collecting the photocurrent from the gridlines for the cathode input side. The input geometry can be visualized from the insert of Figure 1, which shows the electroluminescence image of the chip at 3 mA, at a forward bias of 6.256 V during needle-probed testing. A standard blanket backside metal is used for the anode, forming the back of the chip. More device details are described in the section below. To obtain a 10 W output from the above geometry, using a conversion efficiency of at least 50%, the chip must be able to receive at a minimum an average power of 20 W. This constraint imposes a minimum irradiance capability of the order of 150 W/cm<sup>2</sup> for the new 10 W chip. With such a high irradiance (the equivalent of about 1500 suns in terms of typical solar irradiance), it is certainly valuable to optimize the spot size impinging on the active area. For that purpose, the measurements shown in Figure 1 are used. The input of a commercial multimode pigtailed laser diode with a numerical aperture of NA ~ 0.22 is used. The distance between the tip of the laser pigtail and the input surface of the OPC varies here between 5 mm and 14 mm. Figure 1 is for an optical input power of 10 W. It shows the resulting distance dependence of the efficiency (blue round data points and left vertical axis) and the short circuit current,  $I_{sc}$ , (black data points and right vertical axis). From this data, a working distance between 8 and 9 mm is clearly optimal for such multimode high-power laser sources for an NA of ~0.22.

The data matches reasonably well with our numerical evaluation for an NA = 0.22: black dotted curve in Figure 1. The numerical evaluation was obtained by simulating the incident power received within the clear aperture of the chip for the diverging super-Gaussian beam having an NA = 0.22 [29]. The small deviations are likely due to the beam profile deviating slightly from a super-Gaussian shape. For example, at larger separations, the chip apparently collects slightly more optical power than expected, suggesting that the beam was more concentrated toward the center of the beam profile.

For short working distances, the beam is underfilling the active area, and the more concentrated beam slightly reduces the conversion efficiency due to marginally lower fill-factor and maximum power point voltage ( $V_{mpp}$ ) values. It should be noted that denser gridline patterns could still maintain high fill factors for tighter beam profiles but would result in larger shadowing losses. Meanwhile, the photocurrent stays substantially constant as all the input beam is still captured in the underfilled condition. It also indicates that the increased beam non-uniformity does not affect the subcell current-matching, the beam profile being comparable for each subcell. An efficiency reduction of less than 4% (relative)

is obtained at a 5 mm working distance, but for the remainder of this study, we adopt an optimal working distance of  $\sim 8.5$  mm. For working distances larger than 10 mm, the input beam overfills the chip, and an increasing fraction of the incident power is lost outside the active area, thereby reducing the photocurrent.



**Figure 1.** Dependence of the conversion efficiency (left vertical axis, blue round data points) and of the short-circuit current,  $I_{sc}$ , (right vertical axis, black round data points) on the tip-to-sample distance for a laser diode pigtailed with a NA  $\sim 0.22$  multimode fiber. The sample, measured at 20 °C, is a six-junction GaAs-based device with an area of 0.14 cm<sup>2</sup>. The insert shows the electroluminescence image of the chip at 3 mA, with a 6.256 V forward bias. The black dotted curve shows the modeled values of  $I_{sc}$  vs tip distance.

## 2. Materials and Methods

For the above PT6 chip, the epitaxial layers are grown using commercial Aixtron metal–organic chemical vapor deposition (MOCVD) reactors on 100 mm diameter GaAs substrates. Common commercial n-type and p-type dopant sources have been used, as is customary for industrial devices. The total thickness of all the absorbing emitter and base layers (here GaAs) from the different subcells is such that the impinging optical beam is almost completely absorbed, with nominally over 99% of the input light being absorbed in the first pass through the structure. As described previously, to realize the required photocurrent matching condition, the structure usually has increasing subcell thicknesses from the top subcell (thinnest) toward the bottom subcell (thickest) [14,15,37].

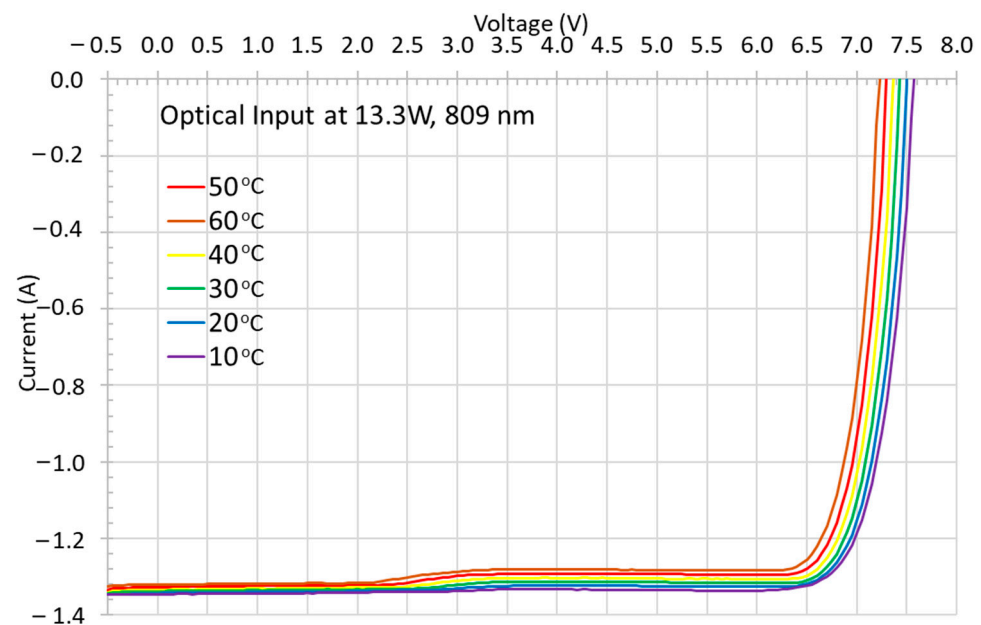
The device fabrication included standard blanket back-metallization, front ohmic contacts (such as Pd/Ge/Ti/Pd/Ag/Au) [71], and antireflection coatings (ARC). The ARC is targeted to reduce the reflectivity ( $R$ ) of the incident beam to  $R < 3\%$  for the spectral range of interest.

To replicate typical PoF operating conditions, the testing was conducted using fiber-coupled semiconductor laser diodes (specifically: underfilled mode with non-uniform illumination). However, unlike a final PoF product, which features a connector-securing housing, the experimental setup uses a mechanical holder to maintain the tip of the laser pigtail in position. GaAs subcells, lattice-matched to GaAs, are expected to contribute about 1.2 V of output voltage each, as observed previously in single junction or multijunction measurements [17,82,85]. For the GaAs-based system, we have previously demonstrated that the output voltage scales linearly up to PT30 devices, with 30 subcells [18].

The PT6 design was selected for the new 10 W chip because it is expected to achieve an output voltage capable of maintaining an optimal load greater than a few ohms over

the operating conditions. It is based on the previously described Vertical Epitaxial HeteroStructure Architecture (VEHSA design) [14,15]. This means that the Beer–Lambert law can be utilized to determine the required absorber thicknesses of the individual subcells. Each subcell needs to absorb  $\sim 1/6$  of the incident light. The six thin (optically partially transparent) photovoltaic semiconductor subcells are interconnected with tunnel junctions (TJs). The optimization of TJs and the subcell thicknesses has been studied in detail previously [14,15,17,75,84,88] and will not be discussed here.

In particular, the PT6 heterostructure was selected to ensure that enough output voltage can be maintained over the industrial temperature range of  $-40\text{ }^{\circ}\text{C}$  to  $85\text{ }^{\circ}\text{C}$ . To that effect, understanding the thermal properties of this new OPC chip is important to ensure the targeted performance is achieved for the intended operating conditions. For example, Figure 2 shows the current–voltage (I–V) curves measured between  $10\text{ }^{\circ}\text{C}$  (purple curve) and  $50\text{ }^{\circ}\text{C}$  (red curve) at an optical input power of  $\sim 13\text{ W}$ , at an input wavelength of  $809\text{ nm}$ . The corresponding voltage temperature behavior is shown in Figure 3a. In Figure 2, the flatness of the I–V curve obtained at  $10\text{ }^{\circ}\text{C}$  is a clear signature of successfully achieving the current-matching conditions from all 6 subcells at that temperature.

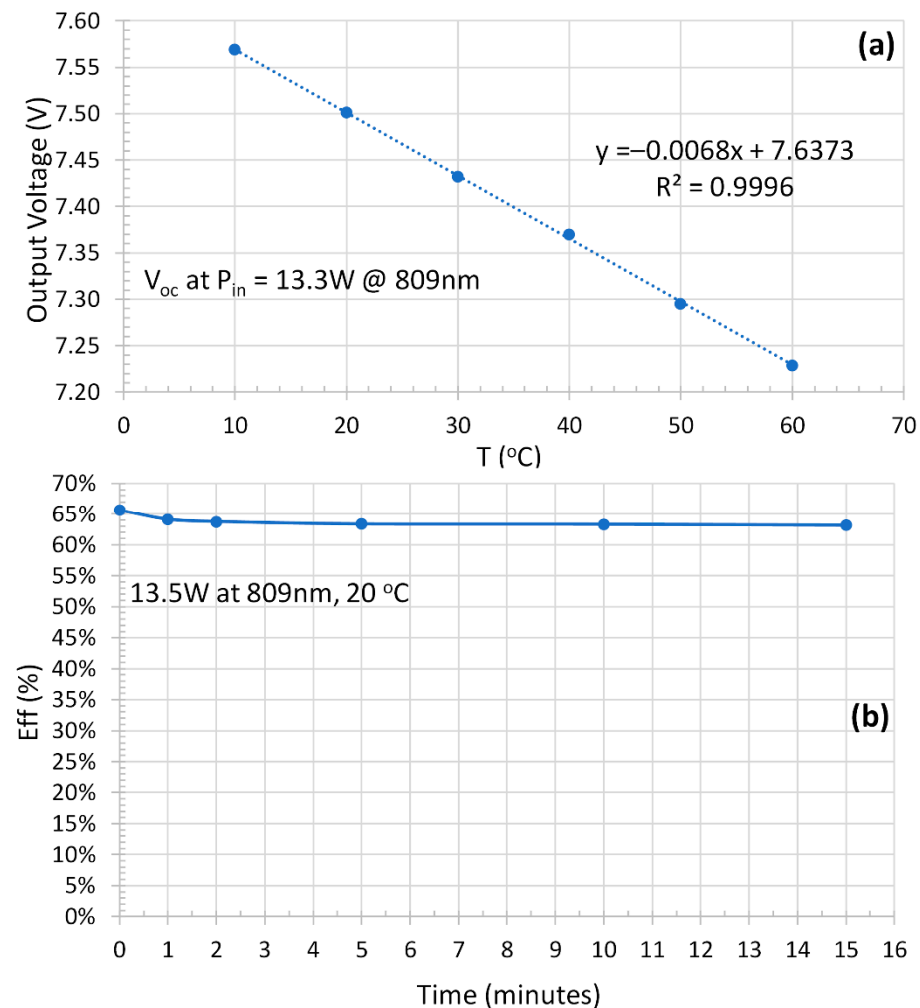


**Figure 2.** Current–voltage characteristics of candidate 10 W OPC chip obtained between  $10\text{ }^{\circ}\text{C}$  (purple curve) and  $50\text{ }^{\circ}\text{C}$  (red curve) at an optical input power of  $13.3\text{ W}$  at  $809\text{ nm}$ .

The plateau observed between  $2.5\text{ V}$  and  $\sim 6\text{ V}$  for the higher temperatures indicates an increasing level of current mismatch for increasing temperatures: as the temperature is increased, the bandgap is reduced, therefore, the upper subcells can capture a larger fraction of the incoming light, and the OPC becomes “bottom cell limited”. In that condition, the overall current is limited by the photocurrent generated in the bottom subcell.

From the linear regression of Figure 3a, an open-circuit voltage ( $V_{oc}$ ) temperature coefficient of  $-6.8\text{ mV}/^{\circ}\text{C}$  is obtained at input powers around  $13\text{ W}$ . The measurements of Figures 1, 2 and 3a were obtained by having the bare chip in good thermal contact with a temperature-controlled copper chuck and by using a cold-start mode. The cold-start mode reduces the temperature effects as much as possible by measuring the I–V responses within about one second from the start of the OPC illumination. In contrast, Figure 3b shows the steady-state performance over a period of  $15\text{ min}$  of continuous illumination at  $\sim 13\text{ W}$  of optical input power. Within  $\sim 2\text{ min}$ , a thermal equilibrium is obtained, the conversion efficiency stabilizes at  $\text{Eff} \sim 63\%$ . A reduction of about  $2.4\%$  absolute from the

cold-start value is observed, here using a copper chuck. The voltage difference between the cold-start condition and the steady-state condition is  $\sim 10$  mV. Using the temperature coefficient of Figure 3a, a junction temperature increase of less than about  $2^\circ\text{C}$  is deduced for the steady-state condition, confirming effective heat extraction from the chip by using the metal chuck setup. In practice, the actual temperature increases in a steady state will be determined by the heatsink performance of the provided environment.

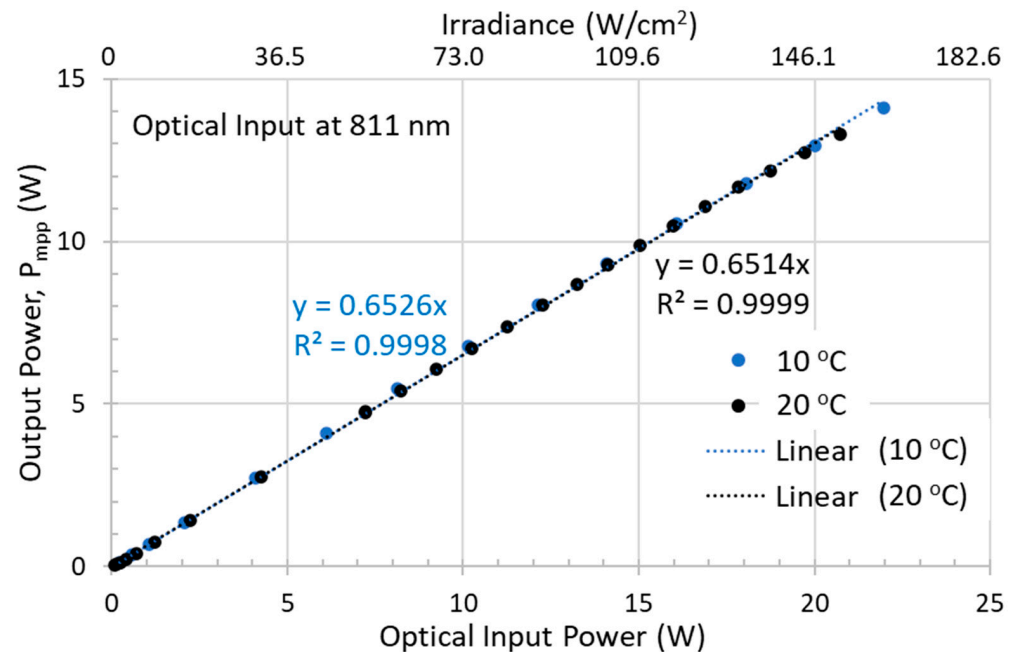


**Figure 3.** Measured temperature dependence of the open-circuit voltage ( $V_{oc}$ ) for an optical input power of 13.3 W at 809 nm in cold-start mode (a), and stabilization of the conversion efficiency with time in steady-state measurement with an optical input power of 13.5 W (b).

### 3. High-Irradiance Results of the 10 W Chip

For an optical input at 811 nm, Figure 4 shows the chip's input power dependence for the output power ( $P_{mpp}$ ) measured at  $10^\circ\text{C}$  (blue) and at  $20^\circ\text{C}$  (black). The corresponding linear regressions are indicated with the same colors. For both temperatures, the output power  $P_{mpp}$  has a measured slope efficiency just above  $\text{Eff} \sim 65\%$ , with negligible deviations from linear regression for optical input powers up to 22 W ( $160\text{ W}/\text{cm}^2$ ). The corresponding irradiance is indicated on the top horizontal axis.

The efficiency in Figure 4 is only slightly higher for the  $10^\circ\text{C}$  base temperature compared to the  $20^\circ\text{C}$  results, which is consistent with the temperature data of Figure 2. The output power reaches 14 W at  $160\text{ W}/\text{cm}^2$  in cold-start testing, suggesting that there are enough margins for achieving 10 W output powers in steady-state measurements with a package providing adequate thermal management.



**Figure 4.** The optical input power dependence of the output power ( $P_{mpp}$ ) for an input at 811 nm measured at 10 °C (blue) and 20 °C (black). The corresponding linear regressions are indicated with corresponding colors, giving an efficiency of about 65% in both cases up to ~22 W of input power (160 W/cm<sup>2</sup>). The corresponding irradiance is indicated on the top horizontal axis.

Figure 5 shows the corresponding optical input power dependence of the conversion efficiency (at 10 °C in black and 20 °C in blue), and of the output voltages:  $V_{oc}$  in purple and  $V_{mpp}$  in green. The maximum efficiencies are obtained in the range of 4 W to 10 W, corresponding to irradiances between 30 and 75 W/cm<sup>2</sup>. The peak efficiency is  $\text{Eff} \sim 67\%$ , and efficiencies just above 64% are still obtained at 160 W/cm<sup>2</sup>. To our knowledge, this is the highest irradiance achieved for high-efficiency OPCs with 14 W capabilities.

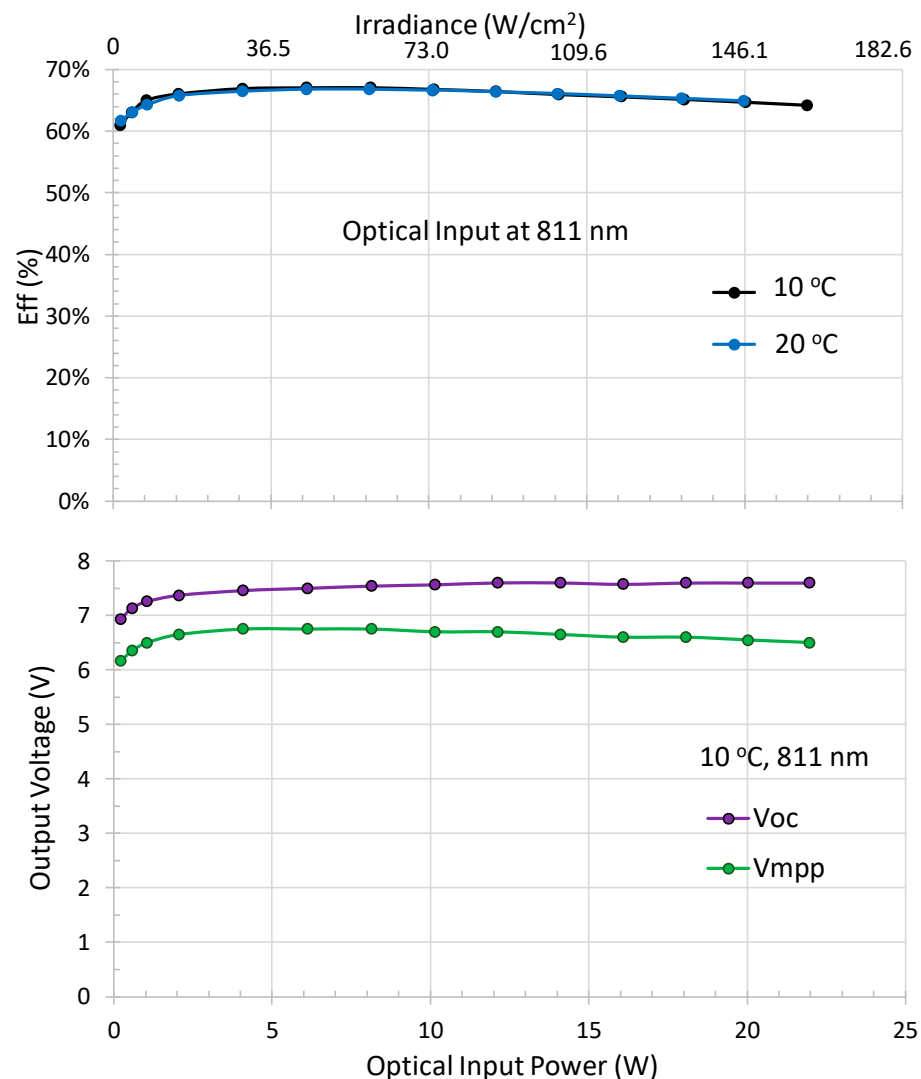
For the cold-start measurements of Figures 4 and 5, the open-circuit voltage ( $V_{oc}$ ) reaches a maximum value of 7.60 V, while the maximum power point voltage ( $V_{mpp}$ ) is 6.75 V at its peak.  $V_{oc} = 7.60$  V corresponds to an average voltage of 1.267 V per subcell, yielding a bandgap voltage offset value of  $W_{oc} \sim 0.153$  V, where  $W_{oc} = (E_g/q) - V_{oc}$  with  $E_g$  being the bandgap energy (here GaAs) and  $q$  is the electronic charge.

The optimal load  $R_{mpp}$  dependence is found from the data to fit  $R_{mpp} = 65.0 \times P_{in}^{-0.987}$  at 10 °C and  $R_{mpp} = 66.0 \times P_{in}^{-0.991}$  at 20 °C, with a regression factor of  $R^2 = 1.0$ , where  $P_{in}$  is the input power in Watts and  $R_{mpp}$  is the optimal load in ohms. It results in a manageable, optimal load that is still 3.4 ohms at 20 W of input power and validates the design strategy for the new 10 W OPC chip. It is also worth remarking that an ideal single junction OPC under the same condition would have an optimal load 36 times smaller, collapsing to  $R_{mpp} \sim 0.09$  ohm. It is therefore practically impossible to operate efficiently at such high irradiances with single junction devices due to excessive power losses caused by unavoidable internal and external resistive losses.

The output current at the maximum power point ( $I_{mpp}$ ) also varies linearly with the input power, with a slope giving a responsivity of 99.0 mA/W. Taking into account the six junctions of the GaAs PT6, for a wavelength of ~811 nm, this corresponds to an  $\text{EQE}_{I_{mpp}}$  of 90.8%: the external quantum efficiency measured at the maximum power point.

Based on the measured I-V curves of Figures 4 and 5, the output voltage as a function of the output load can be plotted for the new six-junction chip. For an optical input at ~809 nm, Figure 6 shows the measurements at 20 °C for optical input powers between 1.21 W and 20.72 W. The plot can be used to determine the minimum optical input power

necessary to maintain a targeted output voltage at a specific load. Conversely, the plot can be used to determine the smallest output load that could still sustain a targeted voltage for a specified optical input power.

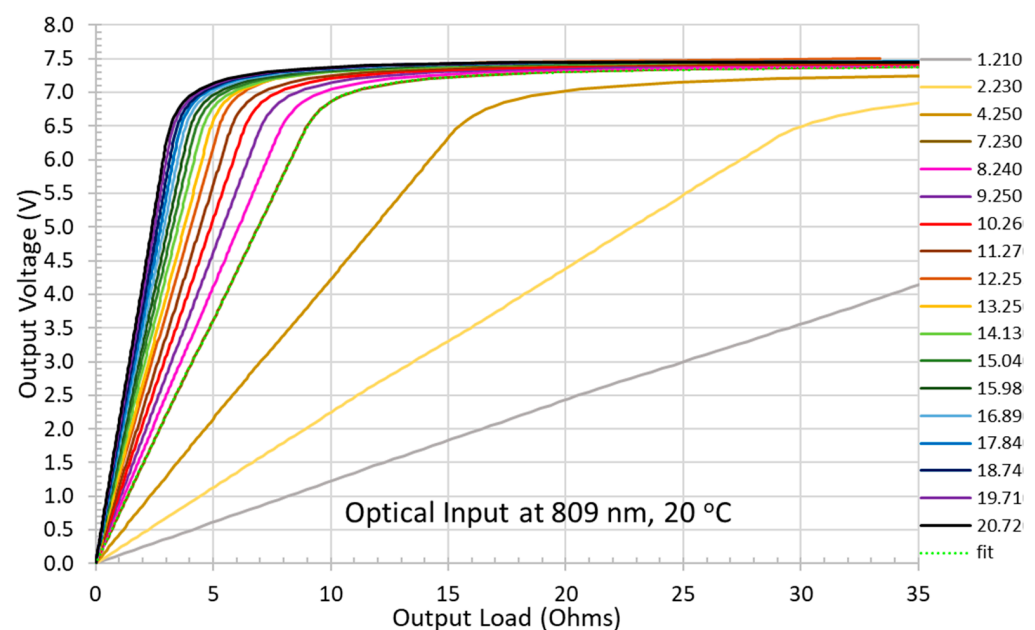


**Figure 5.** The measured optical input power dependence of the conversion efficiency (for 10 °C in black and 20 °C in blue), and for the output voltages at 10 °C ( $V_{oc}$  in purple and  $V_{mpp}$  in green).

The experimental data have also been fitted using an ideal diode model. To illustrate the fit, the dashed-green curve shows the ideal diode model results, compared to the 7.23 W data, using an ideality factor of  $n = 1.35$  for all six subcells. The ideal diode model fits closely the experimental data by using a current mismatch of 2% between the subcells with the lowest and the highest photogeneration currents. For example, Figure 6 reveals that an optical power of at least 10 W is necessary to maintain a 5 V output into a load of 5 ohms. Whereas, for an optical input of about 20 W, an output voltage of 5 V, 6 V, and 6.5 V can be maintained on loads of 2.4 ohms, 2.87 ohms, and 3.18 ohms respectively. Furthermore, for an optical input of about 20 W, PoF systems with external circuits having an effective load of 4 ohms or larger would be self-regulated at an output voltage between 7.0 and 7.5 V.

A good approach to understanding in detail the impact of the heat extraction on the chip performance is to examine the behavior of the output voltage at high irradiances [82]. Figure 7a shows an example of measured  $V_{oc}$  values as a function of the irradiance (area-averaged irradiance values). The black data points are for measurements obtained in cold-start mode with a temperature-regulated copper chuck at 20 °C. A clear saturation of

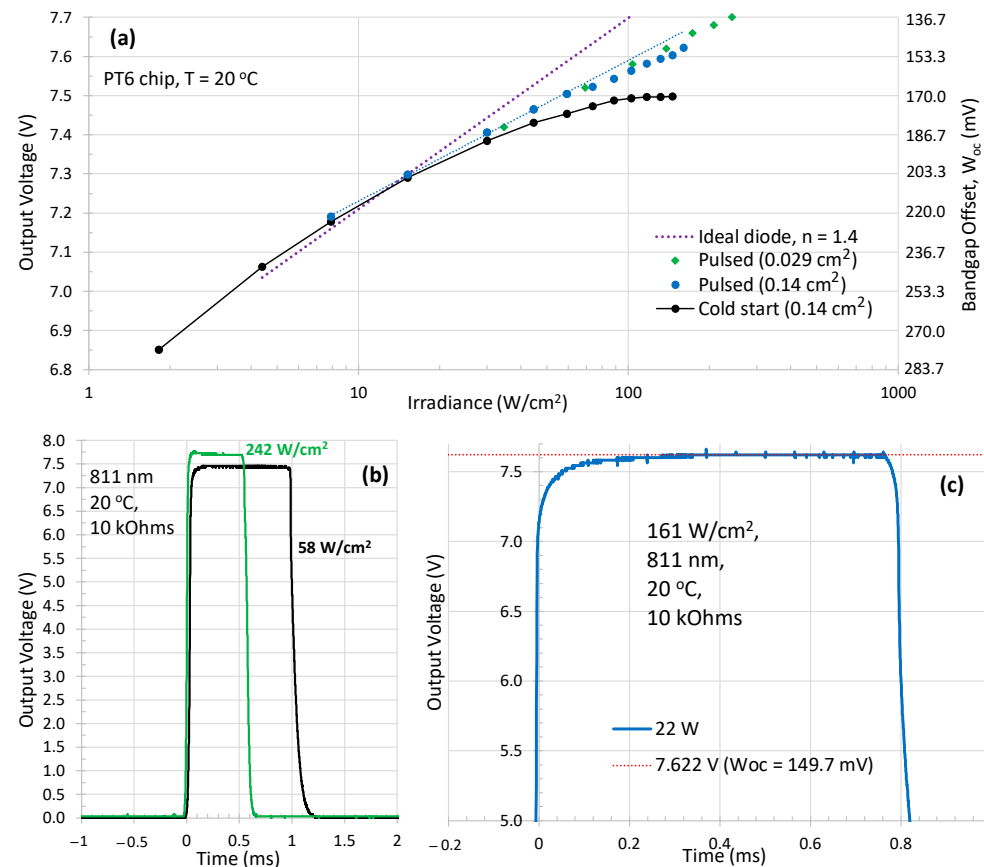
$V_{oc}$  at around 7.5 V is observed here with irradiances of  $100 \text{ W/cm}^2$  or above. It suggests that some heat generated by a fraction of non-converted optical input is not efficiently evacuated and effectively increases the junction temperature. This is better visualized by plotting the expected logarithmic  $V_{oc}$  progression for ideal diodes: the dotted purple line corresponds to the expected voltage for an ideality factor of  $n = 1.4$ . Ideal diode parameters as in the fit of Figure 6 were used. The model indicates that  $V_{oc}$  values as high as 7.7 V could be obtained for perfect heat extraction away from the junction. The heat extraction is hindered by the intrinsic thermal resistance of the layers of the heterostructure, and mainly by the material choice of the thermal interface layers adjoining the chip. Clearly, the selected overall chip heatsinking and thermal management strategies are key aspects determining the realizable performance.



**Figure 6.** Output voltage as a function of the output load for the new six-junction chip measured at  $20^\circ\text{C}$  for optical input powers between 1.21 W and 20.72 W at 809 nm. The dashed-green curve (fit) is an ideal diode model fitted to the 7.23 W data using an ideality factor of  $n = 1.35$  for all six subcells.

To test the chip under a further reduced heat load, the optical input can be used in pulsed mode with a low duty-factor. The round blue data points are for measurements obtained in pulsed mode, with a laser pulse width of 1 ms and a duty-factor of 10% or smaller. It should be noted that the key purpose of the pulse testing here is not to accurately determine the bandwidth properties of the device, but instead to minimize the thermal load and allow measuring the performance with minimal temperature perturbations.

The dotted blue line is the logarithm fit of this pulsed mode data between 1 W and 8 W of input power. A small deviation from a pure logarithmic increase can still be detected at high irradiances, but a clear improvement is observed by reducing the heat load in pulse operation:  $V_{oc}$  values as high as 7.62 V are obtained. This corresponds to a band offset value improvement from  $W_{oc} \sim 170 \text{ mV}$  in cold-start mode down to  $W_{oc} \sim 150 \text{ mV}$  in pulsed mode. Examples of output pulses are shown in Figure 7b,c for an output load of 10 kohms (i.e., quasi open circuit). The black curve of Figure 7b shows a 1 ms output pulse at an input of  $58 \text{ W/cm}^2$  using the  $0.14 \text{ cm}^2$  chip, and the blue curve of Figure 7c shows the top of the output pulse for a 22 W input ( $161 \text{ W/cm}^2$ ) for which a  $V_{oc}$  of 7.622 V is measured ( $W_{oc} = 149.7 \text{ mV}$ ).



**Figure 7.** Output voltage ( $V_{oc}$ ) as a function of the input irradiance (a) the dotted purple line is the expected voltage for an ideality factor of  $n = 1.4$ , the black data points are for measurements obtained in cold-start mode, the round blue data points are for measurements obtained in pulsed mode, and the dotted blue line is the logarithm fit of the pulsed mode data between 1 W and 8 W of input power. The green diamond data points are for measurements obtained in pulsed mode on a smaller chip (0.029 cm²). The corresponding bandgap voltage offset ( $W_{oc}$ ) is shown on the right vertical axis. Examples of measured pulses are shown for an output load of 10 kohms (b) for a 1 ms pulse at an input of 58 W/cm² using the 0.14 cm² chip (black curve), and for a 0.5 ms pulse at an input of 242 W/cm² using a 0.029 cm² chip (green curve). An example of pulse measurement is shown (c) for a 22 W pulse (161 W/cm²) for which a  $V_{oc}$  of 7.622 is measured ( $W_{oc} = 149.7$  mV). The rise and fall times shown here can be limited by the high resistance value used following  $\tau \sim RC$ .

To extend the measurements to even high irradiances, a smaller PT6 chip of the same design was also tested, here fabricated in the same way, but with an area of 0.029 cm². The green diamond data points of Figure 7a are for measurements obtained in pulsed mode on such a smaller chip. The corresponding 0.5 ms output pulse, obtained at the highest irradiance input of 242 W/cm², is also shown in Figure 7b for this 0.029 cm² chip (green curve). It confirms that for the smaller chips in pulse mode, output voltages around 7.7 V are indeed practically obtainable. The corresponding bandgap offset values are shown on the right vertical axis of Figure 7a: remarkably, at 242 W/cm², a bandgap offset value of  $W_{oc} = 136.7$  mV is obtained for a 0.5 ms pulse when using the smaller 0.029 cm² PT6 chip. With such a high average irradiance, the equivalent of more than 2400 suns in terms of typical solar irradiance, the logarithmic increase in the diode voltage allows reaching record  $W_{oc}$  values. In cold-start mode at 208 W/cm², an output of 3.65 W was obtained with  $\text{Eff} = 60.8\%$  with this smaller chip. However, the smaller chip cannot reasonably reach 10 W of output power in practice (unless the irradiance is increased to the equivalent of an area-averaged value of close to 7000 suns). Therefore, the best candidate for the 10 W PoF application remains the 0.14 cm² PT6 chip from this study.

## 4. Discussion

This study shows that operating OPC chips at high irradiance can be advantageous for delivering high output powers with high performance. To successfully achieve top conversion efficiencies at high irradiances, prerequisite aspects are necessary. Figure 1 shows that the performance penalty for working away from the optimal working distance can be of the order of 5% relative to the optimal value. Nevertheless, for PoF applications, the optimal working distance value still delivers a slightly underfilled beam. Moreover, by the nature of the output of multimode pigtailed laser diodes, the OPC illumination will always be non-uniform. For previous characterization of such laser beams, a factor of two or more between the peak illumination relative to the average illumination is often typical [29]. The chip candidate for the new 10 W OPCs operates with conversion efficiencies well above 60% at area-averaged irradiance values reaching at least  $160 \text{ W/cm}^2$ . The smaller chip testing at up to  $242 \text{ W/cm}^2$  of area-averaged irradiances in Figure 7 also confirmed that the chip design works very efficiently at much higher peak irradiances.

Figures 2 and 3 showed that by mounting the chip to an adequate heatsink, the OPCs can operate in a stable way, with a minimal temperature increase. A temperature coefficient of  $-6.8 \text{ mV/}^\circ\text{C}$  was measured, and detuning of the current matching reduces the conversion efficiency as the temperature increases. The packaging and the thermal management strategies need to carefully consider these aspects. Minimizing the thermal resistance of the interface materials adjoining the OPC and the optimization of the heat evacuation will be key considerations for packaging and mounting the 10 W OPCs based on these PT6 chips. For example, assuming the chip needs to dissipate of the order of 10 W of heat when operating at higher temperatures, further assuming a target maximum chip temperature increase of  $20^\circ\text{C}$  from ambient, a heatsink performance specification of at least  $2^\circ\text{C/W}$  would be necessary [37].

Figures 4 and 5 demonstrate that the chip can deliver 14 W of output power at irradiances up to  $160 \text{ W/cm}^2$ , with conversion efficiencies well above 60% at  $20^\circ\text{C}$ . It is therefore expected that this  $0.14 \text{ cm}^2$  chip will be suitable for a new 10 W OPC product for PoF applications. Figure 6 showed that the PT6 design allows manageable output loads: for example, at 20 W of optical input, an output voltage of 5 V, 6 V, and 6.5 V can be maintained on loads of 2.4 ohms, 2.87 ohms, and 3.18 ohms respectively. Furthermore, PoF systems with external circuits having an effective load of 4 ohms or larger would be self-regulated at an output voltage between 7.0 and 7.5 V.

Figure 7 demonstrated that remarkable output voltages can be obtained with multi-junction OPCs operated at high irradiances. The key prerequisite aspects for unlocking these attributes are: multijunction designs enabling efficient photocarrier absorption and extraction, tunnel junction designs capable of supporting high irradiances with minimal voltage losses, and efficient thermal management. The logarithmic voltage increase in the photovoltaic diode allows reaching record  $W_{oc}$  values with such multijunction OPCs. For example, in pulsed mode,  $W_{oc}$  values as low as 150 mV have been obtained at  $20^\circ\text{C}$  for the  $0.14 \text{ cm}^2$  chip at  $160 \text{ W/cm}^2$  and  $0.029 \text{ cm}^2$  devices yielded  $W_{oc}$  values around 137 mV at  $240 \text{ W/cm}^2$ , which is the equivalent of more than 2400 suns in terms of typical solar irradiance.

## 5. Conclusions

In conclusion, the high-efficiency capabilities of multijunction laser power converters have been demonstrated at very high irradiances. The vertical multijunction VEHSa strategy has once again proven very effective at trading photocurrent in favor of increasing the operating voltage for an 808 nm chip capable of 10 W operation: an important development for power-over-fiber applications at higher powers. At the chip level, the maximum

efficiencies are obtained in the range of 30 to 75 W/cm<sup>2</sup>, and efficiencies > 64% are still attained at 160 W/cm<sup>2</sup> with an electrical output of 14 W. In pulsed mode,  $W_{oc}$  values as low as 150 mV have been obtained for a device base temperature of 20 °C. For even smaller 0.029 cm<sup>2</sup> devices,  $W_{oc}$  values around 137 mV were obtained at 240 W/cm<sup>2</sup>.

This study has built the foundation for chip-level properties and the characterization of new 10 W laser power converters. Key data has been revealed on the working distance, input/output power capabilities, output voltage properties, conversion power/efficiencies, and the related thermal properties and requirements. Subsequently, the reliability aspects will be studied in detail, but it is expected that Broadcom will be packaging this chip into a suitable housing, optimized for thermal management, and with an ST optical connector for high-power-over-fiber applications.

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