sustainability

MDPI

Article

Design and Performance Evaluation of a Step-Up DC–DC Converter with Dual Loop Controllers for Two Stages Grid Connected PV Inverter

Muhammad Yasir Ali Khan [1], Haoming Liu [1,*], Salman Habib [1,*], Danish Khan [2] and Xiaoling Yuan [1]

[1] College of Energy and Electrical Engineering, Hohai University, Nanjing 211100, China; m.yasir_alikhan@yahoo.com (M.Y.A.K.); lingx@hhu.edu.cn (X.Y.)
[2] School of Electrical Engineering, Zhejiang University, Hangzhou 310027, China; daniskhandirvi@alumni.sjtu.edu.cn
* Correspondence: liuhaom@hhu.edu.cn (H.L.); salmanhabib@hhu.edu.cn (S.H.)

Abstract: In this work, a non-isolated DC–DC converter is presented that combines a voltage doubler circuit and switch inductor cell with the single ended primary inductor converter to achieve a high voltage gain at a low duty cycle and with reduced component count. The converter utilizes a single switch that makes its control very simple. The voltage stress across the semiconductor components is less than the output voltage, which makes it possible to use the diodes with reduced voltage rating and a switch with low turn-on resistance. In particular, performance principle of the proposed converter along with the steady state analysis such as voltage gain, voltage stress on semiconductor components, and design of inductors and capacitors, etc., are carried out and discussed in detail. Moreover, to regulate a constant voltage at a DC-link capacitor, back propagation algorithm-based adaptive control schemes are designed. These adaptive schemes enhance the system performance by dynamically updating the control law parameters in case of PV intermittency. Furthermore, a proportional resonant controller based on Naslin polynomial method is designed for the current control loop. The method describes a systematic procedure to calculate proportional gain, resonant gain, and all the coefficients for the resonant path. Finally, the proposed system is simulated in MATLAB and Simulink software to validate the analytical and theoretical concepts along with the efficacy of the proposed model.

Keywords: adaptive controller; DC–DC converter; DC-link control; grid connected PV system; PR controller; single switch

Citation: Khan, M.Y.A.; Liu, H.; Habib, S.; Khan, D.; Yuan, X. Design and Performance Evaluation of a Step-Up DC–DC Converter with Dual Loop Controllers for Two Stages Grid Connected PV Inverter. *Sustainability* **2022**, *14*, 811. https://doi.org/10.3390/su14020811

Academic Editor: Alberto-Jesus Perea-Moreno

Received: 25 November 2021
Accepted: 7 January 2022
Published: 12 January 2022

1. Introduction

In recent years, Photovoltaic (PV) holds a pivotal position in ever-increasing energy demand due to easy accessibility, easy installation, high return on investment, and low maintenance cost [1]. A complete PV system consists of a PV array, DC–DC converter (optional), DC-link (DCL) capacitor, inverter, filter, and a grid. Therefore, based on the devices, the PV system configuration is categorized into two types i.e., single-stage and two-stage configuration systems. A single-stage system consists of a PV array, DCL capacitor, inverter, filter, and a grid. In this system, the weight and size of the system are considerably reduced but complexity is greatly increased due to the handling of different functionalities (Maximum Power Point Tracking (MPPT), current control, voltage control, and grid synchronization) by the inverter alone. Moreover, for some applications, the PV voltage needed to be increased to the desired level that cannot be achieved without the use of a DC–DC converter. Therefore, to reduce the system complexity and widen its applications range, a DC–DC converter is introduced in the two-stage configuration system [2]. A schematic of the 2-stage three-phase (3Φ) grid-connected PV system used in this research work is shown in Figure 1.

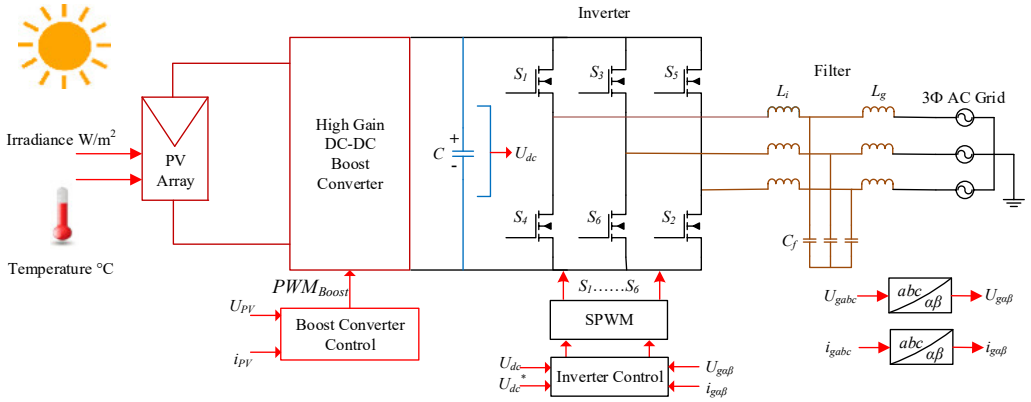

Figure 1. Schematic of a 2-stage 3Φ grid connected PV system.

In the 1st stage of the PV system, a DC–DC boost converter is used to extract the maximum power from the PV panel through the maximum power point technique and lift-up the voltage level according to the desired application. Generally, the classical converters such as boost, Single Ended Primary Inductor Converter (SEPIC), and cuk, etc. are used to attain a High Voltage Gain (HVG). For this purpose, a converter is needed to be operated at a high duty cycle, which has some disadvantages, such as (a) increased duty cycle causing lower efficiency due to increased losses in parasitic resistances of a diode, capacitor, and inductor; (b) as the duty cycle increases, the voltage stress on the switch increases; and (c) increased conduction and switching losses [3].

To overcome the above-mentioned limitations, numerous researchers have designed different converter topologies that can be categorized into isolated and non-isolated topologies based on coupling [4]. A transformer is used in isolated topologies to attain a HVG; however, due to the heavy weight of the transformer and its core and winding losses, they are not feasible for low power PV applications. Consequently, the authors used non-isolated topologies to overcome the issues in isolated topologies [5–9]. A coupled inductor-based Switch Inductor (SL) configured high lift-up converters for renewable application is proposed in [5]. Due to the usage of coupled inductors, the efficiency of these topologies is low due to the leakage inductances of the windings. The authors proposed single inductor-based converter topologies that can achieve a HVG while maintaining good efficiency [6–9]. In [6], eight different SL-based converter topologies are presented, in which SL is configured with traditional boost, cuk, and SEPIC. Although HVG is achieved by most of these topologies, usage of high component count increases the operational complexity and cost of the converters. An SL and Switch Capacitor (SC)-based improved cuk converter is presented in [7]. This topology is very attractive in terms of HVG but the utilization of two switches and a high number of magnetizing components causes an increment in the control, complexity, and cost. A single switch SEPIC-based modified converter topology is proposed in [8]. However, even though a high voltage gain is achieved for continuous input current, the converter initially suffers from high conduction losses as voltage stress on the switch is equal to the output voltage. An SL/SC-based cascaded boost converter proposed in [9] can achieve HVG with reduced component count but is unable to attain high efficiency. To overcome the limitations in the above-discussed topologies, in this research work, an SL configured hybrid topology that combines the Voltage Doubler Circuit (VDC) with the SEPIC converter is proposed. The most prominent features include high voltage conversion ratio, fewer components, single switch, low voltage stress on semiconductor components, and contiguous input current.

In the second stage of the PV system, besides DC–AC inversion, the functionality of the inverter also involves grid synchronization, current control and protection, and DCL voltage regulation, etc. Therefore, for the smooth and stable performance of the PV system, the inverter control plays a prominent role and is usually implemented in the form of two cascaded loops i.e., outer Voltage Control Loop (VCL) and inner Current

Control Loop (CCL). A VCL is responsible for maintaining a constant DCL voltage and generates a reference for the current loop. A CCL is responsible for grid synchronization and injection of a high-quality current [2]. Generally, a Proportional Integral (PI) controller is implemented in the VCL, however, due to PV intermittency, a PI controller fails to maintain a constant DCL voltage due to its fixed gain parameters [10]. Therefore, to enhance the system performance, an arbitrary real term is introduced in the PI controller through fractional calculus and named the Fractional Order Proportional Integral (FOPI) controller [11]. Although the system performance is improved, high ripple contents and distortion from the reference are observed during uncertainties (PV intermittency). A Sliding Mode Controller (SMC) for DCL regulation in proposed in [12]. This controller has a fast dynamic response but the waveforms suffer from chattering phenomena. To enhance the SMC performance and smoothen the shattering effect, the authors introduced an integral term in the SMC [13]. The performance of the PV system is enhanced to a great extent by using fuzzy PI and fuzzy SMC controllers in [14]. However, these controllers have complex architectures and failed to achieve high-quality waveforms. Due to the above discussed limitations in the DCL controller topologies, there is a need to develop a controller that adopts the system uncertainties and ensures the system stability. Therefore, such a controller is needed to be designed that adopts the system dynamics and regulates a DC-link voltage. Hence, in this research work, a Back Propagation (BP) algorithm-based Adaptive Proportional Integral (API) and Adaptive Fractional Order Proportional Integral (AFOPI) controllers are designed. The parameters of these controllers will be updated automatically, in case of any environmental variation or disturbance, and achieve a regulated voltage at a DC-Link.

To maintain a high-quality grid injected current, PI or Proportional Resonant (PR) controllers are usually applied in the inner current control loop. However, when a PI controller is applied in a stationary frame, it cannot track the sinusoidal reference accurately; therefore, the system variables need to be transformed into a synchronous frame that requires large calculations [15]. On the other hand, a PR controller is highly suitable to track the sinusoidal reference and thus, making it an optimal solution for inverter-based grid-connected PV applications. It provides an infinite gain at the selected resonant frequency (at other frequencies there exists almost no gain), and thus, the zero steady-state error can be easily attained [16]. Although it has a high tracking capability, the output current of the grid connected inverter is not invulnerable for harmonic content that usually occurs due to the non-linearities in converter and inverter. Therefore, to reduce or eliminate the harmonic contents, a selective Resonant Harmonic Compensator (RHC) can be added to a PR controller [16]. The performance of the system is greatly improved by using a PR controller and can be found widely in the literature. However, most of the researchers did not explain the design and tuning procedures of their respective controller in detail, and the trial-and-error method is adopted to find the optimal gain values. Although some of the researchers described the design procedure in a continuous-time domain, most of the Grid Connected PV Inverter (GCPVI) applications involve digital implementation. Therefore, the authors in [17] proposed a digital PR controller that has a simple control architecture and tuning methodology. Compared to the conventional methodology, which involves complex trigonometric equations, this work presents a systematic procedure to calculate proportional gain (k_p), resonant gain (k_{ir}), and the coefficients of the resonant path. However, it shows an effective performance, although it is limited to 1Φ grid connected system and is developed by considering the dynamic behavior of LC filter. However, most of the grid connected power systems involves 3Φ operation and operates at a low frequency. At low frequency the size of L or LC filters becomes very bulky and expensive as a result LCL filters being introduced. In addition to the cost and size, LCL filter offers numerous other advantages such as: (a) smoothens the inverter output current, (b) low Total Harmonic Distortion (THD), (c) improved performance, and (d) and high attenuation [18]. Due to these advantages, in this research work, a PR controller proposed in [17] is modified by considering the dynamics of LCL filter and implemented in a 3Φ grid connected PV system.

The core contributions of this work are listed as:

- A transformer-less high voltage gain DC–DC converter is presented that extracts the maximum power from the PV panel by using Perturb and Observe (P&O) MPPT technique and step-up the low generated PV voltage to a level applicable for grid connected PV inverter. In the proposed topology, a voltage doubler circuit and switch inductor cell are integrated with the SEPIC converter to attain a high voltage conversion ratio. The prominent features of the converter include single switch, simple control, low voltage stress, high efficiency, and fewer components.
- Back propagation algorithm-based API and AFOPI controllers are designed to regulate a DC-link voltage in case of PV intermittency. This adaptive scheme enhances the system performance and handles the system uncertainties by dynamically updating the control law parameters. The proposed controllers have a faster dynamic response and easy implementation, which improves the system stability.
- Based on the Naslin polynomial method, a PR controller is designed, considering the dynamic behavior of an LCL filter. In the proposed controller, no parameter is computed empirically or by trial-and-error method. To show the effectiveness of the controller, it is implemented in a 3Φ grid-connected PV system that results in low THD.

The rest of the manuscript is divided into the following sections as: A schematic and detailed analysis of the first stage of the PV configuration system, including MPPT algorithm and DC–DC converter, which are elaborated on in Section 2, while the second stage that involves DC-link voltage and current controllers are discussed in Section 3. The performance validation of the proposed system is described in Section 4. Finally, this research work is concluded in Section 5.

2. Analysis of DC–DC Converter

Due to the dependency of the Maximum Power Point (MPP) of the PV array on climatic parameters, the position of MPP varies indefinitely. Therefore, to precisely locate the MPP, numerous MPPT algorithms were reported in literature, that vary from each other in various aspects such as complexity, cost, type of sensors required, implementation, and range of effectiveness [19]. In this research, a P&O technique is adopted due to its simplicity and easy implementation, as presented in Figure 2a [19]. According to the operating voltage and current, the P&O technique generates a Pulse Width Modulation (PWM) for the converter as shown in Figure 2b. Generally, the PV system generates a low-level voltage that is needed for amplifying the appropriate operation of the inverter; therefore, a step-up converter is designed, which is discussed below. Moreover, the specifications of the PV panel and the gain parameters of the PI controller used to drive the converter switch are listed in Tables A1 and A2, respectively.

2.1. Proposed Converter Topology and Operating Modes

A schematic circuitry of a single switch high lift-up DC–DC converter is presented in Figure 3. It consists of an input voltage source (U_{PV}), switch (S), diodes (D_1, D_2, D_3, D_4, D_5, and D_6), inductors (L_1, L_2, and L_3), and capacitors (C_1, C_2, and C_{DC}). In this converter, the VDC and SEPIC converter are arranged in such a manner that it enhances the voltage conversion ratio. Furthermore, the primary inductor of the SEPIC converter is replaced with the SL unit (L_1, L_2, D_1, D_2, and D_3) to further enhance the voltage conversion characteristics. The inductors L_1 and L_2 of SL unit have the same magnitude and are always connected to the input source, therefore, the converter input current will always be continuous in nature.

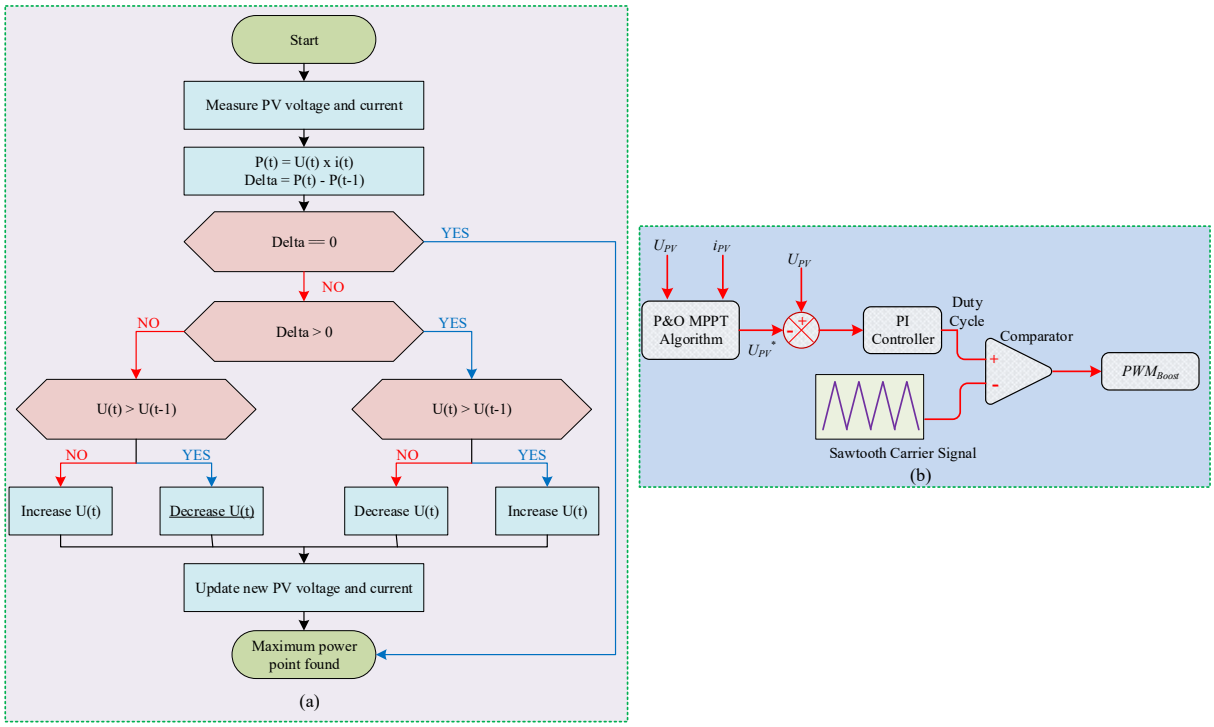

Figure 2. MPPT operation and PWM generator (**a**) P&O MPPT algorithm flow chart and (**b**) boost converter controller block.

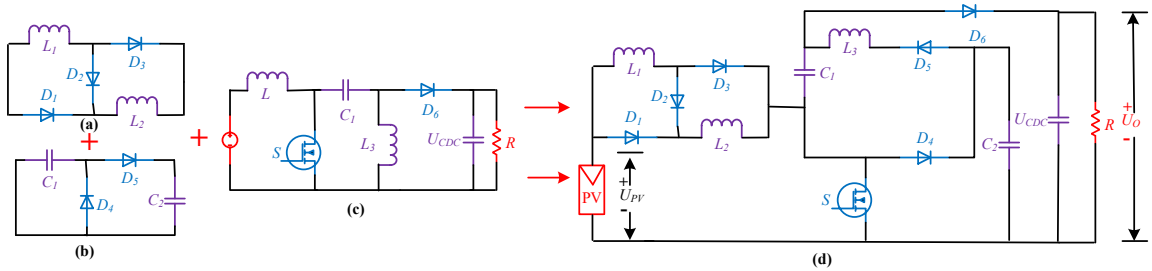

Figure 3. Schematic circuitries of (**a**) SL, (**b**) voltage doubler, (**c**) SEPIC and (**d**) proposed topology.

The proposed converter can operate in two operating modes, i.e., Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The CCM can be divided into two switching intervals, while a DCM can be divided into three switching intervals. A detailed analysis of CCM and DCM are discussed below in detail. However, for simplicity, the following considerations are made in theoretical analysis: (a) the Equivalent Series Resistances (ESRs) value of all components used in converter are not taken into account during the analysis of operating modes, (b) the capacitors are large enough so that they act as a constant voltage source, (c) the leakage inductances have a low value and are not considered in analysis.

2.1.1. Continuous Conduction Mode

Based on the switch characteristics of the converter, its operation is discussed for two switching intervals, i.e., ($t_0 \sim t_1$) (S is ON) and ($t_1 \sim t_2$) (S is OFF). The equivalent circuitries of both switching intervals along with the direction of current flow (red arrows) are presented in Figure 4a,b respectively, whereas its typical waveforms in steady state are sketched in Figure 4c.

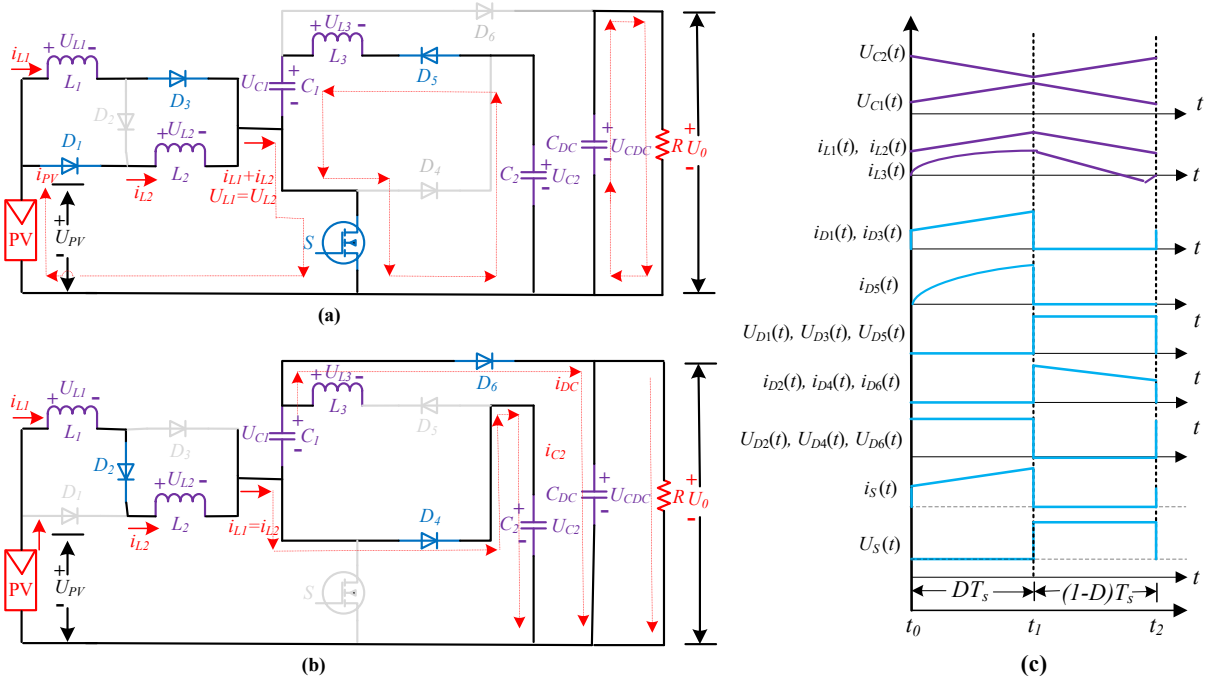

Figure 4. Equivalent circuitry during (**a**) ($t_0 \sim t_1$), (**b**) ($t_1 \sim t_2$), and (**c**) typical waveforms in a switching interval in CCM.

- Switching Interval ($t_0 \sim t_1$)

In this switching interval, switch (S) is turned and diodes (D_1, D_3, and D_5) are in forward conduction mode, while the diodes (D_2, D_4, and D_6) are in reverse biased state as presented in Figure 4a. The inductors (L_1 and L_2) will be charged from input source (U_{PV}) through D_1 and D_3. As L_1 and L_2 have the same magnitude, the same amount of current will therefore be flowing through them and is charged in parallel (i.e., $U_L = U_{L1} = U_{L2}$, and $i_L = i_{L1} + i_{L2}$). The inductor (L_3) is also charge in this interval and $U_{C1} - U_{C2}$ is applied to it. Moreover, C_2 discharges to charge C_1 and L_3. The capacitor C_{DC} also discharges, and its stored energy is used to feed the load.

- Switching Interval ($t_1 \sim t_2$)

During this interval, diodes (D_1, D_3, and D_5) and switch (S) are turned OFF, while the diodes (D_2, D_4, and D_6) are in forward conduction mode as presented in Figure 4b. As D_1 and D_3 are in reverse biased and D_2 is in forward biased, L_1 and L_2 therefore act as a series connected circuit (i.e., $i_{L1} = i_{L2}$). The stored energy in L_1 and L_2 are used to charge C_2 through D_4 and also transfer its energy to support the load through C_1 and D_6. L_3 also discharges in this interval to charge C_{DC} and support the load.

2.1.2. Discontinuous Conduction Mode

Based on the switch characteristics, the operation of the converter in DCM is divided in three switching intervals, i.e., ($t_0 \sim t_1$) (S is ON), ($t_1 \sim t_2$) (S is OFF), and ($t_1 \sim t_2$) (S is OFF). The typical waveforms of proposed converter in steady state operating in DCM are presented in Figure 5a.

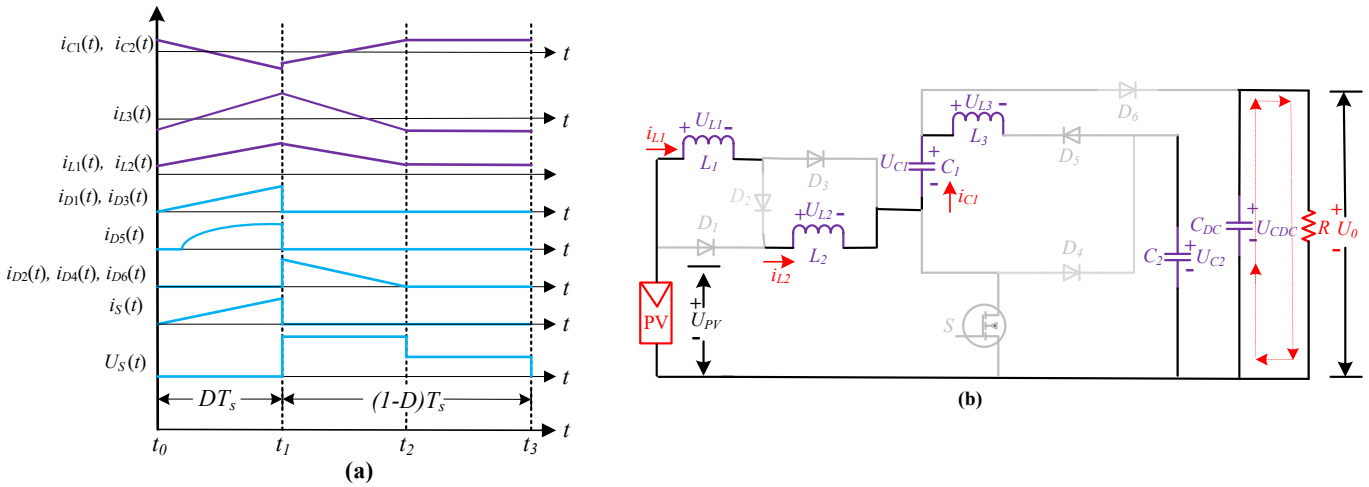

Figure 5. Equivalent circuitry during (**a**) typical waveforms in a switching interval in DCM and (**b**) switching interval ($t_2 \sim t_3$).

- Switching Interval ($t_0 \sim t_1$)

In this switching interval, switch (S) and diodes (D_1, D_3, and D_5) are in forward conduction mode while all other diodes are in reverse biased as shown in Figure 4a. The inductors (L_1, and L_2) stores energy by using input voltage source while $U_{C1} - U_{C2}$ is applied across L_3. This mode ends when the current flows through switch S and diodes (D_1, D_3, and D_5) becomes zero at t_1.

- Switching Interval ($t_1 \sim t_2$)

In this interval, the diodes (D_2, D_4, and D_6) are in forward biased while all other semiconductor components are in reverse conduction mode as shown in Figure 4b. The inductors discharges in this interval to charge the capacitors and supports the load. This mode ends when the current flowing through diodes (D_2, D_4, and D_6) becomes zero.

- Switching Interval ($t_2 \sim t_3$)

During this interval, switch (S) remains in turned OFF state and all the diodes (D_1, D_2, D_3, D_4, D_5, and D_6) are in reverse conduction mode as presented in Figure 5b. The voltage that appears across inductors (L_1, L_2, and L_3) becomes zero and the current flowing through inductors is continued as constant. During this mode, the load is supported by the output or DC-link capacitor (C_{DC}). This mode ends when the switch (S) is turned ON and returns to the first operating mode.

2.2. Performance Evaluation of Converter

In this section, different characteristics such as voltage stress, voltage gain, design of inductors and capacitors, and loss analysis of the proposed converter in CCM mode are discussed. Moreover, a comparative analysis of proposed topology with other topologies is also presented.

2.2.1. Voltage Gain Derivation

The output voltage (U_O) of the converter is given as,

$$U_O = U_{C1} + U_{C2} \quad (1)$$

as it is assumed that the converter is operating in a CCM and therefore that the average inductor voltage at steady state condition is zero. Therefore, by applying inductor volt-second balance theorem over one switching cycle to L ($L_1 = L_2 = L$) we produce,

$$\int_0^{Ts} U_L(t)dt = (U_{PV})(DT_S) + \left(\frac{U_{PV} - U_{C2}}{2}\right)((1-D)Ts) \tag{2}$$

where D is the duty cycle of the switch. By solving (2), we produce the capacitor voltage (U_{C2}) as,

$$U_L = 0 \Rightarrow U_{C2} = \frac{1+D}{1-D}U_{PV} \tag{3}$$

Similarly, by applying inductor volt-second balance theorem to L_3 over one switching cycle we produce,

$$\int_0^{Ts} U_{L3}(t)dt = (U_{C1} - U_{C2})(DT_S) + (U_O - U_{C2})((1-D)Ts) \tag{4}$$

Solve Equation (4) for U_{C1} we produce,

$$U_{L3} = 0 \Rightarrow U_{C1} = \frac{D}{1+D}U_O \tag{5}$$

Put (3) and (5) in (1) and rearrange them, we produce a voltage gain of the proposed converter in CCM as,

$$\frac{U_O}{U_{PV}} = \frac{(1+D)^2}{1-D} \tag{6}$$

2.2.2. Voltage Stress Calculation

The voltage stress on the semiconductor components can be calculated as,

$$U_S = U_{D4} = U_{D6} = \frac{1+D}{1-D}U_{PV} \tag{7}$$

$$U_{D1} = U_{D3} = \frac{D}{1-D}U_{PV} \tag{8}$$

$$U_{D2} = U_{PV} \tag{9}$$

$$U_{D5} = U_O - U_{C2} \tag{10}$$

From (7), it can be observed that the proposed topology exhibits lower voltage stress compared to the classical converters, thus results in lower conduction losses.

2.2.3. Design of Inductors and Capacitors

The design of inductors is based on the value of current ripples (Δi_L), and is considered between 5–10% of the nominal output current to achieve optimal inductor size [20]. Therefore, the inductances can be calculated as:

$$L = L_1 = L_2 = \frac{U_{PV} + U_{C1}}{i_L f_{SW} \Delta i_L} D \tag{11}$$

$$L_3 = \frac{V_{C2}(1-D)}{f_{SW}\Delta i_{L3}} \tag{12}$$

where f_{sw} is the switching frequency and i_L is the inductor current and can be calculated as:

$$i_L = \frac{1}{1+D}(i_{PV} - i_O D) \tag{13}$$

where i_O is the output current of the converter. The capacitors (C_1 and C_2) are designed by using the voltage ripples (ΔU_C), which are assumed to be 5–10% of the output or DC-link voltage of the capacitor [20]. Hence, the capacitances can be calculated as,

$$C_1 = C_2 = \frac{i_O}{f_{SW}\Delta U_C} \tag{14}$$

where voltage ripples (ΔU_C) is given as,

$$\Delta U_C = \left(\frac{U_{PV}}{1-D}\right)10\% \tag{15}$$

The main functionality of the DCL capacitor is to store or supply the surplus power demand during transience and to lower the DC ripples [13]. It is designed according to [21] as,

$$C_{DC} = \frac{P_{CDC}}{4\pi f_g U_{DC}\Delta U_{DC}} \tag{16}$$

where P_{DC} is the DCL power, ΔU_{DC} is the peak-to-peak voltage ripples, and f_g is the grid frequency.

2.2.4. Loss Analysis

Equivalent circuitries of proposed converters, including the parasitic resistances in switching interval ($t_0 \sim t_1$) and ($t_1 \sim t_2$) are presented in Figure 6a,b respectively. In the Figure 6a,b, the parasitic resistances of the components are considered as; (a) r_{ONS} is the resistance of the switch in turn ON state, (b) r_{D1}, r_{D2}, r_{D3}, r_{D4}, r_{D5}, and r_{D6} are the ON-resistances of diodes D_1, D_2, D_3, D_4, D_5, and D_6, respectively, (c) U_{D1}, U_{D2}, U_{D3}, U_{D4}, U_{D5}, and U_{D6} are the threshold voltages of D_1, D_2, D_3, D_4, D_5, and D_6, respectively, (d) r_{L1}, r_{L2}, and r_{L3} are the equivalent ESRs of inductors L_1, L_2, and L_3, respectively, and (e) r_{C1}, r_{C2}, and r_{CDC} are the ESR of capacitors C_1, C_2, and C_{DC}, respectively.

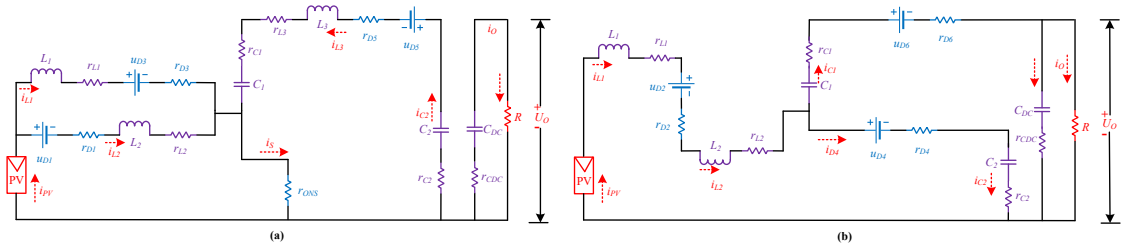

Figure 6. Equivalent circuitry with losses during (**a**) [$t_0 \sim t_1$] and (**b**) ($t_1 \sim t_2$).

- Inductor Copper Loss

  The copper loss of inductor is given as,

$$P_L = 2i_{L-A}^2 \; r_L + i_{L3-A}^2 r_L \tag{17}$$

where i_{L-A} and i_{L3-A} are the average current of L ($L_1 = L_2 = L$ hence $r_{L1} = r_{L2} = r_L$) and L_3, respectively. Solving (17) would yield us to:

$$P_L = \left(\frac{1}{1+D}(i_{PV} - i_O D)\right)^2 r_L \tag{18}$$

- Capacitor Loss

The power loss in the capacitor mainly depends on the Root Mean Square (RMS) value of the current flowing through capacitor and ESR of capacitor. Moreover, as C_1 and C_2 are of same rating thus $r_{C1} = r_{C2} = r_C$. The power loss can be calculated as,

$$P_C = \left(i_{C1-R}^2 + i_{C2-R}^2\right) \; r_C + i_{CDC-R}^2 \; r_{CDC} \tag{19}$$

Solving (19) in term of duty cycle would give us:

$$P_C = \left(\frac{2i_O^2 + i_L^2 - 2i_O i_L}{D(1-D)}\right) r_C + \left(\frac{i_O^2}{D}\right) r_{CDC} \tag{20}$$

- Switch Loss

There are two types of switch losses, i.e., conduction loss and switching loss and can be given as:

$$P_{S-Total} = P_{S-Swt} + P_{S-Cond} \tag{21}$$

The switching loss depends on the turn ON and OFF time, peak current (i_{S-P}), switching frequency, and voltage appeared across switch (U_S). Hence, the switching power loss can be given as:

$$P_{S-Swt} = \frac{t_{ON} + t_{OFF}}{2} (U_S . i_{S-P} . f_{SW}) \tag{22}$$

Putting values in (22) and solve in term of duty cycle would give us:

$$P_{S-Swt} = (t_{ON} + t_{OFF}) \left(\frac{1+D}{1-D}\right) \left(\frac{(1-D)i_L - i_O}{D}\right) U_O . i_O . f_{SW} \tag{23}$$

The conduction loss of the switch can be calculated as:

$$P_{S-Cond} = i_{S-R}^2 . r_{ONS} = 2\left(\frac{(1-D)i_L - i_O}{D}\right)^2 i_O^2 . r_{ONS} \tag{24}$$

where i_{S-R} is the RMS current of S.

- Diode Loss

The forward voltage drop and the conduction loss are the two types of losses associated with the diode.

$$P_{D-Total} = P_{D-UD} + P_{D-Cond} \tag{25}$$

The forward voltage drop loss is given as:

$$P_{D-UD} = (i_{D1-A} + i_{D2-A} + i_{D3-A} + i_{D4-A} + i_{D5-A} + i_{D6-A}) U_D \tag{26}$$

where i_{D1-A} to i_{D6-A} are the average current flows through diodes D_1 to D_6, respectively. Solving (26) would give us:

$$P_{D-UD} = \left(2i_L + i_O\left(1 + (1+D)^2\right)\right) U_D \tag{27}$$

The conduction loss of diodes is calculated as,

$$P_{D-Cond} = \left(i_{D1-R}^2 + i_{D2-R}^2 + i_{D3-R}^2 + i_{D4-R}^2 + i_{D5-R}^2 + i_{D6-R}^2\right) r_D \tag{28}$$

where i_{D1-R} to i_{D6-R} are the RMS current of diodes D_1 to D_6, respectively, where r_D is the equivalent ON-resistance of diodes. Solving (28) in term of duty cycle would yield us to:

$$P_{D-Cond} = (1-D) i_{PV}^2 + (1+D)\left(i_L^2 + i_{L3}^2\right) + \left(\frac{1}{D(1-D)}\right) i_O^2 + \left(\frac{((1-D)i_L - i_O)^2}{1-D}\right) r_D \tag{29}$$

- Total Loss

  The total loss of the proposed converter can be calculated as:

$$P_{Loss} = P_L + P_C + P_{S-Swt} + P_{S-Cond} + P_{D-Vf} + P_{D-Cond} \quad (30)$$

  The efficiency of the converter is obtained as:

$$\eta_{Converter} = \left(\frac{P_o}{P_o + P_{Loss}}\right)100\% \quad (31)$$

2.2.5. Comparative Analysis

A comparative analysis of the proposed converter with the conventional and newly developed topologies on the basis of some main indicators such as capacitors, inductors, diodes, and switches count, are listed in Table 1. Moreover, the comparative analysis of the voltage conversion ratio and voltage stress on switch are sketched in Figure 7a,b, respectively. A topology presented in [6] has used one more component than the proposed converter but it cannot attain a high voltage gain as at 90% duty cycle its voltage conversion ratio is 18 and its switch also suffers from high voltage stress. A topology presented in [8] attains a high conversion ratio (i.e., at 90% duty the conversion ratio is 27) as compared to [6] but low compared to the proposed topology, despite it using one more inductor. However, the voltage stress across the switch is lower compared to the proposed converter. A converter proposed in [22] attains a low voltage conversion ratio and a switch suffers from a very high voltage stress. Moreover, the topologies proposed in [23–25] attain a high voltage gain compared to the proposed one, i.e., at 90% duty cycle they all attain a voltage gain of 37, while the proposed converter attains a conversion ratio of 36.1. However, these topologies have used more components and the switch suffers from high voltage stress. The topology in [26] has low component count and voltage stress on a switch compared to the proposed converter but it is unable to attain a high voltage conversion ratio. From the above discussion and from Figure 7a,b, it can be observed that most of the topologies have low voltage conversion ratio and high voltage stress on a switch as compared to the proposed topology.

Table 1. Comparative analysis of proposed converter with other converters.

Topology	Switches	Diodes	Inductors	Capacitors	Passive	Total	Voltage Gain	Voltage Stress on Switch
Cuk, SEPIC, Zeta	1	1	2	2	4	6	$\frac{D}{1-D}$	$\frac{1}{1-D}$
[6]	1	7	4	2	6	14	$\frac{2D}{1-D}$	$\frac{1+D}{1-D}$
[8]	1	3	4	6	10	14	$\frac{3D}{1-D}$	$\frac{1}{1-D}$
[22]	2	5	3	4	7	14	$\frac{3D-D^2}{1-D}$	$\frac{3-D}{1-D}$
[23]	2	7	4	1	5	14	$\frac{1+3D}{1-D}$	$\frac{D}{1-D}$
[24]	1	8	4	3	7	16	$\frac{1+3D}{1-D}$	$\frac{1+D}{1-D}$
[25]	2	4	4	6	10	16	$\frac{1+3D}{1-D}$	$\frac{1+D}{1-D}$
[26]	1	3	3	5	8	12	$\frac{3D}{1-D}$	$\frac{D}{1-D}+1$
Proposed	1	6	3	3	6	13	$\frac{(1+D)^2}{1-D}$	$\frac{1+D}{1-D}$

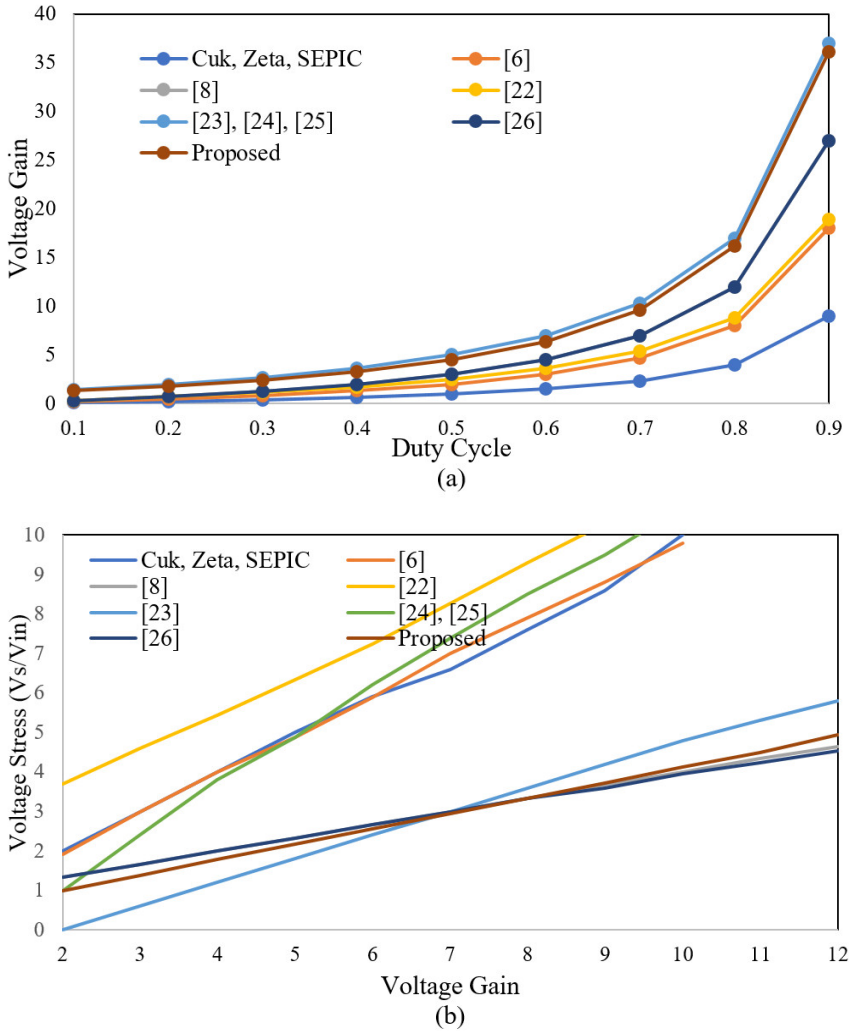

Figure 7. Comparative analysis of proposed converter with other topologies (**a**) voltage conversion ratio and (**b**) voltage stress on a switch.

3. Inverter Controller Design

A 2nd stage of the PV configuration system consists of DC–AC inverter, LCL filter, and a grid as shown in Figure 1. The most important part in the 2nd stage is the control of the inverter that is implemented in the form of two cascaded loops, i.e., inner and outer loop. In the proposed model, the dual loop control architecture is implemented using a stationary reference frame ($\alpha\beta$), as presented in Figure 8 [27]. The voltages and currents are transformed from abc frame to $\alpha\beta$ frame as:

$$\begin{bmatrix} U_\alpha \\ U_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} \tag{32}$$

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{33}$$

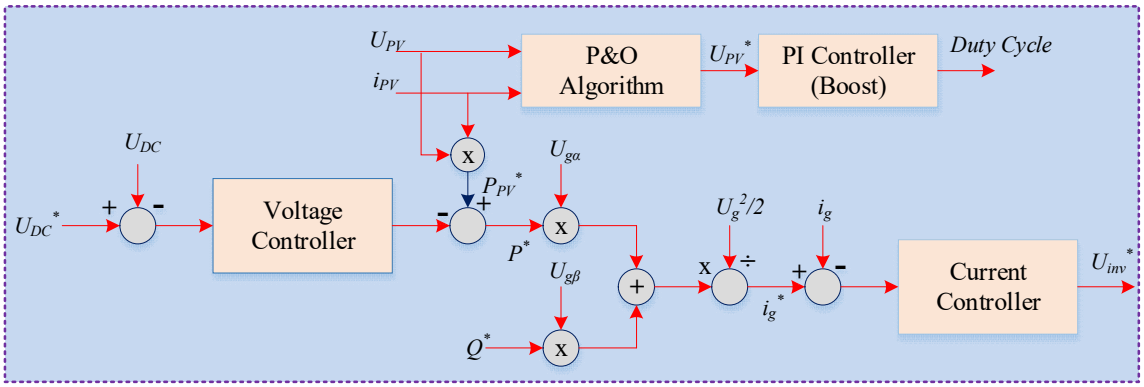

Figure 8. Feed-forward control structure of PV inverter.

Initially, the measured DCL voltage is compared with the reference to generate an error. The error is then subjected to the voltage control block where different controllers such as PI, FOPI, API, and AFOPI are used for DCL regulation. A PR controller is implemented in the inner loop to generate the voltage reference. The desired voltage generated by the current controller has transformed again to abc reference frame, which is used to generate the PWM for the inverter.

3.1. DC-Link Voltage Regulation

In this research, BP algorithm-based API and AFOPI controllers are designed that dynamically update the control parameters in case of any disturbance or uncertainty and maintain a constant voltage at DCL. These controllers are discussed below in this section.

3.1.1. Adaptive PI Controller

To regulate a DCL voltage, a PI controller according to [10] is given as:

$$U_{CDC}^*/i_g^* = k_p e(t) + k_i \int e(t)\, dt \tag{34}$$

where $U_{DC}{}^*/i_g{}^*$ is the controller output, e (error) is the controller input and is defined as $e = U_{CDC}{}^* - U_{CDC}$, k_p is the proportional gain, and k_i is the integral gain. From (34), it can be observed that the values of k_p and k_i are fixed and unable to change in case of parametric variations. Therefore, the performance of the PV system will be greatly affected. To tackle the above discussed problems, in this research work, a Back Propagation (BP) algorithm-based API is designed [28]. A BP optimization technique uses a gradient descent function as it measures all the changes in weights according to change in error and is defined as,

$$J = \frac{1}{2}e^2 \tag{35}$$

The gain of BP algorithm is given as,

$$k_{new} = -\gamma e x \tag{36}$$

where $k_{new} \in \{k_{p\text{-}new}, k_{i\text{-}new}\}$, γ presents the learning rate, and x is the input parameter of k. The BP algorithm is used to improve the transient response and minimize the error. The learning procedure and updated parameters are defined as,

$$k_{p-new} = -\gamma e x_1 \quad and \quad k_{i-new} = -\gamma e x_2. \tag{37}$$

where x_1 and x_2 are the input parameter for $k_{p\text{-}new}$ and $k_{i\text{-}new}$, respectively. The anticipated updated values of $k_{p\text{-}UP}$ and $k_{i\text{-}UP}$ can be calculated as,

$$k_{p-UP} = k_p + K_{p-new} = k_p - \gamma e x_1 \tag{38}$$

$$k_{i-UP} = k_i + K_{i-new} = k_i - \gamma e x_2 \tag{39}$$

The updated values of $k_{p\text{-}UP}$ and $k_{i\text{-}UP}$ enable the DC-link voltage to return to the condition where the steady state error is almost zero. Hence, the API controller can be defined as,

$$U^*_{DC}/i^*_g = k_{p-UP}e(t) + k_{i-UP}\int e(t)\,dt \tag{40}$$

Using (38) and (39) in (40), we produce the API controller as,

$$U^*_{DC}/i^*_g = \left[k_p - \gamma x_1 e^2(t)dt\right] + \left[k_i - \gamma e x_2 \int e(t)\,dt\right] \tag{41}$$

3.1.2. Adaptive FOPI Controller

To regulate a DCL voltage, an FOPI controller used in [11] is given as:

$$U^*_{DC}/i^*_g = k_p e(t) + k_i D_t^{-\lambda}\int e(t)\,dt \tag{42}$$

whereas λ is any arbitrary real number. Compared to PI controller, in FOPI controller, three parameters (k_p, k_i, and λ) are required to be designed. Thus, this modification increases the system flexibility and accuracy. However, the issue of fixed parameters of the FOPI persists, therefore, the FOPI controller is made adaptive according to the procedure discussed for API controller (see Section 3.1.1). Thus, the AFOPI controller is given as,

$$U^*_{DC}/i^*_g = \left[k_p - \gamma x_1 e^2(t)dt\right] + \left[k_i - \gamma e x_2 D_t^{-\lambda}\int e(t)\,dt\right] \tag{43}$$

3.2. Current Controller

A simplified diagram of PR controller presented in Figure 9 consists of proportional gain (k_p) that is added to the resonant path. The resonant path comprises of a resonant gain (k_{ir}) and a filter whose transfer function (TF) in z-domain is presented by H_r (z). A proportional gain is given as,

$$k_p = \frac{(\gamma)\sqrt{(\gamma)}\omega_r(L_i + L_g) - (R_i + R_g)}{U_{dc}/2} \tag{44}$$

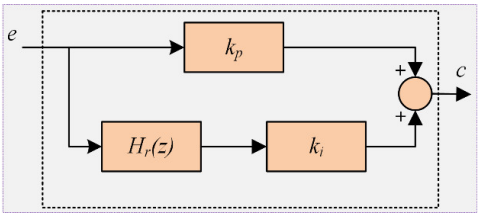

Figure 9. Block diagram of PR controller with single resonant path.

Comparatively, $\gamma = 2\xi + 1$ and ξ is the damping factor and its value lies in the range of 0.9–1.0. L_i and R_i are the inverter side inductance and resistance of LCL filter, while the grid side incidence and resistance of an LCL filter are presented by L_g and R_g, respectively. U_{CDC} describes the DC-link voltage and ω_r represents the resonant angular frequency and $\omega_r = 2 \times \pi \times f_r$, where f_r presents the resonant frequency. Moreover, ω_r must be equal to f_g because the controller acts in fundamental frequency for the accurate injection of active power in the grid. The value of k_{ir} and TF of resonant filter can be calculated as,

$$k_{ir} = \frac{{\omega_r}^2(L_i + L_g)(\gamma^2 - 1)}{U_{DC}} \tag{45}$$

$$H_r(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \tag{46}$$

where the coefficients of H_r (z) can be calculated from (47–52) according to [17,29] as,

$$b_0 = k_r B_r T_a \tag{47}$$

$$b_1 = \left[-k_r B_r e^{-0.5BrTa} \mathrm{Cos}\left(T_a \sqrt{{\omega_r}^2 - 0.25{B_r}^2}\right) - C\right] T_a \tag{48}$$

$$b_2 = 0 \tag{49}$$

$$a_0 = 1 \tag{50}$$

$$a_1 = -2e^{-0.5B_r T_a} \cos\left(T_a \sqrt{{\omega_r}^2 - 0.25{B_r}^2}\right) \tag{51}$$

$$a_2 = e^{-B_r T_a} \tag{52}$$

where k_r is the resonant gain, $B_r = 2\pi Bs$ is the resonant angular bandwidth, T_a is the sampling period, and C is constant defined in (53) as,

$$C = \frac{0.5 k_r {B_r}^2}{\sqrt{{\omega_r}^2 - 0.25{B_r}^2}} e^{-0.5B_r T_a} \sin\left(T_a \sqrt{{\omega_r}^2 - 0.25{B_r}^2}\right) \tag{53}$$

The transfer function of the controller presented in (46) is simulated in MATLAB environment to check its stability by considering the parameters values presented in Table 2. The magnitude and phase response of the resonant filter are shown in Figure 10a. The efficiency and accurate performance of the filter can be observed that at only 60 Hz the gain turns to 0 dB. It means that only the elements at 60 Hz are multiplied by 01 while all other components are attenuated significantly and cannot pass through the filter. Moreover, a phase shift of 180° is observed at the resonant frequency due to the placement of poles of TF. Similarly, the magnitude and phase response of the proposed PR controller is presented in Figure 10b. Unlike the resonant filter, the highest amplification occurs at 60 Hz and is equal to 47.4 dB. Moreover, similar to the filter response, a phase shift of 180° is also observed at 60 Hz. The overall procedure of designing a proposed controller can be summarized in Figure 11.

Table 2. Parameters value of PV system.

Parameter	Value
Grid Voltage (U_g)	230 V rms
Grid frequency (f_g)	60 Hz
Converter-side inductor (L_i)	1.74×10^{-4} H
Converter-side resistance (R_i)	0.01 ohm
Grid-side inductor (L_g)	1.2×10^{-3} H
Grid-side resistance (R_g)	0.01 ohm
LCL capacitance (C_f)	3.31×10^{-5} F
LCL damping resistance (R_d)	20.5 ohm
DC-link voltage (U_{DC})	700 V
Grid resistance (R_s)	2 ohm
Grid inductance (L_s)	3×10^{-3} H
Switching frequency (f_{sw})	10×10^{-3} Hz
Sampling frequency (f_a)	$1/1 \times 10^{-6}$ Hz
Sampling period (T_a)	1×10^{-6} s
Resonant frequency (f_r)	60, 300 Hz
Resonant frequency bandwidth (B_s)	1.5
Resonant angular bandwidth (B_r)	$B_r = 2\pi B_s$
Resonant gain (k_r)	1
Damping factor (ζ)	0.95

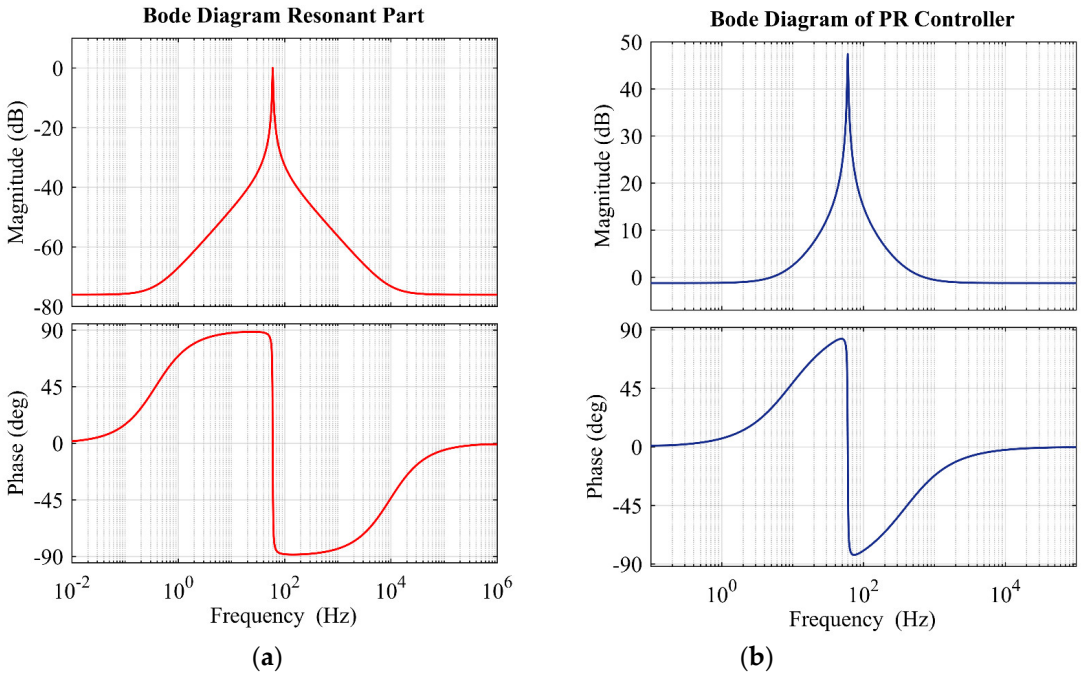

Figure 10. Bode diagram of (**a**) resonant filter and (**b**) current controller.

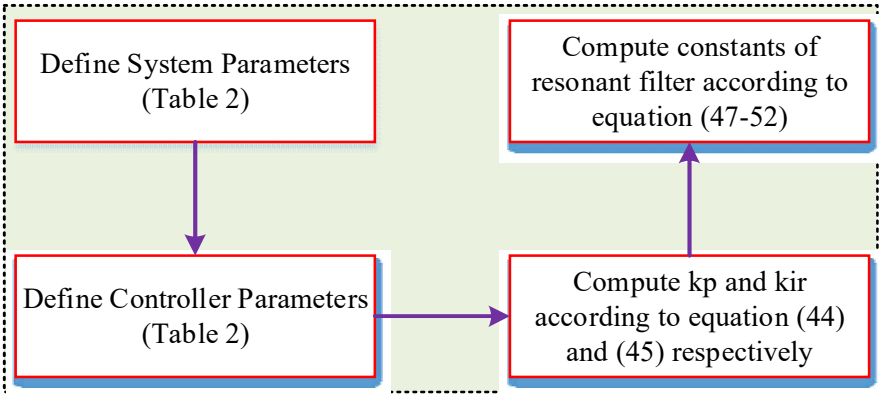

Figure 11. Design procedure of PR controller.

4. Results and Discussion

To validate the effectiveness of theoretical and analytical concepts of the proposed system, it is simulated in MATLAB and Simulink software. In this section, the results of the proposed system are discussed for two parts. In the first part, the simulation results of the proposed DC–DC converter are carried out while in the second part the simulation results of the whole PV system are conducted and discussed.

4.1. Simulation Results of DC–DC Converter

To validate the effectiveness and the theoretical analysis of the proposed DC–DC converter presented in Section 2, the converter is simulated according to the components' values presented in Table 3 (note that the Table 3 values are only limited to Section 4.1). In this simulation, the PV system is considered as an independent DC voltage source that generates a DC voltage of 70 V as presented in Figure 12a. The duty cycle of the switch is set to 71% as depicted in Figure 12b, so that the converter can attain a voltage conversion ratio of 10 and a voltage of 700 V is achieved at the output port, as the output voltage is equal to the sum of voltages across C_1 and C_2, according to Equation (1). From Figure 12c, it can be observed that a 297 V and 408 V appeared across C_1 and C_2 according to Equations (3)

and (5), respectively, which creates a total of 705 V at the output as shown in Figure 12d. The switching voltage on the semiconductor devices such as U_S, U_{D4}, and U_{D6} is equal to 408 V as presented in Figure 12e,f, which satisfies the calculated values in Equation (7). In a similar manner, a switching voltage across D_1, D_3, D_2, and D_5 are presented in Figure 12g–i, respectively. From these results, it can be concluded that the proposed converter attains a high voltage gain with low duty cycle and with reduced voltage stress on diodes and the switch.

Table 3. Component values of DC–DC converter.

Components	Values
Input Voltage	70 V
Output Voltage	705 V
Inductors (L_1 and L_2)	205×10^{-6} H
Inductor (L_3)	180×10^{-6} H
Capacitors (C_1 and C_2)	2.2×10^{-6} F
Capacitor (C_{DC})	450×10^{-6} F
Duty Cycle	71%
Switching Frequency	24 kHz
Load Resistance	100 Ω

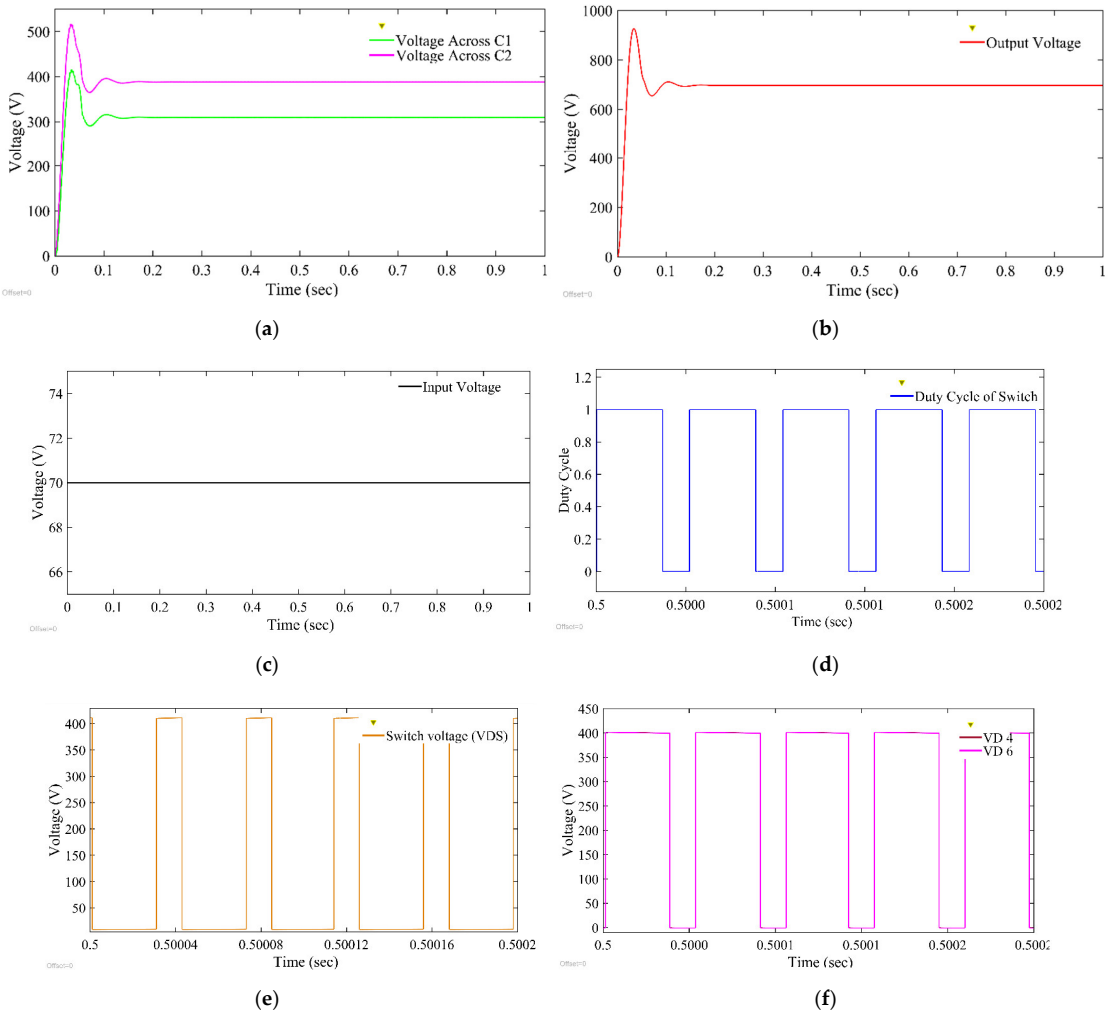

Figure 12. *Cont.*

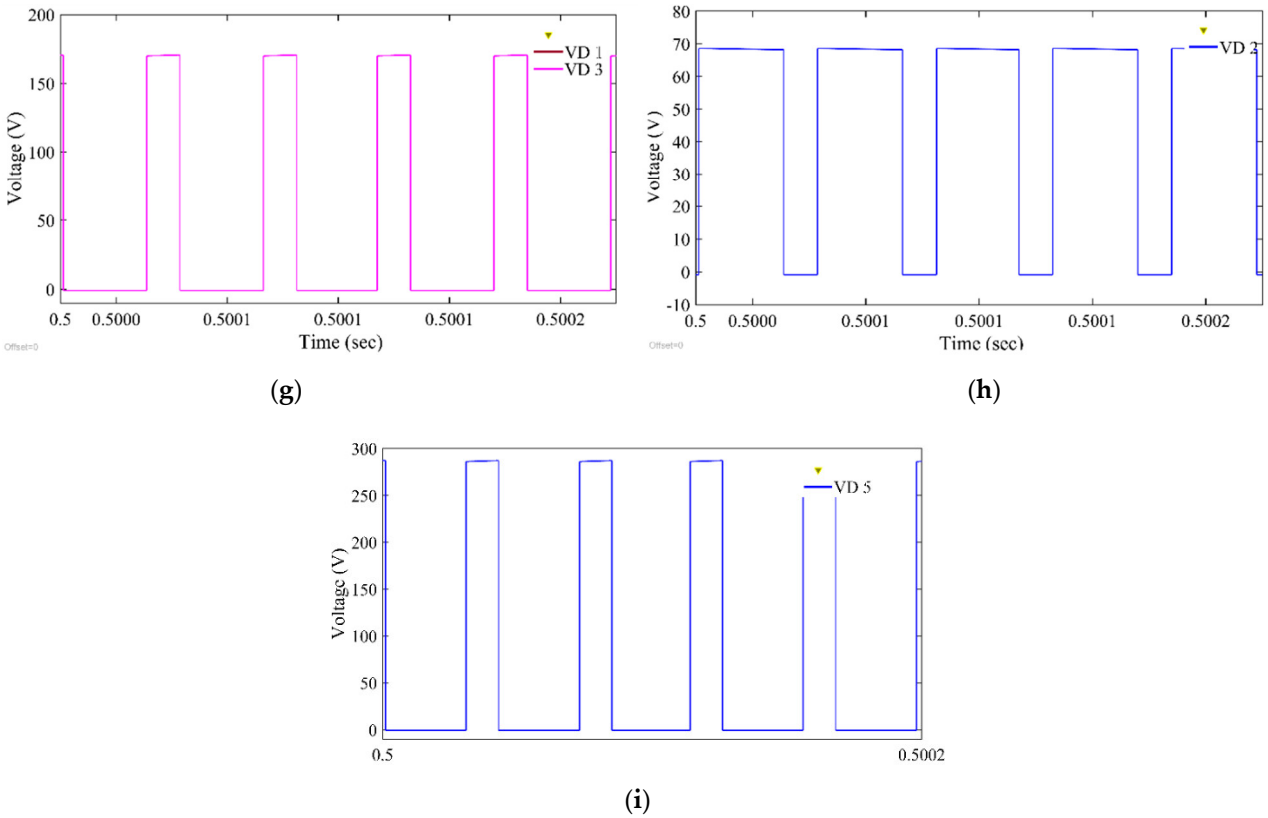

Figure 12. Simulation results of DC–DC converter (**a**) input voltage, (**b**) duty cycle of switch, (**c**) voltage across C_1 and C_2, (**d**) output voltage, (**e**) voltage across S, (**f**) voltage across D_4 and D_6, (**g**) voltage across D_1 and D_3, (**h**) voltage across D_2, and (**i**) voltage across D_5.

4.2. Simulation Results of Overall PV System

To validate the theoretical concepts of the proposed DC–DC converter along with the dual control loops, a PV system is simulated in MATLAB and Simulink software according to the feed-forward control architecture presented in Figure 8. The simulation is prepared according to the parameters listed in Table 3. Figure 13a shows the temperature and irradiance (T&G) of the PV panel. At the start of the simulation, the values of T&G are kept at 800 W/m^2 and 25 °C. At time 1.0 s, the system is subjected to disturbance (due to the intermittent nature of the PV system) and the values of T&G change to 600 W/m^2 and 30 °C. Similarly, at t = 2 s, the T&G values change again to 1000 W/m^2 and 20 °C. To extract the maximum power from the PV array, a P&O technique is used, and the PV output voltage, current, and power according to these changes are presented in Figure 13b–d, respectively. From Figure 13b, it can be observed that the PV output voltage is very low and varies according to environmental conditions and cannot be used as an input for the inverter.

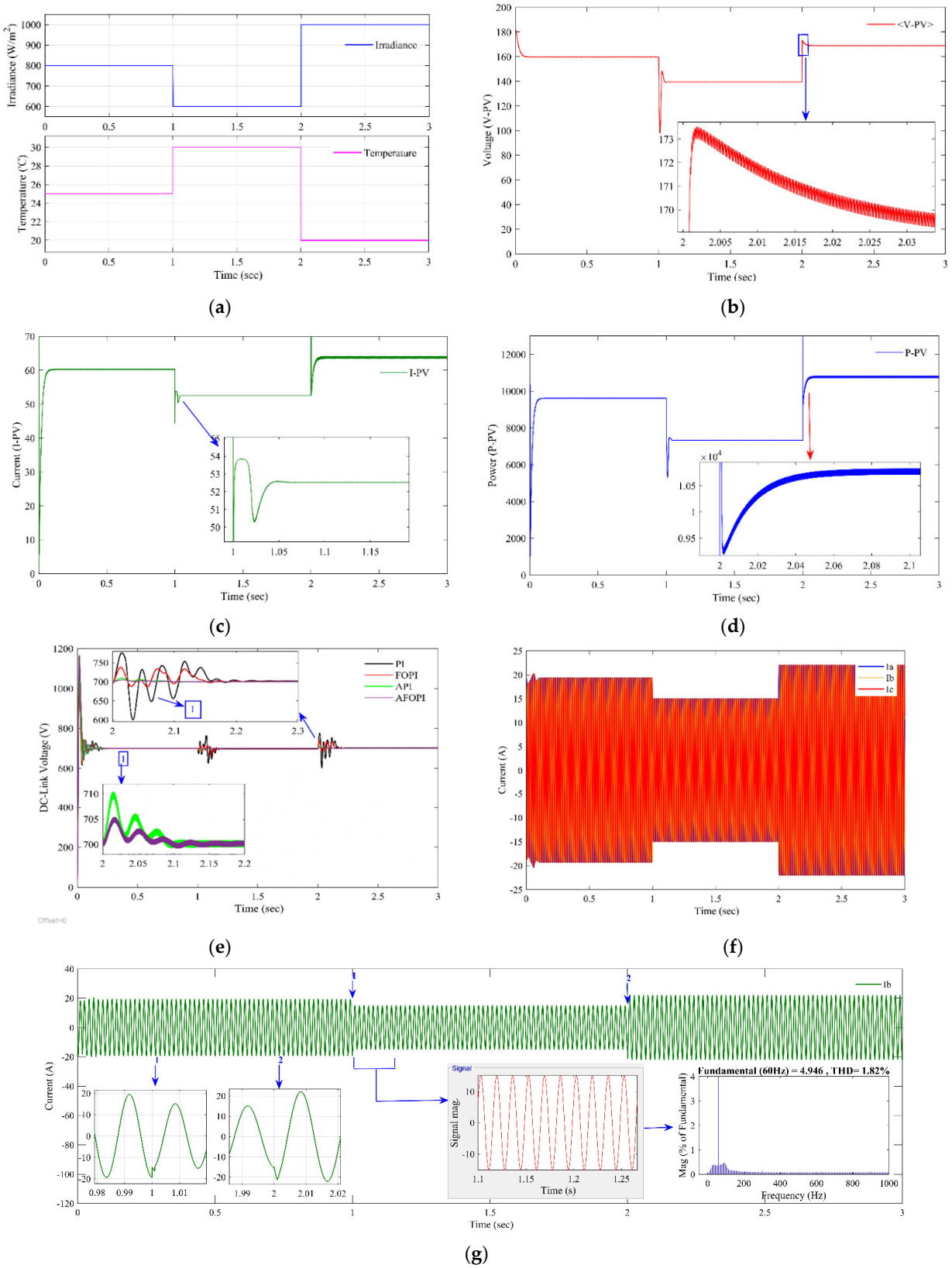

Figure 13. Simulation results of (**a**) PV panel irradiance and temperature, (**b**) PV panel voltage, (**c**) PV panel current, (**d**) PV panel power, (**e**) DC-link voltage using PI, FOPI, API, and AFOPI, (**f**) 3Φ grid injected current, and (**g**) 1Φ (i_b) grid injected current with THD analysis.

Therefore, this low generated PV voltage is amplified by using a proposed high gain DC–DC converter. However, to maintain a constant DC-link voltage, this amplified voltage needed to be regulated. For this purpose, PI, FOPI, API, and AFOPI controllers are used and their comparative performances are presented in Figure 13e while the values of the controllers gain are listed in Table A2. From the zoom-in view, it can be observed that the conventional PI controller has the worst performance in terms of tracking accuracy and dynamic response and is then followed by the FOPI controller. Both these controllers have fixed parameters that need to be updated according to the disturbances, therefore, the proposed API and AFOPI controllers are developed. It can be seen that both the proposed controllers have considerably improved the tracking accuracy, dynamic response, and eliminated the zero steady-state error. At t = 2 s, the spike in the VDC reaches approximately to 780V (PI), 740V (FOPI), 710V (API), and 705V (AFOPI). Moreover, the PI and FOPI controllers take almost 0.2 s, while API and AFOPI controller takes 0.1 s to reach its steady-state condition. Hence, the proposed API and AFOPI controllers are fast, less sensitive to disturbance, and more robust compared to the conventional PI and FOPI.

For better understanding and clarity, the grid injected current waveforms are presented in a case when an AFOPI controller is applied in the outer voltage loop. The 3Φ grid injected current for the varying climatic conditions is presented in Figure 13f whereas a single-phase current (i_b) is presented in Figure 13g. According to Figure 13a, the variation in T&G occurs at every 1 s accordingly. If we examine the zoom-in view of Figure 13g, the current controller acts accordingly and tracks its reference rapidly with zero steady-state error. Moreover, to analyze the total harmonic distortion, a current waveform starting from 1.1 s to almost 10 cycles is also presented in Figure 13g. It can be examined that the proposed PR controller results in only 1.82% of THD and efficiently removes the harmonic contents. The simulation results guaranteed the smooth and stable performance of the proposed system.

5. Conclusions

In this research work, a single switch non-isolated hybrid DC–DC converter is proposed. It attains a high voltage conversion ratio without the use of a transformer or extreme high duty cycle. The usage of a single switch makes its control simple hence the cost is considerably reduced. Moreover, due to hybrid structure and low voltage stress on semiconductor components, a proposed converter attains high efficiency compared to classical converters at high duty cycle. The operating principle, steady-state and comparative analysis of the proposed converter are also discussed. From the comparative analysis and simulation results, it is concluded that the proposed converter attains a high step-up conversion ratio with a low duty cycle, and reduced component count.

In the 2nd stage of the PV system, API and AFOPI controllers are employed in the outer voltage control loop to regulate the DC-link voltage in case of PV intermittency. Compared to the conventional PI and FOPI (having fixed parameters), the proposed controllers ensure (a) high tracking accuracy and efficiency, (b) fast dynamic response, (c) reduction in steady-state error, (d) reduced fluctuation in DC-link voltage during the transient state, and (e) less sensitivity to sudden disturbances. Furthermore, a PR controller is used in the inner control loop. In the proposed PR controller, there is a unique equation for every parameter, hence no parameter is computed empirically or by a trial-and-error method such as a conventional PR controller. The Bode diagram of the controller is plotted according to pre-indicated desired parameters. From the result, it is concluded that the controller accurately follows its reference with zero steady-state error, unpredictable behavior, and results in high-quality grid injected current.

Author Contributions: Conceptualization, supervision, and project administration, H.L.; writing—original draft and methodology, M.Y.A.K.; methodology, investigation, writing—review and editing, software, and formal analysis, S.H.; software, investigation, resources, and visualization, D.K. and X.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data is contained within the article.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Table A1. PV panel specifications at (1000 kW/m^2, 25 °C).

Parameter	Symbol	Value
Voltage at MPP	V_{MPP}	29.9 V
Current at MPP	I_{MPP}	7.65 A
Nominal power	P_{MPP}	228 W
Open circuit voltage	U_{OC}	37.1 V
Short circuit current	I_{SC}	8.18 A

Table A2. Controllers Gains.

Controller	Parameter	Value
	Controller of Boost Converter	
PI	k_p	0.01
	k_i	0.5
	DC-Link Voltage Controller	
PI	k_p	32
	k_i	210
FOPI	k_p	17
	k_i	105
	λ	0.715
API	k_p	8
	k_i	23
	γ	400
AFOPI	k_p	18
	k_i	145
	λ	0.545
	γ	230
	Current Controller	
PR	K_p	7.074702865475842
	K_i	5.716971169217982
	a_0	1
	a_1	−1.999990433144820
	a_2	0.999990575266452
	b_0	$9.424777960769379 \times 10^{-6}$
	b_1	$-9.424777291035913 \times 10^{-6}$
	b_2	0
	C	$4.441300946117881 \times 10^{-5}$

References

1. Khan, M.Y.A.; Liu, H.; Rehman, N.U. Design of a Multiport Bidirectional DC–DC Converter for Low Power PV Applications. In Proceedings of the 2021 International Conference on Emerging Power Technologies (ICEPT), Topi, Pakistan, 10–11 April 2021; pp. 1–6.
2. Ali Khan, M.Y.; Liu, H.; Yang, Z.; Yuan, X. A Comprehensive Review on Grid Connected Photovoltaic Inverters, Their Modulation Techniques, and Control Strategies. *Energies* **2020**, *13*, 4185. [CrossRef]
3. Das, M.; Pal, M.; Agarwal, V. Novel high gain, high efficiency dc–dc converter suitable for solar PV module integration with three-phase grid tied inverters. *IEEE J. Photovolt.* **2019**, *9*, 528–537. [CrossRef]
4. Habib, S.; Khan, M.M.; Abbas, F.; Ali, A.; Faiz, M.T.; Ehsan, F.; Tang, H. Contemporary trends in power electronics converters for charging solutions of electric vehicles. *CSEE J. Power Energy Syst.* **2020**, *6*, 911–929.

5. Pop-Calimanu, I.-M.; Lica, S.; Popescu, S.; Lascu, D.; Lie, I.; Mirsu, R. A new hybrid inductor-based boost DC–DC converter suitable for applications in photovoltaic systems. *Energies* **2019**, *12*, 252. [CrossRef]
6. Sanjeevikumar, P.; Bhaskar, M.S.; Dhond, P.; Blaabjerg, F.; Pecht, M. Non-isolated sextuple output hybrid triad converter configurations for high step-up renewable energy applications. In *Advances in Power Systems and Energy Management*; Springer: Berlin/Heidelberg, Germany, 2018; pp. 1–12.
7. Almalaq, Y.; Matin, M. Two-Switch High Gain Non-Isolated Cuk Converter. *Eng. Technol. Appl. Sci. Res.* **2020**, *10*, 6362–6367. [CrossRef]
8. Banaei, M.R.; Sani, S.G. Analysis and implementation of a new SEPIC-based single-switch buck–boost DC–DC converter with continuous input current. *IEEE Trans. Power Electron.* **2018**, *33*, 10317–10325. [CrossRef]
9. Zhang, G.; Iu, H.H.-C.; Zhang, B.; Li, Z.; Fernando, T.; Chen, S.-Z.; Zhang, Y. An impedance network boost converter with a high-voltage gain. *IEEE Trans. Power Electron.* **2017**, *32*, 6661–6665. [CrossRef]
10. Ma, M.; Liu, X.; Lee, K.Y. Maximum Power Point Tracking and Voltage Regulation of Two-Stage Grid-Tied PV System Based on Model Predictive Control. *Energies* **2020**, *13*, 1304. [CrossRef]
11. Lakshmi, M.; Hemamalini, S. Decoupled control of grid connected photovoltaic system using fractional order controller. *Ain Shams Eng. J.* **2018**, *9*, 927–937. [CrossRef]
12. Asadi, M.; Ebrahimirad, H.; Mousavi, M.; Jalilian, A. Sliding mode control of DC-link capacitors voltages of a NPC 4-wire shunt active power filter with selective harmonic extraction method. In Proceedings of the 2016 7th Power Electronics and Drive Systems Technologies Conference (PEDSTC), Tehran, Iran, 16–18 February 2016; pp. 273–278.
13. Kumar, N.B.; Urundady, V. Sliding Mode Controller with Integral Action for DC-Link Voltage Control of Grid-Integrated Domestic Photovoltaic Systems. *Arab. J. Sci. Eng.* **2020**, *45*, 6583–6600. [CrossRef]
14. Zeb, K.; Islam, S.U.; Din, W.U.; Khan, I.; Ishfaq, M.; Busarello, T.D.C.; Ahmad, I.; Kim, H.J. Design of fuzzy-PI and fuzzy-sliding mode controllers for single-phase two-stages grid-connected transformerless photovoltaic inverter. *Electronics* **2019**, *8*, 520. [CrossRef]
15. Bielskis, E.; Baskys, A.; Valiulis, G. Controller for the grid-connected microinverter output current tracking. *Symmetry* **2020**, *12*, 112. [CrossRef]
16. Zhang, N.; Tang, H.; Yao, C. A systematic method for designing a PR controller and active damping of the LCL filter for single-phase grid-connected PV inverters. *Energies* **2014**, *7*, 3934–3954. [CrossRef]
17. Busarello, T.D.C.; Pomilio, J.A.; Simoes, M.G. Design procedure for a digital proportional-resonant current controller in a grid connected inverter. In Proceedings of the 2018 IEEE 4th Southern Power Electronics Conference (SPEC), Singapore, 10–13 December 2018; pp. 1–8.
18. Yagnik, U.P.; Solanki, M.D. Comparison of L, LC & LCL filter for grid connected converter. In Proceedings of the 2017 International Conference on Trends in Electronics and Informatics (ICEI), Tirunelveli, India, 11–12 May 2017; pp. 455–458.
19. Mao, M.; Cui, L.; Zhang, Q.; Guo, K.; Zhou, L.; Huang, H. Classification and summarization of solar photovoltaic MPPT techniques: A review based on traditional and intelligent control strategies. *Energy Rep.* **2020**, *6*, 1312–1327. [CrossRef]
20. Waly, H.M.; Osheba, D.S.; Azazi, H.Z.; El-Sabbe, A.E. Design and analysis of a proposed transformerless/non-isolated high- gain DC–DC converter for renewable energy applications. *Int. J. Electron.* **2020**, *107*, 1127–1145. [CrossRef]
21. Biricik, S.; Redif, S.; Khadem, S.K.; Basu, M. Improved harmonic suppression efficiency of single-phase APFs in distorted distribution systems. *Int. J. Electron.* **2016**, *103*, 232–246. [CrossRef]
22. Jiao, Y.; Luo, F.; Zhu, M. Voltage-lift-type switched-inductor cells for enhancing DC–DC boost ability: Principles and integrations in Luo converter. *IET Power Electron.* **2011**, *4*, 131–142. [CrossRef]
23. Tang, Y.; Fu, D.; Wang, T.; Xu, Z. Hybrid switched-inductor converters for high step-up conversion. *IEEE Trans. Ind. Electron.* **2014**, *62*, 1480–1490. [CrossRef]
24. Almalaq, Y.; Matin, M. Three topologies of a non-isolated high gain switched-inductor switched-capacitor step-up cuk converter for renewable energy applications. *Electronics* **2018**, *7*, 94. [CrossRef]
25. Sedaghati, F.; Azizkandi, M.E.; Majareh, S.H.L.; Shayeghi, H. A high-efficiency non-isolated high-gain interleaved DC–DC converter with reduced voltage stress on devices. In Proceedings of the 2019 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC), Shiraz, Iran, 12–14 February 2019; pp. 729–734.
26. Banaei, M.R.; Bonab, H.A.F. A novel structure for single-switch nonisolated transformerless buck–boost DC–DC converter. *IEEE Trans. Ind. Electron.* **2016**, *64*, 198–205. [CrossRef]
27. Zeb, K.; Nazir, M.S.; Ahmad, I.; Uddin, W.; Kim, H.-J. Control of Transformerless Inverter-Based Two-Stage Grid-Connected Photovoltaic System Using Adaptive-PI and Adaptive Sliding Mode Controllers. *Energies* **2021**, *14*, 2546. [CrossRef]
28. Haroon, Z.; Khan, B.; Farid, U.; Ali, S.; Mehmood, C. Switching control paradigms for adaptive cruise control system with stop-and-go scenario. *Arab. J. Sci. Eng.* **2019**, *44*, 2103–2113. [CrossRef]
29. Bacha, S.; Munteanu, I.; Bratcu, A.I. Linear Control Approaches for DC–AC and AC–DC Power Converters. In *Power Electronic Converters Modeling and Control*; Springer: Berlin/Heidelberg, Germany, 2014; pp. 237–296.