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An Input-Series-Output-Parallel Cascaded Converter System Applied to DC Microgrids

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Abstract: Direct current transformer (DCT) is a key piece of equipment in direct current (DC) microgrids, and the mainstream topologies mainly include LLC resonant converter (LCL) and dual active bridge (DAB). In this paper, a novel bi-directional buck/boost + CLLLC cascade topology is proposed for the input-series-output-parallel cascade converter system of a DC microgrid. To solve the problem that frequency variation causes the converter to deviate from the optimal operating point, resulting in low efficiency, and the inability to achieve a soft switching function. The CLLLC converter operates near the resonant frequency point as a DCT, only providing electrical isolation and voltage matching, while the buck/boost converter controls the output voltage and the voltage and current sharing of each module. Compared to other cascaded converter systems, the cascaded converter proposed in this paper has high efficiency, simplifies the parameter design, and is suitable for wide input and wide output operating conditions. The system adopts a three-loop control strategy, establishes the small-signal modeling of the system, and its stability is verified by theoretical analysis and simulation. The simulation and experimental results verify the correctness of the proposed cascaded converter based on buck/boost + CLLLC and the effectiveness of the control strategy.

Keywords: DC transformer; cascaded converter; CLLLC converter; buck/boost converter

1. Introduction

In recent years, with the development of power electronics technology, the technical problems faced by DC transmission and distribution have gradually been solved. With better compatibility with distributed renewable energy sources, higher efficiency, and higher system reliability, DC microgrids have a broad development prospect. Distributed renewable energy (DER) is connected to the microgrid through power electronic converters (PEC) [1]. This paper presents a comprehensive literature review of DC-DC converter topologies used in DC microgrids [2,3]. Due to the existence of a buck-to-back process inside the converter, it is inevitable to add more switch tubes and energy storage components. Due to the pursuit of power density in converters, high-frequency converters usually need to solve switching losses and other issues. Therefore, high-frequency switches must achieve soft switching, and DC/DC converters with soft switching characteristics are gradually receiving attention [4,5]. Converters with bi-directional energy flow topologies are numerous while the topologies that guarantee high efficiency are limited. Several topologies will be described below.

The most widely used is the DAB converter, which has been widely studied by scholars due to its ability to achieve bi-directional power flow and soft switching technology,
and its easy scalability. It has been applied in fields such as data centers, electric vehicles, and power electronic transformers. However, there are still some problems with current DAB converters, which usually only enable the soft switching of two switches at zero voltage over a narrow power range and are relatively complex to control [6–9].

The DC transformer with a DAB structure has the problem of current and voltage sharing, which requires additional circuit design to solve, increasing engineering costs and limiting its promotion in high-power range situations. However, traditional LLC resonant converters can only operate in a unidirectional power transmission state. Because of its asymmetric structure, there are differences in the resonant frequency and gain characteristics between the forward and reverse operation of the converter, which increases the complexity of converter parameter design and control [10,11].

The CLLLC resonant converter operates symmetrically in both forward and reverse directions, enabling bi-directional power transfer. Similar smooth switching characteristics to those of the CLLLC resonant converter can be achieved in bi-directional operation without the need for additional buffering auxiliary circuits [12,13].

Reference [14] introduces three DC/DC converter topologies suitable for high-power density and high-power applications. Ref. [15] introduces the average model of the ISOP DAB DC converter and analyzes the power distribution of its modular topology. Then, they propose an input-oriented fast dynamic response power-sharing control scheme to ensure the power-sharing ability and fast dynamic performance of DC converters. Ref. [16] proposes a wireless IVS control strategy for ISOP systems based on the positive output voltage gradient method, which can effectively improve the reliability and modularity of the ISOP system. Ref. [17] proposes a detailed design method for a bi-directional CLLLC resonant converter for an onboard charger (OBC), which can achieve a wide output voltage range. Ref. [18] presents a fully modular control strategy for input-series-output-parallel (ISOP) inverter systems. The proposed control strategy allows for a fully modular design without any interconnection of control signals between the constituent inverters, thus achieving superior modularity and reliability.

CLLLC best fits the resonant frequency point, and when the working frequency is not equal to the resonant frequency, there is an error between the theoretical analysis and the actual situation. In addition, when the operating frequency exceeds the resonant frequency, the converter cannot achieve the soft switching function, and the large range of frequency variations caused by large regulation is not conducive to the selection and efficiency of inductors, capacitors, and high-frequency transformers.

To solve these problems, this paper proposes a bi-directional buck/boost + CLLLC cascade structure [19,20]. By controlling the CLLLC converter to operate near the resonant frequency point, it exhibits the characteristics of a DC transformer, providing only electrical isolation and voltage matching, while the buck/boost converter controls the output voltage of each module. The system adopts a three-loop control strategy, and both the CLLLC converter and the buck/boost converter adopt dual closed-loop control. A voltage-sharing loop has been added to the buck/boost converter to achieve system input voltage sharing [21–24]. This design ensures the conversion efficiency of the resonant converter, as well as its good soft switching and dynamic characteristics. Compared to other topology structures mentioned, the advantages of a multi-converter combination system can be summarized: (1) reducing the power of submodules, facilitating device selection, and reducing costs. (2) The series-parallel structure of multiple converters facilitates system expansion and maintenance, while also improving system redundancy. Finally, the correctness and effectiveness of the parameter design and control method were verified through a 1 kW experimental prototype.
2. Converter Topology and System Structure

2.1. System Structure and Converter Topology

Figure 1 shows the topology of the DAB converter. Due to the presence of auxiliary inductor L, the DAB converter can achieve soft switching and zero voltage switching (ZVS) during operation, which also enables the efficiency of the DAB converter to reach over 97% in high-power applications [25,26].

Figure 2. LLC resonant converter topology.

In order to solve the problem of ZVS changing with load in DAB converters, LLC resonant converters have attracted widespread attention for their superior comprehensive performance. The LLC topology is shown in Figure 2. The LLC resonant converter has natural soft-switching characteristics and can achieve ZVS for the primary inverter switch tubes and ZCS for the secondary rectifier diodes over a wide range of input voltages and full loads, without an auxiliary network and with simple control.

Figure 3. CLLCC resonant converter topology.

In order to solve the problems of forward and reverse differences and the complex design of LLC converters, a CLLCC resonant converter topology is proposed, as shown in Figure 3.

Figure 4 shows the buck/boost converter topology. The buck-boost converter has the advantages of wide-range voltage conversion and bi-directional power transfer. It has
received wide attention from scholars at home and abroad in recent years and is used in DC microgrids [27–31].

![Synchronous switching topology.](image)

Figure 4. Synchronous switching topology.

Figure 5 shows the DC transformer composed of a bi-directional buck/boost + CLLLC cascade converter; this new topology input side is connected in series and the output side in parallel, wherein the buck/boost converter works in voltage regulation mode [32] and the CLLLC converter works near the resonant frequency, through parameter design to achieve the role of DCX. A modular multi-converter series-parallel combination structure has been proposed, which is characterized by not only the normal operation of a single converter module but also the ability to achieve voltage/current sharing between multiple standardized modules through bus connection, achieving a modular combination structure of the system. Compared to other topologies, it has higher efficiency and fast dynamic response, which is suitable for high-power DC microgrids.

![Schematic diagram of system structure and topology.](image)

Figure 5. Schematic diagram of system structure and topology.
2.2. Subsection Analysis of Cascaded Converter Model

In this paper, we first establish the independent mathematical model of each module converter separately to obtain the equivalent circuit model. By cascading the circuit models of each level, we obtain the equivalent circuit model of the cascaded converter system so that we can establish the mathematical model of the cascaded converter system based on this circuit model. According to the buck/boost converter mathematical model and the CLLLC converter mathematical model, the steady-state equivalent circuit diagram of the buck/boost + CLLLC converter cascaded system can be obtained, as shown in Figure 6.

![Steady-state equivalent circuit diagram of the buck/boost + CLLLC cascaded converter system.](image)

Figure 6. Steady-state equivalent circuit diagram of the buck/boost + CLLLC cascaded converter system.

According to the above equivalent circuit diagram, the DC voltage gain $M$ of the buck/boost + CLLLC cascaded converter is:

$$M = M_{BB} \cdot M_{CLLLC}$$  \hspace{1cm} (1)

The state space averaging model of the buck/boost converter is obtained by averaging the modes over one switching cycle:

$$\dot{X}_s = A_s X_s + B_s U_s$$ \hspace{1cm} (2)

where $R'$ is the buck/boost converter output impedance

$$A_s = \begin{bmatrix} -\frac{1}{C_1 R_1} & 0 & -\frac{1}{C_1} \\ 0 & -\frac{1}{C_2 R'} & 1-D \frac{1}{C_2} \\ 1 & -\frac{1}{L} & 0 \end{bmatrix}, \quad B_s = \begin{bmatrix} \frac{1}{C_1 R_1} & 0 \\ 0 & C_2 R' \\ 0 & 0 \end{bmatrix}$$

If $\dot{X}_s = 0$, a static solution can be obtained according to Equation (3):

$$X_{s0} = -A_s^{-1} B_s U_s$$ \hspace{1cm} (3)

If the static working point $X_{s0} = [V_{s1}, V_{s2}, I_1]^T$, therefore, the static operating point of the buck/boost converter is:

$$X_{s0} = $$ \hspace{1cm} (4)

where $V'$ is buck/boost converter output voltage.

Taking input variables $U_s = V'$, output variables $V_s = V_1$, the steady-state output voltage gain is:
\[ M_{BB} = \frac{V_s}{U_s} = \frac{(1-D)^2 RV_i + (1-D) RV'}{(1-D)RV_i + RV'} \] (5)

According to Figure 5, the input and output transfer functions of the CLLLC resonant converter are:

\[ H(j\omega) = \frac{u_{CD}}{u_{AB}} = \frac{Z_m(Z_2 + R_m)}{Z_2 + Z_m + (R_m)} \cdot \frac{R_{eq}}{R_{eq} + Z_2} \] (6)

\[
\begin{align*}
Z_1 &= j\omega L_1 + \frac{1}{j\omega C_3} \\
Z_2 &= j\omega L_2 + \frac{1}{j\omega C_4} \\
Z_m &= j\omega L_m \\
\omega &= 2\pi f
\end{align*}
\] (7)

Defining \( k = \frac{L_m}{L_1}, \ h = \frac{L_2}{L_1}, \ g = \frac{C_4}{C_1}, \ \omega_1 = 1/\sqrt{L_1 C_3}, \ \omega_2 = 1/\sqrt{L_2 C_4}, \ \omega_0 = \omega_1/\omega_2 \), and bring in simplification:

\[ H(j\omega) = \frac{k\omega C_1 R_m}{\left(\omega C_3 - \frac{1}{\omega L_1} + k\omega C_3\right) R_m + j\left(k\frac{\omega^2}{\omega_1} + kh\frac{\omega_0^2}{\omega_2} + h\frac{\omega_0^2}{\omega_1} - k\frac{1}{g} - h - \frac{1}{g} + \frac{1}{g}\right)} \] (8)

When the converter is operating at the resonant operating point, the imaginary part of the transfer function is zero, and the expression \( \omega_r \) of the resonant frequency containing the resonant network can be found in Equation (8):

\[ (k + h + kh)\omega_r^4 - \left(k + h + \frac{k}{g} + \frac{1}{g}\right)\omega_r^2 + \frac{1}{g\omega_1^2} = 0 \] (9)

Obtaining

\[ \omega_r = \sqrt{\frac{b + \sqrt{b^2 - 4ac}}{2a}} \omega_1 \] (10)

Among

\[
\begin{align*}
a &= k + h + kh \\
b &= k + h + k/g + 1/g \\
c &= 1/g
\end{align*}
\] (11)

Defining the normalized frequency, the characteristic impedance of the resonant network, the system figure of merit, and in Equation (8), the reduced transfer function is:

\[ H_t(j\omega_n) = \frac{1}{\frac{Q}{k}(k + h + kh)\omega_n - \left(k + h + \frac{k}{g} + \frac{1}{g}\right)\omega_n + \frac{1}{g\omega_0^2} + \left(1 + \frac{1}{k} - \frac{1}{k\omega_0^2}\right)} \] (12)

The voltage gain of the CLLLC resonant converter is then obtained:
\[ M_{CLLC} = \frac{1}{\frac{1}{g-h} h} \]  

(13)

When the tube is operating at resonance, Equation (11) is substituted into (13), and the converter gain in the quasi-resonant operating state is:

\[ M_{CLLC} = \frac{1}{1 + \frac{1}{g-h} h} \]  

(14)

Substituting Equations (5) and (14) into Equation (1) to find the dc voltage gain of the buck/boost + CLLLC cascaded converter is:

\[ G = \frac{h(1-D)^2 R V' + h(1-D) R V'}{[(1-D) R V' + R V'] \left[ 1 + \frac{1}{g-h} \right]} \]  

(15)

According to the equivalent circuit diagram shown in Figure 5, the input-output transfer function \( G \) of the buck/boost + CLLLC cascaded converter is:

\[ G = H (j \omega) \cdot G_m \]  

(16)

At the static working point \( (X_s, U_s, D) \), introduction of low-frequency small signals disturbances \( \hat{d} \), \( \hat{u} \). The small-signal model of the buck/boost converter is obtained by neglecting the small-signal disturbances of the second order and above.

\[
\begin{bmatrix}
\dot{x}_1 \\
\dot{x}_2 \\
\dot{x}_3
\end{bmatrix} =
\begin{bmatrix}
\frac{1}{C_1 R_1} & 0 & \frac{1}{C_1} \\
0 & \frac{1}{C_2 R'} & 1-D \\
\frac{1}{L} & \frac{1}{1-D} & 0
\end{bmatrix}
\begin{bmatrix}
\dot{x}_1 \\
\dot{x}_2 \\
\dot{x}_3
\end{bmatrix}
+ \begin{bmatrix}
\frac{1}{C_1 R_1} & 0 \\
0 & \frac{1}{C_2 R'} & 0 \\
\frac{1}{L} & \frac{1}{C_2} & 0
\end{bmatrix}
\begin{bmatrix}
\hat{u}_1 \\
\hat{v}_2 \\
\hat{i}_L
\end{bmatrix} + \begin{bmatrix}
0 \\
0 \\
V_d
\end{bmatrix} \hat{d}_s
\]  

(17)

Among \( \hat{x}_s = [\hat{v}_1 \hat{v}_2 \hat{i}_L]^T \), \( \hat{u}_s = [\hat{v}_1 \hat{v}_2]^T \).

Status variables \( x_s \) and input variables \( u \), the transfer function is:

\[
G_{ss} = \begin{bmatrix}
\dot{x}_s(s) \\
\hat{u}_s(s)
\end{bmatrix} = (sI - A_s)^{-1} B_s =
\begin{bmatrix}
\frac{R'LC_s s^2 + L s + (1-D)^2 R'}{P(s)} \\
\frac{R'(1-D)}{P(s)} \\
\frac{R'C_s s + 1}{P(s)}
\end{bmatrix}
\]  

(18)

Among

\[ P(s) = LC_s R s^3 + L(C_s R_s + C_R s^2 + L + (C_s + C_R)(1-D)^2 R R')s + R_s + (1-D)^2 R' \]  

(19)

Substituting Equations (6) and (18) into Equation (16) gives the input-output transfer function \( G \) of the buck/boost + CLLLC cascaded converter as:


$$G = \frac{R_m \left[ \frac{Z_m}{Z_m + R_m} \right]}{Z_m + \frac{1}{Z_m + R_m}} \begin{bmatrix} \frac{R'LC_s s^2 + Ls + (1-D)s}{P(s)} & \frac{R(1-D)}{P(s)} \\ \frac{R'(1-D)}{P(s)} & \frac{R'LC_s s^2 + Ls + R_C}{P(s)} \\ \frac{R'C_C s + 1}{P(s)} & \frac{(R_C s + 1) (D-1)}{P(s)} \end{bmatrix}$$ (20)

3. Parametric Design

In order to make the ISOP system automatically achieve intermediate bus voltage equalization, the key is to ensure that the CLLLC converter presents DC transformer characteristics, and the converter parameters are designed based on this requirement. The resonant converter resonant network gain is approximately equal to 1, so the transformer transformation ratio is 1.5. The switch tube used in the CLLLC converter experiment is FGH40N60SFD, and its junction capacitance size is 2.3 nF. The maximum excitation inductance can be calculated to be 187 µH. In order to reduce the volume of the converter and reduce the influence of stray parameters on the resonant network, the transformer-integrated leakage inductance is used as the resonant inductance in the resonant network, and the leakage inductance affects the design of the transformer, so the k value is selected as 15, the excitation inductance $L_m$ is 172 µH, and the resonant inductance $L_1$ is 11.53 µH. Since the converter is designed to work at the resonance point, the resonant capacitance of 220 nF can be found according to the resonant inductance sought. According to the original secondary side, resonance parameters should be equivalent and equal, and the secondary side resonance parameters can be obtained. In summary, the parameter design of the system converter is shown in Table 1.

<table>
<thead>
<tr>
<th>Transformer Name</th>
<th>Parameter Name</th>
<th>Numerical</th>
</tr>
</thead>
<tbody>
<tr>
<td>Buck/boost</td>
<td>High-side voltage $V_1$</td>
<td>134 V</td>
</tr>
<tr>
<td></td>
<td>Low-side voltage $V_2$</td>
<td>72 V</td>
</tr>
<tr>
<td></td>
<td>Rated power $P_1$</td>
<td>500 W</td>
</tr>
<tr>
<td></td>
<td>Switching frequency $f_{s1}$</td>
<td>20 kHz</td>
</tr>
<tr>
<td></td>
<td>Energy storage inductors $L/mH$</td>
<td>0.6</td>
</tr>
<tr>
<td></td>
<td>Input capacitor $C_{1/\mu F}$</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td>Output capacitor $C_{2/\mu F}$</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td>Inductor current ripple $\Delta i_L$</td>
<td>&lt;20%</td>
</tr>
<tr>
<td></td>
<td>Output voltage ripple $\Delta V$</td>
<td>&lt;5%</td>
</tr>
<tr>
<td>CLLLC</td>
<td>High voltage $V_3$</td>
<td>72 V</td>
</tr>
<tr>
<td></td>
<td>Low voltage $V_4$</td>
<td>48 V</td>
</tr>
<tr>
<td></td>
<td>Rated power $P_2$</td>
<td>500 W</td>
</tr>
<tr>
<td></td>
<td>Switching frequency $f_{s2}$</td>
<td>100 kHz</td>
</tr>
<tr>
<td></td>
<td>Resonant inductance $L_1, L_2/\mu H$</td>
<td>11.53, 5.12</td>
</tr>
<tr>
<td></td>
<td>Resonant capacitors $C_3, C_4/nF$</td>
<td>220,560</td>
</tr>
<tr>
<td></td>
<td>Excitation inductance $L_m/\mu H$</td>
<td>172</td>
</tr>
</tbody>
</table>

As the converter operates in buck mode, the output voltage is $V_1$ on the low voltage side, so at this point let

$$\hat{v}_2(s) = 0$$ (21)

The transfer function $G_d(s)$ from the current loop $d(s)$ to $i_L(s)$ can be obtained as:

The transfer function \( G_v(s) \) from the voltage outer loop \( d(s) \) to \( i_L(s) \) can also be obtained as:

\[
G_v(s) = \frac{\hat{v}_d(s)}{d(s)} \bigg|_{d(s)=0} = \frac{V_2}{L_2C_2s^2 + \frac{Ls}{R} + 1}
\]  

(23)

The transfer function \( G_i(s) \) from the outer loop of the voltage to \( i_L(s) \) to \( V_1(s) \) is:

\[
G_i(s) = \frac{\hat{v}_d(s)}{d(s)} \bigg|_{d(s)=0} = \frac{1}{C_1s + \frac{1}{R}}
\]  

(24)

Draw the Bode diagram of the loop voltage and current loop transfer function based on the parameters and Equations (23) and (24) of the buck/boost converter.

Define the PI controller expression as:

\[
G_p(s) = k_p + \frac{k_i}{s}
\]  

(25)

Figure 7 shows the Bode diagram of the controlled object of the voltage loop. The system gain in the low-frequency band is small and the slope is 0. The dynamic performance of the system is poor and there are steady-state errors, so a PI controller needs to be introduced to increase the gain of the system in the low-frequency band and increase the slope of descent. After system compensation, the system has a low-frequency slope of 20 dB/dec, a cutoff frequency of 100 Hz, and a phase margin of 120°, which is in line with the design criteria, and the PI controller parameters are reasonably designed.

As can be seen from the Bode diagram of the current loop-controlled object in Figure 8, the system gain in the low-frequency band is 40 dB, but the slope is 0. This makes the converter output have a steady-state error, and the PI controller needs to be introduced to increase the system slope down in the low-frequency band. After system compensation, the slope of the system in the low-frequency band is 20 dB/dec, the end frequency is about
1 kHz, the phase margin is 80°, which corresponds to the design standard, and the PI controller parameters are reasonably designed.

![Figure 8. Current loop-controlled object bode diagram.](image)

4. Simulation Results and Analysis

In order to verify the correct parameter design, dynamic performance, and stability of the proposed control strategy of the system, an ISOP system with two identical module parameters was built based on Matlab/Simulink to simulate load and input voltage sudden changes [33]. The simulation results verify that the system can naturally achieve voltage and current sharing of the intermediate bus under different load conditions. When the input voltage suddenly changes, the voltage of the intermediate busbar and the system output voltage change very little, and have a fast adjustment speed, achieving a good dynamic voltage-sharing effect.

The ISOP topology adopts a series structure on the input side and a parallel structure on the output side. The CLLLLC converter in the submodule is equivalent to a wire. The buck/boost converter operates in buck mode, which controls the output voltage and equalizes the voltage and current of each module. The operation of the combined converter in buck mode is analyzed and Figure 9 shows a structural diagram of the three-loop control of an ISOP system. Figure 10 is the topology and control block diagram.

![Figure 9. Three-loop control structure diagram of ISOP system.](image)
For the ISOP system, the key issue is to ensure that each module shares voltage on the input side and current on the output side. In recent years, many scholars have proposed various control schemes, which can be summarized into two categories: three-loop control and double-loop control. This system adopts three-loop control, which refers to the control system including the system output voltage loop, input voltage sharing loop of each module, and current inner loop of each module. Superposition of the output signal of the system output voltage loop and the output signal of the input voltage equalizing loop of each module as the given signal of the corresponding module current inner loop. The output of the current inner loop is compared with the sawtooth wave and processed accordingly to obtain the drive signal for each module’s switching tubes. Finally, the stability of the system output voltage and the input voltage equalization of each module is achieved. If the inner current loop of each module in the three-loop control strategy is removed and only the input voltage sharing loop and output voltage loop are retained, a dual loop control strategy can be obtained. All modules in the system share a voltage loop to ensure stable output voltage. The input voltage sharing ring directly adjusts the duty cycle of each module, increasing the duty cycle of modules with high input voltage. The duty cycle of modules with low input voltage is reduced, thereby achieving input voltage equalization.

Whether there is coupling between two control loops and whether the buck/boost converter operates in buck or boost mode, it will not affect the coupling relationship of the control loop. In order to ensure the stability of the system, an input voltage-sharing control strategy was adopted, which can be equivalent to the same input power for each module. Due to the consistent parameters of each module, the output current of each module is balanced and equal.

4.1. Simulation Experiment of Load Sudden Change

Figure 11 is the main circuit simulation model. Figure 12 is the control circuit simulation model.
Figure 12. Control circuit simulation model.

Defined (1) in Figures 13–15 as a load of 2.304 Ω, (2) load is 9.216 Ω, (3) load is 2.304 Ω. Figure 13a,b show the waveforms of the input voltage and intermediate voltage of each module when the system output load changes suddenly at full load and light load. The simulation results verify that each module can achieve equal input voltage distribution and a reasonable selection of control parameters.

The sudden load change is set to rise from 2.304 Ω to 9.216 Ω at 0.3 s and then fall to 2.304 ohms at 0.6 s. The output voltage and current waveforms of the system when the output load changes suddenly at full load and light load are shown in Figure 14. From the simulation results, it can be seen that when the system load power changes abruptly, the proposed control strategy can control the output voltage fluctuation of the converter to be less than 10%, and the adjustment time is within 100 ms.
Figure 14. Output voltage and current waveforms of ISOP system during load changes suddenly.

Figure 15 shows the current waveform of the module resonant network. The simulation results show that changes in load can also cause changes in the current value of the resonant network. This is because the resonant current decreases under light load conditions, and the efficiency of the converter slightly decreases. However, under full load conditions, it can be seen that the CLLLC converter operates near the optimal operating point. Whether under light load or full load, the peak current of the excitation inductance remains basically unchanged, indicating that the conditions for achieving the ZVS of the switch under different loads are the same, which verifies the effectiveness of the resonant parameter design.

4.2. Simulation Experiment of Voltage Sudden Change

Defined ① in Figures 16–18 as an input voltage of 266 V, ② input voltage of 226 V, ③ input voltage of 266 V. Figure 16 shows the waveform of the input voltage and intermediate stage voltage of each module in the system during a sudden voltage change. Due to the different values of input and output capacitance, the simulation results show that when the input voltage changes, the transient voltage distribution is not uniform due to the difference in capacitance between the input and intermediate stage voltages of each module.
Figure 16. Input and intermediate voltage waveforms of each module with voltage changes suddenly. (a) Input voltage waveform; (b) intermediate stage voltage waveform.

Figure 17 shows the waveform of the system output voltage and current when the input voltage of the system undergoes a sudden change. The simulation results show that the proposed control strategy can control the output voltage fluctuation of the converter to be less than 2.4%, the adjustment time is within 40 ms, and the output voltage can be stable at 48V. The ISOP system not only has a fast-dynamic response speed but also achieves good dynamic voltage equalization.

Figure 18 shows the current waveform of the resonant network when the voltage suddenly changes. The simulation results show that the change in input voltage has no effect on the resonant current, and the converter is still in the optimal working state.
Figure 18. Current waveform of resonant network when voltage changes suddenly.

The ISOP system can only operate stably under input voltage-sharing control and adopts a three-loop control strategy. We designed the PI parameters of the buck/boost converter and determined the range of parameter values.

5. Experimental Results and Analysis

In order to verify the feasibility and effectiveness of the proposed automatic input voltage and output current sharing method, this chapter designed and completed a 1 kW ISOP system prototype consisting of two basic modules of buck/boost + CLLLC resonant converters.

The experimental results show that under the three-loop control strategy, it can respond quickly no matter when the load and voltage suddenly change. The CLLLC and buck/boost converter parameters are designed to use these submodules to form a buck ISOP system. We built an experimental platform based on the design parameters and conducted experimental analysis on the transient and steady-state characteristics of the ISOP system composed of submodules and multiple modules. The experimental platform and submodule physical platform are shown in Figure 19a,b.

The physical platform uses TMS320F28335 as the submodule control circuit, combined with a touch-screen display to form a system output display.

Figure 19. Physical experiment platform and submodule physical platform. (a) Experimental platform; (b) submodule physical platform.
5.1. Steady-State Experiment of Sub-Moodle Voltage Reduction

The measured module drive signal, steady-state resonant current, and output voltage waveforms are shown in Figure 20 when operating in buck mode when the module input voltage is 134 V. The simulation results show that the output voltage of the CLLLC converter is 48 V and the resonant frequency is 100 kHz. The resonant current is in sinusoidal form, which means that the converter is located near the resonant operating point, where it is most efficient.

Figure 20. Resonant network current and output voltage waveforms of CLLLC converter in steady state.

5.2. Dynamic Experiment of Sub-Moodle Voltage Reduction

Figure 21 shows the waveform of the driving signal, resonant current, and output voltage during output load switching. The load mutation of the submodule was set at $t_1$, and the load suddenly changed from 4.608 Ω to 18.432 Ω. The resonant current changes from a sine wave to a delta wave, the current value decreases and the efficiency of the converter is reduced. At $t_2$, the load suddenly changed from 18.432 Ω to 4.608 Ω, and the working point of the CLLLC converter returned to the resonance point.
When the input voltage suddenly changes from 134 V to 120 V at time $t_1$, the waveform of the module output voltage and resonant current is shown in Figure 22a. The experimental results show that it cannot return to the rated input voltage of 48 V, and there is a deviation, but it is within 10%, meeting the indicator requirements. Similarly, when the input voltage suddenly changes to 145 V at $t_2$, the output voltage also meets the indicator requirements, as shown in Figure 22b. There is no significant change in the amplitude of the resonant current in the resonant network under two operating conditions, and the CLLLC converter is always in the optimal working state.
5.3. Steady State Experiment of ISOP System

The two modules are connected in series on the high-voltage input side and in parallel on the low-voltage output side to form an ISOP system. Figure 23 shows the ISOP system input and output voltage and current waveforms. At this time the system input voltage is 266 V, the two modules have approximately equal input voltage, module 1 input voltage is 130 V, module 2 input voltage is 135 V, the parallel output voltage is 48 V and the output current is approximately 19 A.

Figure 23. Waveform of ISOP system input–output voltage current in steady state.
5.4. Dynamic Experiment of ISOP System

Figure 24a,b show the waveform of the input voltage and system output voltage and current of each module when the output load suddenly changes between 2.304 Ω and 9.216 Ω, respectively. The experimental results show that the input voltage of each module can be considered almost unchanged when the load suddenly changes, and the output voltage is stable at 48 V, which verifies the effectiveness of the control strategy.

Figure 24. Output voltage and harmonic current waveform of ISOP system during sudden load changes. (a) When the output load increases; (b) when the output load decreases.

Figure 25a,b show the waveform of the input voltage and system output voltage and current of each module when the input voltage suddenly changes between 266–226 V, respectively. From the experimental waveform, it can be seen that when the input voltage suddenly increases or decreases, the output voltage will slightly increase and decrease in a steady state. This is because the given reference value of the system output voltage changes, and under voltage mutation conditions, each module can evenly share the input voltage in a steady state.

Figure 25. Output voltage and harmonic current waveform of the ISOP system during sudden voltage changes. (a) The input voltage changes to 266 V. (b) The input voltage changes to 226 V.

The efficiency curve of the submodule and ISOP system is shown in Figure 26. When the output power is less than the rated power, the efficiency of the submodule and ISOP system tends to increase as the output power increases. However, when the output power
reaches about 70–80% of the rated power, the efficiency is the highest, and it will decrease later, but overall, the efficiency is over 96%. In addition, the efficiency of the submodules is better than that of the ISOP system. The comparison of the theoretical and experimental results is shown in Table 2.

![Efficiency curve of submodule and ISOP system](image)

**Figure 26.** Submodules and system efficiency curves.

<table>
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<th>Work Conditions</th>
<th>Output</th>
<th>System Simulation</th>
<th>System Experiment</th>
</tr>
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<td>Output voltage</td>
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<td>47.7 V</td>
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<td>Sudden load change</td>
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6. Conclusions

For a medium-power DC microgrid situation with high voltage input and low voltage output, we propose a new topology with a CLLLC+ buck/boost converter as a submodule of the ISOP system. This system adopts three-loop control, and the proposed control strategy can control the output voltage fluctuation of the converter to less than 10% when the system load power changes abruptly with a control time of less than 100 ms under the case of ±10% difference of input and output capacitance values. When the input voltage of the system changes abruptly, the proposed control strategy can control the output voltage fluctuation of the converter to less than 2.4%, the regulation time is within 40 ms, and the output voltage can be stabilized at 48 V. The proposed new topology has a quick dynamic response and an efficiency of more than 96%, which verifies the effectiveness of the adopted control strategy.

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References


33. Mustafa, E.Ş.; Frede, B. A hybrid PV-battery/supercapacitor system and a basic active power control proposal in MATLAB/Simulink. *Electronics* 2020, 9, 129.

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