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Research and Design on Digital PFC of 2kW On-board Charger

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Abstract

This paper researches and designs a digital controlled boost power factor correction (PFC) of 2kW on-board charger with the method of continuous conduction mode (CCM), which is based on the DSP of TMS320F280. Multiple-loop control strategy with the instantaneous outer voltage loop and inner current loop is used in the PFC converter. The results confirm that digital controllers are able to be used for high performance PFC converters.

Key words：DPFC，On-board Charger，CCM，EV

1. Introduction

Electric vehicles (EV) are major development direction of the future clear energy vehicles. However, the charging system is the premise and foundation. In a broad sense, electric car charging device refers to the general called of electrical energy from the public power grid or the power device that translate into various modes of electrochemical energy battery. This paper is mainly on board charger. With the popularity of electric vehicles, on-board charger will enter more and more families. If the on-board charger using the method of traditional diode bridge rectifier plus electrolytic capacitor filter not only low power factor (about 0.7) , but also contains large amounts of input current harmonics that will cause harmonic pollution on the grid.

Power factor correction is necessary for ac-to-dc switched mode power supply in order to comply with the requirements of international standards, such as IEC 61000–3–2 and IEEE-519. PFC can reduce the harmonics in the line current, increase the efficiency and capacity of power systems, and reduce customers' utility bills. In order to achieve unity power factor in the switched mode power supply, many control methods are explored, including average current control [1], peak current control [2], hysteretic control [3], nonlinear carrier control [4], etc. All of these

control methods have been implemented by the analog circuits.

With the development of digital techniques, more and more control algorithms are implemented in power electronics circuits by the digital chips, such as microprocessors or digital signal processors (DSPs). One reason is that digital control can implement more complicated algorithms. Another reason is that digital control has many advantages over analog control, including programmability, adaptability, low part count and reduced susceptibility to environmental variations, etc [5]. In addition, it is more easily function extension.

The purpose of this paper is to introduce a digital PFC (DPFC) of 2KW on-board charger. In this paper, the structure of the boost PFC converter is presented. Furthermore, a design process for both the current and the voltage loops is presented. Finally waveforms are confirmed the performance of the digital controllers.

2. Boost Power Factor Correction Circuit

When converting AC to DC, all power converters must meet PF standards (e.g., IEC 61000-3-2) given a sizable harmonic generation of current [6]. The main approach to increase the power factor is to control the input current so that it tracks the input voltage waveform even if its magnitude is different. In a boost converter the inductor's current is the input current; therefore, inductor current control can be applied to force the inductor current to follow a reference current that has the rectified voltage waveform.

In the boost topology the output voltage Vo must always be greater than the instantaneous line voltage. Since the universal line voltage is defined as an AC voltage that varies between 85 and 270 Vrms, an output voltage form 380 V to 400 V will satisfy the desired range of operation. The bulk capacitor is usually chosen based on hold up time requirements (between 16 and 20 ms [7]). The inductor, however, is selected so that the PFC power stage operates in continuous conduction mode (CCM).

3. Power Stage in Continuous Conduction Mode

Figure 1 shows the boost PFC converter and its controllers based on DSP. The power stage of the PFC is modeled based on the behavior of the boost converter in CCM. Using state space averaging, the boost converter in CCM can be explained as in (1) thru (3)

$$\dot{i}_L = \frac{1}{L}\left(\mathrm{V}_i - (1-D)V_o\right) \tag{1}$$

$$\dot{v}_c = \frac{1}{C}\left((1-D)I_L - I_o - \frac{V_o}{R}\right) \tag{2}$$

$$V_o = v_c + R_c\left((1-D)i_L - i_o - \frac{V_o}{R}\right) \tag{3}$$

Where iL, vc are small signal variations of inductor current and capacitor voltage, and IL and Vc are the large signal ones. Vo, Io, and D are the large signals of output voltage, output current disturbance and duty cycle. L, C, Rc, and R are converter inductor, converter capacitor, capacitor equivalent series resistor and load resistor. This model is used for converter simulation and its small signal equivalent is used to find the open loop transfer functions.

This circuitry includes boost circuit, A/D and TMS320F280 control systems. The complete PFC control system includes three loops: a fast current loop, a slow voltage loop, and a low-pass feed forward filter [8], The objective

of the current loop is to force the input current to follow the rectified input voltage waveform for the power factor requirement. The voltage loop is used to regulate the output voltage around 380-400 V by specifying the amplitude of the inductor current. The feed-forward filter deals with the energy unbalance that can eventually occur in the system due to an abrupt variation at the input [8].

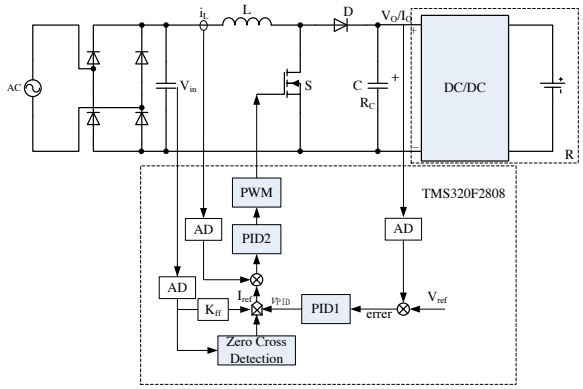

Figure 1: The boost PFC in CCM based on DSP

4. Digital Control Design of Boost PFC

The power stage specifications are:
Input voltage: Vi =220VAC±15%
PFC Output voltage: Vo = 380V
PFC Output power: Po = 200-2000W
Switch frequency: FS = 20kHz
Output filtering capacitor: C = 2240uF
Boost inductance: L = 1.1mH

4.1. Inner Current Loop Design

To design a high performance power factor correction circuit, it is necessary to decouple the system by separating the power factor requirements and the output voltage regulation. The current loop bandwidth is to be much higher than the line frequency so that it is able to follow the voltage waveform's fast variations at its zero crossing points [9]. On the other hand, in a switching converter, the bandwidth should be much smaller than the switching frequency. The bandwidth of current loop is one tenth of the switching frequency. At frequencies well above line frequency, the input and output voltages can be considered constant. Using the small-signal model of the averaged system of a boost converter, while neglecting the series resistance of the inductor and capacitor, the transfer function of the control to inductor current can be derived as in (4) [10],

$$G_{id} = \frac{2V_o}{R(1-D)^2} \frac{1+\frac{sRC}{2}}{1+\frac{sL}{R(1-D)^2}+\frac{s^2LC}{(1-D)^2}} \quad (4)$$

This transfer function can be approximated at high frequencies as shown in (5):

$$G_{id} = \frac{\hat{i}_L}{\hat{d}} = \frac{V_o}{sL} \quad (5)$$

The current loop block diagram is shown in figure 2.

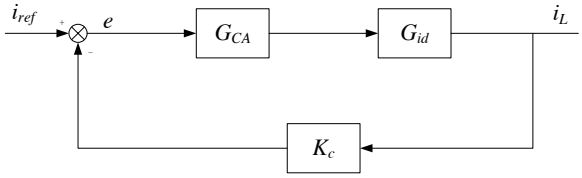

Figure 2: The current loop block diagram

Where

$$G_{CA} = K_{p1}e(k) + K_{i1}\sum_{j=0}^{k} e(j) + K_{d1}(e(k) - e(k-1))$$

, Kp1, Ki1 and Kd1 are proportionality coefficient, Integral coefficient and Derivative coefficient. Kc is the inductor's current gain.

4.2. Outer Voltage Loop Design

To simplify analysis, the model of the voltage loop is based on three assumptions. The first is that the current loop is ideal, which implies that the input current is perfectly tracking the input voltage with unit power factor. The second is that the voltage loop is very slow to compensate for the line frequency voltage ripple of the output voltage. The last

assumption is that the average input power during each cycle is equal to the output power. The bandwidth of the voltage loop is much less than the ac line frequency to minimize the distortion that can be generated in the input current due to the second harmonic that is produced in the output of the multiplier, which creates the current reference.

Under the first assumption:

$$i_L = i_{ref} = K_{ff}\left(K_f |V_i|\right)U_{vo} = \sqrt{2}K_{ff}K_f V_{rms}U_{vo}|\sin \omega t| \quad (6)$$

$$i_L = K_c \frac{\sqrt{2}P_i}{V_{rms}}|\sin \omega t| \quad (7)$$

Where Kff, Kf are the feed forward gain and the input voltage gain. Uvo is the output of voltage loop. Pi is input power.

Under the second assumption:

$$P_i = P_o = V_o I_o \quad (8)$$

The transfer function of the voltage loop for a resistive load is shown by (9),

$$G_{vc} = \frac{\hat{v}_o}{\hat{v}_c} = \frac{K_v V_{rms}^2}{V_o} \frac{\frac{R}{2}}{1+\frac{sCR}{2}} \quad (9)$$

Where $\hat{v}_c$ is the output of the voltage compensator.

The voltage loop block diagram is shown in figure 3.

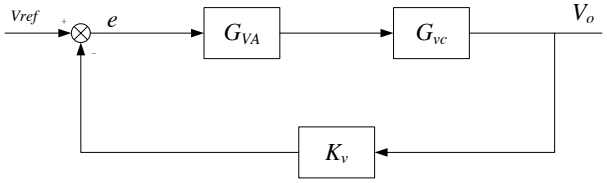

Figure 3: The voltage loop block diagram

Where

$$G_{VA} = K_{p2}e(k) + K_{i2}\sum_{j=0}^{k} e(j) + K_{d2}\left(e(k) - e(k-1)\right),$$

Kp2, Ki2 and Kd2 are proportionality coefficient, Integral coefficient and Derivative coefficient. Kv is the output voltage gain.

4.3. Software Structure

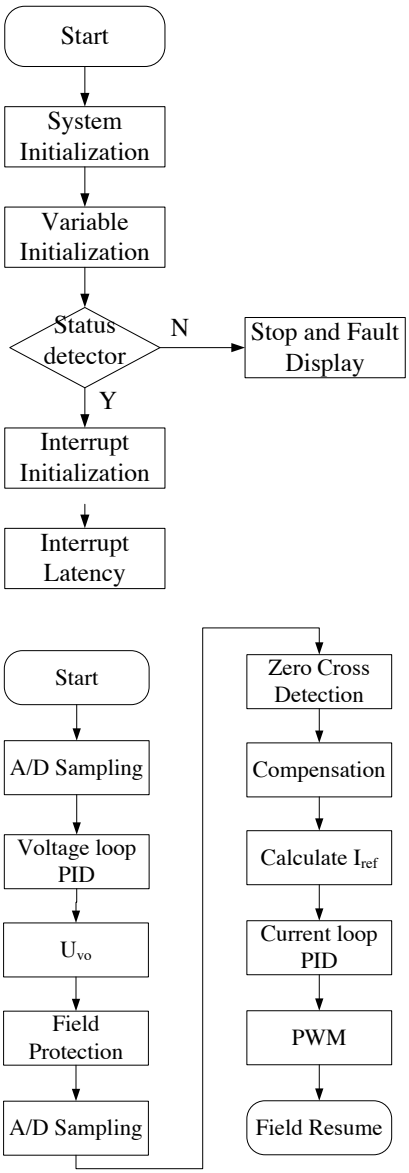

Figure 4: The main program and the interrupt service subprogram.

The control procedures by the main program and interrupt service subprogram, the program is only one interrupt service routine to avoid interrupt nesting, and improve the reliability of the program. Only the current loop is in the interrupt program. The software structure is shown in figure 4.

5. Results

The DPFC is part of on-board charger. So the experimental data is based on the charger, where Kp1=0.62, Ki1 =0.01 and Kd1 =0.025, Kp2=0.2, Ki2 =0.09 and Kd2 = 0.005, Kff =0.003. The PFC output voltage Vo （Vo = 380V） waveform is shown in Figure 5. The output voltage ripple is 10V at full load.

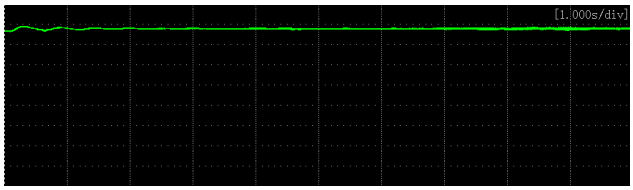

Figure 5: The PFC output voltage Vo waveform (50V/div)

The waveforms of 220VAC and inductor current IL are shown in Figure 6 at light load. The waveforms of Vin and IL are shown in Figure 7 at full load. And the waveforms of 220VAC voltage and current are shown in Figure 8 at full load.

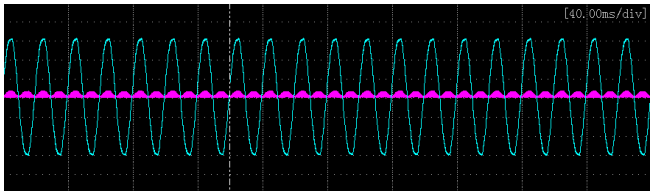

Figure 6: 220VAC and inductor current IL at light load (100V/div, 4A/div)

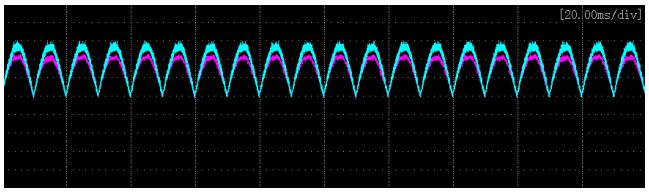

Figure 7: Vin and IL waveform at Full load (100V/div, 4A/div)

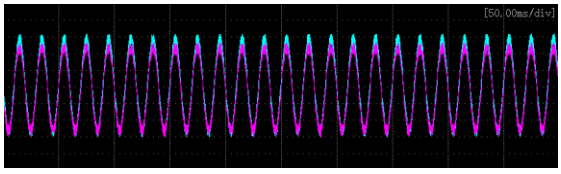

Figure 8: AC voltage and current waveform at full load (100V/div, 4A/div)

6. Conclusions

Applications of digital controllers are becoming more and more widespread in power electronic converters. This paper introduces a DPFC of 2kW on-board charger with the method of continuous conduction mode. As shown as Figure 9, the power factor is 99.68% at full load, and 93.38% at 10% load. The results confirm that digital controllers are able to be used for high performance PFC converters. The charger is used in the Shanghai World Expo of clear energy vehicles.

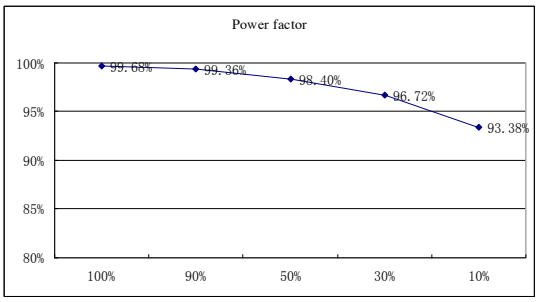

Figure 9: The power factor change form full load to light load

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