

Article

Electro-Thermal, EMI and Reliability Assessment of Post-800 V Traction Inverter Topologies [†]

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Abstract

The transition toward electric vehicle (EV) architectures exceeding 800 V offers key advantages, including shorter charging times, lower operating currents, and reduced system weight due to smaller conductor cross-sections, all of which enhance overall vehicle performance. However, identifying suitable traction inverter topologies that meet automotive requirements for efficiency, electromagnetic interference (EMI), and reliability remains critical. This study presents a simulation-based converter-level electro-thermal and conducted-EMI benchmark of 2-Level H-Bridge, 3-Level Active Neutral-Point Clamped (ANPC), and 3-Level T-Type inverters under identical output-power operating conditions. The distinguishing feature of this work is the unified evaluation of these topologies under a common external thermal boundary, enabling a consistent comparison of semiconductor losses, junction-temperature behaviour, cooling-burden indicators, conducted-EMI tendencies, and first-order lifetime-oriented thermal indicators. Within this framework, the required effective thermal resistance is used as a cooling-burden indicator, while junction-temperature swing and mean junction temperature are used as relative thermal-stress indicators. Under the considered simplified $R-L$ loading conditions, the results show that multilevel topologies reduce semiconductor losses, peak junction temperature, conducted-EMI excitation, and relative thermal-stress indicators compared with the 2L H-Bridge. These findings are interpreted as comparative topology-level trends under the defined converter-level simulation framework rather than as final vehicle-level EMI compliance or power-module lifetime predictions.

Keywords: traction inverter topologies; post-800 V EV powertrain; multilevel inverter; electro-thermal stress; cooling-burden indicator; conducted electromagnetic interference (EMI); lifetime-oriented thermal indicators



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1. Introduction

The automotive industry is transitioning toward higher voltage architectures to meet demands for faster charging, improved efficiency, and extended driving range. While conventional electric vehicles (EVs) relied on 400 V systems, the industry is shifting toward platforms exceeding 800 V [1,2]. Increasing the battery voltage reduces the current required

for a given power output, thereby lowering resistive losses (I^2R) in cables and connectors, minimizing heating, and enabling the use of lighter, thinner conductors [3]. However, scaling beyond 800 V introduces challenges; the 900–1200 V range imposes stringent insulation requirements, increases the risk of partial discharge, and requires components capable of withstanding severe voltage stress (dv/dt) [4,5]. High-voltage-rated components, such as switches, connectors, and capacitors, generally involve larger physical sizes, stricter clearance and creepage distances, and higher material costs [6,7]. Additionally, today's public ultra-fast charging networks, while evolving, are predominantly designed to accommodate up to 800 V systems, as seen in models like the Porsche Taycan, Hyundai IONIQ 6, and Lucid Air [8]. Though there are emerging chargers supporting 900–1000 V levels, widespread support for ultra-high voltages remains limited [9]. Leading this trend, manufacturers like BYD have introduced 1000 V architectures, setting new benchmarks for charging speed and range in next-generation EV platforms (5 min of charging for 400 km of range with Megawatt Flash charging) [10]. Thus, operating within the 800 V to approximately 1000–1200 V range offers a practical trade-off between improved system performance and manageable costs, insulation, and infrastructure compatibility.

In EV systems, the traction inverter becomes critical, acting as the interface between the battery and the motor. The inverter must efficiently manage higher DC-link voltages while minimizing switching losses, conduction losses, electromagnetic interference (EMI), and thermal stress. Two-level (2L) inverters, a widely used traction inverter topology, switch directly between the positive and negative rails of the DC link, subjecting the system to large voltage steps during every switching event [11]. These large voltage transitions (high dv/dt) can excite parasitic capacitances between the inverter, motor, and chassis, leading to elevated common-mode (CM) and differential-mode (DM) EMI emissions. Additionally, sharp voltage edges stress motor insulation and increase the risk of partial discharge, especially in higher-voltage systems [2,12,13].

To mitigate these challenges, even at higher DC-link voltages (i.e., post-800 V), alternative inverter topologies have been investigated for EV applications. Traction inverters operating in this voltage class must therefore satisfy not only efficiency requirements but also stringent constraints related to EMI compliance, thermal management, and long-term device reliability. Several studies highlight that wide-bandgap (WBG) semiconductors, particularly Silicon Carbide (SiC) and Gallium Nitride (GaN), are becoming key enablers for future EV converter systems. SiC devices are recognized for offering higher blocking voltages compared to GaN devices, making them particularly suitable for high-voltage traction applications. Meanwhile, GaN HEMTs are strong candidates for low- to medium-voltage applications such as onboard chargers (OBCs), auxiliary DC–DC stages, high-frequency isolated designs, and multi-level traction inverters [14]. Although SiC devices enable higher switching speeds and improved power density, the associated high dv/dt and di/dt significantly influence conductivity, radiated EMI, junction temperature rise, and thermal cycling behavior. The faster switching transitions inherent to SiC devices result in sharper dv/dt slopes, which, if not carefully managed through inverter design, can worsen high-frequency EMI emissions compared to those of their Silicon (Si)-based counterparts. Consequently, the selection of the inverter topology plays a critical role in distributing the voltage stress, shaping the switching transitions, and influencing thermal stress within semiconductor devices. Among these, three-level (3L) configurations, including the Active Neutral Point Clamped (ANPC) and T-Type topologies, are considered as potential candidates due to their ability to split the DC-link voltage into smaller switching steps [15–18]. By limiting the instantaneous voltage changes across the switches and the motor terminals, these topologies reduce dv/dt , lower EMI, and improve output waveform quality. Moreover, distributing voltage stress across multiple devices can enhance reliability and reduce the demands

placed on individual components. Besides, multi-level inverter topologies reduce current ripple, which allows for a more straightforward motor design. SiC devices offer superior characteristics compared to traditional Si-IGBTs, including lower conduction losses, higher switching speeds, higher breakdown voltages, and better thermal performance [19–22].

Most comparative studies of inverter topologies for EV applications primarily focus on efficiency, switching losses, and instantaneous junction temperature. Limited attention has been given to how the topology influences cooling demand, thermal response during continuous operation, and thermal stress conditions directly related to long-term device degradation [23,24]. In practical traction systems, the cooling system's effectiveness can vary over time due to ageing, coolant temperature rise, or thermal interface degradation. Understanding how different topologies respond to such cooling-boundary variations is therefore essential for reliability. [25,26]. To clearly position the present study, Table 1 summarizes representative literature using a Yes/Partial/No matrix across six evaluation axes: topology-level benchmarking, loss/efficiency assessment, cooling-burden quantification, conducted-EMI benchmarking, lifetime-oriented thermal indicators, and post-800 V focus.

The comparison highlights that prior work typically addresses only a subset of these dimensions—most commonly loss/efficiency—while cooling-burden quantification, conducted EMI, and lifetime-oriented thermal stress indicators are rarely treated within a unified benchmarking framework.

Table 1. Positioning of this work against representative literature (Yes/Partial/No matrix).

Ref.	Topology-Level Benchmark	Loss & Efficiency	Cooling Burden	Conducted EMI	Lifetime-Oriented Thermal Indicators	Post-800 V Focused
[5]	Partial	Yes	Partial	No	No	Partial
[15]	Yes	Yes	No	No	No	Partial
[18]	Yes	Yes	Partial	No	No	Yes
[27]	Yes	Yes	No	No	No	Partial
[28]	Yes	Yes	Partial	Partial	No	Yes
[29]	No	Yes	No	No	Partial	No
[30]	Yes	No	No	Yes	No	Partial
[31]	No	Partial	No	Yes	No	No
[32]	No	Partial	Yes	No	Yes	No
[33]	No	No	No	No	Yes	No
[34]	Yes	Partial	No	Yes	No	No
[35]	No	Partial	Yes	No	Partial	No
This paper	Yes	Yes	Yes	Yes	Yes	Yes

In Table 1, “Yes” indicates that the corresponding evaluation axis is treated quantitatively as a central part of the study. “Partial” indicates that the evaluation axis is addressed only indirectly, qualitatively, for a limited operating point, or without being integrated into a complete topology-level benchmarking framework. “No” indicates that the evaluation axis is not substantially addressed in the referenced work.

Motivated by these gaps, this paper presents a simulation-based converter-level benchmark of three representative post-800 V traction inverter topologies: the 2L H-Bridge, 3L ANPC, and 3L T-Type inverter. The novelty of this work is not the proposal of a new inverter topology or the isolated treatment of a single performance metric. Rather, the contribution lies in evaluating the same set of topologies within a single consistent framework that combines loss and efficiency assessment, junction-temperature comparison under a common external thermal boundary, cooling-burden estimation, LISN-based conducted-EMI benchmarking, and first-order lifetime-oriented thermal indicators. Beyond

conventional loss and efficiency evaluation, the distinguishing feature of this work is not the treatment of any individual axis in Table 1—topology-level loss and efficiency comparison, conducted-EMI benchmarking, and lifetime-oriented thermal analysis have each been addressed in prior studies—but their unified evaluation for the same set of topologies under a single, uniform external thermal boundary. As Table 1 shows, representative prior studies satisfy only a subset of the six evaluation axes, whereas none addresses all six within one framework. Concretely, this work makes the following contributions:

- It imposes an identical external cooling boundary across all topologies, so that differences in junction temperature mainly reflect topology-dependent loss distribution rather than differing cooling assumptions.
- It evaluates the resulting per-device cooling requirement across the investigated output-power range.
- It benchmarks intrinsic DC-side conducted emissions using a LISN-based framework.
- It reports first-order lifetime-oriented thermal indicators based on both junction-temperature swing (ΔT_j) and mean junction temperature ($T_{j,\text{mean}}$), which are important thermal quantities commonly used in power-cycling lifetime models.

Because the inverter is loaded by a controlled R–L network rather than a motor model, these results are positioned as converter-level benchmarking under simplified and repeatable operating conditions rather than as a complete traction-drive assessment.

2. Selected Existing Traction Inverter Topologies

This study focuses on three representative inverter topologies, illustrated in Figure 1, suitable for post-800 V traction applications: the conventional two-level (2L) H-bridge, the three-level (3L) active neutral-point-clamped (ANPC), and the three-level (3L) T-type inverter. Although alternative and more complex multi-level inverter (MLI) configurations, such as the split inductor MLI, flying capacitor MLI, and cascaded H-bridge, are available, the selected topologies remain the most competitive for the automotive applications because they impose fundamentally different voltage blocking and current conduction patterns on the semiconductor devices while delivering the same three-phase output [16,27,36–40]. In Figure 1, the switches of leg-A that are subjected to a blocking voltage equal to the input DC-bus voltage (V_{dc}) are highlighted in light orange, while those facing half the DC-bus voltage ($V_{dc}/2$) are marked with a light green-shaded rectangle. This highlighting indicates the topology-dependent voltage-stress level of each device, since the commutated blocking voltage directly governs the switching energy per event, thereby influencing the comparative loss, EMI, and junction-temperature behavior discussed in the subsequent sections.

2.1. Two-Level H-Bridge Inverter

The 2L H-bridge represents the conventional traction inverter architecture used extensively in commercial EVs. Each phase leg consists of two switches, and the full DC link voltage is directly applied across the upper and lower devices during switching transitions [1,37,41]. While this topology offers structural simplicity and straightforward control, it imposes the highest voltage and switching stress on individual devices. Consequently, switching losses, dv/dt , EMI excitation, and junction temperature rise tend to be more pronounced, particularly at elevated DC link voltages.

2.2. Three-Level Active Neutral Point Clamped (3L ANPC) Inverter

The 3L ANPC inverter topology enhances power conversion efficiency and thermal reliability by employing active switches to control the neutral-point connection, thereby mitigating the inherent loss distribution imbalances characteristic of conventional passive NPC designs [17,40,42]. By strategically utilizing redundant switching states and conduction

paths, the 3L ANPC architecture dynamically redistributes switching and conduction losses across the phase leg. This degree of freedom enables the implementation of advanced modulation strategies that effectively equalize the junction temperature (T_j) across the power semiconductors, thereby mitigating localized thermal stress and preventing accelerated module aging [29]. This topology ensures that each constituent device experiences a blocking voltage of approximately $V_{dc}/2$, significantly reducing dv/dt stress compared to a standard two-level configuration. Because switching energy dissipation scales non-linearly with the commutated voltage, the cumulative losses associated with two devices switching at half the DC-link voltage are substantially lower than those of a single device switching the full DC-link potential, permitting a marked increase in switching frequency without a commensurate degradation in efficiency.

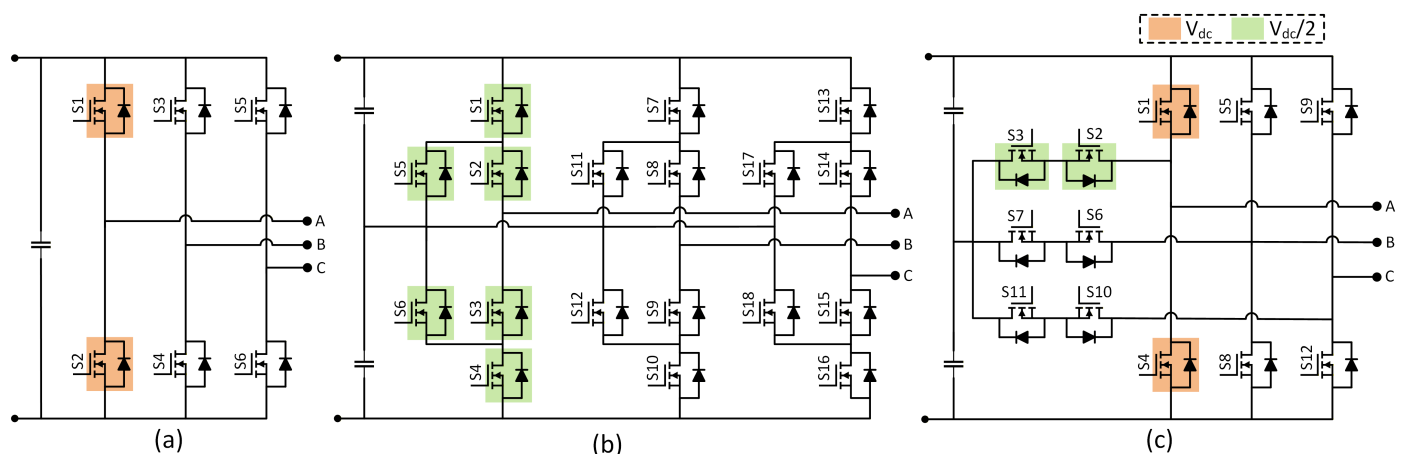


Figure 1. Three-phase Traction inverter topologies: (a) 2L H-Bridge, (b) 3L ANPC, (c) 3L T-Type. A, B, and C denote the three-phase outputs. Light-orange shading indicates switches subjected to the full DC-link blocking voltage, V_{dc} , while light-green shading indicates switches subjected to half the DC-link blocking voltage, $V_{dc}/2$.

2.3. Three-Level T-Type (3L T-Type) Inverter

The 3L T-type inverter serves as an efficient alternative to the ANPC topology by combining the low conduction loss characteristics of a two-level converter with the superior harmonic performance of a three-level architecture. In this structural arrangement, the phase leg consists of two outer switches connected to the positive and negative DC-link rails and a bidirectional auxiliary switch tied to the neutral point. Unlike the ANPC configuration, the outer semiconductor devices in a T-Type leg are exposed to the full DC-link voltage (V_{dc}) during active switching states, while the inner clamping devices operate under reduced voltage stress, typically blocking only $V_{dc}/2$ during neutral point clamping intervals [27]. This inherent asymmetry in voltage blocking requirements results in a distinct distribution of conduction and switching losses between the inner and outer switches. Consequently, the localized T_j rise varies significantly across the phase leg, often necessitating specialized pulse-width modulation (PWM) strategies to manage the thermal gradient between the high-voltage outer devices and the low-voltage clamping switches [43]. Despite these thermal asymmetries, the 3L T-type inverter is often regarded as a hybrid solution that combines the benefits of both the 2L H-bridge and the 3L ANPC topologies.

3. Simulation Framework and Uniform Thermal Boundary Definition

These three inverter topologies were implemented in the PLECS simulation environment (Plexim GmbH, Zurich, Switzerland) using manufacturer-provided electro-thermal device models. These models contain temperature-dependent electrical characteristics

and detailed junction-to-case thermal impedance descriptions extracted from the device datasheets. Consequently, the junction temperature is not computed from simplified analytical thermal equations; instead, it is solved internally by PLECS from the instantaneous device losses and the embedded thermal network of each MOSFET and body diode. The numerical values of the electrical and thermal parameters used in the simulations are summarized in Table 2. The exact load-resistance values used for each topology, DC-link voltage, and output-power condition are reported in Appendix A; the load inductance was fixed at $L_{load} = 2$ mH for all cases.

Table 2. Electrical and thermal parameters used in the simulations.

Parameter	Symbol	Value
DC-link voltage (V)	V_{dc}	800, 1000, 1200
Switching frequency (kHz)	f_{sw}	10, 20, 30
Fundamental frequency (Hz)	f_1	50
Modulation index	m	0.9
Load resistance (Ω)	R_{load}	1.5–7.5
Load inductance (H)	L_{load}	0.002
Cooling reference temperature ($^{\circ}\text{C}$)	T_{ref}	25
Case-to-heatsink resistance (K/W)	$R_{th,ch}$	0.05
Heatsink-to-coolant resistance (K/W)	R_{th}	0.1
Heatsink thermal capacitance (J/K)	C_{th}	1000
Simulation time (s)	T_{sim}	20

Note: The load resistance is varied to equalize output power across the investigated topologies. The exact values are reported in Appendix A.

Modulation and Switching Assumptions

All inverter topologies were controlled using carrier-based sinusoidal pulse-width modulation (SPWM) with a fundamental frequency of $f_1 = 50$ Hz. For the 2L H-Bridge, conventional two-level SPWM was applied. For the 3L ANPC and 3L T-Type topologies, carrier-based three-level SPWM was used to generate the corresponding positive, zero, and negative output voltage states. The same modulation principle was applied across the investigated topologies to maintain a consistent basis for comparison. The modulation index was kept at $m = 0.9$, as reported in Table 2.

For the three-level topologies, the DC-link midpoint was assumed to remain balanced during the investigated operating conditions. Therefore, no additional closed-loop neutral-point voltage-balancing controller was implemented. This assumption allows the comparison to focus on topology-dependent loss distribution, junction-temperature behaviour, and conducted-EMI tendency under identical converter-level operating conditions, rather than on topology-specific neutral-point control dynamics.

A dead time was included in the switching signals. In the implemented model, the dead time was defined as $T_{dt} = 0.005/f_{sw}$, corresponding to 250 ns at the baseline switching frequency of $f_{sw} = 20$ kHz. The same dead-time formulation was applied consistently to all topologies. The external turn-on and turn-off gate resistances used in the device parameter definitions were $R_{g,on} = R_{g,off} = 2.5 \Omega$. Switching losses and switching transitions were evaluated using the manufacturer-provided PLECS electro-thermal device descriptions, which include device-specific MOSFET and body-diode loss characteristics. Additional gate-loop parasitics, propagation-delay mismatch, package-layout-induced ringing, and voltage overshoot were not explicitly modelled. Therefore, the reported switching-loss, EMI, and thermal results should be interpreted as comparative trends under the defined modulation and switching assumptions rather than as gate-driver- or layout-specific predictions.

During simulation, the conduction losses of a device are evaluated at every solver time step as

$$P_{\text{cond}}(t) = V_{\text{ds}}(I(t), T_j(t)) \cdot I(t), \quad (1)$$

where V_{ds} is obtained from the temperature-dependent device characteristics and $I(t)$ is the instantaneous device current. Switching losses are evaluated from the tabulated turn-on and turn-off energy data provided in the device thermal description as

$$P_{\text{sw}} = f_{\text{sw}} [E_{\text{on}}(I, V, T_j) + E_{\text{off}}(I, V, T_j)], \quad (2)$$

where f_{sw} is the switching frequency. The total instantaneous device losses are therefore

$$P_{\text{dev}}(t) = P_{\text{cond}}(t) + P_{\text{sw}}. \quad (3)$$

These losses are injected into the internal junction-to-case thermal network of the device model, allowing PLECS to compute the dynamic junction temperature $T_j(t)$ directly. To enable a fair electro-thermal comparison among the three inverter topologies, a uniform external thermal boundary is imposed for all semiconductor devices. Each device is connected to a common heatsink node through a case-to-heatsink thermal resistance $R_{\text{th,ch}}$, representing the thermal interface material (TIM) and mounting contact. The heatsink node is modeled by a first-order lumped thermal network consisting of a heatsink-to-coolant thermal resistance R_{th} and an effective thermal capacitance C_{th} , capturing the dominant thermal inertia of the cooling plate/cold-plate assembly. The reference temperature is held constant at T_{ref} (Table 2), representing the imposed thermal boundary at the cooling interface. Under this configuration, the heatsink temperature $T_h(t)$ follows

$$C_{\text{th}} \frac{dT_h(t)}{dt} = \sum_i P_i(t) - \frac{T_h(t) - T_{\text{ref}}}{R_{\text{th}}}, \quad (4)$$

where $\sum_i P_i(t)$ denotes the total heat flow injected into the heatsink node by all devices. The junction temperature is resolved internally by the semiconductor electro-thermal model. This uniform boundary ensures that any differences in junction-temperature rise among topologies originate from topology-dependent loss distribution and device voltage/current stress, rather than from differences in cooling assumptions.

An R – L load is used at the inverter output instead of a motor model to provide a controllable and topology-independent means of setting the operating point. The resistive component is adjusted to equalize the output power across topologies, while the inductive component maintains realistic current ripple and prevents unrealistically steep current transients. Since the objective of this study is to benchmark inverter electro-thermal stress and conducted-EMI behavior under comparable electrical loading (rather than motor–inverter interaction or field-weakening dynamics), the R – L load ensures consistent and repeatable operating conditions for all topologies.

It should be noted that the R – L load does not reproduce the complete behaviour of an electric traction machine. A realistic PMSM or induction-motor drive model would introduce speed-dependent back-EMF, variable power factor, field-weakening operation, controller-dependent current dynamics, and mission-profile-dependent current waveforms. These factors can influence conducted-EMI spectra, thermal-cycling amplitude, and junction-temperature evolution. Therefore, the present R – L -load model is used solely to establish a repeatable converter-level benchmark, with the same electrical loading framework applied to all topologies. The resulting EMI and thermal-stress trends should be interpreted as comparative topology-level tendencies under the defined simulation conditions, rather than as final vehicle-level EMI compliance or lifetime predictions.

4. Electro-Thermal and EMI Performance at Equal Output Power

To ensure a physically meaningful comparison among inverter topologies, all simulations in this study are performed at identical output power levels rather than identical load parameters. Consistent with the scope defined in the previous section, the following results are interpreted as converter-level comparative trends under the specified R – L loading conditions. All simulations have been carried out using an identical total simulation time of 20 s to ensure a uniform basis for comparison. Maintaining a fixed simulation duration ensures that all topologies are evaluated over the same transient observation window, so that the reported junction-temperature trends are compared on a consistent time basis. For each operating point, the modulation index is kept constant while the resistive component of the R – L load is tuned such that the inverter delivers the same output power for the 2L H-bridge, 3L ANPC, and 3L T-type configurations. This approach ensures that each topology operates under equivalent electrical power handling conditions, allowing the observed differences in losses, junction temperature, and EMI behavior to be attributed solely to inherent topological characteristics.

A critical aspect of the comparative framework is selecting semiconductor devices based on the voltage stress imposed by each topology. Rather than using identical devices across all configurations, SiC MOSFETs are selected based on the maximum blocking voltage experienced by each switch position. This ensures that each device operates within its appropriate voltage class, avoiding artificial penalization or overdesign in any topology. Specifically, 1700 V-rated SiC MOSFETs (C2M0045170P) are used in the 2L H-bridge and in the upper and lower switches of the 3L T-type inverter, as these devices are directly exposed to the full DC-link voltage. In contrast, the switches forming the neutral clamping path in the 3L ANPC and the ‘T’ branch of the 3L T-type inverter experience only half of the DC-link voltage and therefore employ 900 V-rated SiC MOSFETs (C3M0030090K). To satisfy the targeted current requirement at higher output power levels, four devices of each selected type are connected in parallel. This maintains realistic current density, conduction resistance, and thermal distribution while preserving the inherent voltage-stress characteristics of each topology.

It should be noted that the present comparison is based on topology-dependent voltage-stress matching rather than equal total semiconductor chip area or equal total installed silicon area. Although four MOSFETs are connected in parallel at each selected switch position to satisfy the targeted current requirement, the total number of semiconductor devices and gate-driver channels still differs among the topologies because of their inherent circuit structures. The manufacturer-provided PLECS electro-thermal models include device-specific electrical loss characteristics and thermal impedance data; however, the complete inverter systems are not explicitly normalized by total semiconductor chip area, total installed silicon area, or total current rating. Therefore, the results should be interpreted as an application-oriented comparison using voltage-stress-appropriate device selection, rather than as an equal-chip-area, equal-device-count, or equal-total-rated-current-capability comparison. The 2L H-Bridge has the lowest semiconductor count and simplest gate-driver structure, the 3L ANPC has the highest structural complexity, and the 3L T-Type remains intermediate. Consequently, the lower losses, reduced junction-temperature rise, and lower conducted-EMI tendency observed for the multilevel topologies should be assessed together with the associated increase in semiconductor count, gate-driver requirements, layout complexity, and potential part-count-related failure risk.

4.1. Power Losses and Efficiency for Different Input Voltages

Figure 2 presents the conduction losses, switching losses, and corresponding efficiency of the three inverter topologies at a constant output power of 100 kW and a fixed switching

frequency (f_{sw}) of 20 kHz while the DC-link voltage is varied from 800 V to 1200 V, considering only power semiconductor device losses. For all topologies, an increase in DC-link voltage results in a systematic reduction in total power losses. This trend is primarily governed by the reduction in phase current required to deliver the same output power, which directly lowers the conduction losses since $P_{cond} \propto I_{rms}^2 R_{on}$. As a result, the conduction losses decrease most significantly as the DC voltage increases from 800 V to 1200 V. In contrast, the switching losses vary more moderately with voltage because it depends on both switching energy and switching frequency, with the device voltage stress and commutation energy playing a secondary role compared to the dominant current reduction effect.

In the 2L H-bridge, the devices are subjected to the full DC-link voltage during each switching transition. Consequently, both conduction and switching losses remain comparatively high. The total losses reduce from 826.8 W at 800 V to 452.0 W at 1200 V, with the conduction losses being the dominant contributor across all operating points.

The 3L ANPC topology demonstrates a consistent reduction in total losses relative to the 2L inverter. This is attributed to the fact that several devices in the current path experience only half the DC-link voltage, reducing both switching energy and voltage stress. The total loss decreases from 634.0 W at 800 V to 361.3 W at 1200 V, indicating a clear advantage of the multilevel structure in lowering device stress and loss generation.

The 3L T-type exhibits the lowest total loss among the three topologies across all voltage levels. The inner devices operate at reduced voltage stress and provide a shorter current path, minimizing conduction losses while limiting switching energy. The total losses reduce from 573.3 W at 800 V to 270.7 W at 1200 V.

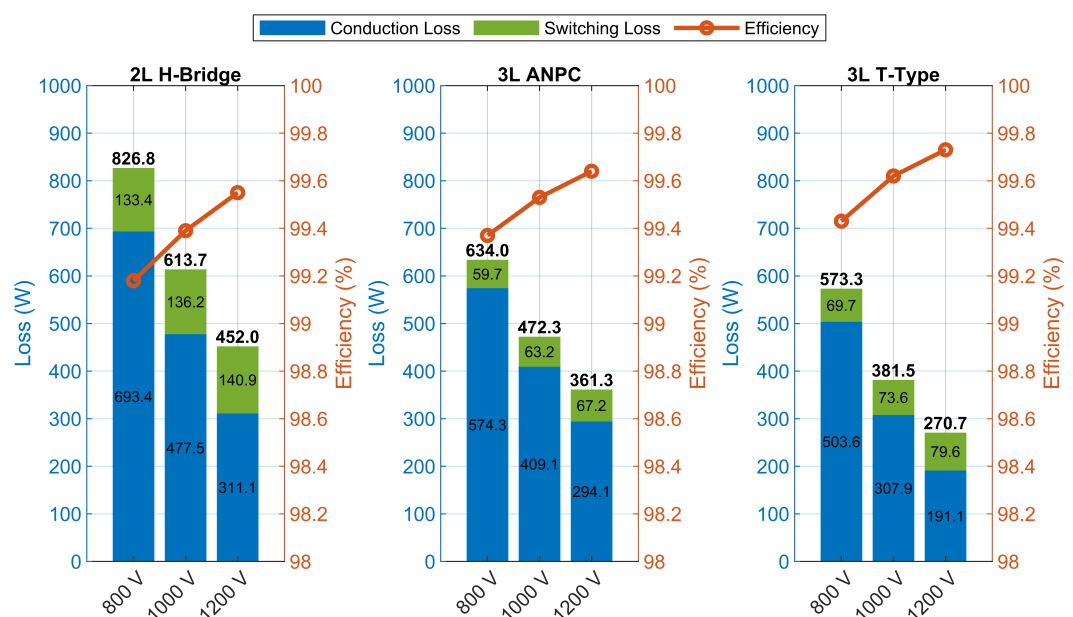


Figure 2. Power losses breakdown and efficiency of the three considered inverter topologies for an equal output power of 100 kW at different input voltages.

The efficiency trend directly follows the behavior of total losses. While all topologies benefit from higher DC-link voltage, the T-type inverter consistently achieves the highest efficiency, followed by the ANPC and, finally, the 2L H-Bridge. This result highlights the intrinsic advantage of multilevel topologies in post-800 V traction applications, where reduced conduction current and redistributed voltage stress significantly improve electro-thermal performance under identical output power conditions.

4.2. Power Losses and Worst Case Switch Junction Temperature

Figure 3 shows the maximum junction temperature of the device facing the highest thermal stress considered as the worst-case semiconductor device in leg-A for the three inverter topologies when delivering the same output power at different DC-link voltages.

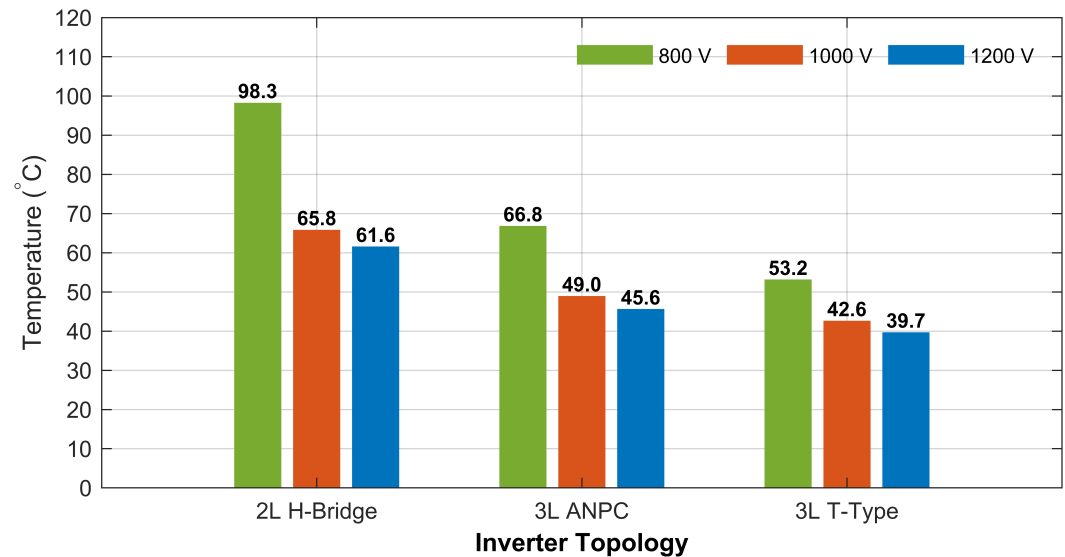


Figure 3. Worst case junction temperature ($T_{j,max}$) for leg-A of the considered inverter topologies at different input voltages.

A clear reduction in peak junction temperature is observed for all topologies as the DC-link voltage increases from 800 V to 1200 V. This trend is mainly due to the lower RMS phase current required to maintain the same output power under the adjusted R – L loading conditions. Since the dominant conduction-loss component is approximately proportional to $I_{rms}^2 R_{on}$, the reduced current stress lowers semiconductor heat generation and therefore reduces the junction-temperature rise under the same imposed thermal boundary.

The topology-dependent loss distribution also contributes to this behaviour. The 2L H-Bridge exhibits the highest junction temperature because its switches carry the full phase current and are subjected to the full DC-link voltage stress. In contrast, the 3L ANPC and 3L T-Type distribute electrical and thermal stress among a larger number of devices. This effect is most pronounced in the 3L T-Type, where favourable conduction paths and lower effective device stress lead to the lowest observed $T_{j,max}$ at 1200 V.

However, higher DC-link voltage also introduces practical trade-offs, including increased semiconductor voltage stress, insulation requirements, creepage and clearance distances, DC-link capacitor voltage rating, protection complexity, switching-transient severity, voltage overshoot, and EMI-mitigation challenges. Therefore, the lower junction temperature observed at 1000–1200 V should be interpreted together with these practical implementation constraints.

Figure 4 extends the electro-thermal comparison by showing the total inverter power losses and corresponding maximum junction temperature as functions of output power at $V_{in} = 800, 1000$, and 1200 V. The left-column plots present the total power-loss trends, while the right-column plots show the corresponding maximum junction-temperature response under the same operating conditions.

For all DC-link voltages, the total losses increase with output power, reflecting the increasing current stress at higher load levels. At 800 V, the loss increase is the most pronounced because a higher phase current is required to achieve the same output power, resulting in higher junction temperatures. As the DC-link voltage increases to 1000 V and

1200 V, the required current decreases, leading to a systematic reduction in both total losses and peak junction temperature across all investigated topologies.

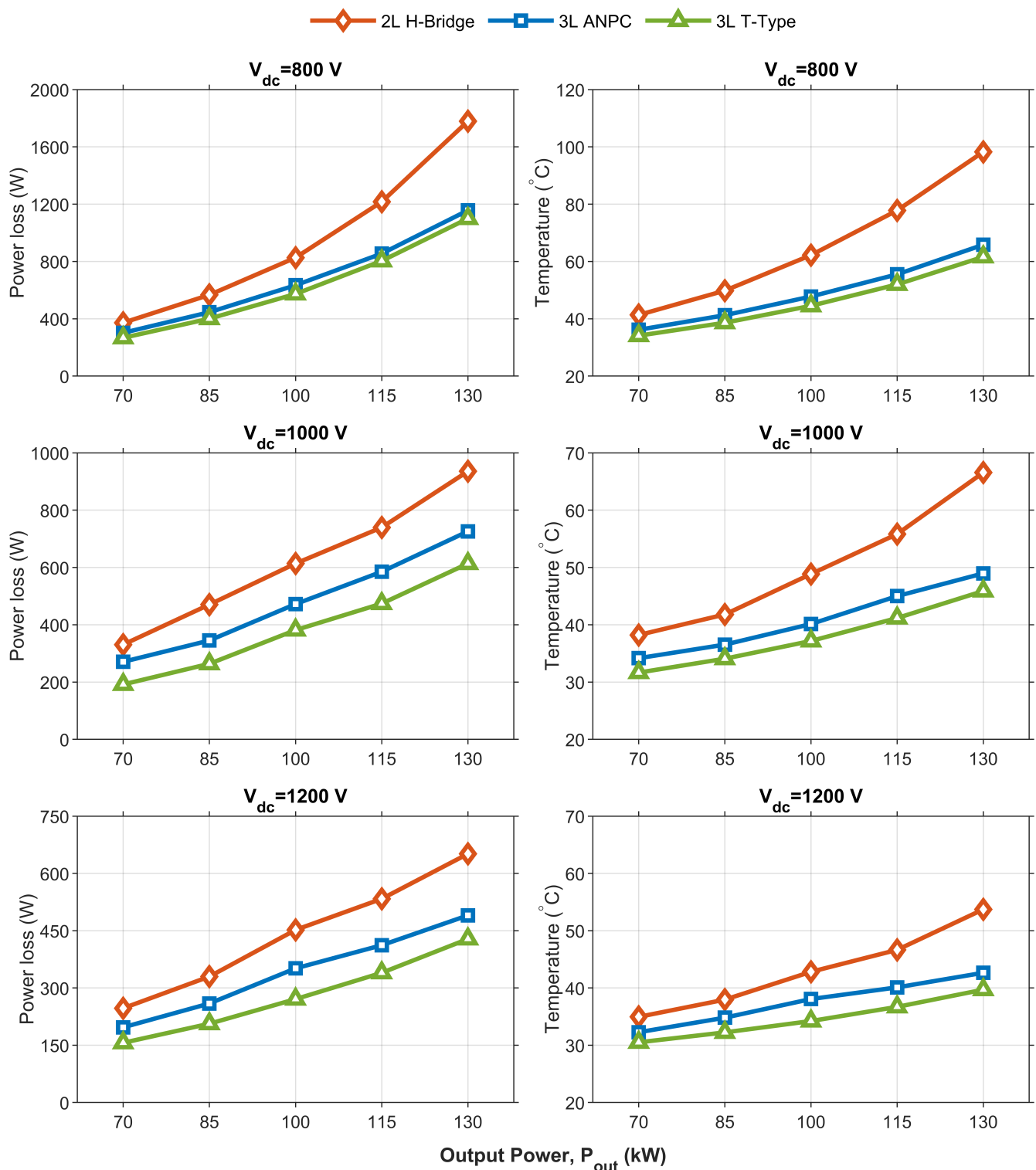


Figure 4. Output power versus total inverter power losses and maximum junction temperature for the investigated inverter topologies at input $V_{dc} = 800, 1000$, and 1200 V. The left column shows the total power loss, while the right column shows the corresponding maximum junction temperature.

The junction-temperature trends follow the loss trends, confirming the strong coupling between semiconductor loss generation and thermal response under identical cooling-boundary conditions. The separation among the topologies becomes more pronounced

at higher output power, indicating that topology-dependent loss distribution becomes increasingly important under high-power operating conditions.

This observation is significant for traction inverter design because the junction temperature is a primary driver of semiconductor reliability. Elevated T_j accelerates thermally activated degradation mechanisms such as bond-wire fatigue, solder layer aging, and metallization wear, while repeated temperature excursions ΔT_j intensify thermo-mechanical stress within the package. Consequently, the absolute junction temperature level and its variation over time directly influence the expected device lifetime, the required cooling capability, and the allowable thermal operating margin under automotive mission profiles. For the same output power, differences in topology-dependent device stress therefore translate into differences in cooling demand, thermal margin, and lifetime potential.

4.3. Switching Loss for Different Switching Frequencies

Figure 5 quantifies the dependence of switching losses on switching frequency for the 2L H-bridge, 3L ANPC, and 3L T-type inverter topologies at $V_{dc} = 1000$ V and a fixed output power of $P_{out} = 100$ kW for a simulation duration of 20 s. The switching losses are explicitly analyzed because they scale approximately linearly with switching frequency and are strongly influenced by topology-dependent voltage stress, current commutation paths, and the number of active switching events per fundamental cycle.

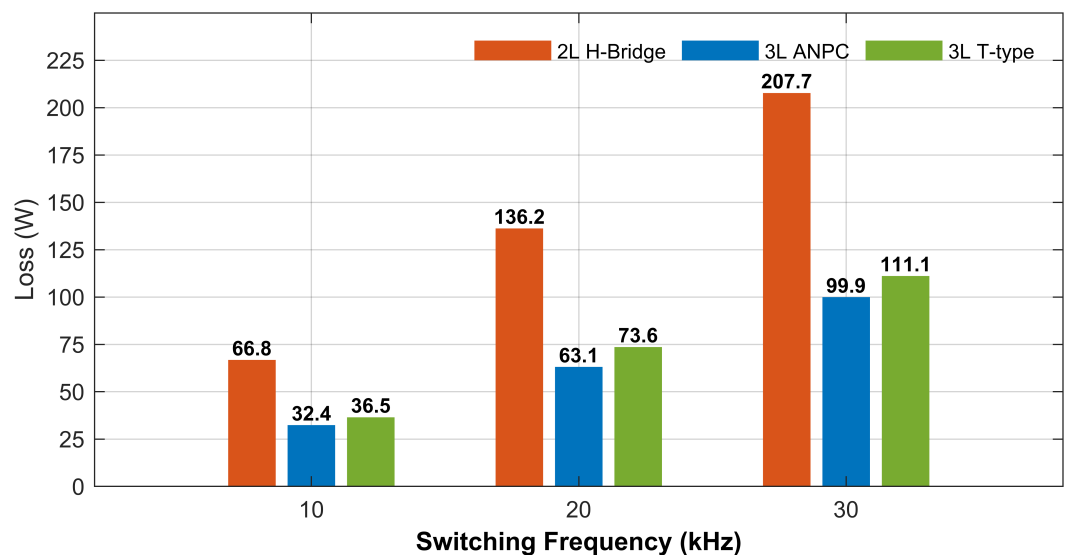


Figure 5. Switching losses at different switching frequencies for the three considered inverter topologies at a voltage of 1000 V and a fixed output power of 100 kW.

To contextualize the investigated range, full-SiC traction-inverter demonstrators for EV powertrains have reported operation at switching frequencies up to 40 kHz to exploit the wide-bandgap switching capability toward higher power density and reduced passive-component volume [44,45]. The 2L H-bridge exhibits the highest switching losses, increasing from 66.8 W at 10 kHz to 136.2 W at 20 kHz and 207.7 W at 30 kHz, due to full DC-link voltage commutation during each switching event. In contrast, the 3L ANPC limits switching losses to 32.4–99.9 W, while the 3L T-type ranges from 36.5–111.1 W over the same frequency span.

These numerical trends highlight that switching frequency scaling imposes a substantially higher thermal penalty on the 2L inverter, particularly at elevated frequencies commonly required in high-speed EV traction applications. Consequently, topology-dependent switching behavior plays a decisive role in determining the feasible limits on switching frequency, efficiency degradation, and thermal stress under high-performance operating conditions.

4.4. Conducted EMI Analysis and Comparative Performance

The conducted EMI is evaluated using a standardized line impedance stabilization network (LISN)-based configuration implemented in simulation, and the results are illustrated in Figure 6. The LISN model consists of a series inductance of $L_{\text{LISN}} = 5 \mu\text{H}$, decoupling capacitors of $1 \mu\text{F}$ and 100 nF , and a sensing resistor $R_{\text{LISN}} = 50 \Omega$ to measure high-frequency voltage disturbances at the DC input terminals. This configuration enables accurate extraction of common-mode (CM) and differential-mode (DM) noise components over the frequency range of interest. To represent parasitic coupling between the inverter switching nodes and the ground, fixed stray capacitances are introduced uniformly across all topologies: 20 pF from the upper switch node to the ground, 20 pF from the lower switch node to the ground, and 120 pF from the midpoint node to the ground. These values are consistent with commonly reported parameters in high-voltage inverter EMI studies [31].

It should be noted that parasitic capacitances are not standardized quantities. They depend strongly on physical layout characteristics such as PCB geometry, layer stack-up, device package type (e.g., TO-247 versus surface-mount modules), heatsink grounding strategy, and mechanical mounting configuration. Nevertheless, identical parasitic values are intentionally applied to all inverter configurations to ensure a fair topology-level comparison independent of mechanical implementation. This approach helps to isolate the intrinsic effect of inverter topology on conducted-EMI excitation, rather than to represent a layout-specific implementation. In practice, the common-mode displacement current associated with each switching node is approximately proportional to $C_p dv/dt$, where C_p is the corresponding parasitic capacitance to the reference ground. Therefore, topology-specific variations in PCB layout, module packaging, heatsink grounding, and cable arrangement can change the absolute CM/DM emission levels and may narrow or widen the differences among the investigated topologies. The EMI results should therefore be interpreted as comparative topology-level tendencies under fixed parasitic assumptions, not as final layout-specific EMI compliance predictions. A complete design-stage assessment would require topology-specific parasitic extraction from the physical layout or a dedicated parasitic-sensitivity sweep.

No external EMI filters are included, enabling direct evaluation of intrinsic emission characteristics. A constant load current of 100 A and a switching frequency of 20 kHz are maintained for $V_{\text{dc}} = 800 \text{ V}$ and 1000 V , ensuring identical di/dt stress while isolating the impact of increased dv/dt resulting from a higher DC-link voltage. Frequency-domain spectra from 10 kHz to 30 MHz are obtained from time-domain LISN voltage signals to extract the CM and DM components.

The results demonstrate pronounced topology-dependent EMI behavior. The 2L H-bridge exhibits the highest emission levels, with dominant DM noise approaching $120 \text{ dB}\mu\text{V}$ at 1000 V . This is driven by full DC-link commutation and large voltage steps ($\pm V_{\text{dc}}$) that generate steep dv/dt and strong displacement currents through parasitic capacitances. In contrast, the 3L ANPC and 3L T-type topologies suppress both CM and DM emissions due to reduced voltage step amplitude (e.g., $\pm V_{\text{dc}}/2$) and distributed switching transitions, which limit high-frequency spectral content. Among the evaluated configurations, the 3L T-type achieves the lowest overall emissions, particularly in the CM domain, due to its symmetric structure and central clamping mechanism, which mitigate ground-referenced current injection. Although increasing the input voltage from 800 V to 1000 V slightly increases the magnitude of the emissions due to the higher transition energy, the multilevel topologies show lower increases in emissions under voltage scaling within the fixed parasitic assumptions used in this study. These simulation findings indicate that, under the fixed parasitic assumptions used in this study, the multilevel inverter topologies

exhibit lower intrinsic conducted-EMI excitation than the 2L H-Bridge, with the 3L T-Type showing the lowest overall emission tendency among the investigated cases.

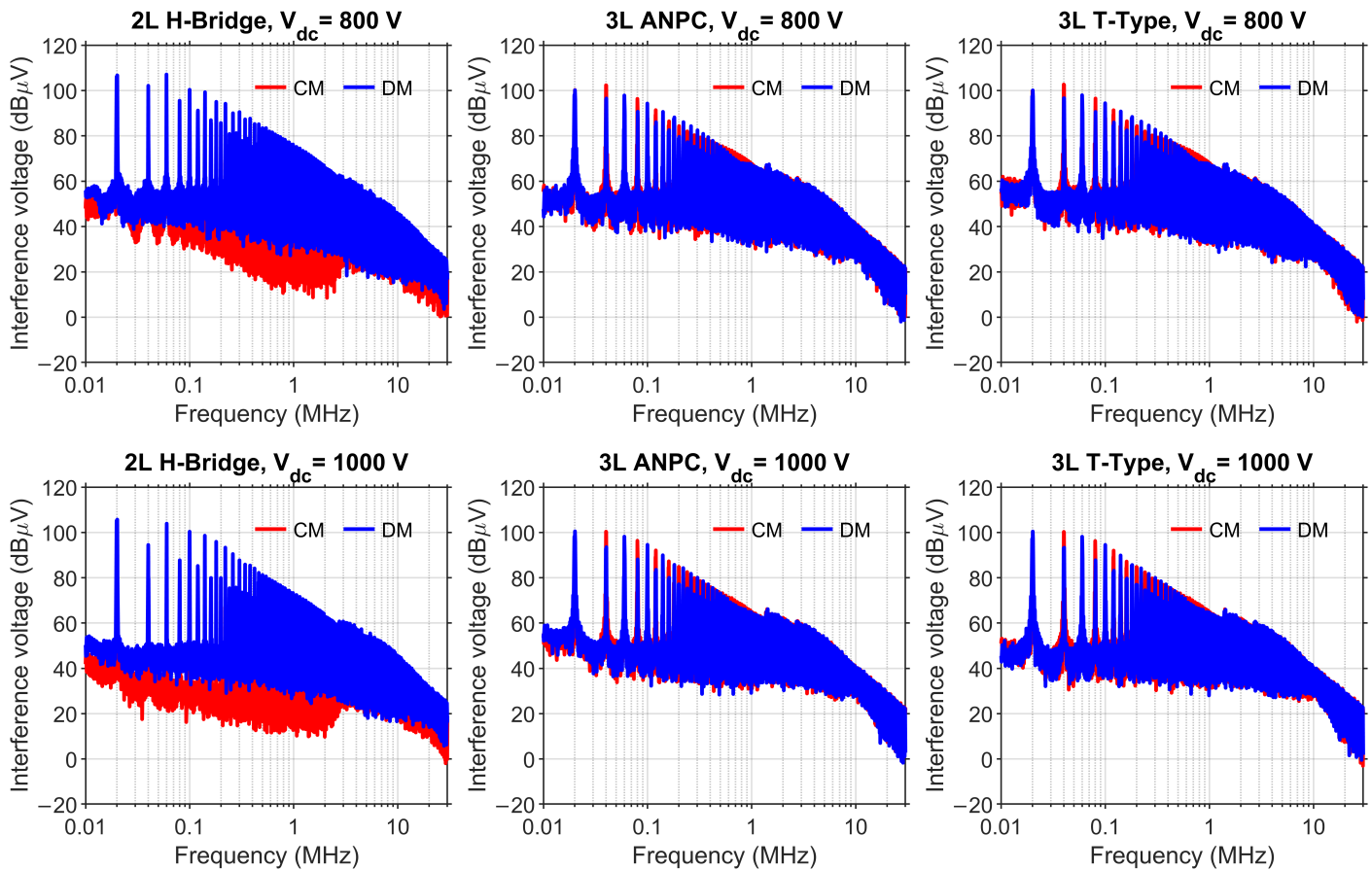


Figure 6. Conducted EMI of the considered inverter topologies at a DC-link voltage of 800 V and 1000 V.

5. Thermal Behaviour and Cooling Demand

Modern traction inverters are constrained by a maximum allowable junction temperature, typically $T_{j,max} = 150\text{ }^{\circ}\text{C}$ to $175\text{ }^{\circ}\text{C}$ [25]. To quantify the topology- and load-dependent cooling burden in a transparent manner, an *effective* maximum allowable per-device thermal resistance, $R_{th,req}$, is derived from the average loss of the worst-case semiconductor switch under the imposed liquid-cooling boundary:

$$R_{th,req} = \frac{T_{j,max} - T_{ref}}{P_{loss,avg,worst}}, \quad (5)$$

where T_{ref} is the controlled reference temperature at the cold-plate/coolant interface and $P_{loss,avg,worst}$ is the corresponding device-average loss of the worst-case semiconductor switch evaluated over the fixed analysis window of $t = 15\text{--}20\text{ s}$. This requirement can be interpreted as an effective junction-to-coolant thermal budget per device, which is partitioned among the internal package path ($R_{th,jc}$), the case-to-heatsink interface (TIM and mounting, $R_{th,ch}$), and the remaining cooling hardware represented by the imposed heatsink-to-reference path. In practical module assemblies, $R_{th,jc}$ and $R_{th,ch}$ can consume a substantial fraction of this budget, thereby reducing the margin available to the cold-plate and coolant loop [35]. Consequently, operating points that push $R_{th,req}$ toward small values indicate a stringent cooling burden and generally motivate higher-performance

liquid-cooling measures, such as enhanced cold-plate designs and/or increased coolant flow, compared with baseline implementations [35,46].

It should be emphasized that $R_{th,req}$ is used here as a comparative cooling-burden indicator derived from the extracted average device loss, rather than as a claim that the complete heatsink/cold-plate network has reached thermal steady state within the simulated time. Since the imposed heatsink network has a dominant thermal time constant of approximately $R_{th}C_{th} = 100$ s, while the electro-thermal simulations have a total duration of 20 s, the reported junction-temperature and cooling-burden results should be interpreted as common-window transient comparative indicators under identical thermal-boundary assumptions. Longer mission-profile simulations over several thermal time constants would be required for a full steady-state cooling-system assessment.

To parameterize a consistent system-level cooling boundary for topology comparison, simulations were conducted with a DC-link voltage of $V_{dc} = 1000$ V and a standardized switching frequency of $f_{sw} = 20$ kHz. The thermal boundary conditions were selected to emulate an automotive water–ethylene glycol (WEG) liquid-cooled cold-plate interface. The case-to-heatsink interface was modeled with $R_{th,ch} = 0.05$ K/W, while the heatsink-to-reference path was represented by a first-order lumped network with $R_{th} = 0.1$ K/W and an effective thermal capacitance $C_{th} = 1000$ J/K. The resulting dominant time constant is $\tau = R_{th}C_{th} \approx 100$ s; this lumped representation provides the same slow thermal-inertia boundary for all topologies, enabling a consistent comparative assessment under identical external cooling assumptions. [47]. For consistency across topologies, the temperature profile of the worst-case semiconductor switch in leg-A was evaluated over the same fixed transient analysis window of 15–20 s. Figure 7 plots the corresponding $R_{th,req}$ across the continuous output-power spectrum.

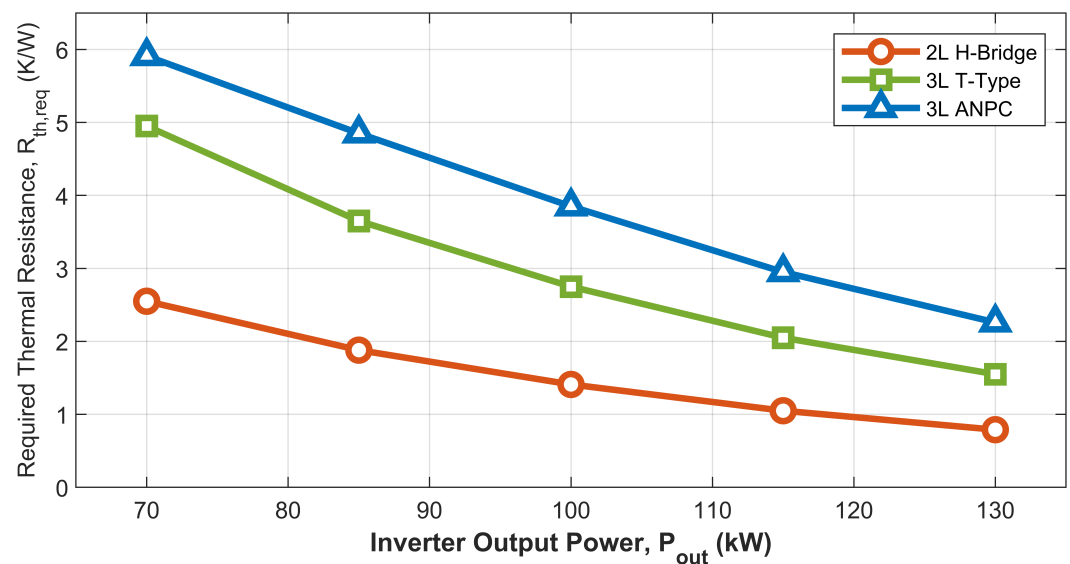


Figure 7. Maximum allowable effective per-device thermal resistance, $R_{th,req}$, for the considered inverter topologies across varying output-power levels at $V_{dc} = 1000$ V and $f_{sw} = 20$ kHz, calculated using $T_{j,max} = 150$ °C and $T_{ref} = 25$ °C.

As output power increases, the results reveal a clear divergence in cooling demand driven by how each topology distributes its switching and conduction losses. At 70 kW output, $R_{th,req}$ ranges from 2.55 K/W for the 2L H-bridge to 5.91 K/W for the 3L-ANPC topology, indicating a comparatively relaxed thermal budget for the multi-level case under the same imposed boundary.

However, at the peak 130 kW traction output, the 2L H-bridge topology dissipates 960.6 W of total losses, heavily concentrating heat flux on the worst-case switch. This

corresponds to a stringent allowable effective thermal resistance of 0.79 K/W, indicating the highest estimated cooling burden among the investigated topologies. In stark contrast, multi-level topologies inherently distribute thermal stress across a larger semiconductor active area. Despite the 3L-ANPC generating higher total system losses (707.4 W) than the 3L T-Type (613.7 W) at 130 kW, its implemented commutation strategy provides a more favourable heat distribution. As a result, the 3L-ANPC shows an allowable $R_{th,req}$ of 2.26 K/W at peak power, while the 3L T-Type requires 1.55 K/W. This indicates that, under the defined simulation framework, the multilevel topologies provide a larger estimated thermal-resistance margin than the 2L H-Bridge at elevated output power.

It should also be noted that the cooling-burden indicator based on $R_{th,req}$ is calculated from the average loss of the worst-case semiconductor switch under the implemented switching-state selection. For the 3L ANPC topology, redundant switching states can in principle be used to redistribute conduction and switching losses among the devices and actively balance junction temperatures. Such optimized thermal-balancing control was not included in the present benchmark, since the objective was to compare the topologies under a common modulation and thermal-boundary framework. Therefore, the reported ANPC cooling-burden result reflects the implemented switching strategy rather than the maximum achievable thermal benefit of an actively thermally balanced ANPC inverter. An optimized redundant-state selection strategy could further reduce the worst-case device thermal stress and improve the estimated cooling margin, but this requires a dedicated control-oriented analysis beyond the scope of this study.

To further examine the effect of coolant/reference temperature on the estimated cooling margin, a post-processed first-order reference-temperature estimate was performed using the extracted average worst-case device losses. In this analysis, $R_{th,req}$ is interpreted as a cooling-burden indicator, where a lower value indicates a more stringent allowable thermal-resistance budget. Since $R_{th,req}$ is calculated from the allowable temperature rise between the junction-temperature limit and the imposed cooling reference temperature, increasing T_{ref} directly reduces the allowable thermal-resistance budget. For a fixed extracted device-average loss, the required effective thermal resistance at a different reference temperature can be estimated as

$$R_{th,req}(T_{ref,new}) = R_{th,req}(25\text{ }^{\circ}\text{C}) \frac{T_{j,max} - T_{ref,new}}{T_{j,max} - 25\text{ }^{\circ}\text{C}}. \quad (6)$$

This post-processing does not replace a full temperature-dependent electro-thermal rerun and should not be interpreted as a complete electro-thermal sensitivity simulation. Instead, it provides a first-order estimate of the reduction in cooling margin at more realistic coolant/reference temperatures. Accordingly, $R_{th,req}$ is treated as a cooling-burden indicator, and the coolant/reference-temperature variation in Table 3 is used to estimate the corresponding change in thermal-resistance margin.

As expected, increasing the coolant/reference temperature reduces the allowable thermal-resistance budget for all topologies. Increasing T_{ref} from 25 °C to 50 °C reduces the allowable $R_{th,req}$ by approximately 20%, while increasing it to 65 °C reduces the allowable budget by approximately 32%. However, the relative topology ranking remains unchanged under this first-order post-processing assumption: the 2L H-Bridge exhibits the most stringent cooling requirement, whereas the 3L T-Type and 3L ANPC retain larger estimated thermal-resistance margins. These values should be interpreted as first-order cooling-margin estimates rather than full temperature-dependent electro-thermal simulation results.

Table 3. Post-processed first-order estimate of the required effective thermal resistance at different coolant/reference temperatures for the investigated high-power operating point. The values are derived from the extracted average worst-case device losses using a conservative junction-temperature limit of $T_{j,max} = 150\text{ }^{\circ}\text{C}$.

Topology	$R_{th,req}$ at $25\text{ }^{\circ}\text{C}$ (K/W)	$R_{th,req}$ at $50\text{ }^{\circ}\text{C}$ (K/W)	$R_{th,req}$ at $65\text{ }^{\circ}\text{C}$ (K/W)
2L H-Bridge	0.79	0.63	0.54
3L T-Type	1.55	1.24	1.05
3L ANPC	2.26	1.81	1.54

6. Thermomechanical Fatigue and Lifetime-Oriented Reliability Assessment

In automotive traction applications, semiconductor lifetime is predominantly limited by thermomechanical solder fatigue. This ageing mechanism is driven by low-frequency junction temperature cycling (ΔT_j) up to 100°C , which induces cyclic shear stress due to the coefficient of thermal expansion (CTE) mismatch between adjacent packaging materials [48].

Comparative thermomechanical reliability is evaluated using the Coffin-Manson model, relating cycles-to-failure (N_f) to the temperature swing amplitude (ΔT_j):

$$N_f = A \cdot (\Delta T_j)^{\alpha_0}. \quad (7)$$

Based on standard power cycling test data, the fatigue exponent α_0 is empirically established as -4.3327 [49]. Because the material-dependent multiplier A requires destructive testing to determine absolute lifetime, the Palmgren-Miner linear damage rule

$$D \propto \frac{1}{N_f} \quad (8)$$

is utilized to formulate a relative damage indicator (D_{rel}). Normalizing against a baseline condition mathematically cancels A , defining fatigue acceleration purely by the ratio of temperature swings:

$$D_{rel} = \left(\frac{\Delta T_j}{\Delta T_{j,base}} \right)^{4.3327}. \quad (9)$$

It should be emphasized that the Coffin-Manson-based quantity used in this work is a relative first-order thermal-stress indicator rather than an absolute power-module lifetime prediction. The formulation captures the influence of junction-temperature swing (ΔT_j), which is an important driver of thermo-mechanical fatigue; however, practical power-module lifetime also depends on additional factors, including mean junction temperature ($T_{j,mean}$), maximum junction temperature, heating and cooling time, current loading, voltage stress, package structure, bond-wire or interconnect technology, solder layer properties, and mission-profile-dependent cycling. Therefore, the relative damage indicator is used only to compare the thermal-stress tendency of the investigated topologies under the same converter-level simulation framework. Absolute cycles-to-failure are not calculated because this would require package-specific lifetime coefficients and mission-profile-dependent loading conditions that are outside the scope of the present R-L-load benchmark.

Figure 8 indicates that the 2L H-Bridge exhibits the largest junction-temperature swing across the investigated output-power range, while the 3L T-Type shows the lowest ΔT_j and the 3L ANPC remains intermediate. At the peak 130 kW operating point, the 3L T-Type limits ΔT_j to approximately $20.9\text{ }^{\circ}\text{C}$ ($D_{rel} \approx 135$), while the 3L ANPC reaches approximately $24.0\text{ }^{\circ}\text{C}$ ($D_{rel} \approx 250$). In comparison, the 2L H-Bridge reaches a higher temperature swing of approximately $41.6\text{ }^{\circ}\text{C}$, corresponding to $D_{rel} \approx 3100$ under the Coffin-Manson-based formulation. Therefore, within the defined converter-level simulation framework, the 2L

H-Bridge shows the highest relative thermal-stress tendency, whereas the 3L T-Type shows the lowest and the 3L ANPC remains intermediate.

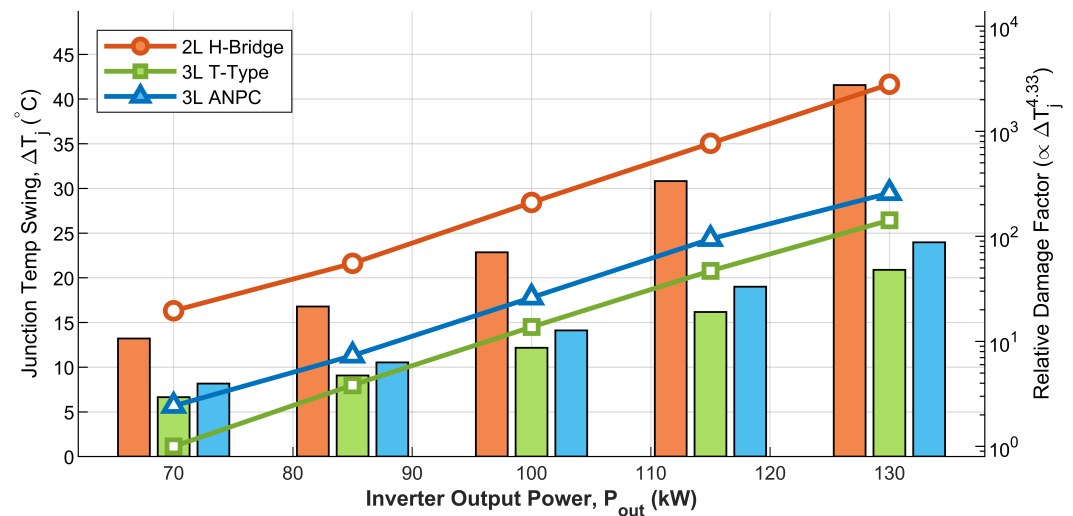


Figure 8. Thermo-mechanical fatigue indicators for the considered inverter topologies at different output-power levels: the bar plot shows the junction-temperature swing (ΔT_j), while the overlaid line plot shows the calculated relative damage indicator (D_{rel}).

Although the relative damage indicator in Equation (9) is calculated from ΔT_j , the corresponding mean junction-temperature trends extracted from the simulated junction-temperature profiles are also considered as supporting lifetime-oriented thermal indicators. The qualitative topology ranking remains unchanged when both ΔT_j and $T_{j,mean}$ are considered: the 2L H-Bridge exhibits the highest thermal-stress tendency, the 3L T-Type shows the lowest thermal-stress tendency, and the 3L ANPC remains intermediate under the defined simulation assumptions. Nevertheless, these results should be interpreted as first-order thermal-stress indicators rather than absolute lifetime predictions, since a complete power-cycling lifetime model would require package-specific empirical coefficients, heating and cooling time, current loading, and mission-profile-dependent thermal cycling.

The qualitative comparison in Table 4 shows that the improved loss, thermal-stress, and conducted-EMI indicators of the multilevel topologies should be weighed against their practical implementation penalties. In particular, the 3L ANPC and 3L T-Type require additional semiconductor devices, gate-driver channels, and more complex PCB layout compared with the 2L H-Bridge, which can increase hardware cost and part-count-related random failure risk. Therefore, topology selection should consider both the converter-level thermal and EMI benefits and the associated system-level complexity under the intended automotive design constraints.

Table 4. Qualitative comparison of thermal-stress indicators, cooling burden, and implementation complexity for the investigated inverter topologies under the defined simulation framework.

Parameter	2L H-Bridge	3L ANPC	3L T-Type
Thermal-Stress and Cooling-Burden Indicators at 130 kW			
Allowable thermal-resistance margin	Most constrained	Largest estimated margin	Intermediate margin
Estimated cooling burden	Highest	Lowest	Intermediate
Junction-temperature swing (ΔT_j)	Highest	Intermediate	Lowest
Relative damage indicator	Highest	Intermediate	Lowest

Table 4. Cont.

Parameter	2L H-Bridge	3L ANPC	3L T-Type
System-Level Implementation Trade-Offs			
Part-count-related random failure risk	Lowest	Highest	Intermediate
PCB layout complexity	Lowest	Highest	Intermediate
Conducted-EMI tendency	Highest	Intermediate	Lowest
Relative hardware cost	Lowest	Highest	Intermediate

7. Conclusions

This study presented a simulation-based converter-level electro-thermal and conducted-EMI benchmark of post-800 V traction inverter topologies, comparing the conventional 2L H-Bridge, 3L ANPC, and 3L T-Type configurations under identical output-power conditions and simplified R – L loading. The results show that increasing the DC-link voltage from 800 V to 1200 V reduces semiconductor losses and worst-case junction temperature across all investigated topologies, mainly due to the reduction in current stress at the same output power. Among the evaluated topologies, the 3L T-Type consistently achieved the lowest total losses, highest efficiency, and lowest peak junction temperature, followed by the 3L ANPC and the 2L H-Bridge.

The cooling-burden analysis further showed that the multilevel topologies reduced the estimated cooling requirement under the defined simulation framework. At the investigated high-power operating point, the 2L H-Bridge required the lowest allowable effective thermal resistance ($R_{th,req} = 0.79$ K/W), indicating the highest cooling burden, whereas the 3L T-Type and 3L ANPC showed higher allowable values of 1.55 K/W and 2.26 K/W, respectively. From a first-order reliability-oriented thermal-stress perspective, the 2L H-Bridge exhibited the largest junction-temperature swing ($\Delta T_j \approx 41.6$ °C), resulting in a relative damage indicator approximately 23 times higher than that of the 3L T-Type ($\Delta T_j \approx 20.9$ °C) when evaluated using the Coffin–Manson-based formulation.

Overall, within the simplified R – L -load converter-level benchmark considered in this work, the 3L T-Type showed the most favourable trade-off among semiconductor losses, conducted-EMI tendency, estimated cooling burden, and first-order thermal-stress indicators. However, the 3L T-Type and 3L ANPC also introduce additional semiconductor devices, gate-driver channels, modulation requirements, and control complexity, which must be considered in practical automotive implementation.

8. Future Work

Future work will extend the benchmark by integrating PMSM or induction-motor models under realistic drive cycles, including speed-dependent back-EMF, variable power factor, field-weakening operation, closed-loop current control, and mission-profile-dependent current waveforms. Further work should also include layout-dependent parasitic extraction, dead-time sensitivity, gate-driver non-idealities, experimental EMI/loss validation, power-cycling lifetime modelling with validated lifetime data, and reduced-order electro-thermal modelling for longer-duration thermal assessment.

AI-assisted and metaheuristic optimization methods could also be explored for future multi-objective inverter design, including optimization of topology selection, switching frequency, modulation parameters, thermal-boundary design, and EMI-related parasitic/layout constraints [50].

A scaled-down experimental prototype should also be developed in future work to validate the simulated loss, thermal, and conducted-EMI trends. The most critical validation step would be a controlled comparison of the 2L H-Bridge and 3L T-Type under

identical DC-link voltage, output power, switching frequency, load condition, gate-drive setting, coolant/reference temperature, and cold-plate condition, with measurements of semiconductor losses, voltage/current waveforms, junction or case temperature, coolant heat extraction, and LISN-based conducted-EMI spectra.

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Conflicts of Interest: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Nomenclature and Abbreviations

The following symbols and abbreviations are used in this manuscript:

V_{dc}	DC-link voltage
V_{ds}	Device drain–source voltage
$I(t)$	Instantaneous device current
I_{rms}	RMS phase current
f_{sw}	Switching frequency
f_1	Fundamental output frequency
m	Modulation index
R_{load}	Load resistance
L_{load}	Load inductance
T_{dt}	Dead time
$R_{g,on}$	External turn-on gate resistance
$R_{g,off}$	External turn-off gate resistance
dv/dt	Rate of change of voltage
di/dt	Rate of change of current
P_{cond}	Conduction loss
P_{sw}	Switching loss
$P_{dev}(t)$	Total instantaneous device loss
$P_i(t)$	Heat flow injected by device i
P_{loss}	Semiconductor power loss
$P_{loss,avg,worst}$	Average loss of the worst-case semiconductor switch
P_{out}	Inverter output power
E_{on}	Device turn-on switching energy
E_{off}	Device turn-off switching energy
T_j	Junction temperature
$T_{j,max}$	Maximum junction temperature
$T_{j,mean}$	Mean junction temperature
ΔT_j	Junction-temperature swing

$\Delta T_{j,base}$	Baseline junction-temperature swing
$T_h(t)$	Heatsink temperature
T_{ref}	Cooling reference temperature
$R_{th,ch}$	Case-to-heatsink thermal resistance
R_{th}	Heatsink-to-coolant thermal resistance
$R_{th,jc}$	Junction-to-case thermal resistance
$R_{th,req}$	Required effective per-device thermal resistance
C_{th}	Heatsink thermal capacitance
τ	Dominant thermal time constant, $R_{th}C_{th}$
T_{sim}	Total simulation time
N_f	Cycles to failure
A	Material-dependent Coffin–Manson multiplier
α_0	Coffin–Manson fatigue exponent
D	Accumulated damage based on the Palmgren–Miner rule
D_{rel}	Relative damage indicator
L_{LISN}	LISN series inductance
R_{LISN}	LISN sensing resistance
C_p	Parasitic capacitance to reference ground

Abbreviations

2L	Two-level
3L	Three-level
AC	Alternating current
ANPC	Active neutral-point clamped
CM	Common-mode
CTE	Coefficient of thermal expansion
DC	Direct current
DM	Differential-mode
EMI	Electromagnetic interference
EV	Electric vehicle
GaN	Gallium nitride
HEMT	High-electron-mobility transistor
IGBT	Insulated-gate bipolar transistor
LISN	Line impedance stabilization network
MLI	Multilevel inverter
MOSFET	Metal-oxide-semiconductor field-effect transistor
NPC	Neutral-point clamped
OBC	Onboard charger
PCB	Printed circuit board
PLECS	Piecewise Linear Electrical Circuit Simulation
PMSM	Permanent-magnet synchronous motor
PWM	Pulse-width modulation
$R-L$	Resistive–inductive
RMS	Root mean square
Si	Silicon
SiC	Silicon carbide
SPWM	Sinusoidal pulse-width modulation
TIM	Thermal interface material
WBG	Wide-bandgap
WEG	Water–ethylene glycol

Appendix A. Load Resistance Values Used in the R–L load Benchmark

Table A1. Load resistance values used for each topology, DC-link voltage, and output-power condition at the baseline switching frequency of $f_{sw} = 20$ kHz. The load inductance was fixed at $L_{load} = 2$ mH for all cases.

V_{dc} (V)	P_{out} (kW)	R_{load} 2L H-Bridge (Ω)	R_{load} 3L ANPC (Ω)	R_{load} 3L T-Type (Ω)
800	130	1.56	1.52	1.56
800	115	1.82	1.81	1.82
800	100	2.15	2.13	2.15
800	85	2.60	2.58	2.60
800	70	3.25	3.21	3.25
1000	130	2.60	2.60	2.69
1000	115	3.00	3.02	3.07
1000	100	3.50	3.58	3.58
1000	85	4.15	4.20	4.25
1000	70	4.90	4.50	5.19
1200	130	3.86	3.95	3.99
1200	115	4.54	4.50	4.54
1200	100	5.25	5.21	5.25
1200	85	6.20	6.00	6.20
1200	70	7.51	7.40	7.53

References

- Reimers, J.; Dorn-Gomba, L.; Mak, C.; Emadi, A. Automotive Traction Inverters: Current Status and Future Trends. *IEEE Trans. Veh. Technol.* **2019**, *68*, 3337–3350. <https://doi.org/10.1109/TVT.2019.2897899>.
- Husain, I.; Ozipineci, B.; Islam, M.S.; Gurpinar, E.; Su, G.J.; Yu, W.; Chowdhury, S.; Xue, L.; Rahman, D.; Sahu, R. Electric Drive Technology Trends, Challenges, and Opportunities for Future Electric Vehicles. *Proc. IEEE* **2021**, *109*, 1039–1059. <https://doi.org/10.1109/JPROC.2020.3046112>.
- Stella, F.; Vico, E.; Cittanti, D.; Liu, C.; Shen, J.; Bojoi, R. Design and Testing of an Automotive Compliant 800V 550 kVA SiC Traction Inverter with Full-Ceramic DC-Link and EMI Filter. In *Proceedings of the 2022 IEEE Energy Conversion Congress and Exposition (ECCE 2022), Detroit, MI, USA, from 9–13 October 2022*; Institute of Electrical and Electronics Engineers Inc.: New York, NY, USA, 2022. <https://doi.org/10.1109/ECCE50734.2022.9948096>.
- She, X.; Huang, A.Q.; Lucia, O.; Ozipineci, B. Review of Silicon Carbide Power Devices and Their Applications. *IEEE Trans. Ind. Electron.* **2017**, *64*, 8193–8205. <https://doi.org/10.1109/TIE.2017.2652401>.
- Poorfakhraei, A.; Narimani, M.; Emadi, A. A review of multilevel inverter topologies in electric vehicles: Current status and future trends. *IEEE Open J. Power Electron.* **2021**, *2*, 155–170. <https://doi.org/10.1109/OJPEL.2021.3063550>.
- Demystifying Clearance and Creepage Distance for High-Voltage End Equipment. Application Report SLUP419, Texas Instruments, Dallas, TX, USA. 2024. Available online: <https://www.ti.com/lit/ml/slup419/slup419.pdf> (accessed on 10 February 2026).
- Mousavi, M.H.; Moradi, H.; Rouzbehi, K. Transition of DC Link Voltage from 400V to 800V in Electric Vehicles: Performance, Trade-Offs, and Technical Insights. In *Proceedings of the 2025 10th International Conference on Technology and Energy Management (ICTEM 2025), Tabriz, Iran, 21–23 April 2025*; Institute of Electrical and Electronics Engineers Inc.: New York, NY, USA, 2025. <https://doi.org/10.1109/ICTEM66196.2025.11063549>.
- Hren, A.; Truntiĉ, M.; Mihaliĉ, F. A Survey on the State-of-the-Art and Future Trends of Multilevel Inverters in BEVs. *Electronics* **2023**, *12*, 2993. <https://doi.org/10.3390/electronics12132993>.
- Mohammed, S.A.Q.; Hakami, S.S.; Kassas, M.; Almuahini, M.M. Critical Review on Powertrain Technologies for Electric Vehicles: Classification, Broadly Adopted Topologies, and Future Challenges. *IEEE Access* **2025**, *13*, 71755–71772. <https://doi.org/10.1109/ACCESS.2025.3561577>.
- BYD Unveils Super e-Platform with Megawatt Flash Charging for Electric Vehicles, Matching Refueling Speeds. 2025. Available online: <https://www.byd.com/mea/news-list/byd-unveils-super-e-platform-with-megawatt-flash-charging> (accessed on 10 February 2026).

11. He, Y.; Zhu, J.; Zhou, B.; Zhao, X. EMI Issues and Reduction in 800 V Electrical Vehicle Systems by Incorporating Cable Effects. In *Proceedings of the IEEE Student Conference on Electric Machines and Systems (SCEMS), Huzhou, China, 7–9 December 2023*; Institute of Electrical and Electronics Engineers: New York, NY, USA, 2023. <https://doi.org/10.1109/SCEMS60579.2023.10379396>.
12. Han, D.; Morris, C.T.; Lee, W.; Sarlioglu, B. A Case Study on Common Mode Electromagnetic Interference Characteristics of GaN HEMT and Si MOSFET Power Converters for EV/HEVs. *IEEE Trans. Transp. Electr.* **2017**, *3*, 168–179. <https://doi.org/10.1109/TTE.2016.2622005>.
13. Haider, M.; Fuchs, S.; Zulauf, G.; Bortis, D.; Kolar, J.W.; Ono, Y. Analytical Loss Model for Three-Phase 1200V SiC MOSFET Inverter Drive System Utilizing Miller Capacitor-Based dv/dt-Limitation. *IEEE Open J. Power Electron.* **2022**, *3*, 93–104. <https://doi.org/10.1109/OJPEL.2022.3143995>.
14. Sakhare, A.; Mikkili, S. Advanced DC–DC Converter Topologies for Electric Vehicles: Wide Bandgap Technologies, Emerging Trends and Future Challenges. *Electr. Mater. Appl.* **2025**, *2*, e70023. <https://doi.org/10.1049/ema3.70023>.
15. Jelodar, Y.J.; Salari, O.; Youssef, M.Z.; Ebrahimi, J.; Bakhshai, A. A Novel Control Scheme for Traction Inverters in Electric Vehicles With an Optimal Efficiency Across the Entire Speed Range. *IEEE Access* **2024**, *12*, 25906–25916. <https://doi.org/10.1109/ACCESS.2024.3366934>.
16. Wang, Z.; Wu, Y.; Mahmud, M.H.; Zhao, Z.; Zhao, Y.; Mantooth, H.A. Design and Validation of A 250-kW All-Silicon Carbide High-Density Three-Level T-Type Inverter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 578–588. <https://doi.org/10.1109/JESTPE.2019.2951625>.
17. Satpathy, S.; Das, P.P.; Bhattacharya, S.; Veliadis, V. Design Considerations of a GaN-based Three-Level Traction Inverter for Electric Vehicles. In *Proceedings of the 2022 IEEE 9th Workshop on Wide Bandgap Power Devices and Applications (WiPDA 2022), Redondo Beach, CA, USA, 7–9 November 2022*; Institute of Electrical and Electronics Engineers Inc.: New York, NY, USA, 2022; pp. 192–197. <https://doi.org/10.1109/WiPDA56483.2022.9955248>.
18. Cittanti, D.; Guacci, M.; Mirić, S.; Bojoi, R.; Kolar, J.W. Comparative Evaluation of 800V DC-Link Three-Phase Two/Three-Level SiC Inverter Concepts for Next-Generation Variable Speed Drives. In *Proceedings of the 2020 23rd International Conference on Electrical Machines and Systems (ICEMS), Hamamatsu, Japan, 24–27 November 2020*; IEEE: New York, NY, USA, 2020; pp. 1699–1704. <https://doi.org/10.23919/ICEMS50442.2020.9291123>.
19. Azab, M. A Review of Recent Trends in High-Efficiency Induction Motor Drives. *Vehicles* **2025**, *7*, 15. <https://doi.org/10.3390/vehicles7010015>.
20. Trovao, J.P. What Is Next for Automotive Electronics? [Automotive Electronics]. *IEEE Veh. Technol. Mag.* **2022**, *17*, 113–120. <https://doi.org/10.1109/MVT.2022.3179790>.
21. Mauromicale, G.; Raciti, A.; Rizzo, S.A.; Susinni, G.; Abbatelli, L.; Buonomo, S.; Cavallaro, D.; Giuffrida, V. SiC Power Modules for Traction Inverters in Automotive Applications. In *Proceedings of the Industrial Electronics Conference (IECON), Lisbon, Portugal, 14–17 October 2019*; IEEE: New York, NY, USA, 2019; pp. 1973–1978. <https://doi.org/10.1109/IECON.2019.8927366>.
22. Hepp, M.; Saur, M.; Bakran, M.M. Reducing the DC-Link Voltage Ripple by Optimized Pulse Patterns to Increase the Power Density of Traction Inverters in Electric Vehicles. *IEEE Open J. Power Electron.* **2024**, *5*, 1767–1781. <https://doi.org/10.1109/OJPEL.2024.3493169>.
23. Anusha, G.; Sudhakar, A.V.; Deshmukh, R.R.R.; Basha, C.H. A bibliometric analysis of research trends in electric vehicle power electronics: Global perspectives and future directions. *Discov. Appl. Sci.* **2025**, *7*, 487. <https://doi.org/10.1007/s42452-025-06996-1>.
24. Kundu, A.; Balamurali, A.; Korta, P.; Iyer, K.L.V.; Kar, N.C. An Approach for Estimating the Reliability of IGBT Power Modules in Electrified Vehicle Traction Inverters. *Vehicles* **2020**, *2*, 413–423. <https://doi.org/10.3390/vehicles2030022>.
25. Zachariae, J.; Tiesler, M.; Singh, R.; Benning, T.A.; Schweikert, C. Silicon carbide based traction inverter cooling in electric vehicle using heat pipes. *Therm. Sci. Eng. Prog.* **2023**, *46*, 102155. <https://doi.org/10.1016/j.tsep.2023.102155>.
26. Wang, Y.; Ilka, R.; Camp, J.; He, J.B. An Immersion Cooled SiC T-Type Traction Inverter—Thermal Performance Evaluation. *IEEE Trans. Power Electron.* **2026**, *41*, 1621–1626. <https://doi.org/10.1109/TPEL.2025.3618787>.
27. Taha, W.; Nahid-Mobarakeh, B.; Bauman, J. Efficiency evaluation of 2L and 3L SiC-based traction inverters for 400V and 800V electric vehicle powertrains. In *Proceedings of the 2021 IEEE Transportation Electrification Conference and Expo (ITEC 2021), Chicago, IL, USA, 21–25 June 2021*; Institute of Electrical and Electronics Engineers Inc.: New York, NY, USA, 2021; Volume 6, pp. 625–632. <https://doi.org/10.1109/ITEC51675.2021.9490082>.
28. Dornala, A.; Lee, K.; Fereydoonian, M.; Halawa, A.; Benson, M.; Lee, W. Efficiency and EMI Analysis of WBG-based Multilevel Inverters for 800 V Electric Vehicle Traction Systems. In *Proceedings of the Conference Proceedings—IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 25–29 February 2024*; Institute of Electrical and Electronics Engineers Inc.: New York, NY, USA, 2024; pp. 157–163. <https://doi.org/10.1109/APEC48139.2024.10509224>.
29. Liu, H.; Wang, S.; Hu, L.; Feng, L.; Wang, Y. Junction Temperature Control of a Traction Inverter Based on Three-Level Active Neutral Point-Clamping. *Energies* **2025**, *18*, 2241. <https://doi.org/10.3390/en18092241>.
30. Lee, K.; Benson, M.; Fereydoonian, M.; Dong, X.; Moon, J.; Lee, W. Comprehensive Electromagnetic Interference Analysis of Neutral-Point-Less (NPL) Multilevel Inverter with Active Common-Mode Voltage Cancellation. In *Proceedings of the Conference*

- Proceedings—IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 19–23 March 2023; Institute of Electrical and Electronics Engineers Inc.: New York NY, USA, 2023; Volume 2023, pp. 237–243. <https://doi.org/10.1109/APEC43580.2023.10131636>.*
31. Miric, S.; Niklaus, P.S.; Huber, J.; Stäger, C.; Haider, M.; Kolar, J.W. Analysis and Experimental Verification of the EMI Signature of Three-Phase Three-Level TCM Soft-Switching Converter Systems. *IEEE Access* **2023**, *11*, 57391–57400. <https://doi.org/10.1109/ACCESS.2023.3283921>.
 32. Soldati, A.; Pietrini, G.; Dalboni, M.; Concarri, C. Electric-Vehicle Power Converters Model-Based Design-for-Reliability. *CPSS Trans. Power Electron. Appl.* **2018**, *3*, 102–110. <https://doi.org/10.24295/CPSSSTPEA.2018.00010>.
 33. Zhang, Y.; Heimler, P.; Abuogo, J.O.; Zhang, X.; Zhang, Y.; Xie, D.; Zhang, Y.; Zhang, K.; Li, X.; Luo, H.; et al. Power Cycling Testing for Power Semiconductor Switches: Methods, Standards, Limitations, and Outlooks. *IEEE Trans. Power Electron.* **2025**, *41*, 849–869. <https://doi.org/10.1109/TPEL.2025.3595180>.
 34. Dai, H.; Torres, R.A.; Jahns, T.M.; Sarlioglu, B. Comparative Study of Conducted Common-Mode EMI in WBG-Enabled DC-Fed Three-Phase Current-Source Inverter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**, *10*, 7188–7204. <https://doi.org/10.1109/JESTPE.2022.3161422>.
 35. Jones-Jackson, S.; Rodriguez, R.; Yang, Y.; Lopera, L.; Emadi, A. Overview of Current Thermal Management of Automotive Power Electronics for Traction Purposes and Future Directions. *IEEE Trans. Transp. Electr.* **2022**, *8*, 2412–2428. <https://doi.org/10.1109/TTE.2022.3147976>.
 36. Poorfakhraei, A.; Narimani, M.; Emadi, A. A Review of Modulation and Control Techniques for Multilevel Inverters in Traction Applications. *IEEE Access* **2021**, *9*, 24187–24204. <https://doi.org/10.1109/ACCESS.2021.3056612>.
 37. Sambhavi, Y.V.; Ramachandran, V. A technical review of modern traction inverter systems used in electric vehicle application. *Energy Rep.* **2023**, *10*, 3882–3907. <https://doi.org/10.1016/j.egy.2023.10.056>.
 38. Kabalcı, E.; Boyar, A., Multilevel inverter applications for electric vehicle drives. In *Multilevel Inverters: Control Methods and Advanced Power Electronic Applications*; Elsevier: Amsterdam, The Netherlands, 2021; pp. 149–172. <https://doi.org/10.1016/B978-0-323-90217-5.00006-X>.
 39. Wang, Z.; Mahmud, M.H.; Uddin, M.H.; McPherson, B.; Sparkman, B.; Zhao, Y.; Mantooth, H.A.; Fraley, J.R. A Compact 250 kW Silicon Carbide MOSFET based Three-Level Traction Inverter for Heavy Equipment Applications. In *Proceedings of the 2018 IEEE Transportation and Electrification Conference and Expo (ITEC 2018), Long Beach, CA, USA, 13–15 June 2018*; IEEE: New York, NY, USA, 2018; pp. 212–216. <https://doi.org/10.1109/ITEC.2018.8450172>.
 40. Deshpande, A.V.; Wang, S.; Pool-Mazun, E.I.; Garza-Arias, E.; Sandoval, R.; Gnegy-Davidson, C.; Byrd, T.; Enjeti, P. A Highly Efficient GaN and SiC Hybrid Active Neutral Point Clamped (ANPC) Inverter for High-Speed Electric Traction Applications. In *Proceedings of the 2024 IEEE 11th Workshop on Wide Bandgap Power Devices and Applications (WiPDA 2024), Dayton, OH, USA, 4–6 November 2024*; Institute of Electrical and Electronics Engineers Inc.: New York, NY, USA, 2024. <https://doi.org/10.1109/WiPDA62103.2024.10773229>.
 41. Soomro, H.A.; Khir, M.H.B.M.; Zulkifli, S.A.B.; Abro, G.E.; Abualnaeem, M.M. Applications of wide bandgap semiconductors in electric traction drives: Current trends and future perspectives. *Results Eng.* **2025**, *26*, 104679. <https://doi.org/10.1016/j.rineng.2025.104679>.
 42. Chen, M.; Pan, D.; Wang, H.; Wang, X.; Blaabjerg, F. Investigation of Switching Oscillations for Silicon Carbide MOSFETs in Three-Level Active Neutral-Point-Clamped Inverters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 4839–4853. <https://doi.org/10.1109/JESTPE.2020.3014742>.
 43. Okilly, A.H.; Kim, C.; Kim, D.W.; Baek, J. Control and Modeling Framework for Balanced Operation and Electro-Thermal Analysis in Three-Level T-Type Neutral Point Clamped Inverters. *Energies* **2025**, *18*, 5587. <https://doi.org/10.3390/en18215587>.
 44. Zhang, C.; Srdic, S.; Lukic, S.; Kang, Y.; Choi, E.; Tafti, E. A SiC-Based 100 kW High-Power-Density (34 kW/L) Electric Vehicle Traction Inverter. In *Proceedings of the 2018 IEEE Energy Conversion Congress and Exposition (ECCE), Portland, OR, USA, 23–27 September 2018*; IEEE: New York, NY, USA, 2018; pp. 3880–3885. <https://doi.org/10.1109/ECCE.2018.8558373>.
 45. Bucher, A.; Schmidt, R.; Werner, R.; Leipenat, M.; Hasenohr, C.; Werner, T.; Schmitz, S.; Heitmann, A. Design of a full SiC voltage source inverter for electric vehicle applications. In *Proceedings of the 2016 18th European Conference on Power Electronics and Applications (EPE 2016 ECCE Europe), Karlsruhe, Germany, 5–9 September 2016*. <https://doi.org/10.1109/EPE.2016.7695414>.
 46. Egin Martin, G.; Verbrugge, B.; Mahedi Hasan, M.; El Baghdadi, M.; Romano, C.; Hegazy, O. Artificial Intelligence-Driven Thermal Management in Electric Vehicle Traction Inverters: Cooling System Optimization and Real-Time Temperature Prediction. *IEEE Access* **2025**, *13*, 167632–167648. <https://doi.org/10.1109/ACCESS.2025.3612315>.
 47. Farkas, G.; Sarkany, Z.; Rencz, M. Structural Analysis of Power Devices and Assemblies by Thermal Transient Measurements. *Energies* **2019**, *12*, 2696. <https://doi.org/10.3390/en12142696>.
 48. Wang, B. Review of Power Semiconductor Device Reliability for Power Converters. *CPSS Trans. Power Electron. Appl.* **2017**, *2*, 101–117. <https://doi.org/10.24295/CPSSSTPEA.2017.00011>.

49. Lai, W.; Chen, M.; Ran, L.; Xu, S.; Qin, H.; Alatisse, O.; Mawby, P.A. Study on the lifetime characteristics of power modules under power cycling conditions. *IET Power Electron.* **2016**, *9*, 1045–1052. <https://doi.org/https://doi.org/10.1049/iet-pel.2015.0225>.
50. Shaikh, M.S.; Raj, S.; Zheng, G.; Xie, S.; Wang, C.; Dong, X.; Lin, Y.; Wang, C.; Junejo, N.U.R. Applications, Classifications, and Challenges: A Comprehensive Evaluation of Recently Developed Metaheuristics for Search and Analysis. *Artif. Intell. Rev.* **2025**, *58*, 390. <https://doi.org/10.1007/s10462-025-11377-6>.

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