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# Section
# Semiconductor Devices

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# Selected Papers

## Short-Circuit Detection and Protection Strategies for GaN E-HEMTs in High-Power Applications: A Review

**Authors:** Haitz Gezala Rodero, David Garrido Díez, Iosu Aizpuru Larrañaga and Igor Baraia-Etxaburu

**Abstract:** Gallium nitride (GaN) enhancement-mode high-electron-mobility transistors (E-HEMTs) deliver superior performance compared to traditional silicon (Si) and silicon carbide (SiC) counterparts. Their faster switching speeds, lower on-state resistances, and higher operating frequencies enable more efficient and compact power converters. However, their integration into high-power applications is limited by critical reliability concerns, particularly regarding their short-circuit (SC) withstand capability and overvoltage (OV) resilience. GaN devices typically exhibit SC withstand times of only a few hundred nanoseconds, needing ultrafast protection circuits, which conventional desaturation (DESAT) methods cannot adequately provide. Furthermore, their high switching transients increase the risk of false activation events. The lack of avalanche capability and the dynamic nature of GaN breakdown voltage exacerbate issues related to OV stress during fault conditions. Although SC-related behaviour in GaN devices has been previously studied, a focused and comprehensive review of protection strategies tailored to GaN technology remains lacking. This paper fills that gap by providing an in-depth analysis of SC and OV failure phenomena, coupled with a critical evaluation of current and next-generation protection schemes suitable for GaN-based high-power converters.

https://doi.org/10.3390/electronics14142875

## Investigation of Temperature-Dependent Gate Degradation in Normally-Off AlGaN/GaN High-Electron-Mobility Transistor p-GaN

**Authors:** Jeonghyeok Yoon and Hyungtak Kim

**Abstract:** The effect of temperature on gate degradation behavior was analyzed in Schottky-type p-GaN gate HEMTs under a positive gate voltage. TDDB measurements were conducted at various temperatures, revealing an accelerated gate failure rate at lower temperatures. A Weibull distribution analysis was employed to predict the 10-year rated gate voltage, showing that the rated voltage at −10 °C is significantly lower than at 60 °C. Furthermore, the derived activation energy of −0.22 eV indicates that gate degradation intensifies in colder environments. Hole accumulation occurring at the p-GaN/AlGaN interface can promote degradation by facilitating electron injection and accelerating defect generation in the presence of strong electric fields. At higher temperatures, hole release mitigates charge accumulation, thereby extending device longevity. These findings highlight the necessity of reliability assessments for p-GaN gate HEMTs suitable for environments with low temperatures, including space and polar environments.

https://doi.org/10.3390/electronics14091764

## Evaluation of a 1200 V Polarization Super Junction GaN Field-Effect Transistor in Cascode Configuration

**Authors:** Alireza Sheikhan, E. M. Sankara Narayanan, Hiroji Kawai, Shuichi Yagi and Hironobu Narui

**Abstract:** GaN HEMTs based on polarization super junction (PSJ) technology offer significant improvements in efficiency and power density over conventional silicon (Si) devices due to their excellent material characteristics, which enable fast switching edges and lower specific on-resistance. However, due to the presence of an uninterrupted channel between drain and source at zero gate bias, these devices have normally-on characteristics. In this paper, the performance of a 1200 V GaN FET utilizing PSJ technology in cascode configuration is reported. The device working principle, characteristics, and switching behavior are experimentally demonstrated. The results show that cascoded GaN FETs utilizing the PSJ concept are highly promising for power device applications.

**https://doi.org/10.3390/electronics14030624**

## Investigation of Source/Drain Height Variation and Its Impacts on FinFET and GAA Nanosheet FET

**Authors:** Mingyu Ma, Cong Li, Jianghao Ma, Wangjun Yang, Haokun Li, Hailong You and M. Jamal Deen

**Abstract:** As semiconductor technology and process nodes advance, three-dimensional devices like FinFET and NSFET are increasingly becoming the primary choice, replacing planar MOSFETs. However, the complex manufacturing processes and high process sensitivity of three-dimensional devices at advanced process nodes inevitably cause significant deviations from the ideal structure during actual fabrication, leading to notable changes in their electrical characteristics. This paper investigates the impact of source/drain region height fluctuations caused by etching and epitaxial growth variations on the electrical characteristics of FinFET and NSFET devices, as well as their related circuits. The electrical characteristics when height variations occur in single and multiple electrodes indicate that, although NSFET and FinFET generally exhibit similar properties such as a decrease in the ON-state current when the source/drain height is reduced, the independent nature of the nanosheets in NSFET and the unidirectional conduction of Schottky contact resistance cause significant differences in their electrical characteristics. Additionally, the related circuit-level simulations show that height fluctuations in the source/drain regions of devices can significantly impact circuit characteristics, including voltage and delay, and in severe cases, they may even lead to circuit failure.

**https://doi.org/10.3390/electronics14061091**

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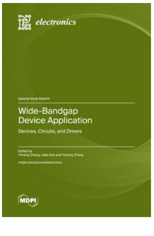


Wide-Bandgap Device Application: Devices, Circuits, and Drivers

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